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Wide-Range Switched-Mode Power Amplifier Architecture

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Abstract: Switched-mode power amplifiers are desired that can work across a wide range of power levels and load impedances with fast response speed while maintaining high efficiency. Such designs would be valuable for many applications including plasma generation and wireless power transfer. We introduce a new wide-range switched-mode power amplifier architecture that provides output voltage modulation, enabling it to modulate output power and compensate for resistive load variations. Dynamic frequency modulation is leveraged to address reactive load variations. The new architecture enables all the semiconductor switches to maintain zero-voltage switching across all operating conditions.

I. Introduction

Switched-mode power amplifiers capable of wide operating ranges, including resistive load range and reactive load range and/or a wide range of power levels, are needed for plasma generation, wireless power transfer, dc-dc converters, battery chargers, induction heating, RF welding, and RF power transmission among other applications. Moreover, such switched-mode power amplifiers - also known as radio-frequency (rf) inverters - must often provide high control bandwidth (i.e., fast response speed) to changes in load and/or desired power level.

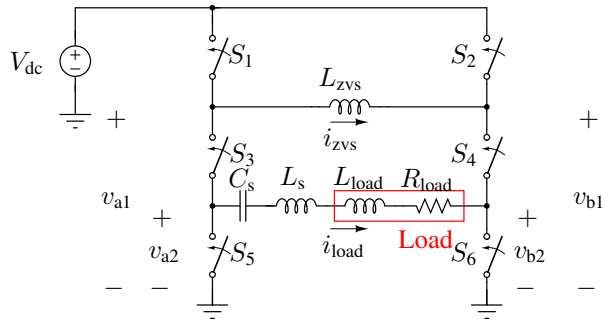
In this work, we propose a new switched-mode power amplifier architecture that can efficiently and rapidly control rf power into a variable load impedance, including loads with variable resistive and reactive components. The new design provides direct rf output voltage modulation to control power and manage load resistance variations and a further control means - such as frequency modulation - to manage load reactance variations. Output power control into a variable load may be achieved while preserving zero-voltage switching (ZVS) of all inverter power devices, which is often important for high-frequency applications. As compared to previous approaches to this design problem (e.g., [1–3]), the proposed inverter offers both a simpler structure and the possibility of much faster response speeds owing to the modulation mechanisms used. As compared to the use of a conventional wide-power-range inverter (e.g., [4]) and a high-bandwith matching network (e.g., [5, 6]), the proposed approach offers a simpler overall system solution.

The proposed wide-range power amplifier architecture offers the ability to provide fast-response control of power over a wide range into a highly-variable load impedance. The amplifier architecture uses a version of phase control (or "reverse" phase control) as a principal to control fundamental rf output amplitude, which we refer to as β modulation hereinafter. The β modulation applies one or more zero-state portions to intermediate ac or dc waveforms, e.g. square-wave waveforms, thus enabling the fundamental component of the output to be controlled. Unlike conventional designs, the proposed approach enables direct output voltage modulation while preserving zero-voltage switching for all devices across a wide operating range. Narrow-band frequency modulation, also called dynamic frequency tuning (DFT), is leveraged to address load reactance variations.

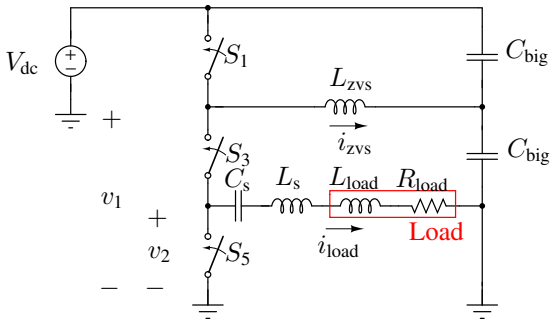
The wide control range and fast response capability come from the topology, β modulation, and frequency modulation. Practically, by introducing a zero state in an intermediate waveform and keeping nonzero state for an electrical angle β, where $\beta_{\text{min}} \leq \beta \leq \beta_{\text{max}}$, we can achieve rapid control of rf power over a wide range including variable resistive and reactive components. DFT can be used in conjunction with an output tank L_{s} and C_{s} to compensate for reactive variations in the load, while preserving ZVS of the all inverter devices. Section II of the paper describes an important implementation of proposed architectural approach, while Section III describes how ZVS is preserved for the inverter devices. Section IV presents a design approach and example. Section V of the paper presents simulations illustrating the performance of the proposed design, and Section VI concludes the paper.

II. Wide-Range Voltage-Mode Class-D Power Amplifier

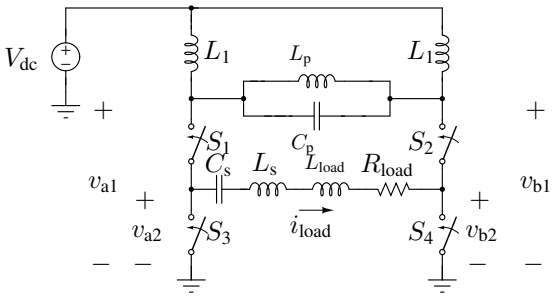
The wide-range switched-mode power amplifier architectures can be implemented based on different circuits, as seen in Fig. 1. Possible implementations include those based on voltage-mode class-D, current-mode class-D and class-E inverters. Depending upon the implementation, the output waveform can be modulated by placing zero states in unipolar or bipolar square waves, sine waves, and half-sine waves. Higher-order power amplifiers are also possible, including class EF



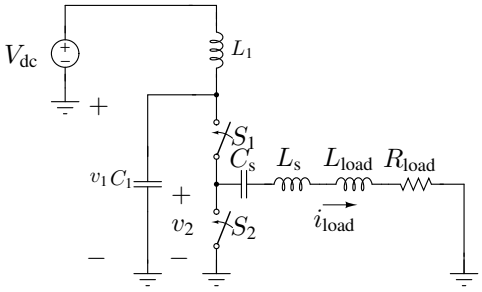
(a) Ideal six-switch wide-range voltage-mode class-D power amplifier.



(b) Ideal three-switch wide-range voltage-mode class-D power amplifier.



(c) Ideal wide-range current-mode class-D power amplifier.



(d) Ideal wide-range class-E power amplifier.

Fig. 1. Wide-range switched-mode power amplifier architecture contains different circuit realizations.

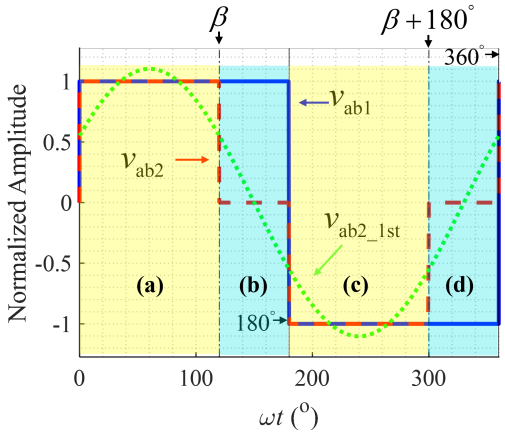


Fig. 2. Ideal modulated square-wave waveforms. The modulation variable β is in the range of $0^\circ \sim 180^\circ$. $v_{ab1} = v_{a1} - v_{b1}$ and $v_{ab2} = v_{a2} - v_{b2}$. The time intervals (a), (b), (c), and (d) match with those in Figs. 3 and 4.

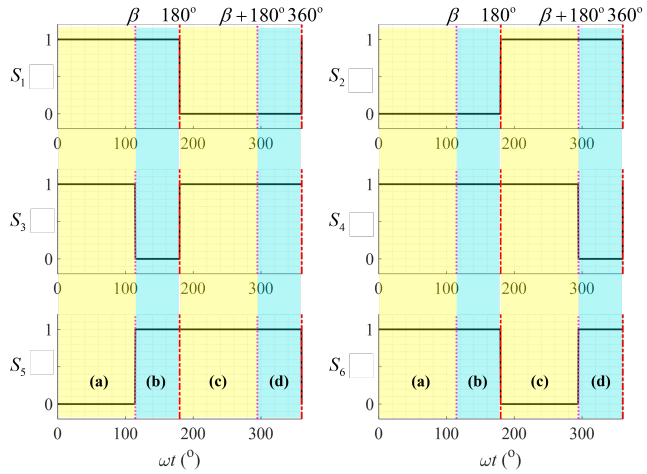
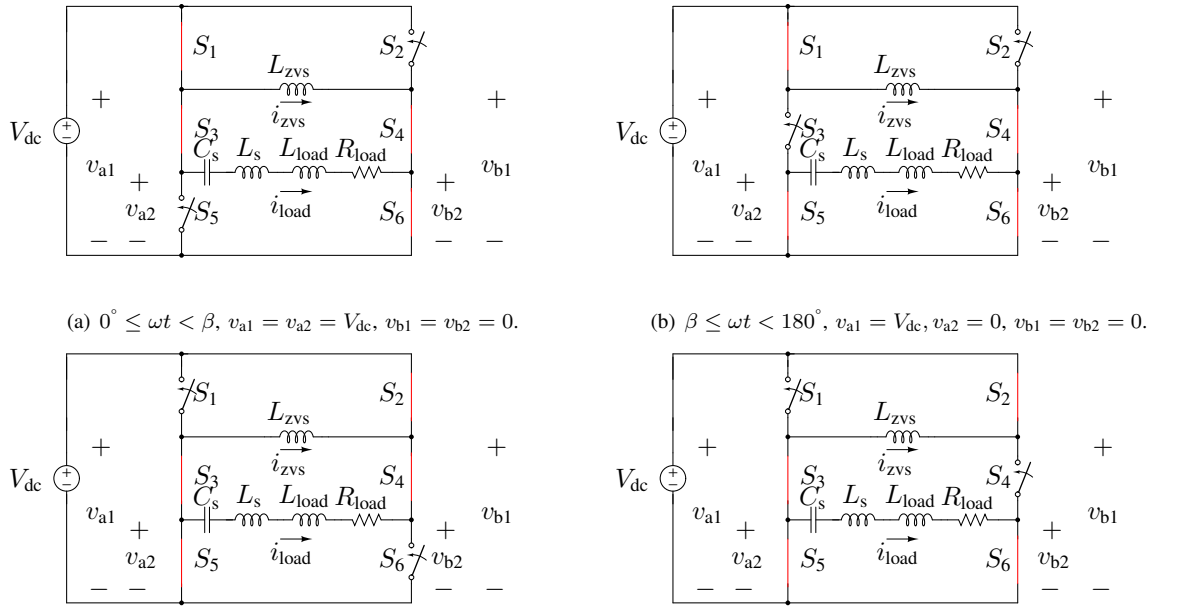


Fig. 3. Ideal control sequences of the wide-range voltage-mode class-D power amplifier. A switching function state of 1 indicates a switch is on and state of 0 indicates a switch is off.

and class ϕ_2 power amplifiers. As an advantageous example of the proposed architecture, we focus on an implementation based on a voltage-mode class-D ZVS inverter, which employs six switches as seen in Fig. 1(a).

A. Idealized Operation

1) Qualitative Analysis: The wide-range voltage-mode class-D power amplifier has six switches for its double-ended (or "differential") version. An idealized version of the six-switch voltage-mode class-D power amplifier is shown in Fig. 1(a). The load is modeled as a series combination of a resistor R_{load} and an inductor L_{load}, which is in series with the output tank L_s and C_s. The inductor L_{zvs} is used in conjunction with the load network to achieve zero voltage switching. The inverter is controlled such that voltage $v_{ab1}(v_{a1\text{-}b1}) = v_{a1} - v_{b1}$ in Fig. 2 is ideally a square wave. Phase control angle β is used to create a phase-controlled (or "chopped") waveform, $v_{ab2}(v_{a2\text{-}b2}) = v_{a2} - v_{b2}$, whose nonzero duration or duty ratio



(a) $0^\circ \le \omega t < \beta$, $v_{a1} = v_{a2} = V_{dc}$, $v_{b1} = v_{b2} = 0$.

(b) $\beta \le \omega t < 180^\circ$, $v_{a1} = V_{dc}$, $v_{a2} = 0$, $v_{b1} = v_{b2} = 0$.

(c) $180^\circ \le \omega t < \beta + 180^\circ$, $v_{a1} = v_{a2} = 0$, $v_{b1} = v_{b2} = V_{dc}$.

(d) $\beta + 180^\circ \le \omega t < 360^\circ$, $v_{a1} = v_{a2} = 0$, $v_{b1} = V_{dc}$, $v_{b2} = 0$.

Fig. 4. Ideal circuit operation of the wide-range voltage-mode class-D power amplifier.

depends on β. The fundamental component $v_{\text{a2-b2\_1st}}$ of $v_{\text{a2-b2}}$, is controlled by β, which provides a means to control the rf output power. In the ideal case, where the rise and fall times of $v_{\text{a1-b1}}$ and $v_{\text{a2-b2}}$ are instantaneous, β has a usable range of $0^\circ \sim 180^\circ$.

The six-switch wide-range voltage-mode class-D power amplifier is related to the full-bridge voltage-mode class-D power amplifier, but utilizes additional switches to achieve a wide output control range while preserving efficient operation. The control sequences (switching functions) of the six switches in the idealized case (with ideal switches) are shown in Fig. 3, where a switching function state of 1 indicates a switch is on and state of 0 indicates a switch is off. S_1 and S_2 ideally operate in a complementary fashion (i.e., neglecting dead time). In the first half cycle, S_1, S_4, and S_6 are on. S_3 also conducts during the first portion of the first half cycle, but turns off at control angle β at which point S_5 turns on (neglecting dead time) and conducts while S_3 is off. In the second half cycle, S_2, S_3 and S_5 are held on. S_4 conducts for the first portion of the second half of the cycle, turning off at $\beta + 180^\circ$, at which point S_6 turns on (again, neglecting deadtime between S_4 and S_6). The circuit operation over these intervals is shown in Fig. 4.

2) Quantitative Analysis: For the waveforms in Fig. 2, we can calculate the peak amplitude and phase of the k^{th} harmonic of $v_{\text{a2-b2}}$

$$|V_k| = \frac{2\sqrt{2}}{k\pi} V_{dc} \sqrt{1 - \cos(k\beta)} \tag{1}$$

$$\phi_k = -\arctan \frac{1 - \cos k\beta}{\sin k\beta} \tag{2}$$

where harmonic order k equals 1 for $v_{\text{a2-b2\_1st}}$. If $\beta = \pi$, $|V_k| = \frac{4}{k\pi} V_{dc}$ and $\phi_k = -\frac{\pi}{2}$ for odd-order harmonics, which are the amplitudes and phases of the square-wave (ideal $v_{\text{a1-b1}}$) Fourier series. The corresponding time-domain waveforms of $v_{\text{a2-b2}}$ harmonic components become

$$v_{\text{a2-b2\_}k^{\text{th}}} = |V_k| \cos(k\omega t + \phi_k). \tag{3}$$

The average load power owing to the k^{th} harmonic component may be calculated as

$$P_k = \frac{1}{2}|I_k|^2 R_{load} = \frac{1}{2} \frac{|V_k|^2 R_{load}}{\left[\omega(L_s + L_{load}) - \frac{1}{\omega C_s}\right]^2 + R_{load}^2} \tag{4}$$

where ω is the operating frequency, $|V_k|$ can be calculated from (1), and $|I_k|$ is the amplitude of k^{th} harmonic component of i_{load}. For a high-quality output filter tank, we may approximate the average load power P as being approximately fundamental power P_1.

For a given resistive load R_{load}, different values of β will result in different voltages applied to the load and hence different load power. To maintain the power range $P_{min} \sim P_{max}$ for a given R_{load}, there is a β range $\beta_{min} \sim \beta_{max}$. There are minimum and maximum load resistance values R_{min} and R_{max} that are the boundaries to achieve a minimum to maximum power range $P_{min} \sim P_{max}$ for $0^\circ < \beta \le 180^\circ$ with a specified dc voltage V_{dc}.

B. Practical Realization

The previous section treats the idealized case in which the switches are ideal and the voltages $v_{\text{a1-b1}}$ and $v_{\text{a2-b2}}$ rise and fall instantaneously. In practice, switches have an output

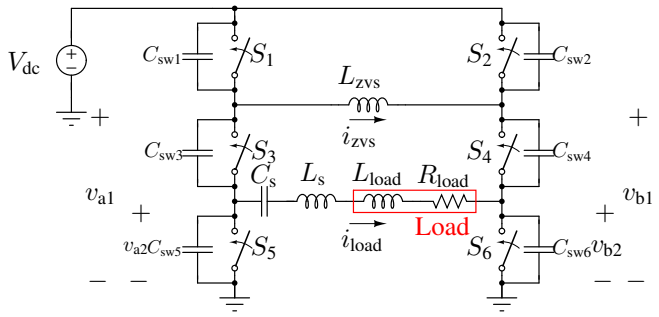


Fig. 5. Wide-range voltage-mode class-D power amplifier with switch capacitances.

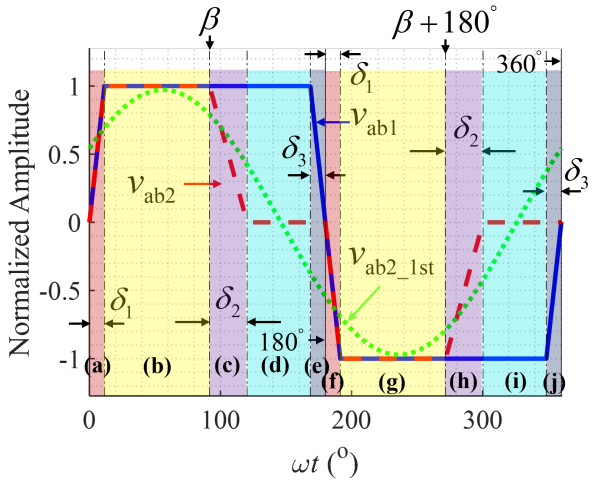


Fig. 6. Practical modulated square-wave waveforms. The modulation variable β is in the range of $\delta_1 \sim 180^\circ - \delta_2$. $v_{ab1} = v_{a1} - v_{b1}$ and $v_{ab2} = v_{a2} - v_{b2}$. The time intervals (a), (b), (c), (d), (e), (f), (g), (h), (i), and (j) match with those in Figs. 7 and 8.

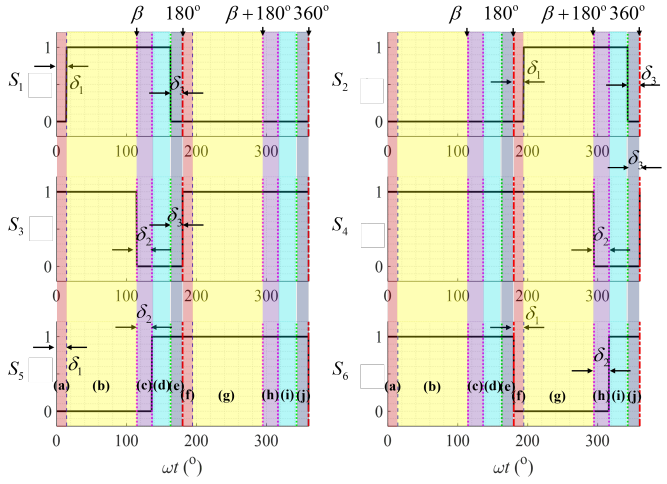


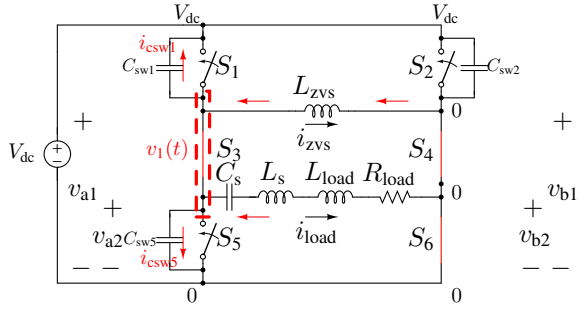
Fig. 7. Practical control sequences of the wide-range voltage-mode class-D power amplifier.

capacitance which may be modeled as a capacitance C_{sw} in parallel with the switch, as illustrated in Fig. 5. The circuit voltage waveforms consequently have nonzero rise and fall times. To avoid switching loss at high frequency, it is important to implement zero-voltage switching (ZVS) in which the switch voltage remains small at device turn-off, and devices are turned on only when they have small voltage across them. A feature of the present design is that despite providing modulated output waveforms, each switch can be turned on and off with zero voltage switching. Some transitions for ZVS switching in the circuits of Fig. 5 depend on the ZVS inductor L_{zvs}. Others depend upon the net inductance L_{net} in the load series branch (L_s, C_s, L_{load}, and R_{load}). While we do not pursue it here, ZVS for this second group of transitions can also be implemented with an additional inductive reactance branch (not shown in Fig. 5) placed in parallel with the load series branch. In Fig. 5, L_{zvs} relates to the ZVS switch voltage transition times δ_1 and δ_3 in Fig. 6 and L_{net} from the load series branch relates to the ZVS switch voltage transition time δ_1 and δ_2 in Fig. 6.

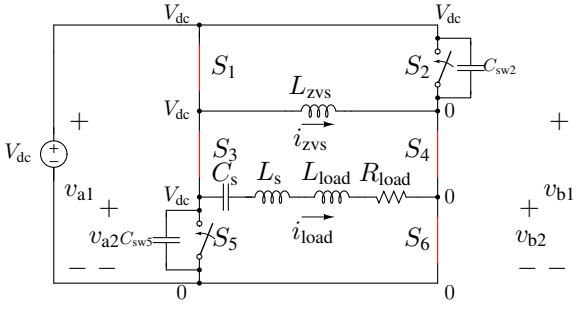
1) Waveform and Circuit: Because of the switch capacitances (C_{sw1}, C_{sw2}, C_{sw3}, C_{sw4}, C_{sw5}, and C_{sw6}), as shown in Fig. 5 and resulting nonzero rise and fall times of voltages $v_{a1\text{-}b1}$ and $v_{a2\text{-}b2}$, as shown in Fig. 6, we define voltage rise time δ_1 and fall time δ_3 in $v_{a1\text{-}b1}$ (expressed in electrical angle). δ_1 and δ_3 can be the same or different and do not need to depend heavily on loading conditions. The rise time of $v_{a2\text{-}b2}$ follows $v_{a1\text{-}b1}$ as δ_1 and its fall time δ_2 depends on the loading conditions.

A set of control sequences and corresponding circuit operation intervals are shown in Figs. 7 and 8, respectively to have voltage waveforms in Fig. 6. Compared to Fig. 3, the control sequences include necessary dead times between switches to permit zero-voltage switching: S_1 turns on with a delay angle δ_1 after S_5 turns off under ZVS. During the dead-time interval, $v_{a1} = v_{a2}$ increases to V_{dc} by charging C_{sw5} so that S_1 can have ZVS turn-on, as shown in Fig. 8(a). S_3 still turns off at β but S_5 turns on with a dead-time delay δ_2. During this dead-time delay, C_{sw5} gets discharged by i_{load}, so that S_5 can have ZVS turn-on, as shown in Fig. 8(c). (As previously mentioned, an additional inductive branch in parallel with the output network branch - not shown in Fig. 5 - can also provide current for ZVS switching.) The turn off of S_1 comes earlier with a dead time δ_3 compared to the idealized case while S_3 still turns on at 180°. During this dead-time delay, C_{sw3} gets discharged by i_{zvs}, so that S_3 can have ZVS turn-on, as shown in Fig. 8(e). The other three switches S_2, S_4, and S_6 operate 180° out of phase with the switches S_1, S_3, and S_5, respectively. The control sequence and circuit operation presented here serve as an illustrative example, demonstrating their functionality. However, it is important to note that they can be further optimized to suit various objectives and goals.

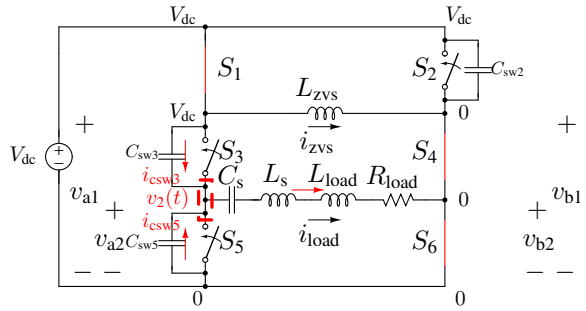
Consider the practical waveforms of $v_{a1\text{-}b1}$, $v_{a2\text{-}b2}$, and $v_{a2\text{-}b2\_1st}$ with switch capacitances and associated dead times shown in Fig. 6. Because of the existence of nonzero rise/fall times δ_1 and δ_2, $|V_k|$ and ϕ_k of the k^{th} harmonic of $v_{a2\text{-}b2}$



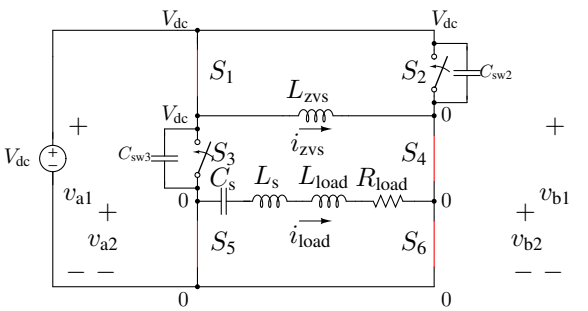
(a) $0^\circ \le \omega t < \delta_1$, $v_{a1} = v_{a2}$, $v_{b1} = v_{b2} = 0$.



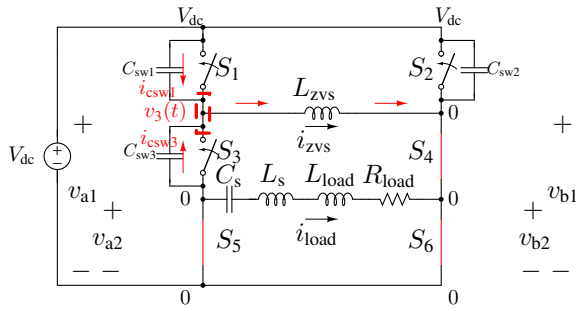
(b) $\delta_1 \le \omega t < \beta$, $v_{a1} = v_{a2} = V_{dc}$, $v_{b1} = v_{b2} = 0$.



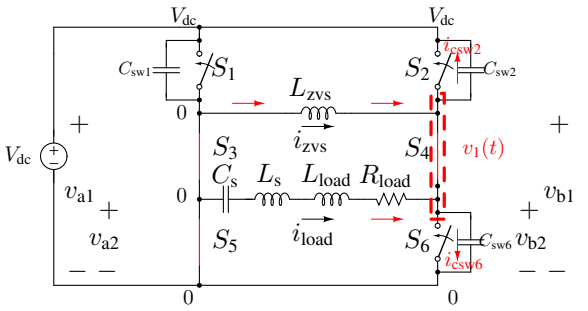
(c) $\beta \le \omega t < \beta + \delta_2$, $v_{a1} = V_{dc}$, $v_{b1} = v_{b2} = 0$.



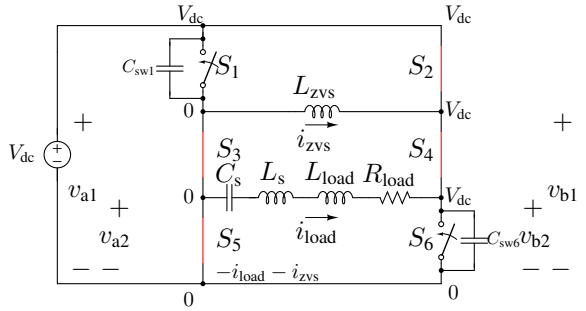
(d) $\beta + \delta_2 \le \omega t < 180^\circ - \delta_3$, $v_{a1} = V_{dc}$, $v_{a2} = 0$, $v_{b1} = v_{b2} = 0$.



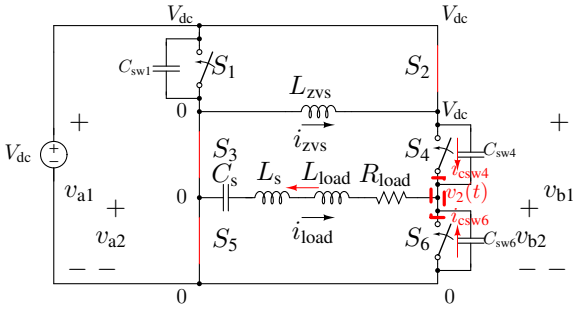
(e) $180^\circ - \delta_3 \le \omega t < 180^\circ$, $v_{a1} = V_{dc}$, $v_{a2} = 0$, $v_{b1} = v_{b2} = 0$.



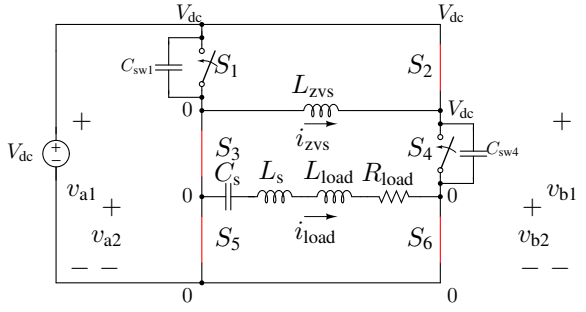
(f) $180^\circ \le \omega t < 180^\circ + \delta_1$, $v_{a1} = v_{a2} = 0$, $v_{b1} = v_{b2}$.



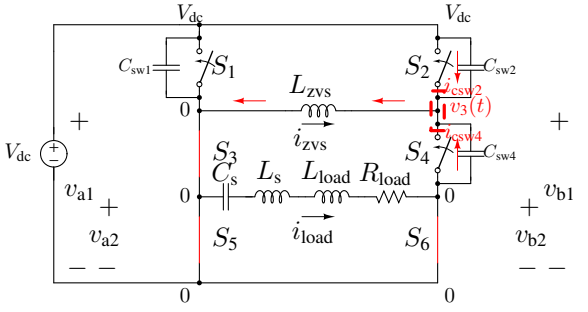
(g) $\delta_1 + 180^\circ \le \omega t < \beta + 180^\circ$, $v_{a1} = v_{a2} = 0$, $v_{b1} = v_{b2} = V_{dc}$.



(h) $\beta + 180^\circ \le \omega t < \beta + \delta_2 + 180^\circ$, $v_{a1} = v_{a2} = 0$, $v_{b1} = V_{dc}$.



(i) $\beta + \delta_2 + 180^\circ \le \omega t < 360^\circ - \delta_3$, $v_{a1} = v_{a2} = 0$, $v_{b1} = V_{dc}$, $v_{b2} = 0$.



(j) $360^\circ - \delta_3 \le \omega t < 360^\circ$, $v_{a1} = v_{a2} = 0$, $v_{b1} = V_{dc}$, $v_{b2} = 0$.

Fig. 8. Practical circuit operation of the wide-range voltage-mode class-D power amplifier.

become

$$
\begin{aligned}
|V_{\rm k}| &= \frac{2\sqrt{2}}{k^2\pi} V_{\rm dc}\sqrt{A+B+C+D} \\
A &= \frac{1-\cos(k\delta_1)}{\delta_1^2}; \\
B &= \frac{1-\cos(k\delta_2)}{\delta_2^2}; \\
C &= \frac{\cos[k(\beta+\delta_2)]+\cos[k(\beta-\delta_1)]}{\delta_1\delta_2}; \\
D &= \frac{-\cos(k\beta)-\cos[k(\beta+\delta_2-\delta_1)]}{\delta_1\delta_2},
\end{aligned} \tag{5}
$$

and

$$
\begin{aligned}
\phi_{\rm k} &= -\arctan\frac{E}{F} \\
E &= \delta_1\sin(k\beta) - \delta_1\sin[k(\beta+\delta_2)] + \delta_2\sin(k\delta_1); \\
F &= \delta_1\cos(k\beta) - \delta_1\cos[k(\beta+\delta_2)] + \delta_2\cos(k\delta_1) - \delta_2,
\end{aligned} \tag{6}
$$

respectively. The corresponding fundamental component of $v_{\text{a2-b2}}$ in time domain is

$$
v_{\text{a2-b2\_1st}} = |V_1|\cos(\omega t + \phi_1) \tag{7}
$$

where $|V_1|$ and ϕ_1 are the amplitude and phase from (5) and (6), respectively.

The average load power owing to the k^{th} harmonic component may be calculated as

$$
P_{\rm k} = \frac{1}{2}|I_{\rm k}|^2 R_{\rm load} = \frac{1}{2}\frac{|V_{\rm k}|^2 R_{\rm load}}{\left[\omega(L_{\rm s}+L_{\rm load}) - \frac{1}{\omega C_{\rm s}}\right]^2 + R_{\rm load}^2} \tag{8}
$$

where ω is the operating frequency and $|V_{\rm k}|$ is from (5).

C. Dynamic Frequency Modulation

Given a high quality-factor output tank $L_{\rm s}$, $C_{\rm s}$, we can select a switching frequency ω that makes the net series reactance posed by the output tank $L_{\rm s}$, $C_{\rm s}$, and load inductance $L_{\rm load}$ provide a desired constant value $X_{\rm net}$. At center operating frequency $\omega_{\rm c}$ and $X_{\rm load} = j0\,\Omega$,

$$
X_{\rm net} = \omega_{\rm c}L_{\rm s} - \frac{1}{\omega_{\rm c}C_{\rm s}}. \tag{9}
$$

For other $X_{\rm load} = \omega L_{\rm load} \neq j0\,\Omega$, by selecting ω, we want

$$
\omega L_{\rm s} - \frac{1}{\omega C_{\rm s}} + X_{\rm load} = X_{\rm net}. \tag{10}
$$

In this way, for a given $R_{\rm load}$, control angle β and fundamental power P_1 range only depend on the resistive load (in the range $R_{\rm min} \sim R_{\rm max}$). Similar circuit operation and waveforms can be maintained irrespective of the load reactance. Thus,

$$
P_1 = \frac{1}{2}\frac{|V_1|^2 R_{\rm load}}{X_{\rm net}^2 + R_{\rm load}^2} \tag{11}
$$

is constant. This will be verified in Figs. 9 and 10 later.

We can use frequency modulation to make the net reactance posed by the tank and the load be some desired value $X_{\rm net}$. $X_{\rm load}$ can be inductive or capacitive as long as the operating frequency ω makes $X_{\rm net}$ constant. While we do not pursue it here, we note that other means - such as switched reactance banks or phase-switched impedance modulation (e.g., [5, 6]) - can be used to set $X_{\rm net}$ while operating at a fixed frequency.

III. Zero-Voltage Switching Conditions

The proposed wide-range power amplifier architecture is able to maintain ZVS for all inverter devices across load and power conditions; this is achieved by charging and discharging switch capacitances $C_{\rm sw}$ by $i_{\rm zvs}$ and $i_{\rm load}$ during dead times δ_1, δ_2, and δ_3.

A. Current Modeling

Modeling $i_{\rm zvs}$ and $i_{\rm load}$ is important for predicting ZVS conditions.

Because the voltage across $L_{\rm zvs}$ is approximately a square wave (albeit with nonzero rise and fall times, as seen in Fig. 6, the current flow through $L_{\rm zvs}$ is an approximately symmetric triangle waveform that can be expressed as:

$$
i_{\rm zvs} = \begin{cases} \frac{2I_{\rm zvs,\,pk}}{\pi}\omega t - I_{\rm zvs,\,pk}, & 0 + k\cdot 2\pi \le \omega t < \pi + k\cdot 2\pi \\ -\frac{2I_{\rm zvs,\,pk}}{\pi}\omega t + 3I_{\rm zvs,\,pk}, & \pi + k\cdot 2\pi \le \omega t < 2\pi + k\cdot 2\pi \end{cases} \tag{12}
$$

with $I_{\rm zvs,\,rms} = \frac{1}{\sqrt{3}}I_{\rm zvs,\,pk}$ and $I_{\rm zvs,\,pk} = \frac{V_{\rm dc}T_{\rm s}}{4L_{\rm zvs}}$.

As long as the quality factor Q of the load branch is high enough, for example, $Q = 5$, the load current $i_{\rm load}$ can be represented as

$$
i_{\rm load} = I_{\rm load,\,pk}\cos(\omega t + \phi_1 - \phi_{\rm load}) \tag{13}
$$

where $I_{\rm load,\,pk} = \frac{|V_1|}{\sqrt{R_{\rm load}^2 + X_{\rm net}^2}}$ and $\tan\phi_{\rm load} = \frac{X_{\rm net}}{R_{\rm load}}$. $|V_1|$ is the fundamental component from (1) or (5).

B. Dead Times and ZVS

ZVS is very important for high-frequency and very-high-frequency power conversion. For practical voltage-mode class D power amplifiers, there are dead times in control sequences as seen in Fig. 7 to enable switch capacitances to losslessly charge and discharge, so that the switches can have zero-voltage turn-on. There are three dead-times: δ_1, δ_2, and δ_3 that need to be considered in the wide-range voltage-mode class D power amplifier.

1) δ_1: Consider the commutation of current from S_5 to S_1 with S_3 held on as shown in Figs. 8(j), 8(a), and 8(b). During δ_1, $v_{\rm a1} = v_{\rm a2}$. The combination of $i_{\rm zvs}$ and $i_{\rm load}$ charge $C_{\rm sw5}$ and discharge $C_{\rm sw1}$. S_1 turns on at zero voltage when $v_{\rm a1} = v_{\rm a2} = V_{\rm dc}$. Assume $v_{\rm a1} = v_{\rm a2} = v_1(t)$,

$$
i_{\rm Csw1} + i_{\rm Csw5} = -i_{\rm zvs} - i_{\rm load} \tag{14}
$$

where

$$
i_{\rm Csw1} = C_{\rm sw1}\frac{d(v_1 - V_{\rm dc})}{dt} = C_{\rm sw1}\frac{dv_1}{dt}
$$

and

$$
i_{\rm Csw5} = C_{\rm sw5}\frac{d(v_1 - 0)}{dt} = C_{\rm sw5}\frac{dv_1}{dt}.
$$

With the integration during δ_1,

$$\int_0^{V_{\rm dc}} (C_{\rm sw1}+C_{\rm sw5})dv_1 = -\int_0^{\delta_1/\omega} (i_{\rm zvs}+i_{\rm load})dt. \quad (15)$$

The precise solution can be derived from

$$\omega(C_{\rm sw1}+C_{\rm sw5})V_{\rm dc} = -\int_0^{\delta_1} [i_{\rm zvs}(\omega t)+i_{\rm load}(\omega t)]d(\omega t). \quad (16)$$

Regarding $i_{\rm zvs}(\omega t) \approx i_{\rm zvs}(0) = -I_{\rm zvs,\,pk}$ and $i_{\rm load}(\omega t) \approx i_{\rm load}(0) = I_{\rm load,\,pk}\cos(\phi_1-\phi_{\rm load})$ from (12) and (13) during δ_1, a linear approximation can be

$$\omega(C_{\rm sw1}+C_{\rm sw5})\frac{V_{\rm dc}}{\delta_1} = I_{\rm zvs,\,pk} - I_{\rm load,\,pk}\cos(\phi_1-\phi_{\rm load}). \quad (17)$$

Assuming $C_{\rm sw1} = C_{\rm sw5} = C_{\rm sw}$ (i.e., equal effective switch capacitances),

$$\delta_1 = \frac{2\omega C_{\rm sw}V_{\rm dc}}{\frac{V_{\rm dc}T_{\rm s}}{4L_{\rm ZVS}} - \frac{|V_1|}{\sqrt{R_{\rm load}^2+X_{\rm net}^2}}\cos(\phi_1-\arctan\frac{X_{\rm net}}{R_{\rm load}})} \quad (18)$$

where $|V_1|$ can be calculated from (1) without considering the dead times for simplicity. Then

$$\delta_1 = \frac{2\omega C_{\rm sw}}{\frac{T_{\rm s}}{4L_{\rm ZVS}} - \frac{\frac{2\sqrt{2}}{\pi}\sqrt{1-\cos\beta}}{\sqrt{R_{\rm load}^2+X_{\rm net}^2}}\cos(\phi_1-\arctan\frac{X_{\rm net}}{R_{\rm load}})} \quad (19)$$

For ZVS turn-on of S_1, there is no requirement on the current direction of $i_{\rm load}$ as long as $I_{\rm zvs,\,pk} > I_{\rm load,\,pk}\cos(\phi_1-\phi_{\rm load})$. δ_1 is almost load independent.

2) δ_2: Consider commutation of current from S_3 to S_5 with S_1 held on, as shown in Figs. 8(b), 8(c), and 8(d). $i_{\rm load}$ charges $C_{\rm sw3}$ and discharges $C_{\rm sw5}$. S_5 turns on at zero voltage when $v_{\rm a2}=0$. Assuming $v_{\rm a2} = v_2(t)$,

$$i_{\rm Csw3} + i_{\rm Csw5} = i_{\rm load} \quad (20)$$

where

$$i_{\rm Csw3} = C_{\rm sw3}\frac{d(V_{\rm dc}-v_2)}{dt} = -C_{\rm sw3}\frac{dv_2}{dt}$$

and

$$i_{\rm Csw5} = C_{\rm sw5}\frac{d(0-v_2)}{dt} = -C_{\rm sw5}\frac{dv_2}{dt}$$

With the integration during δ_2,

$$\int_{V_{\rm dc}}^0 -(C_{\rm sw3}+C_{\rm sw5})dv_2 = \int_{\beta/\omega}^{(\beta+\delta_2)/\omega} i_{\rm load}(t)dt. \quad (21)$$

The precise solution can be derived from

$$\omega(C_{\rm sw3}+C_{\rm sw5})V_{\rm dc} = \int_{\beta}^{(\beta+\delta_2)} i_{\rm load}(\omega t)\,d(\omega t) \quad (22)$$

Regarding $i_{\rm load}(\omega t) \approx i_{\rm load}(\beta) = I_{\rm load,\,pk}\cos(\beta+\phi_1-\phi_{\rm load})$ from (12) and (13) during δ_2, a linear approximation can be made

$$\omega(C_{\rm sw3}+C_{\rm sw5})\frac{V_{\rm dc}}{\delta_2} = I_{\rm load,\,pk}\cos(\beta+\phi_1-\phi_{\rm load}) \quad (23)$$

Similarly,

$$\delta_2 = \frac{2\omega C_{\rm sw}}{\frac{\frac{2\sqrt{2}}{\pi}\sqrt{1-\cos\beta}}{\sqrt{R_{\rm load}^2+X_{\rm net}^2}}\cos(\beta+\phi_1-\arctan\frac{X_{\rm net}}{R_{\rm load}})} \quad (24)$$

where we again assume all switch capacitances are equal.

For ZVS turn-on of S_5, $i_{\rm load}(\beta)$ has to be positive. δ_2 is load dependent.

3) δ_3: Consider commutation of current from S_1 to S_3 with S_5 held on, as shown in Figs. 8(d), 8(e), and 8(f), $i_{\rm zvs}$ charges $C_{\rm sw1}$ and discharges $C_{\rm sw3}$. S_3 turns on at zero voltage when $v_{\rm a1}=0$. Assuming $v_{\rm a1} = v_3(t)$,

$$i_{\rm Csw1} + i_{\rm Csw3} = i_{\rm zvs} \quad (25)$$

where

$$i_{\rm Csw1} = C_{\rm sw1}\frac{d(V_{\rm dc}-v_3)}{dt} = -C_{\rm sw1}\frac{dv_3}{dt}$$

and

$$i_{\rm Csw3} = C_{\rm sw3}\frac{d(0-v_3)}{dt} = -C_{\rm sw3}\frac{dv_3}{dt}.$$

With the integration during δ_3,

$$\int_{V_{\rm dc}}^0 -(C_{\rm sw1}+C_{\rm sw3})dv_3 = \int_{\pi/\omega-\delta_3/\omega}^{\pi/\omega} i_{\rm zvs}(t)\,dt. \quad (26)$$

The precise solution can be derived from

$$\omega(C_{\rm sw1}+C_{\rm sw3})V_{\rm dc} = \int_{\pi-\delta_3}^{\pi} i_{\rm zvs}(\omega t)\,d(\omega t). \quad (27)$$

Regarding $i_{\rm zvs}(\omega t) \approx i_{\rm zvs}(\pi) = I_{\rm zvs,\,pk}$ from (12) and (13) during δ_3, a linear approximation can be

$$\omega(C_{\rm sw1}+C_{\rm sw3})\frac{V_{\rm dc}}{\delta_3} = I_{\rm zvs,\,pk} \quad (28)$$

Similarly,

$$\delta_3 = \frac{8\omega L_{\rm ZVS}C_{\rm sw}}{T_{\rm s}} \quad (29)$$

For ZVS turn-on of S_3, there is no requirement of $i_{\rm load}(t)$ during δ_3 at all. δ_3 is fully load-independent.

In practice, δ_1 and δ_3 can overlap with each other or contain each other. The rise of $v_{\rm a1}$ and the fall of $v_{\rm b1}$ can happen at the same time. The fall of $v_{\rm a1}$ and the rise of $v_{\rm b1}$ can happen at the same time as well. Time intervals of Figs 8(j) and 8(a); Figs 8(e) and 8(f) can be combined together.

IV. Design Procedure and Example

Here we sketch out one possible design procedure for the proposed inverter. Given the input dc voltage $V_{\rm dc}$, it is desired to realize an output power range from $P_{\rm min}$ to $P_{\rm max}$ for a load range from $R_{\rm min}$ to $R_{\rm max}$ with an example reactive component from 0 to $\omega L_{\rm load,\,max}$.

For example, consider an example with $V_{\rm dc} = 300\,{\rm V}$, $P_{\rm min} = 300\,{\rm W}$, $P_{\rm max} = 3000\,{\rm W}$, a 4 X resistive load range, i.e., $R_{\rm max}/R_{\rm min} = 4$, a reactive load component from $j\,0\,\Omega$ to $+j\,15\,\Omega$, and the minimum loaded quality factor $Q_{\rm min} = 5$ of the load branch ($C_{\rm s}$, $L_{\rm s}$, $R_{\rm load}$, and $L_{\rm load}$), e.g., as determined by waveform purity and/or frequency range considerations,

TABLE I
A PRACTICAL REALIZATION EXAMPLE

f	$12.76 \sim 13.56\,\text{MHz}$	V_{dc}	300 V
R_{load}	$4 \sim 19\,\Omega$	L_{load}	$0 \sim 187\,\text{nH}$
P_1	$0.3 \sim 3\,\text{kW}$	C_{sw}	80 pF
L_{zvs}	140 nH	L_{net}	91.4 nH
L_{s}	$1.5\,\mu\text{H}$	C_{s}	97.8 pF

and center operating frequency $f_{\text{c}} = 13.56\,\text{MHz}$, parameters can be determined as follows and concluded in Table I.

A. Frequency Selection

Because of the variable reactive load, (e.g., inductive L_{load} as shown in Fig. 1), the operating frequency may be selected to keep net reactance X_{net} formed by the output tank and load reactance constant. As illustrated in (10), the operating frequency is

$$\omega = \frac{\omega_{\text{c}} L_{\text{net}} + \sqrt{(\omega_{\text{c}} L_{\text{net}})^2 + 4(L_{\text{s}} + L_{\text{load}})/C_{\text{s}}}}{2(L_{\text{s}} + L_{\text{load}})} \tag{30}$$

where $\omega_{\text{c}} L_{\text{net}} = \omega_{\text{c}} L_{\text{s}} - 1/\omega_{\text{c}} C_{\text{s}} = X_{\text{net}}$, which is used to achieve ZVS of the switches. By selecting the operating frequency as per (30), P_1 in (11) is invariant to L_{load} but depends on R_{load}. Also, with high-Q filtering from the output tank, the shape of the relevant operating waveforms remain the same for a given R_{load} as will be shown in Figs. 9 and 10 for different L_{load}.

B. Initialization

Considering the case $X_{\text{net}} = 0\,\Omega$ and neglecting ZVS consideration of dead times, the average power may be approximated as that owing to the fundamental current: $P_1 = \frac{4}{\pi^2} \frac{V_{\text{dc}}^2 (1 - \cos\beta)}{R_{\text{load}}}$. For our example, this results in $R_{\text{max}} = 24\,\Omega$ to have the full power range over the full load range when $\beta_{\text{max}} = 180°$.

C. Inductors and Capacitors

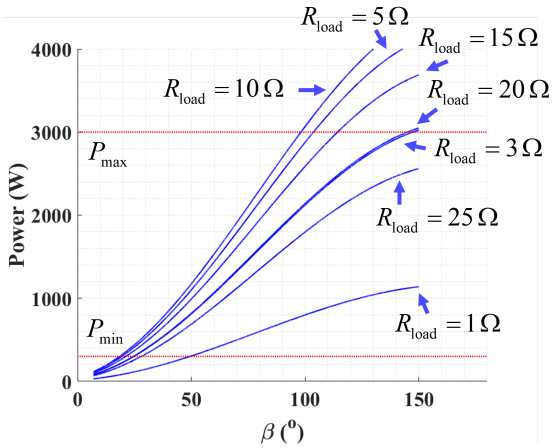
With $Q_{\text{min}} = 5$, $R_{\text{max}} = 24\,\Omega$, and $\omega_{\text{c}} = 2\pi \times 13.56\,\text{Mrad/s}$, the output tank can be calculated from

$$\begin{aligned} L_{\text{s}}'/C_{\text{s}} &= Q_{\text{min}}^2 \times R_{\text{max}}^2; \\ L_{\text{s}}'\, C_{\text{s}} &= 1/\omega_{\text{c}}^2. \end{aligned} \tag{31}$$

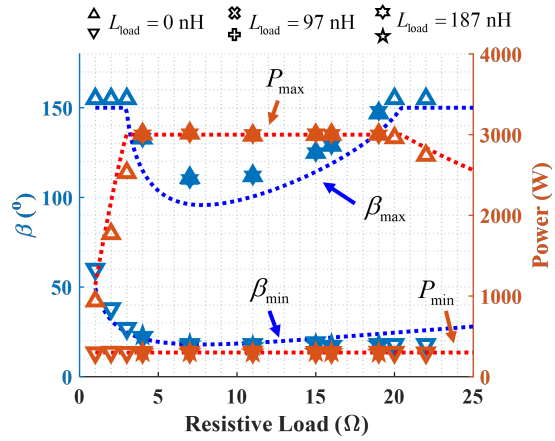
We have $L_{\text{s}}' = 1.41\,\mu\text{H}$ and $C_{\text{s}} = 97.8\,\text{pF}$. $L_{\text{s}} = L_{\text{s}}' + L_{\text{net}}$ where $L_{\text{net}} = X_{\text{net}}/\omega_{\text{c}}$ can be determined to achieve ZVS with $C_{\text{sw}} = 80\,\text{pF}$ during the dead time δ_2 for ZVS. We select $L_{\text{net}} = 91.4\,\text{nH}$ by simulation.

D. Load Range

Given the known variables and requirements, we can plot the relationship among power P_1, β, and R_{load} from (8) when considering ZVS dead times $\delta_1 = \delta_3 = 9°$ and $\delta_2 = 25°$ and $X_{\text{net}} = 7.67\,\Omega$, as shown in Fig. 9. From Fig. 9(a), we can see a specific β range for R_{load} in the range of R_{min} to R_{max}



(a) Power range for different β and R_{load} from (8). To achieve the full power range $R_{\text{min}} = 3\,\Omega$ and $R_{\text{max}} = 20\,\Omega$.



(b) Achievable power range for β within the limits under different R_{load}. The lines come from the theoretical analysis. The single points come from simulation with consideration of different L_{load}.

Fig. 9. The relationship among power, β, and R_{load} for the practical realization.

to meet the power range of 0.3 to 3 kW. Here, $R_{\text{min}} = 3\,\Omega$ and $R_{\text{max}} = 20\,\Omega$. Fig. 9(b) illustrates the relationship among P_1, β, and R_{load} differently. For the load range from 3 to $20\,\Omega$, we are able to achieve the full power range within the practical β range. Too big and too small R_{load} cannot achieve the maximum power because of the limitation of β_{max}. Those single data points come from simulation data with consideration of L_{load}, which will be illustrated later.

V. Simulation Verification

A simulation of an example design is done for 12 cases with parameters in Table I. The load and power for the 12 cases are as follows: R_{load} =4 Ω or 19 Ω; P_1 =300 W or 3000 W; L_{load} =0 nH, 97 nH, or 187 nH.

Those single data points in Fig. 9(b) follows the trends of control angles β and fundamental power P_1 under different R_{load}, which verifies the analytical equations. From simulation, $R_{\text{min}} = 4\,\Omega$ and $R_{\text{max}} = 19\,\Omega$ while from the theoretical result, $R_{\text{min}} = 3\,\Omega$ and $R_{\text{max}} = 20\,\Omega$, which can achieve a 4.75X resistive load range in simulation for the full power range.

The difference comes from the load-dependent dead times in simulation while we have fixed values in the theoretical analysis in Section IV. The simulated waveforms are shown in Fig. 10. Together with Fig. 9(b), we can observe that the waveforms and datapoints from different reactive loads almost overlap with each other, which verifies that as long as the resistive load is the same, the power and operation remains unchanged. Fig. 10 also shows the typical voltage and current waveforms, which match with our theoretical analysis. $v_{\text{a1-b1}}$ in Fig. 10(a) and i_{zvs} in Fig. 10(b) remain unchanged with different load conditions and power levels. Modulated waveforms $v_{\text{a2-b2}}$ with different β from Fig. 10(c) can achieve the full power range P_{min} to P_{max} for the full load range R_{min} to R_{max}. Because of the high enough quality factor in the load branch, current waveforms i_{load} are sine waves, as seen in Fig. 10(d).

Thus, the β modulation can modulate power and manage the resistive load variations while the dynamic frequency modulation can manage the reactive load variations in the wide-range voltage-mode class D power amplifier, as shown in Fig. 5.

VI. Conclusion

The operating principles of the wide-range voltage-mode class D power amplifier are illustrated through idealized and practical realizations by both qualitative and quantitative analysis. ZVS conditions are derived through analytical expressions. A design example followed by the design procedure enables a practical realization. The simulation verification shows that the wide-range voltage-mode class D power amplifier can achieve $300 \sim 3000$ W across a resistive load range of $4 \sim 19\,\Omega$ and an inductive load range from $0 \sim 187$ nH with a fixed input voltage of 300 V and a frequency range of $12.76 \sim 13.56$ MHz.

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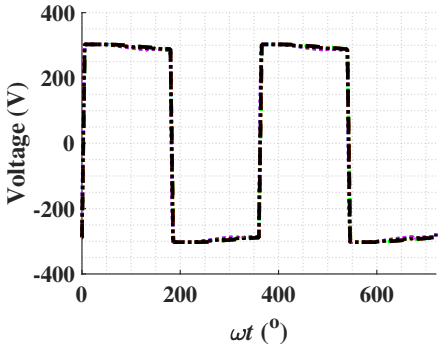
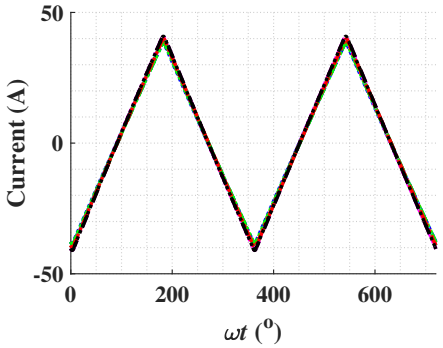
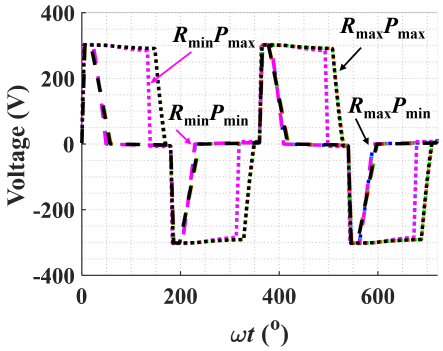


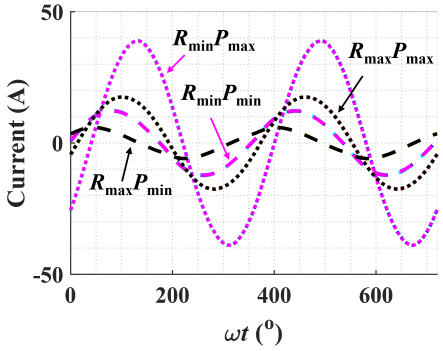
(a) $v_{\text{a1-b1}}$.



(b) i_{zvs}.



(c) $v_{\text{a2-b2}}$.



(d) i_{load}.

Fig. 10. Simulation waveforms for the wide-range voltage-mode class-D power amplifier under different 12 load conditions with V_{dc} =300 V. The power is either P_{min} =300 W or P_{max} =3000 W; the resistive load is either $R_{\text{min}} = 4\,\Omega$ or $R_{\text{max}} = 19\,\Omega$; the inductive load is X_{load} =0 Ω @ 13.56 MHz, X_{load} =8 Ω @ 13.12 MHz, or X_{load} =15 Ω @ 12.76 MHz.