Soft-Switched Pulsed Bias Plasma Supply System

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***Abstract*—Radio Frequency (RF) generators are essential as bias voltage sources in plasma-enhanced semiconductor manufacturing processes. Employing pulsed waveforms to generate plasma offers significant improvements in manufacturing precision. However, producing these waveforms is challenging due to the need for high voltages (in the kV range), high frequencies (hundreds of kHz to low MHz), precise timing, and broadband frequency content. Traditional methods to generate these waveforms are constrained by semiconductor voltage ratings, resulting in either low-voltage outputs or complex circuits to achieve higher pulse voltages. This work introduces a simple and compact method for generating pulsed bias voltages for plasma processing, enabling reduced loss compared to the more complex systems previously described in the literature. The approach synthesizes the pulsed waveform at a low, convenient voltage and then uses an auto-transformer to step up the voltage to the desired level. A coaxial cable-based transformer having low leakage inductance is developed to provide scaling with sufficient fidelity across a wide frequency range. Zero voltage switching (ZVS) is achieved on all devices, ensuring low-loss operation. The proposed system is validated through a lab bench prototype that generates pulses of 2.1 kV at 400 kHz. The proposed system further offers both adjustable pulse duty ratio and slew rate, providing enhanced control and versatility for various applications.**

***Index Terms*—Capacitively coupled plasma (CCP), pulse power generation, soft switching.**

I. Introduction

Future semiconductor manufacturing technologies must enable further miniaturization and increased production throughput of integrated circuits [1]. Essential to these advancements is the improved control of plasma-enhanced semiconductor manufacturing processes, such as plasma etching and plasma-enhanced chemical vapor deposition (PECVD). Plasma generation involves applying an RF power source across gases within a plasma chamber, as illustrated for a capacitively coupled plasma (CCP) in Figure 1a. This power source, known as the bias voltage, facilitates energetic ion bombardment of the substrate (wafer) and is a primary control mechanism for the ion energy [2]. A CCP system can be modeled as a series resistor-capacitor branch with a sheath region represented by a capacitive element, C_{sheath}, and a resistive element R_{plasma}, which sets the real output power [3].

Traditionally, plasma generation employs a sinusoidal RF signal, with modulation of ion energies through adjustments in the bias waveform's amplitude and frequency. However, this approach results in a broadband ion energy distribution function (IEDF) within the CCP, which limits etch feature profiles, etch selectivity, and the quality of PECVD films [5], [6]. In contrast, using a pulsed RF signal — a focal point of research in recent years [1] — produces a narrower IEDF, as seen in Figure 1b, enhancing etch selectivity and overall performance. Its output power is modulated via the pulse duty cycle and amplitude [5].

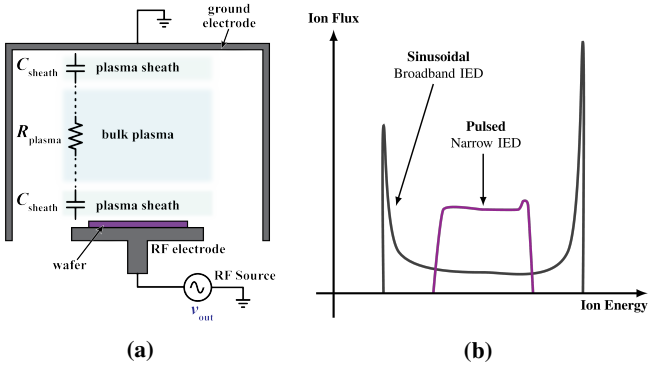


Fig. 1: (a) A representation of a capacitively coupled plasma chamber; (b) IEDFs for a traditional sinusoidal waveform and pulsed waveform [4].

Generating pulsed bias waveforms for capacitively coupled plasma presents significant challenges. It requires high-frequency operation and high voltages that often exceed typical device ratings. Several techniques have been proposed for generating these waveforms. A straightforward method involves feeding the desired waveform into a linear amplifier, such as the Class-A amplifier used in [4]. However, this technique suffers from poor efficiency.

Another approach is to directly synthesize the pulse from a high-voltage dc source using current and voltage source inverters. Various techniques have been demonstrated in both literature and patents. [7] and [8] use a switch-mode inverter with multiple variable dc sources to set the output voltage. A half-bridge inverter structure to generate a positive pulse across the CCP load is patented in [9]. In [10], a current-source type pulse generator is developed, which uses series-stacked devices to maintain a high input voltage.

A multi-level inverter structure can be used to generate pulses with larger amplitudes for a given semiconductor device voltage rating. These topologies enable the use of low-voltage-rated devices but require more complex control [11]–[13]. Both [14] and [15] utilize a neutral-point clamped type inverter structure to accommodate a larger input dc supply voltage,

thereby generating higher amplitude pulses.

Series stacking of devices and multi-level inverters are the dominant techniques to produce higher voltage pulses. However, both methods suffer from high system complexity, component count, and costs. Therefore, a need exists for a simple, compact, and inexpensive approach for generating bias pulsed waveforms.

This work presents the Bias Pulser, a pulsed bias waveform generator that is simpler and more compact than the methods previously described in the literature and which enables low-loss zero-voltage switching of the devices to be achieved. The pulsed waveform is shaped at a convenient, low voltage with a soft-switched inverter and then stepped up via an auto-transformer. This technique enables the use of lower-voltage semiconductor switching devices and leverages low-leakage magnetics design techniques to realize an auto-transformer with reduced output voltage ringing and electromagnetic interference (EMI).

Section II presents the proposed system topology, detailing the circuit operation and component selection. In Section III, a bench-top prototype of the Bias Pulser is developed to drive an equivalent model nominal plasma load. Section IV showcases experimental waveforms generated by the Bias Pulser system, accompanied by performance analysis. Finally, Section V concludes the paper.

II. Proposed Bias Pulser System

The Bias Pulser circuit design consists of a half-bridge inverter used to generate the pulsed waveform across the primary of the auto-transformer, with the output of the auto-transformer connected to the CCP load. The inverter's output voltage capability is determined by the maximum blocking voltage of the MOSFETs and the auto-transformer turns ratio. Low loss is achieved by leveraging the transformer's magnetizing current for zero-voltage switching across all devices.

A. Topology and Control

The circuit topology of the proposed Bias Pulser is depicted in Figure 2. The half-bridge inverter, consisting of MOSFETs Q_1 and Q_2 — each shown with their inherent body diode and output capacitance — produces a bipolar pulsed waveform at the node labeled v_x. The high and low side amplitudes of the pulse are defined by the dc voltage sources V_1 and V_2, respectively. If desired, either V_1 or V_2 can be replaced by a clamping capacitor. The node v_x is located on the primary side of a (tapped) auto-transformer winding. Given that this application - the generation of capacitively coupled plasma - does not require galvanic isolation, the use of an auto-transformer provides additional gain for a given amount of winding loss.

The auto-transformer is designed to have a specific magnetizing inductance L_μ (as seen from the primary winding), which facilitates soft switching of the MOSFET devices. The relative values of input voltage sources V_1 and V_2 are selected to maintain volt-second balance over the magnetizing inductance; balance is maintained automatically if one of the input supplies is replaced by a clamping capacitor. The slew rate of the pulsed waveform is dictated by the dead time required to achieve ZVS. It is easily modified by tuning the equivalent value of L_μ to suit varying application needs.

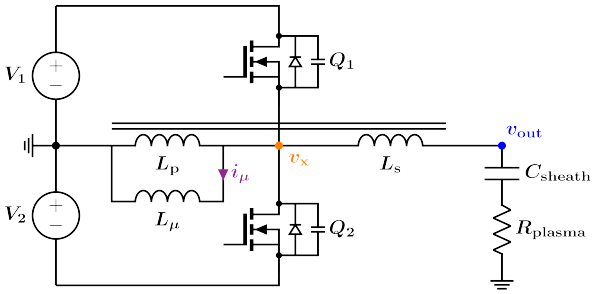


Fig. 2: Bias Pulser circuit topology.

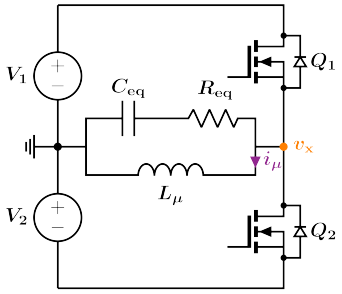


Fig. 3: Simplified ac equivalent circuit model for the Bias Pulser.

B. Circuit Analysis

To streamline the circuit analysis, a simplified circuit model is presented in Figure 3. The simplification involves reflecting the RC equivalent plasma load to the primary side of the transformer, according to the transformer's turns ratio, and re-referencing the MOSFET device capacitances C_Q1 and C_Q2 to ground. The turns ratio N for a step-up auto-transformer is defined as $(N_\mathrm{p} + N_\mathrm{s})/N_\mathrm{p}$, where N_p is the number of turns on the primary winding and N_s is the number of turns on the secondary winding. Thus, the reflected load impedance is $C_\mathrm{sheath,ref} = N^2 C_\mathrm{sheath}$ and $R_\mathrm{plasma,ref} = R_\mathrm{eq} = (1/N^2) R_\mathrm{plasma}$.

As the circuit analysis focuses on the dynamic behavior of the Bias Pulser circuit, we can examine the circuit through an ac perspective, with dc voltage sources replaced by short circuits. In this configuration, the MOSFETs' output capacitances C_Q1 and C_Q2 appear also in parallel with the magnetizing inductance.

In many applications, the plasma resistance is negligible compared to the impedance of the capacitive sheath and is thus excluded from the analysis. The equivalent system capacitance C_eq can then be described by the parallel combination of $C_\mathrm{sheath,ref}$, C_Q1, and C_Q2.

The operation of the Bias Pulser, using the simplified circuit shown in Figure 3, comprises four distinct stages that repeat periodically. The high and low side switches operate alternately, separated by a period of dead time. This dead time

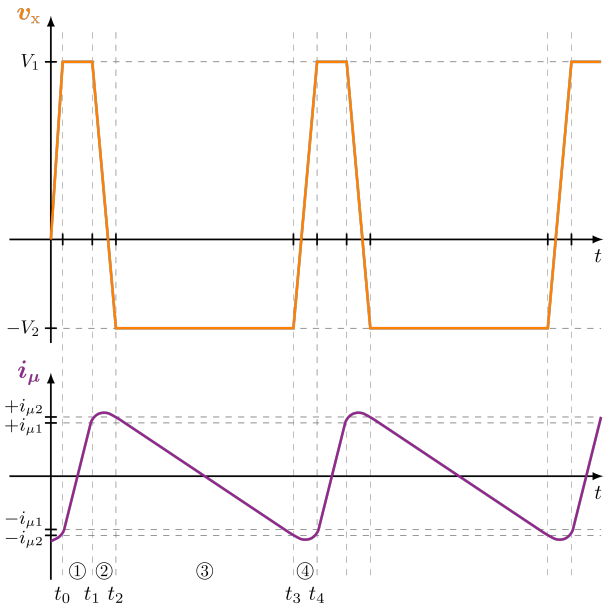


Fig. 4: Relative inverter switching node and magnetizing inductor current waveforms.

	Node Voltage (v_x)	**Inductor Current (i_μ)**
Stage ①	V_1	$\frac{V_1}{L_\mu}t - i_{\mu 1}$
Stage ②	$A_1\sin(\omega_0 t) + B_1\cos(\omega_0 t)$	$\frac{1}{\omega_0 L_\mu}[B_1\sin(\omega_0 t) - A_1\cos(\omega_0 t)] + C_1$
Stage ③	$-V_2$	$-\frac{V_2}{L_\mu}t + i_{\mu 2} + \frac{V_2}{L_\mu}t_2$
Stage ④	$A_2\sin(\omega_0 t) + B_2\cos(\omega_0 t)$	$\frac{1}{\omega_0 L_\mu}[B_2\sin(\omega_0 t) - A_2\cos(\omega_0 t)] + C_2$

$$A_1 = \frac{V_1\cos(\omega_0 t_2)+V_2\sin(\omega_0 t_1)}{\sin(\omega_0(t_1-t_2))} \quad A_2 = -\frac{V_1\cos(\omega_0 t_3)+V_2\cos(\omega_0 t_4)}{\sin(\omega_0(t_3-t_4))}$$

$$B_1 = -\frac{V_1\sin(\omega_0 t_2)+V_2\cos(\omega_0 t_1)}{\sin(\omega_0(t_1-t_2))} \quad B_2 = \frac{V_1\sin(\omega_0 t_3)+V_2\sin(\omega_0 t_4)}{\sin(\omega_0(t_3-t_4))}$$

$$C_1 = i_{\mu 1} + \frac{A_1\cos(\omega_0 t_1)-B_1\sin(\omega_0 t_1)}{\omega_0 L_\mu} \quad C_2 = -i_{\mu 2} + \frac{A_2\cos(\omega_0 t_3)-B_2\sin(\omega_0 t_3)}{\omega_0 L_\mu}$$

TABLE I: Bias pulse generator circuit equations for pulsed waveform voltage and inductor current, where $\omega_0 = \frac{1}{\sqrt{L_\mu C_{eq}}}$.

occurs when both switches are turned off or when clamping occurs through the MOSFET body diode. The corresponding relative waveforms for the node v_x and the magnetizing inductor current i_μ are illustrated in Figure 4.

Stage ① $(t_0 - t_1)$: This stage begins with switch Q_1 on, while Q_2 is off, clamping the node v_x to the top power supply V_1. The switch Q_1 remains on until the rising inductor current i_μ reaches the reference current $+i_{\mu 1}$, signaling the start of Stage 2.

Stage ② $(t_1 - t_2)$: This stage begins with Q_1 turning off. The inductor current begins to flow through the capacitor C_{eq}, which ensures a ZVS turn-off as the voltage across Q_1 begins to rise in a resonant manner. Both switches Q_1 and Q_2 remain off for the remainder of the stage. The inductor L_μ continues to resonate with the capacitor C_{eq} until the output voltage v_x drops to the negative rail $-V_2$. Subsequently, the body diode of switch Q_2 begins conducting and clamps v_x to the bottom supply. The switch Q_2 can then be turned on while the diode is conducting, facilitating a zero voltage turn-on and leading into Stage 3.

Stage ③ $(t_2 - t_3)$: Mirroring Stage 1, Stage 3 involves switch Q_2 remaining on, with v_x clamped to the negative rail voltage $-V_2$. The inductor current i_μ decreases until it reaches the reference current $-i_{\mu 2}$, signaling the start of Stage 3.

Stage ④ $(t_3 - t_4)$: This stage is analogous to Stage 2. It begins with switch Q_2 turning off, which requires the inductor current to flow through the capacitor. This ensures the voltage across Q_2 rises in a resonant manner, enabling ZVS turn-off. With both switches remaining off, the voltage v_x rises until it reaches V_1. This forces the body diode of Q_1 to begin conducting, clamping v_x to the positive rail. As the body diode conducts, Q_1 is turned on with ZVS turn-on, restarting the cycle.

The semiconductor manufacturing application dictates the duration of each operational stage. Table I provides the equations describing these waveforms. User-defined parameters include the duration of each operational stage, the equivalent capacitance C_{eq}, and the voltage level of one of the two input power supplies.

The value of the magnetizing inductance L_μ is particularly critical, as it directly influences pulse rise and fall times. To achieve a faster slew rate, a smaller L_μ is required; however, it must still be large enough to facilitate ZVS of all devices. The method for selecting L_μ is explored in Section II-C.

Additionally, L_μ must maintain a volt-second balance throughout each cycle to avoid core saturation. Therefore, the ratio between the two dc input power supplies V_1 and V_2 is carefully chosen to ensure that the time integral of the pulse waveform remains zero over a complete cycle.

C. Component Value Selection

The Bias Pulser's ability to adjust pulse duty ratio and slew rate relies on precise selection of key component values, particularly the magnetizing inductance L_μ. This inductance is crucial not only for achieving the desired slew rate but also for ensuring ZVS. Additionally, the ratio between the input power supplies must satisfy the volt-second balance across L_μ. A system of equations, derived from the circuit dynamics detailed in Table I and the volt-second balance in Equation 1, is used to determine these values.

The volt-second balance equation for the magnetizing inductance L_μ, based on the equation in Table I, is as follows:

$$\begin{aligned} 0 = {} & V_2(t_2 - t_3) - V_1(t_0 - t_1) + \\ & \frac{1}{\omega_0}\Big[A_1\Big(\cos(\omega_0 t_1) - \cos(\omega_0 t_2)\Big) + A_2\Big(\cos(\omega_0 t_3) - \cos(\omega_0 t_4)\Big) \\ & - B_1\Big(\sin(\omega_0 t_1) - \sin(\omega_0 t_2)\Big) - B_2\Big(\sin(\omega_0 t_3) - \sin(\omega_0 t_4)\Big)\Big] \end{aligned} \quad (1)$$

Equation 2 defines the necessary system of equations to appropriately determine each component's value in the Bias Pulser system. A practical approach to solving these equations involves setting V_1, C_{eq}, t_0, t_1, t_2, and t_4 as known variables. The value of C_{eq} is determined by the CCP load, the transformer turns ratio, and the output capacitances of the

MOSFETs. The timing parameters are chosen based on the desired pulse shape.

$$\begin{cases} \omega_0 & = 1/\sqrt{L_\mu C_{\text{eq}}} \\ i_{\mu 1} & = \frac{V_1}{L_\mu} t_1 - i_{\mu 1} \\ i_{\mu 2} & = \frac{1}{\omega_0 L_\mu}[B_1 \sin(\omega_0 t_2) - A_1 \cos(\omega_0 t_2)] + C_1 \\ -i_{\mu 2} & = -\frac{V_2}{L_\mu} t_3 + i_{\mu 2} + \frac{V_2}{L_\mu} t_2 \\ -i_{\mu 1} & = \frac{1}{\omega_0 L_\mu}[B_2 \sin(\omega_0 t_4) - A_2 \cos(\omega_0 t_4)] + C_2 \\ 0 & = V_2(t_2 - t_3) - V_1(t_0 - t_1) + \\ & \quad \frac{1}{\omega_0}\Big[A_1\Big(\cos(\omega_0 t_1) - \cos(\omega_0 t_2)\Big) + A_2\Big(\cos(\omega_0 t_3) - \cos(\omega_0 t_4)\Big) \\ & \quad -B_1\Big(\sin(\omega_0 t_1) - \sin(\omega_0 t_2)\Big) - B_2\Big(\sin(\omega_0 t_3) - \sin(\omega_0 t_4)\Big)\Big] \end{cases} \tag{2}$$

The remaining unknowns are L_u, V_2, t_3, $i_{\mu 1}$, $i_{\mu 2}$, and ω_0. The values of $i_{\mu 1}$ and $i_{\mu 2}$ are important for determining the maximum magnetizing current, which is a key factor in transformer design. The calculated value of V_2 establishes a relative ratio between V_1 and V_2 that satisfies the volt-second balance equation. In practice, the sum of V_1 and V_2 must remain within the blocking voltage capabilities of the MOSFETs, and adjustments may be required to ensure compatibility.

Due to the complexity of the non-linear equations derived from the circuit's operation, analytical solutions are not feasible. Therefore, computer-aided numerical solvers, specifically 'lsqnonlin' available in MATLAB, are used to find solutions.

To correct any discrepancies in the selected values of V_1 and V_2, a dc blocking capacitor can be placed in series with either supply or directly with the primary transformer winding. The capacitor will charge to maintain volt-seconds balance across L_μ in periodic steady state operation. The capacitor must be sized to store sufficient energy and withstand the maximum voltage required.

Alternatively, one of the two dc power supplies can be entirely substituted with a capacitor. For example, the bottom supply V_2 is replaced by a capacitor while the top supply V_1 remains. Conversely, the bottom supply can be retained while replacing the top supply with a capacitor. L_μ will charge the capacitor to the voltage necessary to achieve volt-second balance. The capacitor must be large enough to store the required energy for a full cycle, clamping the voltage as needed. It may be beneficial to add a damping leg (e.g., a resistor or a resistor-capacitor series combination) in parallel with this capacitor to mitigate any ac oscillations, as discussed in the context of filter design in [16].

III. Bias Pulser Design

A laboratory prototype was designed and constructed based on load and operating specifications for a nominal plasma load, with the design framework outlined in Table II. These parameters guided the selection of the remaining circuit components, transformer gain, and inverter control configurations.

A. Inverter Design

To generate high-voltage pulses while minimizing the required transformer gain and its associated losses, the inverter employs silicon carbide (SiC) devices. 1200 V SiC devices were chosen for their affordability and availability. However, for reliability, these devices are derated to approximately 60% of their maximum blocking voltage, resulting in an allowed dc bus voltage of 700 V. Consequently, a transformer gain of 3 is required to achieve 2.1 kV pulses. The key components selected for the Bias Pulser prototype are listed in Table III. A Kepco KLP 600-4-1.2k programmable dc power supply is used for V_1. V_2 is replaced with a $10\,\mu$F capacitor in parallel with a $3\,\text{k}\Omega$ resistor.

Parameter	Symbol	Value
Output Voltage (peak-to-peak)	V_{out}	2.1 [kV]
Pulse Frequency	f_{sw}	400 [kHz]
Target Duty Ratio	D	10 - 30 [%]
Pulse Rise/Fall Time	t_{d}	100 - 300 [ns]
Equivalent Plasma Load	R_{plasma}	1 [Ω]
Equivalent Sheath Load	C_{sheath}	300 [pF]

TABLE II: Design specifications for Bias Pulser bench prototype.

	Description	Manufacturer	Manufacturer Part
Inverter	SiC MOSFETs	STMicroelectronics	SCT020H120G3AG
	Gate Driver	Infineon	1ED3124MU12HXUMA1
	Gate Isolated PSU	Recom Power	R2S-2405/R2S-2415
Plasma Load	Capacitors	KYOCERA AVX	27 x 1206GXXXXXAT
	Resistors	Bourns Inc.	10 x CRM2512-FX-10R0ELF

TABLE III: Key components used for the Bias Pulser inverter and equivalent plasma load prototypes.

Considerable effort was directed at optimizing the inverter's commutation loop to minimize additional leakage inductance in this high-frequency design, which would otherwise lead to increased ringing on the pulsed waveform and elevated EMI. Efforts to reduce the commutation loop's length were inspired by the design study in [17]. The selected layout for the half-bridge inverter, which uses a single TO-263 packaged SiC MOSFET per switch position, places the two devices in line with a return path directly below on an adjacent circuit board layer, as shown in Figure 5. Due to the soft-switched nature of the design, minimal cooling is required, so top-side surface-mount heat sinks are used.

B. Transformer Design

The Bias Pulser employs a 1:3 auto-transformer to step up the 700 V peak-to-peak pulses generated by the inverter to 2.1 kV peak-to-peak across the plasma load. A critical challenge in using a transformer for this application is ensuring that it can accurately scale the pulsed voltage with high fidelity across the broad frequency spectrum of the pulsed waveform. To this end, the transformer's design is focused on minimizing parasitic effects that could disrupt waveform synthesis, particularly aiming to reduce leakage inductance, which can contribute to poor scaling, voltage ringing, and increased EMI.

Minimizing transformer leakage inductance requires limiting the area where leakage fields can form between the primary and secondary windings, while also adhering to voltage breakdown requirements. A practical approach to achieve this is through the use of a coaxial cable, where one conductor

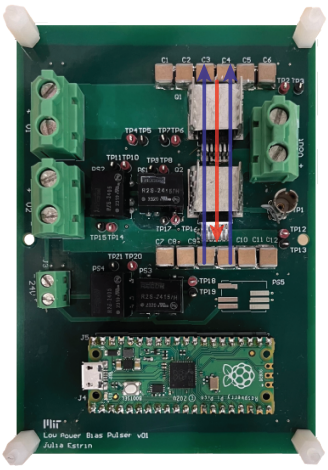


Fig. 5: Bias Pulser inverter PCB, with arrows highlighting the commutation loop.

acts as the primary winding and the other as the secondary winding.

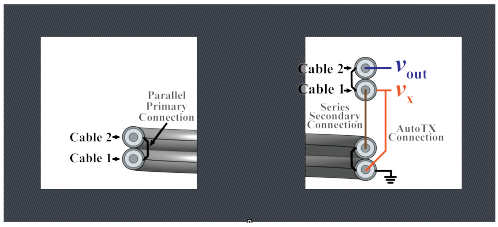
To achieve a gain larger than 1, multiple sections of coaxial cable are employed. The primary winding is formed by connecting one conductor from each section in parallel, while the secondary winding is constructed by series connecting the other conductors from each section. For the implementation highlighted in this work, the outer conductors of the coaxial cables are connected in parallel to form the primary winding, while the inner conductors are connected in series as the secondary winding, as illustrated in Figure 6.

The only unlinked flux between the windings is confined to the space between the inner and outer conductor. Additionally, the coaxial cable provides consistent spacing between the two conductors along the entire cable's length, enabling a simple conversion of the geometrically defined distributed inductance of Equation 3 into lumped parameters that can be included in circuit analysis and simulation:

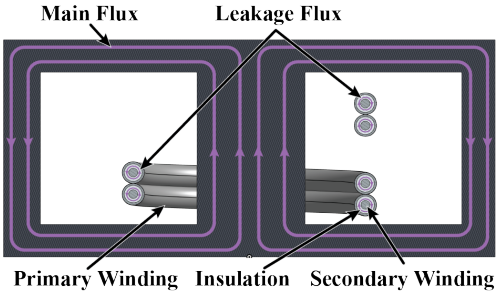
$$L'_{\text{coax}} = \frac{\mu}{2\pi} \ln\left(\frac{b}{a}\right), \tag{3}$$

where L'_{coax} is the distributed inductance of the coaxial cable per unit length, μ is the permeability of the insulating material, a is the inner conductor radius, and b is outer conductor inner radius. Therefore, the transformer's leakage inductance is the distributed inductance of the cable multiplied by the cable length. Adjusting the cable geometry allows for controllable and predictable leakage inductance.

The 1:3 auto-transformer used for this design uses custom-made coaxial cables and an EI core configuration with specifications outlined in Table IV and shown in Figure 7. Based on Equation 3, the theoretical primary side leakage inductance for this single-turn, two-cable auto-transformer is approximately $5\,\text{nH}$. However, due to the additional external connections needed for the coaxial cables, the actual leakage inductance increases to $45\,\text{nH}$.



(a) Connections required to configure the coaxial cable as an auto-transformer, with a single-turn primary winding formed by the parallel connection of the outer conductors of the two cable sections and a secondary winding formed by the series connection of the inner conductors.



(b) Flux paths within the coaxial cable transformer, showing that leakage flux is confined to the region between the inner and outer conductors.

Fig. 6: A 1:3 auto-transformer constructed using 2 coaxial cable sections.

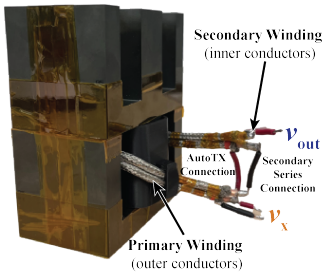


Fig. 7: The constructed 1:3 auto-transformer with specifications detailed in Table IV. The top E core is flipped to be used as a I core section.

	Parameter	Part Description	
Construction	Inner Conductor	Litz - 3000 strand/46 AWG	
	Insulation	10 mil thick FEP heat shrink	
	Outer Conductor	3 mm Copper Braid	
	EI Core	4 x TDK 100/60/28 N97	
	Parameter	**Symbol**	**Value**
Specifications	Turn Ratio	N	$1:3$
	Primary Turn Count	N_p	1
	Magnetizing Inductance	L_μ	$1-10\,\mu\text{H}$
	Leakage Inductance	L_{lk}	$45\,\text{nH}$
	Insulation Level		$10\,\text{kV}$ HiPot

TABLE IV: 1:3 autotransformer components and key specifications.

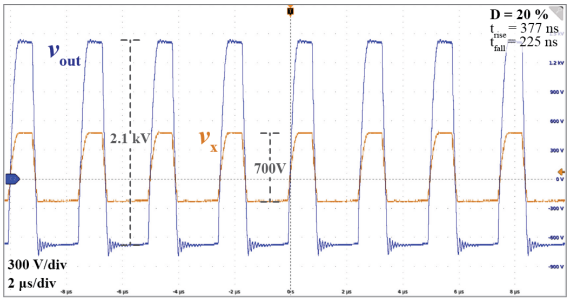
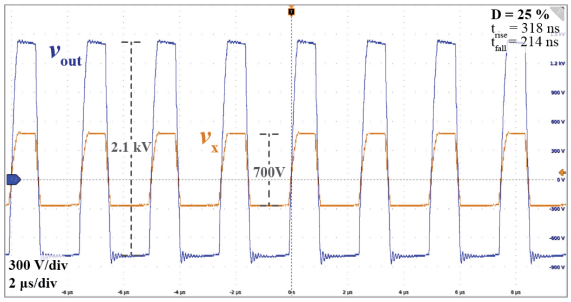
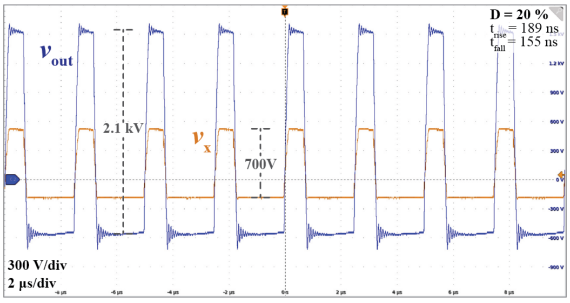
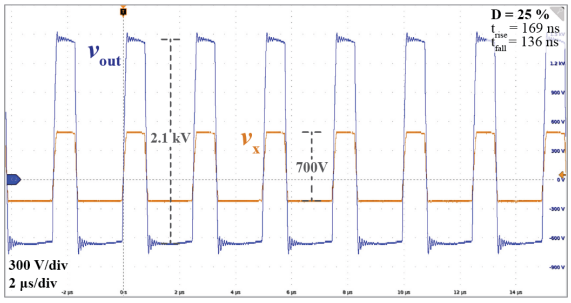
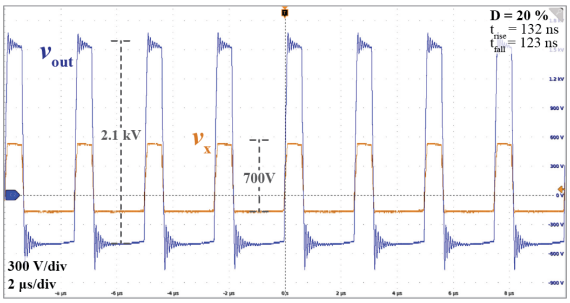
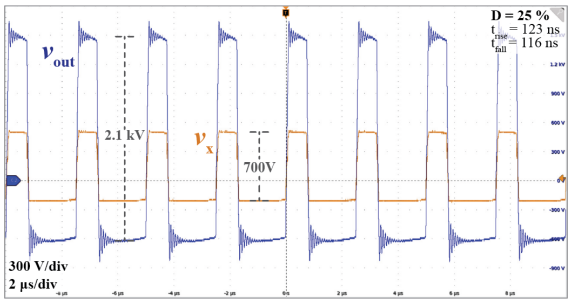
L_μ	$D = 20\%$	$D = 25\%$
7 μH $l_{gap} = 0.03\,\text{mm}$		
5.5 μH $l_{gap} = 0.06\,\text{mm}$		
4.5 μH $l_{gap} = 0.09\,\text{mm}$		

TABLE V: Oscilloscope screenshots of exemplar experimental waveforms for Bias Pulser, performing with various duty ratios and slew rates. The orange waveforms are measured at the primary of the auto-transformer and the blue waveforms are seen across the load.

IV. Experimental Results

The Bias Pulser was operated to meet the design specifications outlined in Table II. For benchtop testing, a representative equivalent plasma load model of 300 pF and 1 Ω was used, as shown in Figure 8.

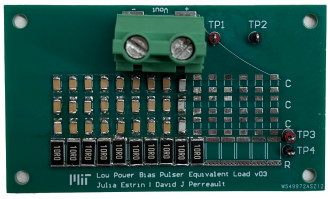


Fig. 8: Equivalent RC plasma load used for benchtop testing, where $C_{\text{sheath}} = 301\,\text{pF}$ and $R_{\text{plasma}} = 1.01\,\Omega$.

The duty ratio is modulated through open-loop control of the MOSFETs' gate drive signals, and, if necessary, adjustments of the input power supplies to ensure the transformer receives the maximum voltage allowable by the inverter (700 V rail-to-rail). This work defines the duty ratio as the pulse high time divided by the period, t_{high}/T. The slew rate is controlled by tuning of the magnetizing inductance L_μ. For these experiments, L_μ is set by adjusting the core gap length. If dynamic tuning of the equivalent magnetizing inductance is required, a switched bank of inductors could be connected in parallel with L_μ.

Table V provides example waveforms with duty ratios of 20% and 25%. Three values of L_μ - 7 μH, 5.5 μH, and 4.5 μH - are used with rise and fall times of approximately 300 ns, 150 ns, and 125 ns, respectively.

The Bias Pulser maintained ZVS throughout its entire operating range, evidenced by smooth transitions between the top and bottom dc voltage rails. The output waveforms exhibit appropriate gain with high fidelity and minimal ringing. For a given duty ratio, the slew rate of the pulse rise and fall time can be adjusted by tuning the value of L_μ. A smaller L_μ

allows for a higher slew rate of the pulse waveform, such that any reasonable slew rate can be achieved. A practical lower limit is set on the value of L_μ such that zero voltage switching is not compromised. Looking across a range of duty ratios for a single value L_μ, the slew rates slightly vary. This is due to the inherent coupling between the duty ratio and slew rate.

V. Conclusion

Using high-voltage pulsed waveforms to generate capacitively coupled plasma represents a transformative advancement for semiconductor manufacturing processes like plasma etching and plasma-enhanced chemical vapor deposition. These waveforms enable precise control over plasma energy, significantly enhancing manufacturing outcomes. However, traditional methods for generating these waveforms typically involve cumbersome, complex, and costly equipment. This paper introduces the Bias Pulser, an innovative approach to pulse generation utilizing a soft-switched half-bridge inverter operating at a low voltage, paired with a low-leakage-inductance auto-transformer. This method facilitates the generation of high-voltage pulsed waveforms for plasma applications with a compact, low-loss design.

The careful design of the Bias Pulser's PCB layout and associated magnetics allows for flexible, low-loss performance. The half-bridge inverter achieves zero voltage switching by utilizing the soft-switching current provided by the transformer's magnetizing inductance. The transformer design uses coaxial cables as windings, which confine leakage flux fields to the insulation between the inner and outer conductors, reducing transformer leakage inductance. Additionally, the system allows adjustable duty ratios and slew rates, managed through inverter control and adjustments to the magnetizing inductance.

Validation of this design was conducted using a laboratory bench prototype that drove an equivalent resistor-capacitor plasma load model ($C_{\text{sheath}} = 300\,\text{pF}$, $R_{\text{plasma}} = 1\,\Omega$). The prototype successfully generated pulsed waveforms with a peak-to-peak voltage of 2.1 kV at a frequency of 400 kHz. Demonstrations of these waveforms, featuring variable duty ratios and slew rates, effectively showcase the robust performance of the circuit and magnetic design.

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