2021 IEEE Energy Conversion Congress and Exposition (ECCE) | 978-1-7281-5135-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/ECCE47101.2021.9595412

# Non-Isolated DC-DC Converter Implementations Based on Piezoelectric Transformers

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***Abstract*—Piezoelectric transformers (PTs) offer several potential advantages for converter miniaturization, but most attempts to use them in dc-dc converters have included magnetic components or have demonstrated poor efficiencies. For converters relying only on a PT for energy storage, we demonstrate that specific topologies and switching sequences that effectively utilize the PT for energy storage can improve performance compared to standard resonant converter topologies. In this work, we systematically enumerate non-isolated dc-dc converter topologies and switching sequences that most efficiently utilize PTs as their only energy storage components. These proposed switching sequences are selected for high-efficiency behaviors (e.g. zero voltage switching (ZVS) and maximum PT cycle utilization), and we provide a model for estimating the PT's efficiency to aid evaluation of these implementations. We then validate these analyses with experimental data from an example prototype for one proposed switching sequence.**

## I. Introduction

The demand for smaller volume power electronics motivates investigation into alternative energy storage components for power conversion. Typical converters rely on magnetic energy storage components, but the achievable power densities of magnetics fundamentally decrease at low volumes and therefore limit converter miniaturization [1], [2]. Piezoelectrics, which can be realized as either single-port piezoelectric resonators (PRs) or multi-port piezoelectric transformers (PTs), are promising energy storage alternatives with more favorable power density capabilities at low volumes [3], [4]. PTs also offer the added benefits of galvanic isolation and inherent voltage conversion, making them more suitable for high step-up/step-down applications compared to PRs.

Despite their potential, PTs have mainly seen use in fluorescent backlight drivers and little use in power converters without auxiliary magnetics [5]. Magnetic-less converter designs that only use PTs for energy storage are proposed in [6]–[11], but these converters are based on standard resonant converter topologies and generally report limited whole-converter efficiencies. Systematic enumeration and downselection processes to identify dc-dc converter implementations that most efficiently use PRs and isolated PTs have been explored in [12] and [13], respectively. However, we hypothesize that non-isolated PT-based topologies may allow for a wider variety of switching sequences that better utilize the PT's resonant cycle, enabling higher efficiencies.

In this work, we systematically enumerate and downselect for non-isolated dc-dc converter topologies and switching sequences that best utilize PTs as their only energy storage components. We constrain this search for (1) high-efficiency behaviors such as zero voltage switching (ZVS) and all-positive instantaneous power transfer, and (2) practical characteristics such as voltage regulation capability and control simplicity. To evaluate the selected switching sequences, we also introduce charge transfer analysis for quantifying how the PT's resonant cycle is utilized and models for estimating the PT's ZVS region and efficiency. Finally, we validate these analyses with experimental data for one example converter implementation.

## II. Topologies

Fig. 1 shows a common-negative source-load system with three nodes ($V_{in}$, $V_{out}$, and *Gnd*) and a non-isolated PT represented by the Mason model [14]–[16]. We assume this configuration for topology enumeration, and we further assume a step-up PT with $N > 1$ (though a similar process can be conducted for step-down PTs). To begin enumerating potential topologies, we identify possible source/load connections for each of the three PT terminals. Each PT terminal can have:

- one source/load connection to $V_{in}$, $V_{out}$, or *Gnd* (three possibilities), creating a fixed node.
- two source/load connections switching between [$V_{in}$, *Gnd*], [$V_{out}$, *Gnd*], or [$V_{in}$, $V_{out}$] (three possibilities),

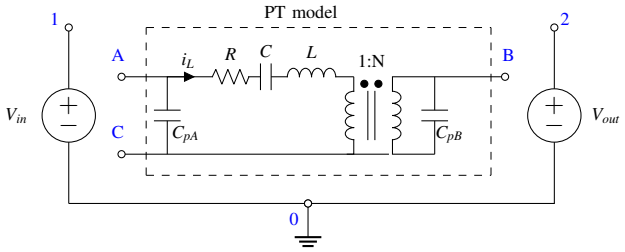


Fig. 1. Source-load system with non-isolated PT assumed for topology enumeration. Nodes have been labeled in blue by the convention introduced in Sections II and III.

This material is based upon work supported by Texas Instruments, the National Science Foundation Graduate Research Fellowship Program under Grant No. 1122374, and the MIT Undergraduate Research Opportunities Program.



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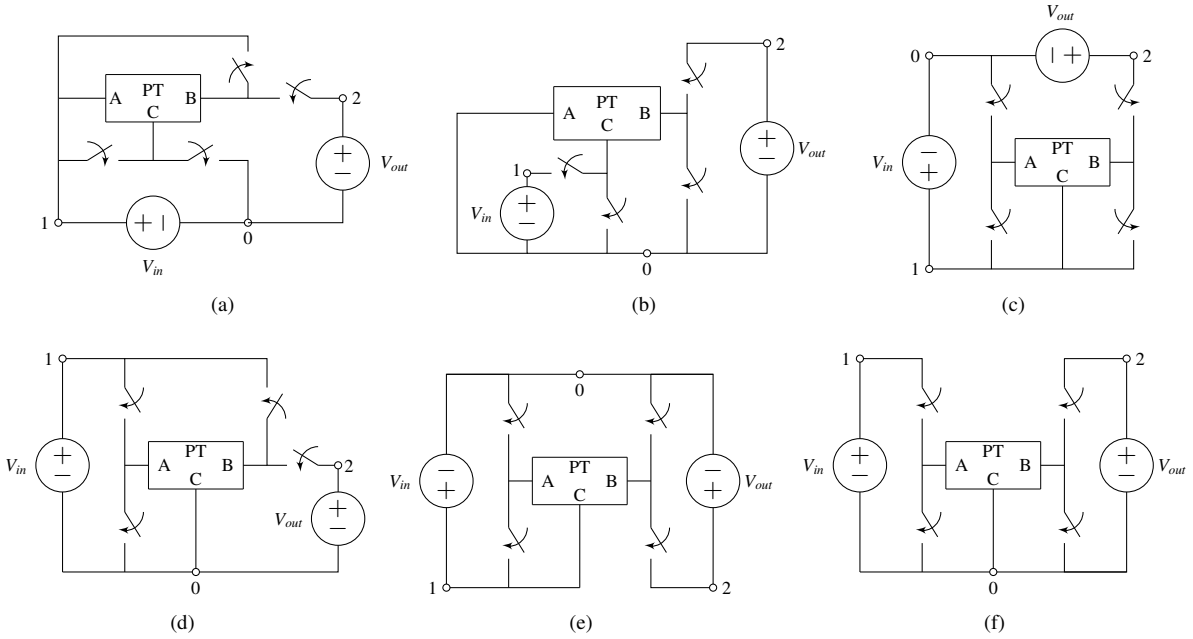


Fig. 2. Resulting five-connection topologies, all of which have switching sequences compatible with the constraints of Sections II and IV.

creating a switch node that requires two unidirectional-blocking switches.
- three source/load connections switching between [$V_{in}$, $V_{out}$, *Gnd*] (one possibility), requiring four unidirectional-block switches (two for the middle-voltage node connection).

We use the following labels for the PT terminals: $A$ for the input terminal, $B$ for the output terminal, and $C$ for the common terminal. For the assumed step-up PT, we also assume that $C_{pA}$, the capacitance between terminals $A$ and $C$, is significantly greater than $C_{pB}$, the capacitance between terminals $B$ and $C$ [*]. Combinations of the above connections yield almost 300 topologies with eight or fewer unidirectional-blocking switches. To reduce this set, we consider topologies following these constraints:

1) The topology contains a maximum of five connections to the source-load system across all terminals for simplicity.
2) The topology contains at least one connection to each of $V_{in}$ and $V_{out}$.
3) The topology contains no more than 1 fixed terminal.
4) Terminals $A$ and $C$ do not connect to $V_{out}$, since $V_{out} > V_{in}$ and $C_{pA} \gg C_{pB}$, (i.e., it would take an impractical length of time for $A$ or $C$ to resonate to $V_{out}$ for ZVS for step-up configurations)[†].

The resulting enumerated topologies (after the downselection processes of subsequent sections) are displayed in Fig. 2.

[*]As shown in the model of Fig. 1, we do not consider capacitance between $A$ and $B$ in this work.

[†]This constraint is specific to step-up configurations. For step-down configurations, terminals A and C should not connect to $V_{in}$.

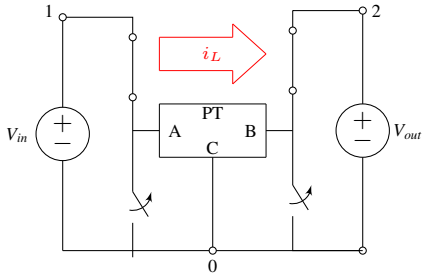


Fig. 3. The A1B2C0 stage realized with topology (f) in Fig. 2 by closing the top switches and opening the bottom switches. Since $A$ is connected to $V_{in}$ and $B$ is connected to $V_{out}$, this stage requires $+i_L$ to transfer power from input to output.

## III. Stages

We now enumerate potential *stages*, or specific PT terminal connection states, for each topology. Stages can be classified as:

- *Connected stages*: each PT terminal is connected to a node in the source/load system.
- *Transition stages*: at least one of the PT terminals is open-circuited, allowing its voltage to increase or decrease through resonance. More than one PT terminal may transition in a single transition stage.

To label connected stages, we list each terminal label ($A$, $B$, and $C$) followed by its connection number using the following scheme: 0 for *Gnd*, 1 for $V_{in}$, and 2 for $V_{out}$. For example, the stage A1B2C0 has terminal $A$ connected to $V_{in}$, terminal $B$ connected to $V_{out}$, and terminal $C$ connected to *Gnd* as shown in Fig. 3.

We constrain this enumeration for *all-positive instantaneous power transfer*, which means energy is always transferred unidirectionally from source to load. This constrains the polarity



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of $i_L$, the current through the inductor in the PT model (refer to Fig. 1), in each connected stage according to:

- Stages that require positive $i_L$ ($+i_L$): A0B2C0, A1B0C0, A1B0C1, A1B1C0, A1B2C0, A1B2C1
- Stages that require negative $i_L$ ($-i_L$): A0B0C1, A0B1C0, A0B1C1
- Stages with no $i_L$ requirement (act as either $+i_L$ or $-i_L$): A0B0C0, A1B1C1

We constrain each stage for unidirectional current to maximize PT cycle utilization, which enables higher efficiencies as detailed in [12], [13]. Stages that are not included in the above list can be eliminated by constraint 3 in Section II or conflicting $i_L$ requirements. With these possible stages, we next enumerate and downselect for suitable switching sequences.

## IV. Switching Sequences

We define a *switching sequence* as the specific order of stages that a converter cycles through to complete a switching period. To enumerate switching sequences, we focus only on connected stages and assume transition stages occur between each connected stage for ZVS. We therefore label a switching sequence by the order of its connected stages only (e.g. A0B2C0-A1B0C0-A0B0C1 is a six-stage sequence, including transition stages between each listed connected stage).

For control simplicity, we focus on switching sequences with a minimum number of stages. Since voltage regulation requires a six-stage sequence (three connected stages and three transition stages) as with PR-based converters [12], we choose to enumerate switching sequences that are permutations of 3 of the possible connected stages in a topology. This yields over 900 total sequences, which we then downselect based on the following constraints:

1) At least one stage of $+i_L$ and one stage of $-i_L$, for charge balance on terminal $C$ over a cycle.
2) At least two connected stages with energy transfer, for energy balance within the PT.
3) At least one connection to node 1 ($V_{in}$) and one connection to node 2 ($V_{out}$).
4) The required $i_L$ polarities of all the stages (including transition stages) fit sequentially in one resonant cycle (to be expanded upon below).
5) No two terminals are always tied together (or else the PT is effectively a two-terminal device).
6) The sequence enables voltage regulation capability beyond fixed voltage conversion ratios (to be expanded upon below).

Constraints 4 and 6 will be elaborated in the next two subsections. After filtering according to these constraints, we likewise eliminate duplicate switching sequences (i.e. the same sequence but with a different first stage).

### A. Single Resonant Cycle

As part of our downselection process, we examine the ability for each switching sequence to be completed in one resonant cycle of the LC branch in the PT as required by its $i_L$ polarities (for ZVS and all-positive instantaneous power transfer). To be completed in one resonant cycle, the $i_L$ polarities of a sequence must consist of only one sequential span of stages requiring $+i_L$ and one span of stages requiring $-i_L$. The $i_L$ polarities of connected stages (set by all-positive instantaneous power transfer) are defined in Section III. For transition stages, the $i_L$ polarity requirement for an *individual* terminal is determined by whether the terminal's voltage must increase or decrease to reach its next-stage voltage for ZVS, assuming $V_{out} > V_{in} > Gnd$. The $i_L$ polarity requirements for each transition are summarized as follows:

- Transitions requiring $+i_L$: A1 → A0, B0 → B2, B1 → B2, C0 → C1
- Transitions requiring $-i_L$: A0 → A1, B2 → B0, B2 → B1, C1 → C0

where $A1 \rightarrow A0$, for example, means terminal $A$ transitions from being connected to node 1 ($V_{in}$) to node 0 (*Gnd*).

Table I
Example Switching Sequence for Single Resonant Cycle Check

| A0B2C0 | Transition | A0B1C0 | Transition | A0B1C1 | Transition |
|---|---|---|---|---|---|
| + | o-o | - | oo+ | - | o+- |

With these requirements, we can label the $i_L$ polarities for conduction through or voltage transition at each terminal in a transition stage with + for $+i_L$, - for $-i_L$, or o for no change in polarity. We can apply these labels to check the $i_L$ polarities of the example sequence in Table I. The $i_L$ polarities of terminal $C$ in each stage in this example are (+, +, -, +, -, -). Since there are two spans of $+i_L$ and two spans of $-i_L$ for terminal $C$, this sequence cannot be completed in one resonant cycle (despite passing this same check for terminals $A$ and $B$).

### B. Ideal Voltage Regulation

We further downselect to switching sequences that are capable of the desired high-efficiency behaviors (e.g. ZVS and all-positive instantaneous power transfer) across wide voltage conversion ranges. A switching sequence's ideal voltage conversion range (i.e., not considering transition stages) can be calculated by enforcing charge and energy balance on the PT over the *connected* stages in a switching cycle.

Charge balance requires the net charge transferred by $i_L$ in $+i_L$ stages to equal the net charge transferred by $i_L$ in the $-i_L$ stages. For example, the charge balance equation for Sequence 5 (A1B2C0-A0B2C0-A0B1C0) is:

$$|q_1| + |q_3| = |q_5| \tag{1}$$

where $q_n$ is the charge transferred by $i_L$ in the nth stage. In this example, the 1st and 3rd stages are $+i_L$ stages (for all-positive instantaneous power transfer from the input and to the output), and the 5th stage is a $-i_L$ stage.

Energy balance requires the energy delivered from the source to equal the energy delivered to the load (in the ideal case). For the same example, the energy balance equation is:

$$|q_1|V_{in} + |q_5|\frac{V_{in}}{N} = |q_1|\frac{V_{out}}{N} + |q_3|\frac{V_{out}}{N} \tag{2}$$



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Table II
SUMMARY OF FIVE-CONNECTION SWITCHING SEQUENCES

| Sequence Number | Switching Sequence | Topology (Fig. 2) | Ideal $\frac{V_{out}}{V_{in}}$ Range | Charge Transfer Utilization Factors ($K$) | Voltage Ranges ($V_{ppA}$, $V_{ppB}$) |
|---|---|---|---|---|---|
| 1 | A1B1C0-A1B2C0-A1B1C1 | (a) | $N < \frac{V_{out}}{V_{in}} < \infty$ | $K_{in,A} = \frac{1}{2}$, $-\frac{1}{2} < K_{in,B} < 0$, $0 < K_{out} < \frac{1}{2}$ | $V_{in}$, $V_{out}$ |
| 2 | A0B2C0-A0B0C1-A0B0C0 | (b) | $N-1 < \frac{V_{out}}{V_{in}} < \infty$ | $K_{in,A} = \frac{1}{2}$, $K_{in,B} = -\frac{1}{2}$, $0 < K_{out} < \frac{1}{2}$ | $V_{in}$, $V_{out}$+$V_{in}$ |
| 3 | A1B1C1-A1B2C1-A0B1C1 | (c) | $1 < \frac{V_{out}}{V_{in}} < N+1$<br>$N+1 < \frac{V_{out}}{V_{in}} < \infty$* | $0 < K_{in,A} < \frac{1}{2}$, $K_{in,B} = \frac{1}{2}$, $K_{out} = \frac{1}{2}$<br>$K_{in,A} = \frac{1}{2}$, $0 < K_{in,B} < \frac{1}{2}$, $0 < K_{out} < \frac{1}{2}$* | $V_{in}$, $V_{out}$-$V_{in}$ |
| 4 | A1B1C0-A1B2C0-A0B1C0 | (d) | $N+1 < \frac{V_{out}}{V_{in}} < \infty$ | $K_{in,A} = \frac{1}{2}$, $0 < K_{in,B} < \frac{1}{2}$, $0 < K_{out} < \frac{1}{2}$ | $V_{in}$, $V_{out}$-$V_{in}$ |
| 5 | A1B2C0-A0B2C0-A0B1C0 | (d) | $1 < \frac{V_{out}}{V_{in}} < N+1$ | $0 < K_{in,A} < \frac{1}{2}$, $K_{in,B} = \frac{1}{2}$, $K_{out} = \frac{1}{2}$ | $V_{in}$, $V_{out}$-$V_{in}$ |
| 6 | A1B0C1-A1B2C1-A0B0C1 | (e) | $N < \frac{V_{out}}{V_{in}} < \infty$ | $K_{in,A} = \frac{1}{2}$, $K_{in,B} = 0$, $0 < K_{out} < \frac{1}{2}$ | $V_{in}$, $V_{out}$ |
| 7 | A1B2C0-A0B2C0-A0B0C0 | (f) | $0 < \frac{V_{out}}{V_{in}} < N$ | $0 < K_{in,A} < \frac{1}{2}$, $K_{in,B} = 0$, $K_{out} = \frac{1}{2}$ | $V_{in}$, $V_{out}$ |
| 8 | A1B0C0-A1B2C0-A0B0C0 | (f) | $N < \frac{V_{out}}{V_{in}} < \infty$ | $K_{in,A} = \frac{1}{2}$, $K_{in,B} = 0$, $0 < K_{out} < \frac{1}{2}$ | $V_{in}$, $V_{out}$ |

(*) $1 < \frac{V_{out}}{V_{in}} < N+1$ is the range when A1B1C1 is a $-i_L$ stage. $N+1 < \frac{V_{out}}{V_{in}} < \infty$ applies when A1B1C1 is a $+i_L$ stage.

The left hand side of the equation is the energy transferred from the source, and the right hand side is the energy delivered to the load.

Using (1) and (2), we derive an expression for the ideal voltage conversion range in terms of the charge transferred in the two connected stages of the same $i_L$ polarity ($q_1$ and $q_3$ in this example):

$$\frac{V_{out}}{V_{in}} = \frac{N|q_1| + |q_1| + |q_3|}{|q_1| + |q_3|} \tag{3}$$

Applying the limits of the two charge transfer terms (i.e., one term dominates while the other is negligible, and vice versa) leads to the ideal voltage conversion ratio range:

$$1 < \frac{V_{out}}{V_{in}} < N + 1 \tag{4}$$

The ideal voltage conversion ranges for all of the five-connection sequences are summarized in Table II. These sequences have also been filtered for their charge transfer utilization factors ($K$) as described in Section V-A. For easier reference, the sequences are numbered 1 through 8. It should be noted that transition-stage energy transfer and PT loss will skew these range limits in a realistic implementation, but these ideal ranges provide the designer with a simple estimate for each switching sequence's applicability.

## V. PT UTILIZATION

In the next two sections, we introduce methods for analyzing and comparing these switching sequences. A highly efficient PT-based converter must effectively utilize the PT's resonant cycle to transfer energy, and charge transfer analysis can be leveraged to evaluate these switching sequences' ZVS and efficiency capabilities. Below, we introduce these charge transfer analysis concepts.

### A. Charge Transfer Utilization Factor ($K$)

The switching sequences in Table II vary widely in how effectively they utilize the PT's resonant cycle to transfer energy. The charge transfer utilization factor ($K$) quantifies the productivity of the connected stages in a switching sequence with respect to a single port. Introduced in [12] and [13], $K$ is the fraction of a sequence's connected-stage charge transfer (by $i_L$) that sources energy from the input port or delivers energy to the output port of the converter. Since both the input terminal $A$ and the output terminal $B$ can connect to the $V_{in}$ node, we define $K_{in,A}$ and $K_{in,B}$ as the fraction of useful charge transfer sourced from the input port through terminals $A$ and $B$, respectively. In contrast, since only terminal $B$ can connect to the $V_{out}$ node (by Constraint 3 in Section II), we define a single $K_{out}$ as the fraction of useful connected-stage charge transfer delivered through the output port to the load.

As an example, $K_{in,B}$ for Sequence 5 can be calculated as:

$$K_{in,B} = \frac{|q_5|}{|q_1| + |q_3| + |q_5|} = \frac{1}{2} \tag{5}$$

where charge balance in connected stages requires $|q_1|+|q_3| = |q_5|$ [‡] The ranges for $K_{in,A}$, $K_{in,B}$, and $K_{out}$ for all of the five-connection sequences are included in Table II.

All of these sequences have either $K_{in,A}$ or both $K_{in,B}$ and $K_{out}$ fixed to allow for maximum PT cycle utilization while maintaining voltage regulation capability. If all three $K$ factors are fixed, the sequence cannot regulate voltage and thus is eliminated. Sequences with no fixed $K$ factors can regulate voltage but are eliminated due to greater control complexity and excess charge circulation as compared to sequences with at least one fixed $K$ factor.

### B. Total Charge Transfer

The total magnitude of charge transferred by $i_L$, $Q_{total}$, can be calculated with respect to the input or output port. [13] derives $Q_{total}$ at the output port (through terminal $B$'s perspective) for an isolated PT switching sequence. We can use this equation to calculate $Q_{tot}$ with respect to the output port for our non-isolated PT sequences because only terminal $B$ can connect to the $V_{out}$ node. Thus $Q_{total}$ with respect to the output port is:

$$Q_{total} = N\Big(\frac{P_{out}}{f K_{out} V_{out}} + 2C_{pB}V_{ppB}\Big) \tag{6}$$

[‡]Other sequences may contain stages where $B$ being tied to $V_{in}$ counters part of the energy sourced through $A$ (e.g. A1B1C0). The charges of these stages in this calculation must be subtracted.



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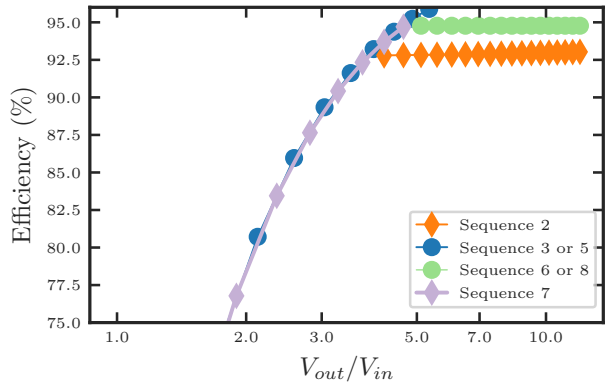


Fig. 4. Estimated efficiencies vs. $\frac{V_{out}}{V_{in}}$ for $V_{in} = 200$ V and $P_{out} = 10$ W., model parameters given in Table III

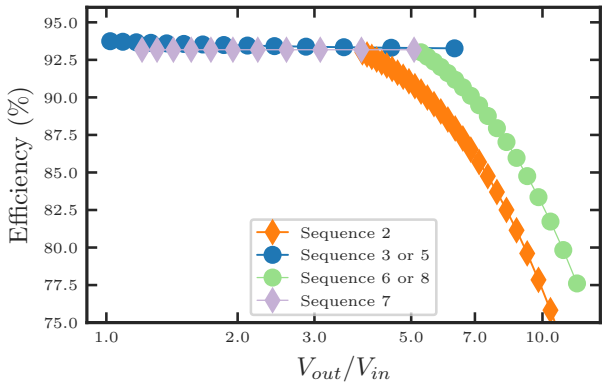


Fig. 5. Estimated efficiencies vs. $\frac{V_{out}}{V_{in}}$ for $V_{out} = 800$ V and $P_{out} = 10$ W., model parameters given in Table III

where the first term is the magnitude of charge transferred in connected stages and the second term is the magnitude of charge transferred in transition stages.

We can use a similar approach to calculate $Q_{total}$ with respect to the input port. However, since the non-isolated PT sequences allow terminal $B$ to interact with the input port, we now also consider how $B$ contributes to or counters the charge transfer from $A$'s perspective when making an input-side-referred calculation. $Q_{total}$ can be expressed as the sum of charge transfer in connected stages and in transition stages as:

$$Q_{total} = Q_{A,conn} + Q_{A,trans} \tag{7}$$

$Q_{A,conn}$, which is the connected-stage charge transfer into the PT through terminal $A$, can be written as:

$$Q_{A,conn} = \frac{Q_{in} - K_{in,B}\left(\frac{Q_{total}}{N} - Q_{B,trans}\right)}{K_{in,A}} \tag{8}$$

where $Q_{in}$ is the total charge sourced from the input port for energy transfer and $K_{in,B}\left(\frac{Q_{tot,in}}{N} - Q_{B,trans}\right)$ is the part of this charge transfer sourced through terminal $B$. Combining (7) and (8) yields the following input-side-referred expression for $Q_{total}$:

$$Q_{total} = \frac{Q_{in} + K_{in,A}Q_{A,trans} + K_{in,B}Q_{B,trans}}{K_{in,A} + \frac{K_{in,B}}{N}} \tag{9}$$

where $Q_{in} = \frac{P}{fV_{in}}$, $Q_{A,trans} = 2C_{pA}V_{ppA}$, and $Q_{B,trans} = 2C_{pB}V_{ppB}$.

### C. Zero Voltage Switching (ZVS) Regions

The ideal voltage conversion ranges derived in Section IV only consider connected-stage charge transfer. To ensure ZVS, we must also consider transition-stage charge transfer. The operating points that allow for ZVS, or the ZVS region, can be derived by equating (6) and (9):

$$\begin{aligned} Q_{total} &= N\left(\frac{P_{out}}{fK_{out}V_{out}} + 2C_{pB}V_{ppB}\right) \\ &= \frac{Q_{in} + K_{in,A}Q_{A,trans} + K_{in,B}Q_{B,trans}}{K_{in,A} + \frac{K_{in,B}}{N}} \end{aligned} \tag{10}$$

Equation 10 only holds across the applicable range(s) of $K$, which are provided by Table II for each sequence. This defines the achievable operating region with ZVS. As power increases, the boundary of the ZVS region approaches the ideal voltage conversion range asymptotes also included in Table II, where connected-stage charge transfer dominates.

## VI. Efficiency Estimation Model

Calculating the PT's exact efficiency is computationally intensive [12], [13]. In this section, we introduce a simpler method for estimating efficiency based on charge transfer analysis.

### A. Amplitude of PT Resonance ($I_L$) and Efficiency Estimation

The efficiency for any operating point can be estimated using the amplitude of resonance ($I_L$), or the amplitude of $i_L$. $I_L$ can be estimated by integrating $Q_{total}$, the magnitude of the total charge transferred by $i_L$ over one resonant cycle. If we assume $i_L$ is sinusoidal, then $Q_{total}$ and $I_L$ are related by:

$$I_L = \frac{\pi}{2} f Q_{total} \tag{11}$$

where $Q_{total}$ can be calculated with either (9) or (6) since they are equivalent. To provide an example, the amplitude of resonance for Sequence 5 can be calculated by substituting (6) into (11), resulting in:

$$I_L = \pi N\left(\frac{P_{out}}{V_{out}} + fC_{pB}(V_{out} - V_{in})\right) \tag{12}$$

Using $I_L$, we can estimate the efficiency for any operating point as:

$$\eta \approx \frac{1}{1 + \mathcal{LR}} \tag{13}$$

where $\mathcal{LR}$ is the loss ratio and is defined as:

$$\mathcal{LR} = \frac{P_{loss}}{P_{out}} = \frac{\frac{1}{2}I_L^2 R}{P_{out}} \tag{14}$$

Our estimation model uses the PT parameters from the manufacturer in Table III and only considers PT mechanical loss (and no other circuit losses). Figure 4 plots the efficiencies estimated by our model as a function of $\frac{V_{out}}{V_{in}}$ at constant $V_{in} = 200$ V and $P_{out} = 10$ W for all of the switching sequences except Sequences 1 and 4 (which require additional analysis)



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Table III
PT PARAMETERS [17]

| Parameter | Value from Manufacturer | Measured On-board Value |
|---|---|---|
| $C_{pA}$ | 960 pF | 1600 pF |
| $C_{pB}$ | 8 pF | 83 pF |
| $R$ | 24 Ω | 27 Ω |
| $L$ | 59 mH | 44 mH |
| $C$ | 60 pF | 72 pF |
| $N$ | 6 | 6 |
| $f_0$ | 84.6 kHz | 89.4 kHz |

Table IV
PROTOTYPE PARTS LIST

| Component | Part |
|---|---|
| Active Switch | EPC2012C |
| Schottky Diode | GB01ST06-214 |
| Gate Driver | UCC27611 |
| PT | SMSTF50P2S6 |

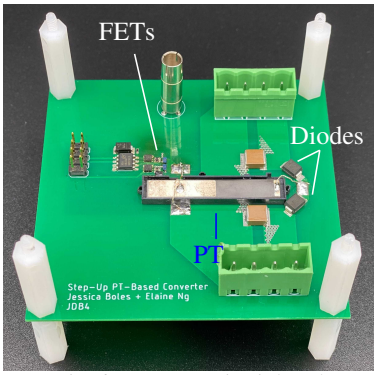

Fig. 6. Prototype circuit board.

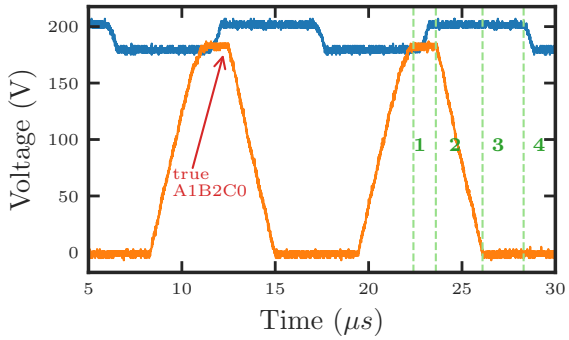

Fig. 7. Time-domain waveforms for $V_{in} = 180$ V, $V_{out} = 200$ V, $P_{out} \approx 900$ mW.

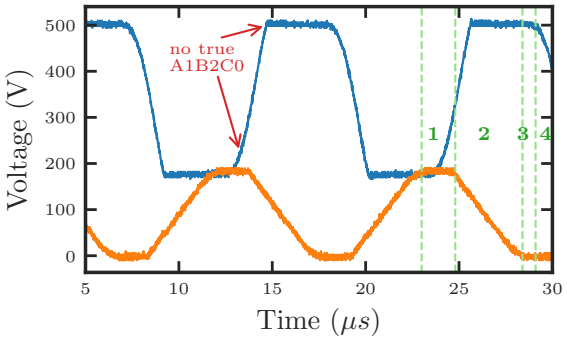

Fig. 8. Time-domain waveforms for $V_{in} = 180$ V, $V_{out} = 500$ V, $P_{out} \approx 900$ mW.

[§]. Figure 5 plots the estimated efficiencies as a function of $\frac{V_{out}}{V_{in}}$ at constant $V_{out} = 800$ V and $P_{out} = 10$ W for the same switching sequences. These plots show that these sequences vary widely in efficiency capability for a given operating point, but also that many sequences can provide voltage regulation with near-constant efficiency, which is advantageous for applications requiring wide voltage conversion ranges. This near-constant efficiency behavior is achieved for sequences 2, 6, and 8 regulating with the output port ($V_{in}$ is fixed), and for sequences 3, 5, and 7 regulating with the input port ($V_{out}$ is fixed).

### B. Peak Efficiency and Minimum Loss Ratio

To estimate peak efficiency, we can directly maximize $\eta$ (or minimize the loss ratio $\mathcal{LR}$) with respect to operating point parameters. For a switching sequence with a fixed $K_{out}$ (like Sequence 5), the loss ratio can be expressed as:

$$\mathcal{LR} = \frac{\pi^2 N^2 R}{2}\left(\frac{P_{out}}{4V_{out}^2 K_{out}^2} + \frac{fC_{pB}V_{ppB}}{V_{out}K_{out}} + \frac{f^2 C_{pB}^2 V_{ppB}^2}{P_{out}}\right) \tag{15}$$

which is minimized with respect to $P_{out}$ when:

$$P_{out} = 2fC_{pB}V_{ppB}V_{out}K_{out} \tag{16}$$

This operating point leads to a minimum loss ratio of:

$$\mathcal{LR}_{min} = \frac{\pi^2 N^2 RfC_{pB}V_{ppB}}{V_{out}K_{out}} \tag{17}$$

[§]The model does apply to Sequences 1 and 4, but a general expression must be calculated for the varying $K_{in,B}$ in these sequences using the method described in [12].

and a corresponding peak efficiency of:

$$\eta_{peak} = \left(1 + \frac{2\pi^2 N^2 RfC_{pB}V_{ppB}}{V_{out}}\right)^{-1} \tag{18}$$

It should be noted that some operating points corresponding to peak efficiency may be outside of the ZVS region for certain switching sequences. In these cases, the peak efficiency of the sequence is determined by the ZVS boundary.

## VII. EXPERIMENTAL RESULTS

We illustrate an example converter implementation using the commercially-available PT (STEMiNC's SMSTF50P2S6), described by the parameters in Table III. The prototype shown in Fig. 6 realizes Sequence 5 and uses topology (d) in Fig. 2, implemented on a two-layer board with the parts shown in Table IV. The switches for the half-bridge at terminal $A$ in topology (d) are implemented with GaN FETs, and the switches for the half bridge at terminal $B$ are implemented with diodes. The switches and diodes in particular are chosen to have small output capacitances as to not greatly increase the capacitance across the PT's input/output ports. The converter is powered by an isolated power supply and operated with open-loop control and a constant-voltage load. The switching times are tuned manually for each operating point for the switching sequence's high-efficiency behaviors (ZVS and all-positive instantaneous power transfer). Below, we present the waveforms and efficiency sweeps for this prototype and compare our experimental data with our predictions from the model, which considers the on-board measurements (including



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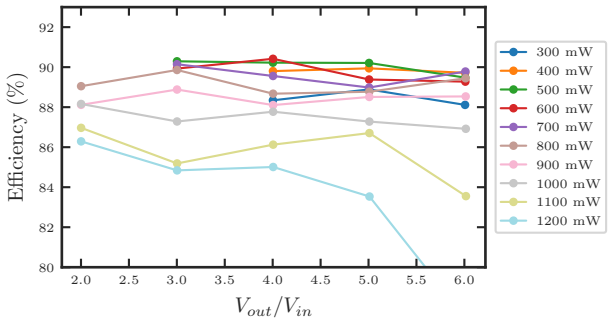


Fig. 9. Experimental whole-converter efficiencies vs. $\frac{V_{out}}{V_{in}}$ for the same $V_{out} = 360$ V and different power levels.

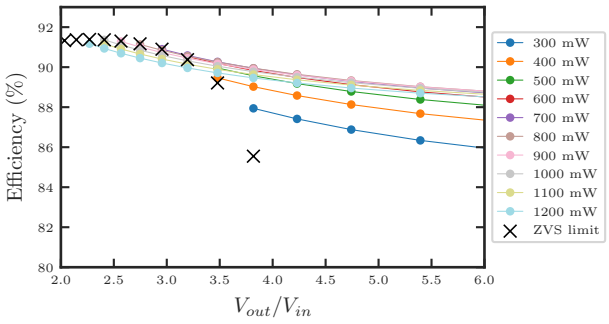


Fig. 10. Estimated PT efficiencies from model vs. $\frac{V_{out}}{V_{in}}$ for the same $V_{out} = 360$ V and different power levels.

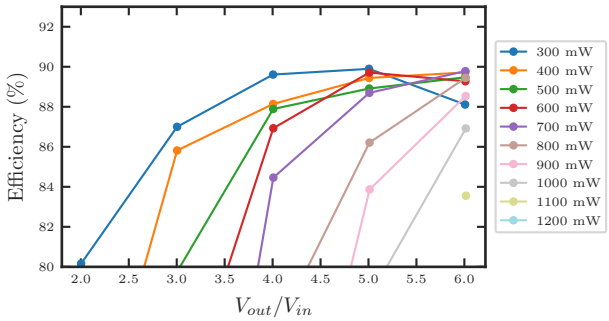


Fig. 11. Experimental whole-converter efficiencies vs. $\frac{V_{out}}{V_{in}}$ for the same $V_{in} = 60$ V and different power levels.

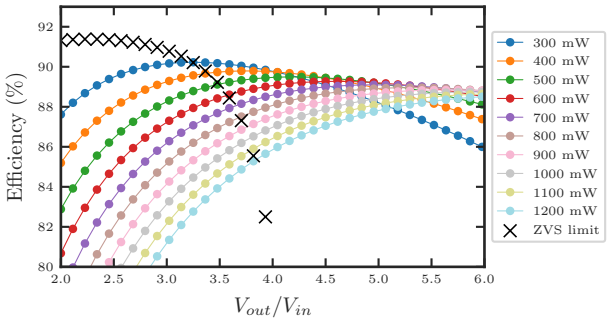


Fig. 12. Estimated PT efficiencies from model vs. $\frac{V_{out}}{V_{in}}$ for the same $V_{in} = 60$ V and different power levels.

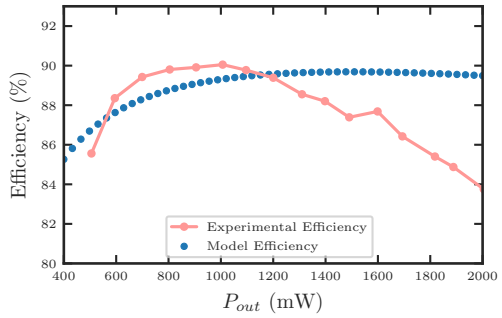


Fig. 13. Experimental whole-converter efficiencies and PT model efficiencies vs. $P_{out}$ for $V_{in} = 120$ V and $V_{out} = 500$ V.

switch capacitances) shown in Table III. Because the PT's parameters have high temperature dependence, all data points are collected shortly after powering up the prototype and not at thermal equilibrium.

### A. Waveforms

Fig. 7 shows the prototype's waveforms operating at $V_{in} = 180$ V, $V_{out} = 200$ V, and $P_{out} \approx 900$ mW, and Fig. 8 shows the prototype's waveforms operating at $V_{in} = 180$ V, $V_{out} = 500$ V, and $P_{out} \approx 900$ mW. These waveforms show that the converter operates as expected for the switching sequence. Sequence 5 consists of connected stages where $V_{pA} = (V_{in}, 0, 0)$, and for both waveforms, regions 1, 3, and 4 respectively show this specific ordering of connected stages. $V_{pB} = (V_{in}, V_{out})$ for Sequence 5, which is also demonstrated by both waveforms with $V_{pB} = V_{out}$ occurring during the input port's $+i_L$ stages. In Fig. 8, the length of region 3 is much shorter relative to the length of region 1 compared to the same stages in Fig. 7, which illustrates how the switching sequence uses these $+i_L$ stages to modulate $K_{in,A}$ for regulation. Fig. 8 also shows that the connected stages between the ports do not necessarily overlap temporally (i.e., there is no true A1B2C0 stage in Fig. 8, because $V_{pB}$ does not reach $V_{pB} = V_{out}$ before region 1 ends). In contrast, Fig. 7 shows a characteristic A1B2C0 stage since $V_{pB}$ reaches $V_{out}$ within the interval of $V_{pA} = V_{in}$.

### B. Efficiency

We next experimentally validate the model with data sweeps over $\frac{V_{out}}{V_{in}}$ for various power levels. Fig. 9 shows whole-converter efficiency as a function of $\frac{V_{out}}{V_{in}}$ at constant $V_{out} = 360$ V. Fig. 10 shows the PT efficiencies estimated from the model using the measured PT parameters in Table III for the same range of operating points. The model predicts that PT efficiency should have a slightly negative slope with respect to $\frac{V_{out}}{V_{in}}$, and that a peak efficiency should be observed within the specified power range though partially constrained by the ZVS limit. The experimental data similarly shows a slightly negative slope, and whole-converter efficiency peaks at around 500 mW. As power decreases, the minimum $\frac{V_{out}}{V_{in}}$ boundary for ZVS shifts higher (i.e., the lowest power levels cannot reach low $\frac{V_{out}}{V_{in}}$), which is similarly predicted by the model of Fig. 10. Though the experimental efficiency trends align with the model, the shift between $P_{out}$ levels is much more significant than anticipated. This can be attributed to the PT model's validity decreasing with higher loss (i.e., model depends on the amplitude of PT resonance for lossless operation) as well as



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other losses in the circuit. Both the modeled and experimental efficiencies exhibit low variation with respect to $\frac{V_{out}}{V_{in}}$ for a given power level. This result supports the notion that the non-isolated PT-based converter implementation can regulate voltage at a high $\frac{V_{out}}{V_{in}}$ ratio without the efficiency penalties for large conversion ratios seen in PRs [12].

In Fig. 11 and Fig. 12, we compare the experimental whole-converter efficiencies and PT efficiencies from the model as a function of $\frac{V_{out}}{V_{in}}$ at constant $V_{in} = 60$ V for different power levels. Both the experimental data and model show the same positive-slope curve that flattens at around $\frac{V_{out}}{V_{in}} = 4$. Fig. 12 also shows that the ZVS boundary and efficiency curve intersects at around $\frac{V_{out}}{V_{in}} = 3.2$; this is close to the peak efficiency point for Sequence 5.

In Fig. 13, we plot the experimental and model efficiencies as a function of $P_{out}$ for $\frac{V_{out}}{V_{in}} = 4.2$. The efficiencies in the experimental data fall off faster than the model predicts, confirming that this model becomes less valid with higher loss. However, both the model and experimental data show similar ZVS limits and peak efficiencies of around $\sim 90\%$.

Thus, this prototype validates the ZVS region and efficiency estimation models as helpful tools for selecting an implementation and predicting behavior in high-efficiency operating regions. It is important to note that both the ZVS limits and peak efficiencies are set by the parameters of the prototype's PT, which is a commercially-available component that has not been designed for this specific application (i.e., higher performance may be achieved through further optimization of the PT). However, through effective utilization of the PT's resonant cycle, the proposed implementation's peak efficiency of $\sim 90\%$ exceeds the whole-converter efficiencies reported for most magnetic-less PT-based dc-dc converters in the literature.

## VIII. Conclusion

An organized enumeration of non-isolated PT-based dc-dc converter implementations yields eight promising switching sequences, which are realizable with six practical converter topologies. These implementations are constrained for high-efficiency behaviors such as ZVS, all-positive instantaneous power transfer, and maximum resonant cycle utilization, enabling higher performance than conventional resonant converter structures. We introduce charge transfer analysis methods to quantify how effectively the PT's resonant cycle is used in these implementations. We also present estimation methods based on charge transfer for the ZVS operating region and the PT's efficiency, which facilitate comparison between implementations and design for maximum efficiency.

An example implementation is experimentally demonstrated using a commercially-available PT, validating the proposed models and showing that even an unoptimized PT can achieve competitive performance across wide ranges of voltage regulation with the proposed topologies and switching sequences. Our results also suggest that non-isolated PT-based converters are capable of even higher efficiencies with further developments in the design of the PT itself. Thus, it can be concluded that non-isolated PT-based converters show great potential in high-voltage, low-power applications, especially those requiring significant conversion ratios.

## References


[1] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, USA, Feb. 2009, pp. 1–14.

[2] C. R. Sullivan, B. A. Reese, A. L. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *Proc. IEEE Intl. Symposium on 3D Power Electronics Integration and Manufacturing*, Raleigh, NC, USA, Jun. 2016, pp. 1–23.

[3] P. A. Kyaw, A. L. Stein, and C. R. Sullivan, "Fundamental examination of multiple potential passive component technologies for future power electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10,708–10,722, 2018.

[4] J. D. Boles, P. L. Acosta, Y. K. Ramadass, J. H. Lang, and D. J. Perreault, "Evaluating piezoelectric materials for power conversion," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics*, Aalborg, Denmark, Nov. 2020, pp. 1–8.

[5] A. Vazquez Carazo, "Piezoelectric transformers: An historical review," in *Actuators*, vol. 5, no. 2. MDPI, 2016.

[6] A. M. Flynn and S. R. Sanders, "Fundamental limits on energy transfer and circuit considerations for piezoelectric transformers," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 8–14, 2002.

[7] J. M. Alonso, C. Ordiz, and M. A. Dalla Costa, "A novel control method for piezoelectric-transformer based power supplies assuring zero-voltage-switching operation," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1085–1089, 2008.

[8] M. Ekhtiari, T. Andersen, M. A. Andersen, and Z. Zhang, "Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 783–793, 2017.

[9] E. L. Horsley, A. V. Carazo, N. Nguyen-Quang, M. P. Foster, and D. A. Stone, "Analysis of inductorless zero-voltage-switching piezoelectric transformer-based converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2471–2483, 2012.

[10] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, "Critical design criterion for achieving zero voltage switching in inductorless half-bridge-driven piezoelectric-transformer-based power supplies," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5057–5066, 2015.

[11] M. Sanz, P. Alou, A. Soto, R. Prieto, J. Cobos, and J. Uceda, "Magnetic-less converter based on piezoelectric transformers for step-down dc/dc and low power application," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Miami Beach, FL, USA, Feb. 2003, pp. 615–621.

[12] J. D. Boles, J. J. Piel, and D. J. Perreault, "Enumeration and analysis of dc-dc converter implementations based on piezoelectric resonators," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 129–145, 2021.

[13] J. D. Boles, E. Ng, J. H. Lang, and D. J. Perreault, "High-efficiency operating modes for isolated piezoelectric-transformer-based dc-dc converters," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics*, Aalborg, Denmark, Nov. 2020, pp. 1–8.

[14] W. P. Mason, *Electromechanical Transducers and Wave Filters*. D. Van Nostrand Co., 1948.

[15] L. Wang and R. P. Burgos, "Comprehensive analysis of models and operational characteristics of piezoelectric transformers," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, New Orleans, LA, USA, Mar. 2020, pp. 1422–1429.

[16] J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, "Influence of spurious modes on the efficiency of piezoelectric transformers: a sensitivity analysis," *IEEE Transactions on Power Electronics*, 2020.

[17] "Equivalent circuit parameters for piezo transformers". Steiner & Martins, Inc. [Online]. Available: http://www.steminc.com/piezo/EquivCircuitPT.asp




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