Design Considerations for Planar Magnetic Terminations

Mike K. Ranjram, Pedro Acosta and David J. Perreault
Massachusetts Institute of Technology
Email: {mranjram, pedroa, djperrea}@mit.edu

***Abstract*—Termination losses in planar magnetics can be important in high-current, high-frequency designs. In this paper, we elucidate the loss mechanisms involved and offer simplified models for estimating their impact so that designers using planar magnetics can gauge their potential significance in a given design. The use of the model and possible loss mitigation strategies are explored in an example case study for a 20:1 planar transformer. Experimental results highlight the importance of termination effects and demonstrate the relative performance of example mitigation strategies.**

I. Introduction

In planar magnetics, the windings of inductors or transformers are typically implemented as copper traces in a printed circuit board (PCB), with traces on many PCB layers stacked together to achieve the desired winding configuration. These constructions offer tremendous potential for improved fabrication and planar form factor of the magnetic components in power electronic converters, with benefits including the use of a lower profile core with good thermal characteristics, ease of manufacturability, and strong repeatability [1]. However, planar magnetics present key design constraints over their non-planar counterparts. For example, planar transformer windings must adhere to manufacturable inter-turn and inter-layer spacings which can greatly reduce the core window area available for the windings. Further, while prior work has identified planar winding constructions that can mimic the benefits of Litz wire [2], planar magnetic windings cannot be directly replaced by the wealth of commercially available Litz wire options that a wire-wound design can exploit to improve high-frequency performance. This drawback is partly mitigated by the fact that, in principle, interleaved windings can be easily arranged within the core window owing to the flexibility with which different winding layers can be connected using through-hole via connections [1].

A common approach to reducing power magnetic component size is to operate at high frequencies. At a minimum typical PCB copper thickness of 0.5 oz/ft^2, the frequency for a single skin depth at 25°C is 13.8MHz, making it attractive for high frequency applications, especially compared to Litz wire windings where a typical minimum strand of 48AWG reaches a single skin depth at only 4.5MHz. However, in applications in which the planar magnetic component must carry high currents, many parallelized winding layers must be used in order to achieve low dc resistance. This further aggravates the inter-layer spacing penalty of the planar magnetic construction and also increases the number of termination connections that must be made.

These terminations are important to consider for planar magnetic designs, especially those carrying high current and/or employing high layer counts. This topic was first explored in the early 1990s: for example in [3] it is estimated that the interconnection resistances of an eight-layer PCB planar transformer comprise 65-80% of the measured short-circuit resistance, and the authors propose a four-via interleaved structure to reduce the ac resistance of these vias. A second study [4] focuses on the trade-offs of termination styles on the measured leakage inductance, and proposes design guidelines to minimize this inductance. While [3] presents an insightful observation of the importance of considering via terminations in certain applications, the subject is broached qualitatively. Furthermore, few recent publications comment on the potential impact of these terminations in planar magnetic designs.

There are two key termination loss components in planar transformers that can be problematic. A first component is the loss in the interconnection vias themselves, especially when multiple vias are placed in close proximity to one another. A second key component is the loss in the winding trace segments leading outside the core for termination to external circuitry, as may occur in interleaved designs where the secondary windings must extend beyond the farthest extent of the primary windings before they can be terminated.

This paper explores the impact of termination losses in planar magnetics in order to stress their potential importance in contemporary designs. Further, we present simplified models that can be used to assess when certain termination losses may be important and should be more carefully accounted for in loss estimates. Finally, example mitigation strategies are discussed in the context of a 20:1 transformer design and experimental results validate the importance of termination loss in this design and the benefit of the proposed mitigation strategies.

II. Via Loss Mechanisms

A via can be modeled as a conductive cylindrical shell with thickness t. The dc resistance of the via is

$$R_{via} = \frac{h}{\sigma \pi t(2a - t)}, \tag{1}$$

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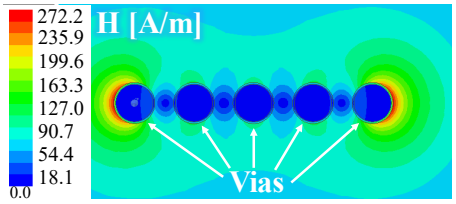

Fig. 1: 2D ANSYS Maxwell simulation showing magnetic field strength around a 1x5 via array in isolation. The array dimensions are a=10 mil and s=10mil (ref. Fig. 2). The vias are in parallel and carry a total sinusoidal current of 1A peak at 1MHz. The top view (looking down through the vias) is shown.

where h is the height of the via, t is the plating thickness, a is the outer radius, and σ is the conductivity of the plating at the expected operating temperature (typically the conductivity of copper). The plating thickness of a via is typically 1 mil (25.4 μm), corresponding to a single skin depth at a frequency of 3.5MHz in copper at 25°C. Thus, for frequencies on the order of a few MHz, the ac resistance factor ($F_R \equiv R_{ac}/R_{dc}$) of a single via should be close to one. However, F_R can increase substantially when multiple vias are deployed in parallel owing to proximity effect.

A. Via Arrays in Isolation

In this study, we focus on the frequency regime where the plating thickness of the via is smaller than a skin depth such that current flowing through the via uses much or all of the full extent of the plating thickness[1]. Although a single via in isolation has similar dc and ac losses in this regime, this is not necessarily the case when the vias are paralleled in an array. In this case, the vias are exposed to the fields generated by currents in the other members of the array, causing the current distribution to shift from being uniform to crowding near the edges of the array where the magnetic field strength is highest. This shift in the current distribution increases the ac loss of the array, which we can observe as an increase in ac resistance. An example of this shift in magnetic field and current distribution is shown in Fig. 1, which shows 2D results obtained from an example ANSYS Maxwell simulation of a 1x5 via array. In this case, we observe that the magnetic field nulls between the vias and has maxima around the outer edges of the array, with $F_R = 1.38$ at 1MHz. An alternative perspective to interpret this increase in ac resistance is to quantify an "effective" number of vias (N_e) that would have the same resistance at dc as the array has at the frequency of interest. Namely, $N_e = N/F_R$ where N is the total number of parallel vias in the array. For example, $F_R = 1.38$ means that the five vias in Fig. 1 operating at 1MHz have the same resistance as 3.6 vias operating at dc. We can interpret this value of F_R as "losing" the conduction capability of 1.4 vias.

[1]Above this frequency regime, the vias themselves experience skin effect in addition to the proximity effects described in this section.

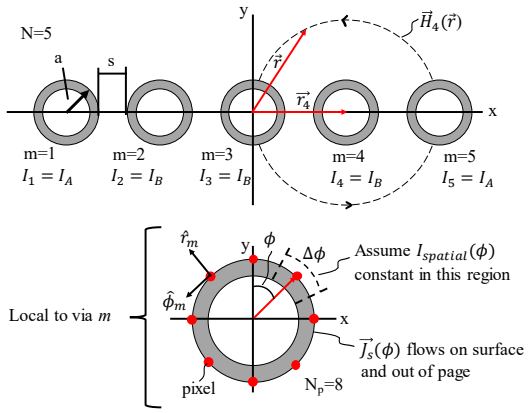

Fig. 2: Example model geometry for a 1x5 via array.

B. Via Array Modeling

It is desirable to present a general scaling law on F_R for an arbitrary via array, but this is challenging since the field interaction between the vias is a function of via size and array geometry, and results not only in current being split unevenly among the members of the array, but also changes the distribution of current in each via. For example in Fig. 1, the edge vias carry more current than the other vias and also carry more of their current on their outer edges than on their inner edges.

Instead of a general scaling law, we propose a simplified model of the array from which F_R can be solved. This model is developed with the intent to provide a simple-to-compute estimate of F_R for a general array configuration, with the notion that once this reasonable estimate has been obtained, the designer can turn to a more exact analysis (e.g. Finite Element Analysis (FEA)) if needed. The model assumptions are defined below and an example geometry for a 1x5 array is provided in Fig. 2

1) Assumption 1: Current flow is symmetric about the center of the array: This is a direct result of the physical symmetry of the array and reduces the number of currents that must be solved. For example, in a 1x5 array in isolation, as in Fig. 2, there are only three possible current values ($I_1 = I_5$, $I_2 = I_4$, and I_3) due to symmetric current flow. We can make a stronger but less precise assumption on symmetry by characterizing the array according to two currents of interest. The first current, I_A, is relatively large and assigned to vias on the extreme edges of the array, which will sit in regions of highest magnetic field. The second current, I_B, is in phase with I_A and is assigned to all other vias that we expect to carry current. This simplifies the model by allowing the current distribution in the array to be parameterized by a scalar $k \equiv I_B/I_A$ where $k \in [0, 1]$[2]. For example, in the 1x5 array in Fig. 2, current I_A is assigned to the two outer vias, and the remaining vias are assumed to carry I_B. In practice we expect I_3 to be smaller than I_2, but assuming they are

[2]In principle, this distribution can be parameterized by a vector k to increase estimate accuracy at the cost of a larger search space.

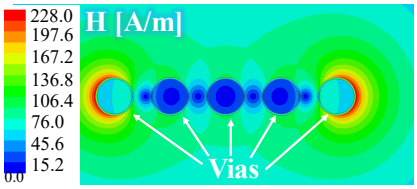

Fig. 3: Example 2D ANSYS Maxwell simulation for a 1x5 via array having the same geometry and current distribution as the 1MHz example in Fig. 1 but assuming circular fields are produced by each via as in Assumption 1 of the model.

equal is reasonable to the extent that current will dominantly flow on the edges of the array, and minor differences in the distribution of current amongst the internal vias is unimportant. In "grid" via arrangements with multiple rows, we apply this assumption by assigning I_A to corner vias, I_B to all other vias on the perimeter, and zero current to the remaining vias. This is reasonable in the high frequency limit where the inner vias are shielded from conduction.

2) Assumption 2: Vias produce circular fields: Once a current distribution k is specified, the magnetic field produced by each via can be computed using the Biot-Savart law for a circular conductor. Indexing the vias in the array by m where $m \in [0, N]$ and N is the total number of vias in the array, the magnetic field at a location $\overrightarrow{r}$ produced by the m_{th} via is

$$\overrightarrow{H}_m(\overrightarrow{r}) = \frac{I_m}{2\pi|\overrightarrow{r} - \overrightarrow{r}_m|}\hat{\boldsymbol{\phi}}_{\boldsymbol{m}}, \tag{2}$$

where $|\overrightarrow{r} - \overrightarrow{r_m}|$ is the distance from the center of the m_{th} via, I_m is the current in the via, and $\hat{\boldsymbol{\phi}}_{\boldsymbol{m}}$ is the tangential unit vector in cylindrical coordinates about the center of the via, as indicated in Fig. 2. In practice, the field produced by a via will only be concentric as in (2) when it carries current uniformly, which is not the case in the high frequency regime we are interested in. Thus, this assumption will underestimate the maximum field intensity seen by the via array, and this error will be worse for arrangements where individual vias carry highly asymmetric currents. However, in many via arrays of interest this assumption provides a simple means of estimating the field distribution directly from the current distribution k without having to consider the details of how magnetic diffusion through the conductors [5] impacts the overall field distribution. Fig. 3 shows an example consequence of this assumption for a 1x5 array having the same current distribution as the 1MHz simulation in Fig. 1 but assuming uniform current density on each via. The overall field distribution is similar in shape, but the maximum field intensity is approximately 20% lower.

3) Assumption 3: Vias have zero internal field: The via is assumed to behave as a perfect electric conductor such that the surface current density of the m_{th} via, $\overrightarrow{J}_{s,m}$, is entirely determined by the external field $\overrightarrow{H}_{m,ext}$ on its outer surface according to the boundary condition

$$J_{s,m}(\phi) = |\overrightarrow{H}_{m,ext}(\phi) \times \hat{\boldsymbol{r}}_{\boldsymbol{m}}| = H_{m,\phi}(\phi), \tag{3}$$

where $\hat{\boldsymbol{r}}_{\boldsymbol{m}}$ is the radial unit vector in cylindrical coordinates about the center of the m_{th} via (ref. Fig.2) and $H_{m,\phi}$ is the tangential component of the external field on the external surface of the via, which varies as a function of ϕ in that coordinate frame. This condition is associated with zero internal field in the via, and is a good approximation for a thin conductive shell in the limit where $2\pi f \mu_0 \sigma t a >> 1$, where μ_0 is the permeability of free space [5].

The spatial distribution of current in the m_{th} via, $I_{m,spatial}(\phi)$, can be computed as

$$I_{m,spatial}(\phi) = I_m \frac{H_{m,\phi}(\phi)}{H_{m,\phi,max}} \tag{4}$$

where $H_{m,\phi,max}$ is the maximum value of the external tangential magnetic field on the outer surface of the via.

C. Solving the Via Array Model

The simplified model allows the resistance factor to be solved in the programming environment of the user's choice. First, we solve for the current distribution k according to the following steps.

1) Define the array geometry, including the outer radius of the vias, a, and the spacing between the vias, s.
2) Specify a boundary around the array. This defines the region in which the magnetic field produced by the vias is computed.
3) Assume a current distribution based on Assumption 1 (e.g. In Fig. 2, we assume I_A on the outer vias and I_B on the inner vias). The distribution is parameterized by $k = I_A/I_B$.
4) Assume a value of k (e.g. $k = 0$) and assume 1A flowing through the array ($I_A + I_B = 1$).
5) Compute the fields produced by each via in the defined region according to (2).
6) Compute the net field, $\overrightarrow{H}$, in the region by taking the vector sum of the individual field components.
7) Compute $|\overrightarrow{H}|^2$ at each point in the region and store the sum.
8) Increment k and return to Step 4 unless $k = 1$.

The solution for k is the value which minimizes the energy stored in the defined region (i.e. minimizes the sum in Step 6)[3].

Once this distribution is known, the spatial distribution of current in the array can be determined.

1) Partition the perimeter of each via into N_p pixels and define $\Delta\phi = 2\pi/N_p$ (ref. Fig. 2).
2) Compute the field at each pixel of each via according to the solved value of k and (2).
3) Compute the spatial distribution of current in each via by solving (4) at each pixel. We assume this current value is constant over $\Delta\phi$ centered around the pixel (ref. Fig. 2).

[3]This is the case in the high-frequency limit where the inductive portion of the via's impedance dictates current flow, but this simplifying assumption enables a useful estimate of the value of F_R.

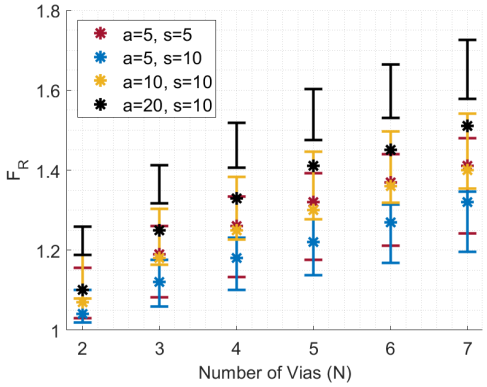

Fig. 4: Comparison between model estimates for F_R and ANSYS Maxwell 2D simulations for 1xN array configurations with different via radii, a, and via edge-edge separation, s, in mils. The asterisks show the estimate computed from the model and the error bars indicate the range of F_R obtained from 2D ANSYS simulations between 500kHz and 2MHz.

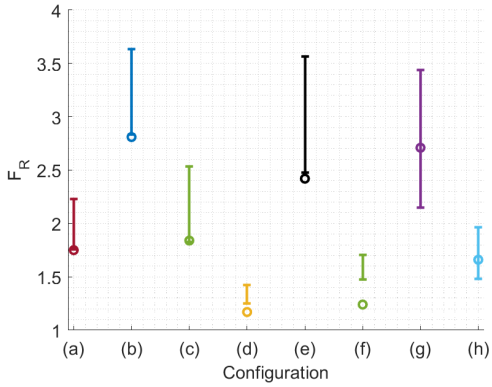

Fig. 5: Example comparisons between model F_R, indicated by a circle, and 2D ANSYS Maxwell simulation results between 500kHz and 2MHz. In (a)-(f), a=s=10 mils (ref. Fig. 2). (a) 2x5 via grid. (b) 5x5 via grid. (c) Edge termination (ref. Section II-D), 1x3 array, $d_t = 10$ mils. (d) Edge termination, 1x3 array, $d_t = 100$ mils. (e) Edge termination, 1x5 array, $d_t = 10$ mils. (f) Edge termination, 1x5 array, $d_t = 10$ mils. (g) Excursion (ref. Section III), $w = 3.3$mm, $d_e = 10$ mils. (h) Excursion, $w = 3.3$mm, $d_e = 100$ mils.

Finally, the resistance factor can be computed as $F_R = NN_p \sum_{m=1}^{N} \sum_{j=1}^{N_p} I_{m,j}^2$ where $I_{m,j}$ is the current about the j_{th} pixel of the m_{th} via in the array.

The developed model produces a result that is ignorant of the frequency of operation. Instead, the model is set up under "high frequency regime" approximations, and we expect a value of F_R that is representative of operation in this regime. Fig. 4 compares the results of this modeling to results obtained from 2D ANSYS Maxwell simulations. The marked points indicate the estimated F_R from the model for different via array configurations defined by the via radii, a, and edge spacing, s, in mils, and the corresponding error bars show the range of F_R obtained for ANSYS 2D simulations between 500kHz and 2MHz. The estimates sit near the middle of the frequency range in three example cases, but are consistently underestimated in the $a = 20, s = 10$ case. This is an example where the second simplifying assumption in Section II-B does poorly. Namely, these vias are relatively close together owing to $s < a$, so the magnetic fields generated by the vias interact strongly with the other members of the array. This leads to more crowding in the vias, and more asymmetric current distribution within the vias, which compromises Assumption 2. We note that these estimates remain within approximately 10% of the middle of the simulated range, and in the sections below we highlight the usefulness of this simple-to-estimate F_R even though it is not exact.

Data for 2x5 and 5x5 via grids with a=s=10 mil are shown in Fig. 5a and Fig. 5b. In these cases, we tend to underestimate F_R more than in the 1xN cases, with errors up to approximately 16% from the middle of the simulated range. This is again a limitation of the second simplifying assumption in the model. Namely, in grid configurations there is stronger asymmetry in the via current distributions due to current crowding on the corners of the array compared to current crowding on the side edges in the 1xN case. Because the model does not account for the impact of current distribution within a via, these asymmetries lead to higher error. However, it is important to note that the computed estimates are still useful from a design perspective. For example, if a designer needed to rely on a 5x5 via grid with 10 mil radii and 10 mil edge-to-edge spacing for their design at 1MHz, the model estimates an effective number of vias of $N_e = 8.9$ while the ANSYS simulation indicates $N_e = 7.5$. While this represents an error of approximately 16%, this is the difference between estimating use of 35% of the available 25 vias versus an actual usage of 30%. If a designer expected to utilize all 25 vias, the answer obtained by the model remains useful design information which can be simply obtained.

D. Via Array Terminations

The current distribution in a via array depends on the magnetic fields surrounding each via. For an array in isolation these fields all originate from current flow in the array itself. However, in many planar magnetic constructions, a pair of via arrays terminate the windings. In this case, the arrays may be in close proximity to each other while carrying equal and opposite current. This further aggravates the current distribution in the array, with current crowding on the edge closest to the other array where the field strength is highest.

One common method for terminating a winding is to use a pair of via arrays with their broad sides each along the breadth of their respective winding as shown in Fig. 6a and illustrated in Fig. 7. We call this an "edge" configuration, as the two terminations face each other along their short edges. This configuration is highly susceptible to the fields of the other termination's vias and may yield a large increase in F_R as current crowds into the via closest to the opposite termination.

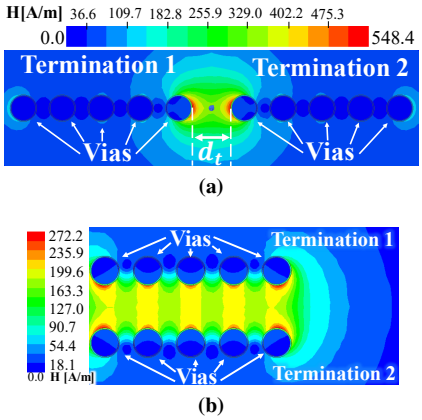

Fig. 6: 2D ANSYS Maxwell simulations showing magnetic field strength around example 1x5 via array terminations. The via arrays have a=s=10 mil and the spacing between the two terminations is d_t=0.8mm. The top view (looking down through the vias) is shown. (a) Edge configuration. (b) Broadside configuration. The vias in each termination are in parallel and carry net sinusoidal current of 1A at 1MHz, with negative current flowing in Termination 2.

On the other hand, if the via arrays terminating the two ends of the winding are oriented in a "broadside" configuration such that they face each other along their long edges as shown in Fig. 6b, the detriment of the neighbouring fields is mitigated as more of the vias sit in the region of high magnetic field strength. For example, in Fig. 6b, $F_R = 1.61$ as compared to $F_R = 2.1$ in Fig. 6a. Both of these configurations can be modeled as described in Section II-B, being sure to note that the magnitude of current in the arrays is now symmetric about the midpoint between the two arrays. For example, in Fig. 6a, we assign I_A and $-I_A$ to the inner two vias, and I_B and $-I_B$ to all other vias in Termination 1 and 2, respectively.

We focus on the edge configuration of Fig. 6a, since this is most naturally implemented in many winding terminations. Example comparison data between the model and ANSYS 2D simulations are shown in Figs. 5(c)-(f). These data are collected for 1x3 and 1x5 via array terminations with the distance between the terminations, d_t, set to either 10 mils or 100 mils. First, we note that the shorter separation configurations in Figs. 5(c) and (e) have much larger resistance factors, as expected due to the interacting fields being stronger when the terminations are closer. Second, we observe a tendency for the model to underestimate F_R, which we attribute to the limitation of Assumption 2 in cases where facing vias have highly asymmetric current distributions. However, these estimates remain useful for a first-cut estimate on the actual resistance of these terminations, as we explore in Section IV.

III. Winding Excursion Losses

Another important source of termination loss occurs when a set of windings is brought outside the core window before being terminated - we refer to this as an "excursion." This can

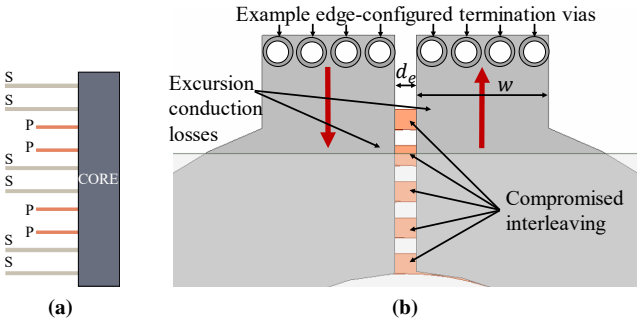

Fig. 7: Example structure of an interleaved transformer with series wound primary (P) layers and parallel secondary (S) layers. (a) Side view. (b) Top view of the excursion region (with translucent core boundary overlaid and red arrows indicating the direction of current flow).

be important, for example, in an interleaved transformer where the secondary comprises many layers in parallel and must be extended beyond the furthest extent of the primary windings in order to terminate the paralleled windings, as shown in Fig. 7. This termination excursion - which is not captured in many basic loss models [6] - can increase loss both due to the conduction losses associated with the excursion path and due to the potential detriment on the interleaving structure of the transformer.

A. Excursion Conduction Loss

Once the windings have been brought outside the core window, the magnetic fields around them are no longer shaped by the core. These winding elements carry equal and opposite current, and a region of high magnetic field will exist between them (similar to the effect in Fig. 6a). Thus, current will crowd on the edge of the conductor that faces the other winding element, yielding high ac resistance. The closer the windings are to each other, the worse this effect becomes. For example, for two 2.8 mil thick, 3.3mm wide traces with separation of 10 mils, $F_R = 2.7$.

This configuration of two rectangular traces carrying equal and opposite current is one that has been explored in the literature, for example [7] provides the solution to the 2-D magnetic diffusion equation for a single rectangular conductor and [8] provides an empirical fit for F_R accounting for the proximity effect experienced by two rectangular conductors carrying equal and opposite currents. A modified version of the approach in Section II-B can also be used to estimate F_R in these configurations by modeling each wide thin trace of thickness Δ as an array of circular conductors with $a = \Delta/2$ and $s = 0$[4]. Further, we partition each circular conductor with $N_p = 4$ so as to treat each conductor as producing four spatial current components on the four sides of a square of side-length Δ. The distribution of current between these conductors is

[4]We omit a porosity factor, which is often included when converting between a rectangular trace and a circular wire array, in order to maintain the relative position of the edges of the traces.

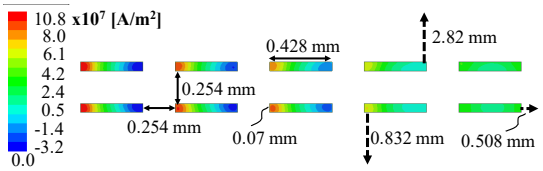

Fig. 8: 2D ANSYS Maxwell simulation of the current density of the primary windings in the region of compromised interleaving indicated in Fig. 7b. The cross-section of ten primary windings is shown and the dashed arrows indicate the distances of the windings to an EQ20/PLT core. A net sinusoidal current of 1A peak at 1MHz flows through each cross-section.

symmetric about the center of the two excursion traces, similar to the case in Section II-D. However, due to the relatively large width of the traces, it is beneficial to use a two-dimensional current distribution factor k in order to identify both edges of the traces as potentially carrying high current. The results of this modeling are shown in Figs. 5(g) and 5(h), and show that the estimate is reasonable within the range of interest. We note that there is great benefit in keeping these excursion traces far apart, however this trades-off with another loss mechanism described in the following section.

B. Interleaving Impact

Interleaved windings in transformers improve the ac resistance of windings inside the core window by preventing the build-up of magnetic field impinging on the surface of the windings. Structurally, this relies on currents in the windings being anti-parallel. When only one set of windings is brought out of the core as in Fig. 7b, it is possible to have regions where non-parallel currents flow on adjacent primary and secondary layers, and also regions where no current flows. For example, in the region of the winding where there is no secondary coverage in Fig. 7b, no secondary current exists and the magnetic field is free to build up between the adjacent primary layers, increasing their ac resistance. For example, in the configuration of Fig. 8, $F_R = 3$, and this will worsen as the number of primary layers increases.

Unfortunately, this arrangement does not lend itself to a simple modeling approach. For example, in Fig. 8 any presumed symmetry relies on the windings being symmetrically distributed relative to the core, which may not be the case (e.g. one layer may sit closer to the core). Further, the system does not have a simple parition into "important" current components due to the gradual buildup of current crowding and the possibility of current circulation in the traces of these series windings. Finally, although a core is present, the traces are not laid out in such a way that a 1-D assumption on the direction of the magnetic field can be made reliably (e.g. each layer is effectively a thin wide trace that faces the core on its edge rather than its broad side).

We note, however, that although F_R may be large in these configurations, its impact is mitigated by reducing the length of primary traces that are exposed to this region of compromised interleaving. This can be achieved, for example, by keeping the distance between the excursion traces, d_e, as small as possible. However, this aggravates both the via losses and the trace excursion losses.

TABLE I: Parameters for case study in Section IV.

Windings	S P P S	**Prim. trace width**	0.428 mm
Num. turns	1 5 5 1	**Copper weight**	2 oz/ft^2
Sec. width	3.16 mm	**Board thickness**	1.6 mm

IV. Example Case Study for Mitigating Termination Loss

The simple models developed in the previous sections allow a designer to assess the potential detriment of via arrays and excursion winding losses. Using these models, one can estimate the impact of these two loss components when the separation distance d_e is small (e.g. equal to the minimum manufacturable trace-to-trace spacing). If these loss components appear problematic in this case, it is recommended to turn to an FEA tool to pursue mitigation strategies. In this section, we explore possible mitigation strategies by considering the example design of a 20:1 transformer.

Before proceeding, it is worthwhile to highlight the importance of the termination path outside of the transformer in choosing the best termination design. For example, in practice the minimum d_e may depend on the physical size of the components that connect to the transformer windings. Similarly, mitigation strategies are different in cases where the windings can terminate onto different layers. These distinctions impact the choice of termination structure, and therefore there is not necessarily one "universally good" structure. Our intent in this section is to elucidate considerations that factor into designing good terminations.

Assume an initial design search, e.g. using 1D analysis [6], leads us to a planar transformer design with an EQ20/PLT core. Further, assume we are in a copper loss dominated design corner such that we employ the Variable-Inverter-Rectifier-Transformer (VIRT) architecture [9], to achieve an effective 10:1/2 transformer. The details of the VIRT are not necessary for this study except to note that it employs half-turn secondary windings as shown in Fig. 9a and can achieve a 20:1 effective step-down ratio using only 10 primary turns[5]. However, due to the half-turn structure there are terminations on both sides of the windings, aggravating termination loss. A summary of the design parameters are in Table. I.

Our initial analysis predicts a primary-referred short-circuit resistance, which we will term the "net resistance" for convenience, of 0.45Ω. However, this prediction does not account for via termination loss or excursion losses. Our initial design uses edge-configured 1x7 via arrays terminations, with $a = 10$ mils, $s = 10$ mils, and $d_t = 45$ mils. In order to clear the primary

[5]This allows a designer to trade-off core and copper loss in order to minimize overall loss beyond what is achievable in a "conventional" single-turn transformer.

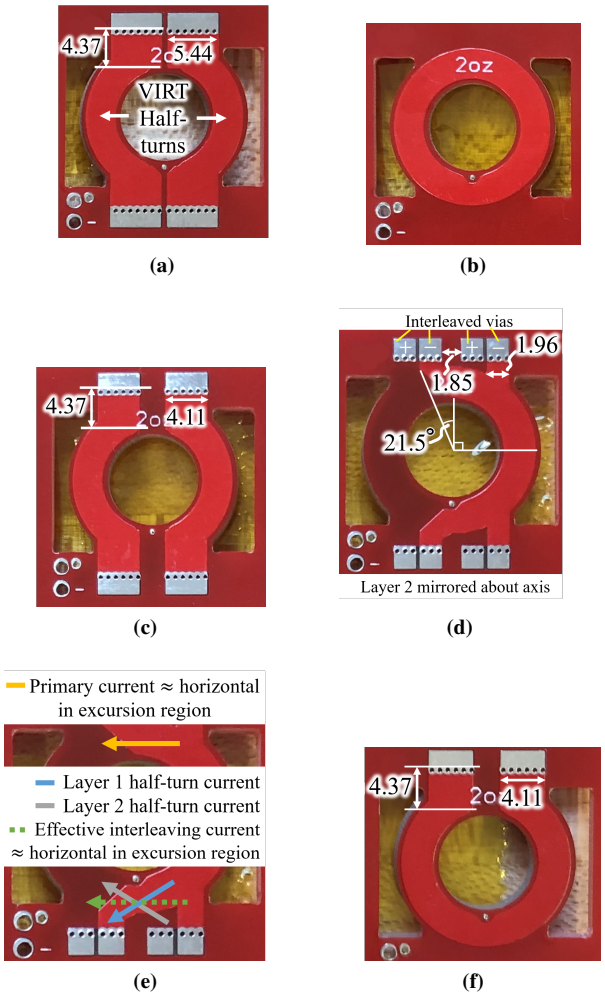

Fig. 9: Example transformer termination designs with key dimensions shown (units in mm). VIRT configurations are shown in Figs. (a), (c), and (d). These employ two half-turns on the secondary and therefore have a termination pair on both sides of the transformer. All via arrays have $a = s = 10$ mils. (a) $d_e = d_t = 20$ mil. (b) Idealized design with short-circuited secondary. (c) $d_e = d_t = 100$ mil. (d) Effective interleaving current (EIC) termination design. (e) Illustration of EIC in (d). (f) "Conventional" (non-VIRT) design with $d_e = d_t = 100$ mil.

traces, an excursion path 4.9mm long and 5.9mm wide is used and we assume d_e=10 mil.

At dc, we estimate that a single termination, comprising one pair of via arrays and one excursion path as shown in Fig. 7b, increases the net resistance by approximately 5.5%. Thus, based only on dc considerations, the two terminations together increase the net resistance to 0.50Ω. However, through our developed model, we estimate $F_{R,vias} = 1.8$ and $F_{R,excursion} = 3.1$. In this case, a single termination increases the net resistance by approximately 16%, and together the two terminations yield a total increase in net resistance to 0.59Ω. This increase suggests it is worthwhile to analyze the structure using FEA in order to pursue possible reductions in loss.

Inputting this structure into a 3D ANSYS Maxwell simulation and running a short-circuit test, we compute a net resistance of 0.58Ω[6]. For reference, we also obtain the net resistance for the idealized short-circuit case in which each secondary turn is short-circuited as shown in Fig. 9b. This construction does not have any terminations, and the resulting net resistance is 0.34Ω, suggesting our termination loss estimate has an error of $\approx 40\%$.

An initial strategy to improve this resistance may be to increase d_e as this can reduce F_R for the via terminations and excursion loss. However, this will aggravate the interleaving losses described in Section III-B. A design with $d_e = 100$ mil is shown in Fig. 9c and the net resistance computed in ANSYS is 0.59Ω. Thus, increasing d_e has slightly increased loss. There are a number of additional possibilities for minimizing loss, and we explore some of these below.

1) Reduce via lengths: This reduces the via resistance proportionally according to (1). In order to achieve this, the overall board thickness must be reduced, bringing the layers of the PCB closer together.

2) Overlap excursion traces: Excursion losses are aggravated by the traces being edge-facing, such that current crowds on the thin edge of the conductor. If the excursion traces are layered on their broad sides, current will flow more uniformly over the available winding width. However, in a planar construction of a conventional (non-VIRT) transformer, the winding cannot change layers as it proceeds through a turn unless vias are used, which introduces another potential loss penalty.

3) Try a non-interleaved design: In non-interleaved designs, via lengths are reduced since there is no need for terminating vias to span the full thickness of the board. Further, excursion losses can be mitigated if blind vias are used, since the secondary layers can be terminated within the core window without having to extend beyond the primary winding. However, the loss of interleaving can significantly increase winding resistance in the core window.

4) Exploit via interleaving: In [3] the authors discuss the possibility of interleaving vias in order to reduce their loss. An example of interleaved vias is shown in Fig. 9d. These interleaved termination vias are exposed to similar field on both of their edges, thus improving current sharing in the arrays.

5) Introduce "effective interleaving current": A key difficulty with increasing d_e is the increase in interleaving loss arising from a loss of anti-parallel current flow, as described in Section III-B. However, the VIRT structure offers a means to mitigate this impact while also achieving interleaved vias. The proposed arrangement is shown in Fig. 9d. Here, each half-turn is placed on a different layer, such that the excursions overlap at an angle towards an interleaved via termination. Net current flow in the overlapping regime produces a magnetic

[6]Note that this value omits the loss of the trace used to short the two terminations, so as to provide a fairer comparison to the estimate.

field that mimics the field that would be set up set up by a current flowing anti-parallel to the primary, as illustrated in 9e. This "effective interleaving current" (EIC) mitigates the interleaving loss associated with increasing d_e. This termination structure can be useful in cases where the transformer can terminate onto different layers. Simulating this structure in ANSYS yields a net resistance of 0.45Ω, representing an approximately 20% reduction compared to Fig. 9a.

V. Experimental Results

Experimental primary-referred short-circuit resistance measurements confirm the the benefits of the mitigation strategies discussed in Section IV. These results are shown in Table II.

First, we evaluate a 10:1/2 transformer with parameters similar to Table I except with an additional secondary layer on both sides to form a six layer board. The spacing between layers is 0.24mm. The measurements confirm a significant discrepancy between the ideal case and practically implementable designs[7]. As also expected, the EIC configuration offers a substantial improvement in loss.

Next, we consider a 12 layer version of the 10:1/2 transformer, with the primary winding distributed over four layers. Two three-turn layers and two two-turn layers are used, with trace widths of 0.88mm and 1.45mm, respectively. This is implemented by stacking two 6 layer boards and connecting the termination vias using copper wire. The results in Table II show a much larger increase over the ideal case than in the 6 layer version, attributable to the longer via connections and increased loss when primary interleaving is lost in the excursion regions. The EIC configuration again helps to reduce the net resistance. This thick, highly interleaved board is an example where consideration of the terminations is important to avoid underestimates of the net resistance.

Finally, we consider a 12 layer 20:1 non-VIRT transformer which comprises 20 primary turns distributed on four layers. Termination losses are still important here, even though there is only one termination region. In particular, the penalty paid for loss of interleaving in the excursion region is steep when there is a high number of primary turns distributed over many layers. Finally, we note that the net resistance is much higher than in the VIRT case, highlighting the benefit of this technique.

VI. Conclusion

An analysis of the components of the termination structure of planar magnetics elucidates the loss mechanisms associated with termination vias and winding excursions outside the core window. We provide a physical explanation for these loss mechanisms, and offer models that designers can use to estimate the loss increase of these mechanisms. This allows a relatively simple litmus test that informs pursuing more detailed analysis and simulation. The developed models agree reasonably well with 500kHz-2MHz results obtained in 2D ANSYS Maxwell simulations, and cases of relatively large error can be understood in the context of the simplifying assumptions of the model. A case study and experimental results demonstrate the importance of considering termination effects in an example 20:1 step-down ratio transformer, and an example termination structure that allows for an effective interleaving current to flow is shown to be beneficial for mitigating termination losses.

[7]These measurements include the resistance of the short-circuit traces, so these increases are not entirely attributable to the discussed termination effects. However, the trends remain indicative of their relative performance.

TABLE II: Experimental results. Where indicated d=d_e=d_t.

Configuration	Net res. (Ω)	Increase over ideal
10:1/2, 6 layers		
Ideal (Fig. 9b)	0.56	-
d = 20 mil (Fig. 9a)	0.91	63%
d = 100 mil (Fig. 9c)	1	79%
EIC config. (Fig. 9d)	0.72	29%
10:1/2, 12 layers		
Ideal	0.29	-
d = 100 mil	0.73	152%
EIC config.	0.43	48%
20:1, 12 layers		
Ideal	1.13	-
d = 100 mil	1.83	62%

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