Design Considerations for Very High Frequency dc-dc Converters

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Abstract— **This document describes several aspects relating to the design of dc-dc converters operating at frequencies in the VHF range (30-300 MHz). Design considerations are treated in the context of a dc-dc converter operating at a switching frequency of 100 MHz. Gate drive, rectifier and control designs are explored in detail, and experimental measurements of the complete converter are presented that verify the design approach. The gate drive, a self-oscillating multi-resonant circuit, dramatically reduces the gating power while ensuring fast on-off transitions of the semiconductor switch. The rectifier is a resonant topology that absorbs diode parasitic capacitance and is designed to appear resistive at the switching frequency. The small sizes of the energy storage elements (inductors and capacitors) in this circuit permit rapid start-up and shut-down and a correspondingly high control bandwidth. These characteristics are exploited in a high bandwidth hysteretic control scheme that modulates the converter on and off at frequencies as high as 200 kHz.**

I. INTRODUCTION

MODERN APPLICATIONS are driving demand for power supply systems with increasingly fast transient response. Moreover, there is a desire for improvements in the size, cost, and integration of dc-dc power converters. These goals motivate the development of switching power converters operating at greatly increased switching frequencies. Greatly increased frequencies enable reduction in the numerical values and energy storage of the passive components that limit achievable transient response and account for the majority of converter size and cost. Furthermore, operation at sufficiently high frequencies enables the elimination of magnetic materials (along with their attendant manufacturing and performance limitations) and opens the way towards greater integration of passive components.

This paper introduces circuit designs and methods suitable for dc-dc converters operating at very high frequencies (VHF, 30-300 MHz). These developments are introduced in the context of the design and experimental evaluation of a 100 MHz dc-dc converter. Special emphasis is placed on key design elements including a low-loss multi-resonant gate drive, a radio frequency (RF) resonant rectifier, and methods for realizing high-bandwidth output control. Section II of the paper provides background in the area of radio-frequency dc-dc power conversion, and describes the overall system design and control approach. Section III explains the design and operation of a multi-resonant gate drive circuit that provides rapid, low-loss gating transitions at very high frequencies. Operation and design of the radio-frequency resonant rectifier is presented in Section IV. Experimental measurements and performance evaluation of a closed loop dc-dc converter implementing the proposed methods are presented in Section V, and Section VI concludes the paper.

II. SYSTEM STRUCTURE AND CONTROL

A. Background

Achieving high efficiency in dc-dc converters operating at very high frequencies necessitates means to keep the switching loss to a minimum. In hard-switching converters some energy is lost every time the semiconductor switches commutate, yielding a loss component that is proportional to the switching frequency. Soft switching – and in particular zero voltage switching (ZVS) – reduces the switching loss by maintaining a low voltage across the semiconductor device during the on/off transitions [1], [2]. Furthermore, ZVS operation is beneficial because it reduces the electromagnetic interference (EMI) normally associated with rapid transitions in hard-switched converters. However, the resonant methods used to realize ZVS operation tend to incur losses that do not scale back with load, making it difficult to achieve efficient light-load operation. A challenge, then, is to take advantage of the high-frequency capabilities of ZVS topologies while still maintaining efficient operation at light load.

A further challenge in implementing VHF power converters is reducing the losses due to the gating of the semiconductor devices. With conventional gate drives, gating loss is proportional to switching frequency and rapidly becomes unacceptable as frequency is increased. Recovering at least a portion of the energy delivered to charge the gate is thus an important means for extending the achievable switching frequency range [3]–[11].

Parasitic elements are another important consideration in RF converters, and become more so with increasing switching frequency. In many RF circuit implementations, the size of some circuit elements is comparable to the parasitics introduced by the devices, packages and interconnections. For

1-4244-9717-7/06/$20.00

example, the parasitic capacitance of the semiconductor device is typically an important consideration in RF converter design. To address this issue, and to allow for even higher switching frequencies, topologies that absorb or utilize the component parasitics (especially device capacitances) as an integral part of their operation are desirable. This, however, leads to a tighter dependance of circuit performance on device parasitics than is typical in conventional designs.

B. Converter System Structure

This paper describes a design approach that can meet all the above requirements. A block diagram of a system realizing this approach is shown in Fig. 1, consisting of a radio-frequency resonant inverter, a transformation stage, and a resonant rectifier, along with an appropriate control system.

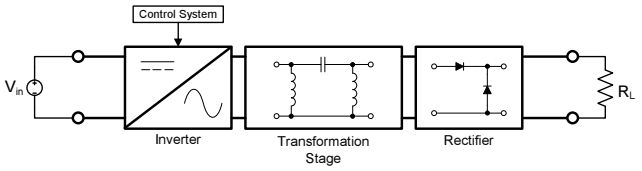


Fig. 1. A block diagram illustrating the structure of a high frequency dc-dc converter.

Figure 2 shows a simplified schematic of the prototype dc-dc converter implemented to demonstrate this approach. Subsequent sections will focus on key system elements, and will present an evaluation of the different functional blocks of the system.

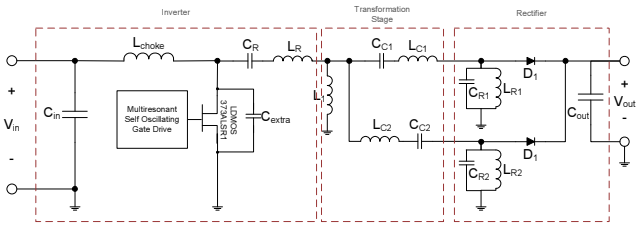


Fig. 2. Schematic of a 100 MHz dc-dc converter.

An inverter at the system input transfers power from the input source to the subsequent stages by transforming the dc input voltage into a VHF sinusoid. The inverter can be implemented using any of a number of switched-mode RF power amplifier topologies that provide the required ZVS (e.g., [12]–[17]). For the particular implementation in this paper, the inverter utilized was a class E power amplifier operating with a low loaded Q (Q_L) to deliver power efficiently[1]. Details on the design, characteristics, and limitations of this class of power amplifiers can be found in [14], [19], [20], and [21, Chapter 15], and so will only be treated briefly here.

[1]In conventional RF designs, the loaded Q of the inverter tank is usually chosen to be large, resulting in waveforms with high spectral purity [14], [18]. For power conversion, however, the requirements on Q_L are different since the goal is to maximize power transfer with minimum loss. A low value of Q_L results in less energy resonated in the tank, which implies reduced conduction loss in the parasitic elements of the inverter.

Inverter output power (under ZVS conditions) is proportional to the capacitance in parallel with the switch. For the intended output power range in the practical implementation described here, the required capacitance is provided by the parasitic drain-source capacitance of the MOSFET and 20 pF of external capacitance.

The device selected for the main switching element of the inverter is a lateral doubly-diffused MOSFET (LDMOSFET) of the type typically used in cell phone base stations. This semiconductor device offers the characteristics required to operate at high frequencies: it presents an acceptably low output capacitance (C_{oss}) as well as a low input capacitance (C_{iss}), gate resistance (R_G) and reverse transfer capacitance (C_{rss}) that allow for a small gating loss under resonant drive conditions.

The system described in this paper also incorporates a new low-loss gate driver that recovers most of the energy used to control the gate of the semiconductor device. Furthermore, it provides fast response times compatible with control schemes that achieve high bandwidth. An important attribute of this gate drive is the trapezoidal wave-shaping of the gate voltage; this characteristic allows fast commutation of the switch, requires only small passive components for its realization, and provides near-minimum loss.

As shown in Fig. 1, the inverter is followed by a transformation stage, which provides a means of scaling the voltages and currents of the inverter to a level at which a set of balanced resonant rectifiers can operate efficiently. This stage also provides resistance compression [22] to mitigate the inherent sensitivity of the class E to variations in load. Design of this type of circuit is treated in [22] so is not considered further here.

The next stage in the dc-dc structure is a resonant rectifier which transforms the intermediate RF ac waveforms back down to dc. Rectifier circuits having characteristics similar to tuned resonant inverters can operate efficiently under certain conditions [23]–[26]. This paper introduces a resonant rectifier structure in which two single-diode resonant rectifiers deliver power to a constant voltage output. The effective impedance of these rectifiers at the switching frequency is desired to be resistive to ensure suitable operation of the previous stages. Design methods for this rectifier are presented in Section IV.

The design of high efficiency dc-dc converters requires the implementation of output control techniques compatible with all of the requirements described in Section II-A. One suitable technique is the on/off or "burst-mode" modulation [27], [28] sometimes used to obtain high efficiency in converters operating at light load[2]. In the implemented converter, regulation of the output voltage is achieved by modulating the converter on and off ("bang-bang" control), forcing the voltage to comply with a ripple specification. The simplicity of this control scheme overcomes the difficulty in efficiently controlling RF amplifiers through other means (e.g. frequency modulation [1],

[2]Some cellular architectures, like the ones introduced in [9], also allow for high efficiency operation over wide load ranges.

[8], [29], [30]). The converter system developed here is regulated with a hysteretic controller that maintains the output voltage within a 100 mV hysteresis band through on/off or bang-bang control of the converter. Section V will evaluate the performance of a 10 W dc-dc converter switching at a frequency of 100 MHz with closed-loop voltage control.

III. Self-Oscillating Multi-Resonant Gate Drive

As discussed in the previous section, reducing gating loss is essential to operating at very high switching frequencies. Conventional hard-switched gate drives dissipate all of the energy delivered to the gate from the gate drive supply each cycle. This results in a frequency dependent gate drive loss:

$$P_{gate} = C_{iss} \cdot V_{gate}^2 \cdot f_s \tag{1}$$

To achieve very high frequency operation while maintaining acceptable gating loss, a resonant energy recovery gate drive is necessary. Switch transitions are effected by ringing charge on and off of the gate [3]–[10]. Under these conditions, most of the energy stored on the gate is recovered and total loss is a fraction of what can be expected if the device were hard gated.

One approach that has been used previously is a sinusoidal gate drive [7]–[11]. In this approach, a resonant network is used to ring charge on and off the gate such that the gate voltage is sinusoidal (possibly with a dc offset). For switching times much longer than a gate RC time constant, this can be an effective method, providing a reduced loss of:

$$P_{gate} = 2\pi^2 \cdot f_s^2 \cdot C_{iss}^2 \cdot R_G \cdot V_{G,ac}^2 \tag{2}$$

where C_{iss} is the gate input capacitance, R_G is the effective series resistance of the MOSFET gate and drive circuit, and $V_{G,ac}$ is the peak amplitude of the sinusoidal ac gate voltage.

While a sinusoidal resonant drive is effective in some applications, it does have some important limitations. First, many of the commercially-available LDMOS devices suitable for VHF power conversion incorporate a protective diode between the source and gate terminals, preventing the use of gate drivers which impose negative voltage excursions on the gate. Moreover, even when a sinusoidal gate drive can be used, the ac drive magnitude often has to be larger than needed to fully enhance the device in order to provide a fast gate drive transition time, increasing overall gate loss by a square law as in (2). The negative excursions of the gate drive voltage also induce unnecessary gate loss.

The most efficient way to charge/discharge the gate capacitance C_{iss} for a specified transition time is a constant current source [31, Appendix A]. A trapezoidal drive voltage waveform applied at the gate of the semiconductor switch will yield an approximately constant current on the rising and falling edges of the gate voltage (for small gate resistance R_G), thus minimizing the power dissipated in the gate resistance. As shown in [32], the power dissipated in R_G of an MOS transistor driven by a trapezoidal waveform is:

$$P_{gate} = C_{iss}^2 \cdot V_{gate}^2 \cdot R_G \cdot \left[\frac{1}{t_r} + \frac{1}{t_f}\right] \cdot f_s \tag{3}$$

where V_{gate} is the maximum voltage of the trapezoid, C_{iss} is the input capacitance of the LDMOS,and t_r and t_f are the rise time and the fall time respectively of the drive waveform.

Consider driving the gate of a MRF373ALSR1 LDMOSFET (having C_{iss}=114 pF and R_G=0.3 Ω) at a switching frequency f_s=100 MHz with the three driving schemes described above. Hard gating with a peak gate voltage V_{gate}= 10 V dissipates 1.17 W. By contrast, the power dissipated by a sinusoidal gate drive with $V_{G,ac}$=15 V (large enough to rapidly enhance the device) is only 173.16 mW. A trapezoidal driving scheme with $t_r = t_f$=1 ns and V_{gate}=10 V yields a further reduced dissipation of only 78 mW.

Here we introduce an efficient gate drive using a simple multi-resonant structure to implement trapezoidal voltage wave shaping. This circuit, shown in Fig. 3, is a switched mode driver incorporating wave shaping methods similar to those employed in class F power amplifiers and related circuits [16], [17], [33]–[35], [36, Chapter 7]. Unlike traditional class F power amplifiers, the driver proposed here operates in switched mode, thus providing maximum efficiency.

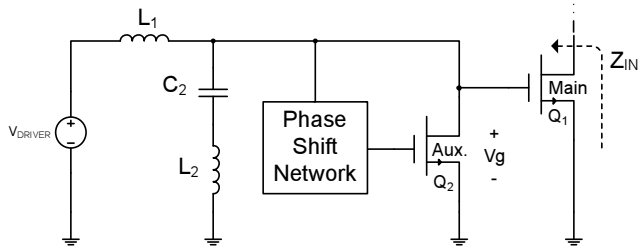


Fig. 3. Schematic of the multi-resonant gate drive. The input impedance Z_{IN}, when properly tuned, peaks in the vicinity of the fundamental and the third harmonics and has low impedance at the second harmonic.

Figure 4 shows a simple multiresonant passive network that is at the core of the gate drive. The input impedance

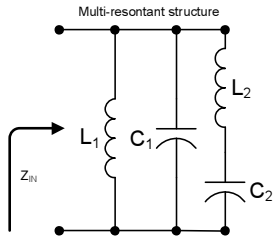


Fig. 4. Simple multiresonant network.

of the network (Z_{IN}) has maxima at two frequencies (poles). The impedance is zero at dc and at a frequency somewhere between the two maxima. The components L_2 and C_2 are tuned to be series resonant close to the second harmonic as viewed from the drain/source port of the auxiliary device. The resonant components L_1 and C_1 are tuned in conjunction with L_2 and C_2 such that the input impedance Z_{IN} in Fig. 4 presents relatively high impedance at the switching frequency and the third harmonic of the switching frequency. This is done in such a manner that the voltage v_g in Fig. 3 can support

approximately trapezoidal waveforms that contain a dominant fundamental voltage component and a smaller third harmonic component. A good design starting point for tuning the multi-resonant network is to start with impedance maxima (poles) at the fundamental and third harmonic, and a low impedance (zero) at the second harmonic of the switching frequency as shown in Fig. 5. Component values for tuning the poles of Z_{IN} in Fig. 4 at exactly the fundamental and third harmonic and placing the zero at the second harmonic can be determined starting from a selected value for C_1 [37], [38]:

$$L_1 = \frac{1}{9\pi^2 f_s^2 C_1}\,, \qquad L_2 = \frac{1}{15\pi^2 f_s^2 C_1}\,, \text{ and } \qquad C_2 = \frac{15}{16}C_1\,. \tag{4}$$

Note that the component C_1 incorporates the output capacitance C_{oss} of the auxiliary switch and the gate capacitance C_{iss} of the main semiconductor switch. It is important to minimize the stray inductance between the gate of the main MOSFET and the auxiliary drain node, such that both C_{oss} of the auxiliary device, and the gate capacitance C_{iss} of the main device can be considered connected in parallel. Because the inductor L_1 acts as a resonant inductor, it has a very small numerical value and small energy storage.

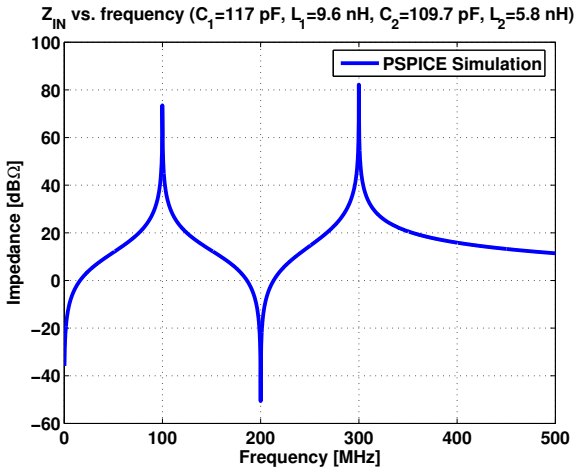


Fig. 5. Input impedance vs. frequency of the simple multiresonant structure shown in Fig. 3 when the reactive elements follow the relations given in Equation 4.

When the gate drive auxiliary switch in Fig. 3 drives this structure at the switching frequency with a duty ratio of somewhat less than 0.5, the voltage waveform at the gate is roughly trapezoidal and offset so that it never swings negative. Moreover, the dynamic characteristics provide zero voltage switching of the driver switch, such that energy delivered to the gate capacitance is naturally returned to the gate drive supply. These conditions arise as a result of the half-wave symmetry imposed by the impedance of the network [16], [17]. A simulation of the gate to source voltage of the main switch with a switching frequency of approximately 100 MHz is shown in Fig. 6. One can easily appreciate that the trapezoidal waveform and dc offset characteristics are achievable. Experimental results confirming practical low-loss operation of this drive are presented in Section V.

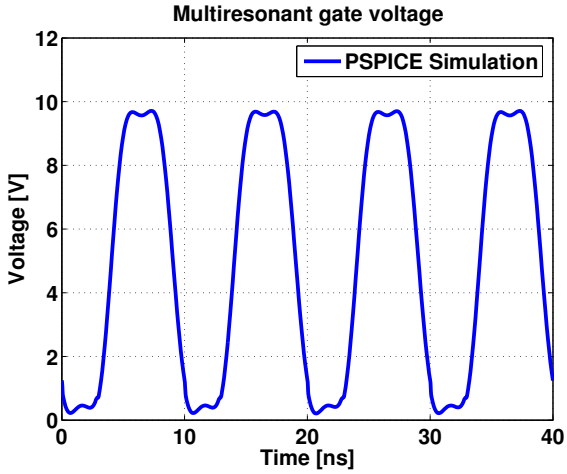


Fig. 6. Gate to source voltage at input of the main MOSFET of the converter.

Controlled self-oscillation of the driver is achieved by using an appropriate feedback network around the gate drive circuit. A fraction of the drain to source voltage of the gate drive MOSFET is phase shifted and applied to its gate. Figure 7 shows the network that provides the required phase shift along with a simplified schematic of the start up circuit. The start up circuit is required to initiate the oscillation at the application of the gate-drive input voltage. (As shown in Section V, modulating this input on and off provides a means of controlling the converter.)

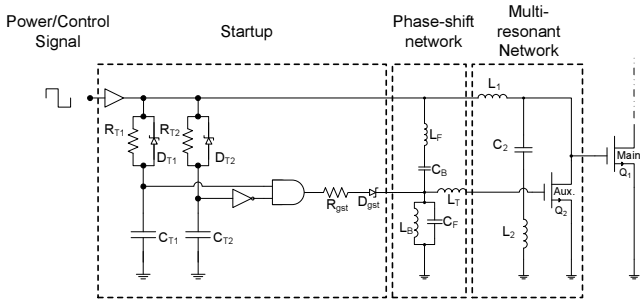


Fig. 7. Simplified schematic circuit of the startup control strategy.

Components L_F, C_F and L_T provide a phase shift of -180° of the fundamental voltage at the drain of the auxiliary device in order to achieve self-oscillation while at the same time the components are selected to minimize loading that could significantly change the impedance Z_{IN} of the multiresonant network.

This section presents PSPICE simulations of the self-oscillating multiresonant gate driver implemented in the prototype described in Section V. For this simulation, the gate of the main LDMOSFET (Freescale MRF373ALSR1) is modeled as a series RLC branch with $L_{G,main}$=700 pH, $R_{G,main}$=0.3 Ω and $C_{iss,main}$=114 pF. Referring to Fig. 7, the

values of the multiresonant elements are: L_1=8.1 nH, L_2=4 nH, C_2=150.56 pF. $C_{oss,aux}$=48 pF, which together with $C_{iss,main}$ makes C_1 =162 pF. Figure 8 shows the magnitude of the impedance Z_{IN} at the drain of the auxiliary LDMOSFET. The phase-shift network responsible for the self-oscillation is also included in the simulation as well as the parasitic elements present in the printed circuit board (PCB). The magnitude of Z_{IN} at the switching frequency (approximately 100 MHz) is higher that than at the third harmonic as explained above.

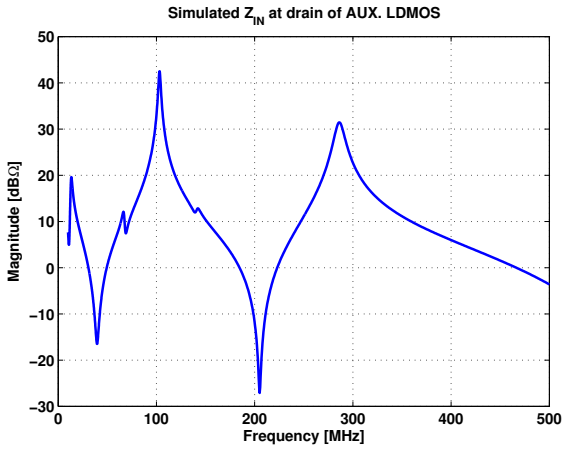


Fig. 8. Simulated input impedance at the drain of the auxiliary switch of Fig. 7. This simulation accounts for parasitics in the PCB and assumes linear device capacitances and 0.7 nH lead inductance in series with the gate of the main LDMOSFET. Notice that the phase-shift network does not significantly change the impedance at the frequencies of interest (fundamental, 2^{nd} and 3^{rd} harmonic).

The gate of the auxiliary MOSFET Q_2 (a Polyfet L8829) is part of the phase shift network and is modelled as series RLC branch with $R_{G,aux}$=3 Ω and $C_{iss,aux}$=30 pF. The gate inductance $L_{G,aux}$ is not significant and is included in the value of L_T. The values of the elements comprising the phase shift network are: L_F=100 nH, C_F=56.8 pF, L_B=100 nH, C_B=2 nF and L_T=84 nH. The magnitude and phase of the transfer function (TF) of the phase-shift network responsible for achieving self-sustained oscillation is shown in Fig. 9. As described above, the figure shows that at the intended frequency of oscillation (100 MHz), the phase-shift angle of the TF is -180°. The phase-shift network also provides filtering to attenuate the third harmonic, as is demonstrated in the figure.

The mechanism for starting the oscillation (and thereby tuning on the converter) is as follows. After the gate drive power supply is applied, a delay of duration T_h is provided to allow the voltage at the drain of the auxiliary device to settle. After this interval (T_h) a pulse of voltage of duration T_p is applied to the phase-shift network. This momentarily drives down the drain to source voltage of the auxiliary switch. At the end of the pulse, the drain to source voltage will naturally ring with the harmonic characteristics of the network. This voltage, in turn, drives the gate of the main switch. To stop the oscillations, the supply voltage to the multi-resonant gate

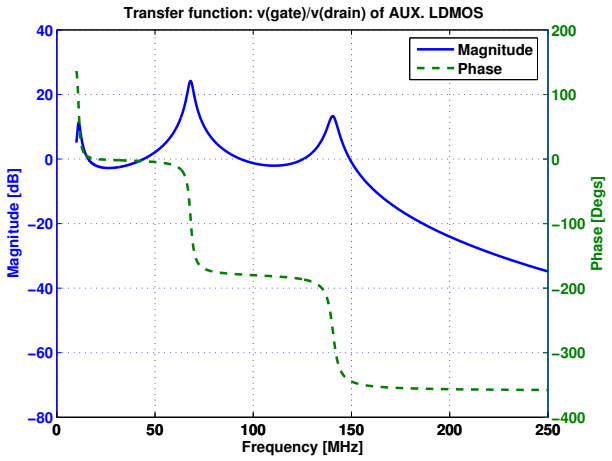


Fig. 9. Simulated magnitude and phase of the transfer function v_{gate}/v_{drain} of the auxiliary LDMOSFET. At the switching frequency (100 MHz), the phase shift is -180°.

driver is cut by a logic control signal. The durations of the hold interval (T_h) and the pulse interval (T_p) are determined by the timing components R_{T1},C_{T1} and R_{T2}, C_{T2} respectively. Diodes D_{T1} and D_{T2} provide a low impedance path to rapidly discharge the timing capacitors to allow for faster activation rates. Figure 10 shows the simulated voltage at the drain of the auxiliary LDMOSFET (gate of the main switch) under self-oscillating conditions at f_s=102.2 MHz.

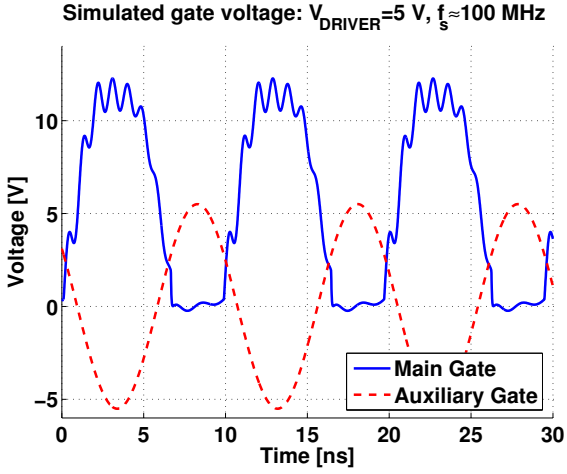


Fig. 10. Simulated gate voltages at the gates of the main and auxiliary switches. The switching frequency f_s=102.2 MHz.

When modulating the dc-dc converter on and off, the energy stored in the bypass capacitors, the timing elements of the network, and the output tank is lost in each transition. This energy loss, as well as the time required for the cell to achieve steady state operation, limits the maximum modulation frequency. On the whole, the small size of the energy storage components keeps this loss to a minimum and allows a relatively large control bandwidth on the order of 200 kHz.

Section V will present component values for the multi-resonant gate drive used in the prototype. This gate driver utilizes less than 100 mW at 100 MHz switching frequency (less than 10% of an equivalent hard-switched gate drive).

IV. Resonant Radio-Frequency Rectifier

The high-frequency sinusoidal voltage at the output of the inverter in Fig. 2 generates sinusoidal currents at the outputs of the transformation/compression stage. These currents are rectified to provide dc power to the converter output.

As described in [22] it is desirable for the fundamental voltages at the rectifier inputs to be substantially in phase with the currents at the output of the transformation/compression stage. Under this condition, the transformation/compression network will provide appropriate loading to the inverter to maintain the desired ZVS.

Figure 11 shows the schematic of the resonant rectifier investigated here, loaded with a constant voltage at the output. The rectifier is driven by a sinusoidal current source of magnitude I_{IN}. A resonant capacitance C_r represents the sum of an external capacitor C_{EXT} and an equivalent diode capacitance C_D. Resonant inductor L_R provides a path for the dc current and resonates with capacitance C_r so that the input looks resistive at the fundamental frequency. A similar rectifier structure was presented in the literature in [26] but for very different drive and loading conditions that are not applicable to the cell-modulation converter system considered here.

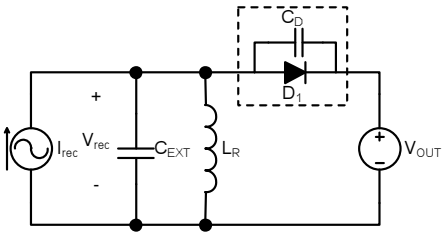


Fig. 11. Resonant rectifier connected to a constant output voltage. The resonant capacitance C_r is the sum of the diode capacitance C_D and an (optional) external capacitance C_{EXT}. C_{EXT} may also be placed directly in parallel with the diode.

The conduction duty cycle of the diode current depends on the component values. By adjusting the net capacitance C_R in parallel with the resonant inductor, it is possible to trade off the length of the conduction interval and the peak reverse voltage across the diode. It is convenient to have a conduction interval close to 50 percent, as this provides a good tradeoff between peak diode forward current and reverse voltage. This additional capacitance can either be added externally or can be solely provided by additional diode area, which can have the added benefit of reducing the overall conduction loss in the rectifier. The value of L_R of the resonant rectifier is selected in conjunction with C_r to provide the desired "resistive" input characteristics (fundamental rectifier input voltage in phase with rectifier input current). Appropriate values can be found through straight parametric search using a simulation tool (e.g. PSPICE or a piecewise linear simulator) by looking at the fundamental component of the voltage v_{rec} and minimizing the phase angle between the input current and the fundamental component of the rectifier input voltage at a given nominal output power.

Figure 12 shows the input current and voltage of a resonant rectifier (like the one in Fig. 11) simulated using PSPICE. For the simulation shown, L_R=18.8 nH, C_{EXT}=32 pF, C_D is the non-linear device capacitance of the diode (D_1, an MBRS260T3 Schottky diode), V_{OUT}=12 V, and the sinusoidal input current I_{IN}=0.67 A at a frequency of 100 MHz. The average power delivered to the load under these conditions is 6.2 W. Note that Fig. 12 shows that the fundamental component of the input voltage and the current are nearly in phase resulting in a rectifier with an equivalent resistance (only at the fundamental) of approximately 29.8 Ω. The equivalent impedance at the fundamental frequency of the rectifier will change with the input current. Over the operating range of the rectifier, it is desired that this equivalent input impedance remain substantially resistive. Table I shows how the equivalent impedance of the rectifier changes as P_{OUT} changes from 4 W to 14.47 W. Notice how even as the equivalent resistance changes over the operating range, the equivalent reactance remains small.

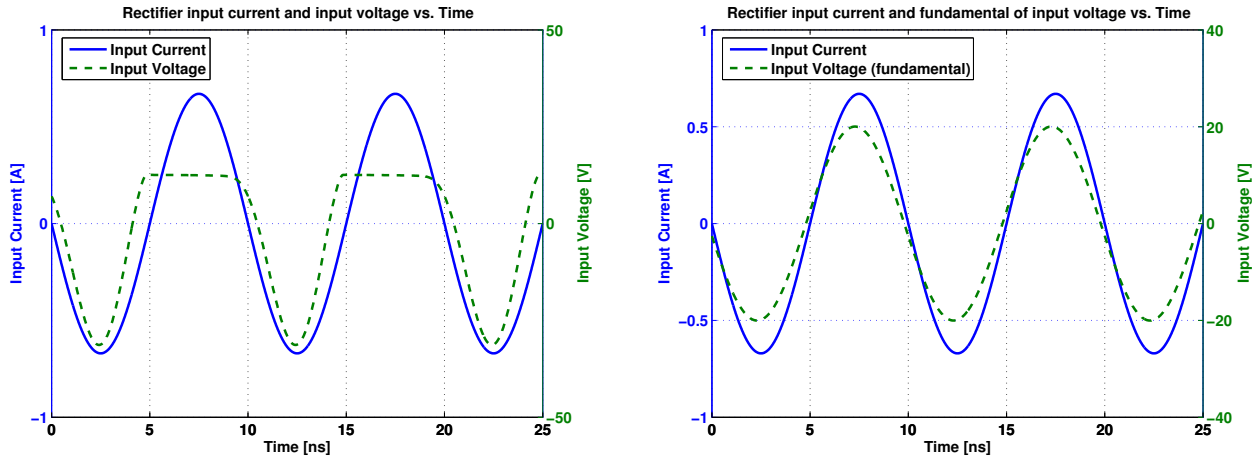
TABLE I
Equivalent impedance of the rectifier of Fig. 11.

P_{OUT} [W]	$\lvert Z_{IN}\rvert$ [Ω]	$\angle Z_{IN}$ (degrees)	$\Re e\{Z_{IN}\}$ [Ω]	$\Im m\{Z_{IN}\}$ [Ω]
4.000	38.52	21.6	35.81	14.18
5.398	32.87	7.2	32.61	4.12
6.554	28.61	0	28.61	0
7.621	25.33	-3.6	25.28	-1.59
8.643	22.73	-10.8	22.33	-4.26
9.634	20.62	-12.6	20.12	-4.50
10.611	18.87	-14.4	18.28	-4.69
11.583	17.40	-16.2	16.71	-4.85
12.549	16.16	-18.0	15.37	-4.99
13.509	15.10	-19.8	14.21	-5.11
14.470	14.17	-21.6	13.17	-5.22

The rectifier, a non-linear circuit, will generate an input voltage v_{rec} with significant harmonic content. For optimum operation of the inverter, it is desirable to block the effects of the harmonic components on the inverter current. This is accomplished as part of the transformation stage and resistance compression network as described in [22].

V. Experimental Results and Evaluation

This section evaluates the performance of a prototype dc-dc converter implementing the techniques described in the previous sections. Figure 13 shows a photograph of the 11.5 W converter operating at a switching frequency of approximately 100 MHz. Schematics and component values for the power stage are provided in Figs. 2 and 7 and Tables II and III. The input voltage range is from 11 V to 16 V and the output voltage is 12 V with an output voltage ripple of 100 mV.



(a) Time domain

(b) Fundamental

Fig. 12. Rectifier input voltage and input current, when driven by a sinusoidal current source I_{IN} at a frequency of 100 MHz. The resonant rectifier is delivering 6.2 W to a 12 V output.

TABLE II

COMPONENTS USED IN 100 MHZ DC-DC CONVERTER OF FIG. 2.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value
C_{C1}	18 pF +15 pF	CDE Chip-Mica 100 V	MC08EA180J MC08EA150J	36.22 pF
C_{C2}	56 pF +7 pF	CDE Chip-Mica 100 V	MC12FA560J MC08CA070C	66.5 pF
C_{extra}	10 pF × 2	CDE Chip-Mica 100 V	MC08CA100D	
C_{in}	2.2 μF +0.68 μF +0.047 μF × 12	Tantalum 35 V Tantalum 35 V Ceramic 50 V	PCT6225CT PCT6684CT Kemet	
C_R	82 pF +2 pF	CDE Chip-Mica 100 V	MC12FA8205 MC08CA020D	
C_{R1}, C_{R2}	15 pF × 2	CDE Chip-Mica 100 V	MC08EA150J	C_{R1}=32.6 pF C_{R2}=32 pF
C_{out}	0.1 μF × 19	Kemet Ceramic 50 V	C0805C104M5UAC	
D_1, D_2	Schottky Power Diode	ON Semi 60V, 2.0A	MBRS260T3	
L_1	17.5 nH	Coilcraft	B06T6	
L_{C1}	33 nH	Coilcraft	1812SMS-33N	38.1 nH
L_{C2}	68 nH	Coilcraft	1812SMS-68N	69.9 nH
L_{choke}	120 nH × 2	Coilcraft	1812SMS-R12G	
LDMOS		Freescale 70 V (max V_{ds})	MRF373ALSR1	
L_R	12.5 nH + Two-turn magnet wire coil +8.9nH board parasitic	Coilcraft	A04TJ 18 AWG	Approx. 22 nH
L_{R1}, L_{R2}	18.5 nH	Coilcraft	A05T	L_{R1} =18.9 nH L_{R2} =18.7 nH

Waveforms showing the operation of the inverter for $V_{in,dc}$ = 11 V and $V_{out,dc}$ = 12 V can be seen in Fig. 14. In the top panel of the figure are the drain to source voltage and the voltage at the input of the transformation stage in Fig. 2. It is clear from the figure that zero-voltage turn-on of the LDMOSFET is achieved, indicating a proper impedance

TABLE III

COMPONENTS USED IN THE SELF-OSCILLATING MULTI-RESONANT GATE DRIVE OF FIG. 7.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value
L_1		PCB trace		8.1 nH
C_1	48 pF +114 pF		$C_{oss,aux}$ $C_{iss,main}$	162 pF
L_2		PCB trace		4 nH
C_2	100 pF +47 pF +4 pF	CDE Chip-Mica 100 V	MC12FA101J MC12FA470J MC08CA040D	150.56 pF
L_F	100 nH	Coilcraft	1812SMS-R10 L	100 nH
C_B	2 nF	Ceramic 50 V	Kemet	2 nF
C_F	47 pF +5 pF +3 pF	CDE Chip-Mica 100 V	MC12FA470J MC08CA050D MC08CA030D	56.8 pF
L_B	100 nH	Coilcraft	1812SMS-R10 L	100 nH
L_T	82 nH	Coilcraft	1812SMS-82N L	84 nH
R_{T1}	1 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF1001	1 kΩ
C_{T1}	100 pF +220 pF	Kemet, 0805, 50 V Kemet, 0805, 50 V	C0805C101J1GAC C0805C221J5GACTU	325 pF
D_{T1}		Diodes Inc.	BAS70-7	
R_{T2}	2.43 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF2431	2.43 kΩ
C_{T2}	100 pF +220 pF	Kemet, 0805, 50 V Kemet, 0805, 50 V	C0805C101J1GAC C0805C221J5GACTU	325 pF
D_{T2}		Diodes Inc.	BAS70-7	
R_{gst}	100 Ω‖100 Ω	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF1000	50 Ω
D_{gst}		Diodes Inc.	BAS70-7	
IC_1		National LLP-6	LM5115	
IC_2		National LLP-6	LM5115	
Auxiliary LDMOS		Polyfet SO-8	L88219	

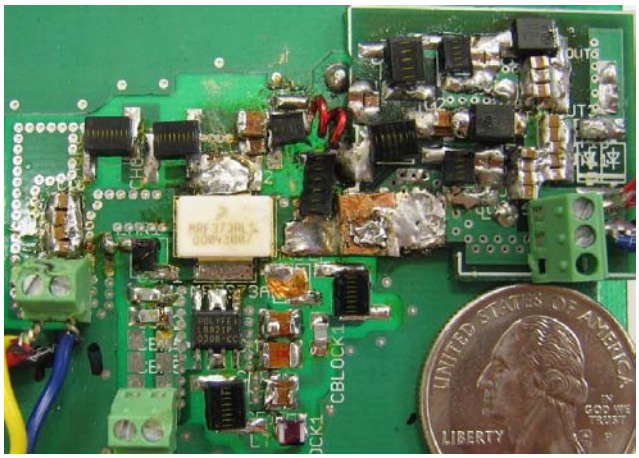


Fig. 13. Power stage of the prototype 100 MHz dc-dc power converter.

match. Shown at the bottom of the same figure is the gate to source voltage driving the semiconductor switch. The total power dissipated by the gate driver, including the startup circuitry, was measured to be less than 100 mW, which is more than an order of magnitude less than the power that would be dissipated had the switch been driven with conventional hard-switched gating (and lower than the 300 mW dissipation of an earlier implementation of this gate drive [22]).

The output voltage ripple is shown in Fig. 15 when $V_{OUT,DC} = 12$ V, $P_{OUT} = 10$ W. Under these conditions, the controller modulates the converter on and off at 83.3 kHz to provide the average power required to regulate the output. The control signal modulating the converter system on and off is shown in the lower trace of Fig. 15. This control signal commands the converter either to operate or to remain inactive depending on the conditions of the output voltage. The resulting output ripple is approximately 100 mV peak to peak, independent of load. In the figure, the 100 MHz switching ripple (observed as the "hash" when the output voltage is rising) is under-sampled in the time scale shown. While the modulating frequency is on the order of 100 kHz, most of the the energy storage components in the converter are sized based on the 100 MHz switching frequency. Only the input and output capacitors are sized based on the modulation frequency. The modulation frequency is determined by the loading conditions, the allowed hysteresis band around the nominal output voltage, and the size of the output filter capacitor. In the implemented design, the maximum modulation frequency was in excess of 200 kHz. Figure 16 shows the schematic for the hysteretic modulation controller and the switched-mode

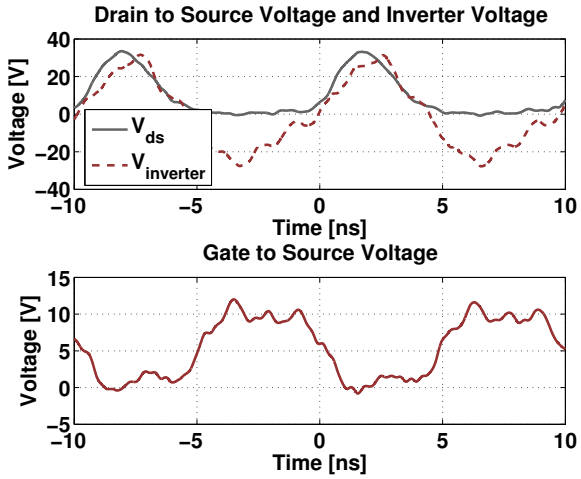


Fig. 14. Drain to source voltage and gate to source voltage of the prototype converter. Also shown is the voltage at the input of the transformation stage. Values are shown for a dc input voltage of 11 V and dc output voltage of 12 V.

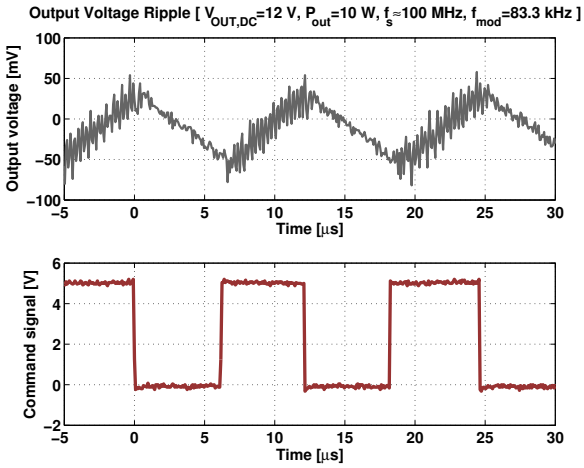


Fig. 15. Output voltage ripple and modulation control signal during steady state operation. $V_{OUT,DC} = 12$ V, $P_{OUT} = 10$ W, $V_{IN} = 16$ V.

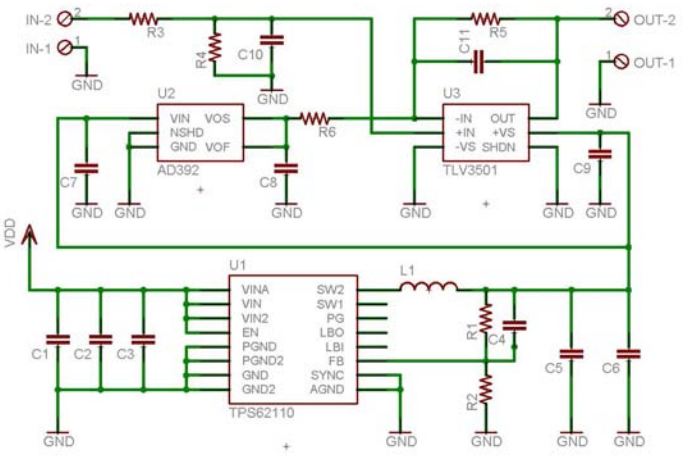


Fig. 16. Schematic of the hysteretic controller.

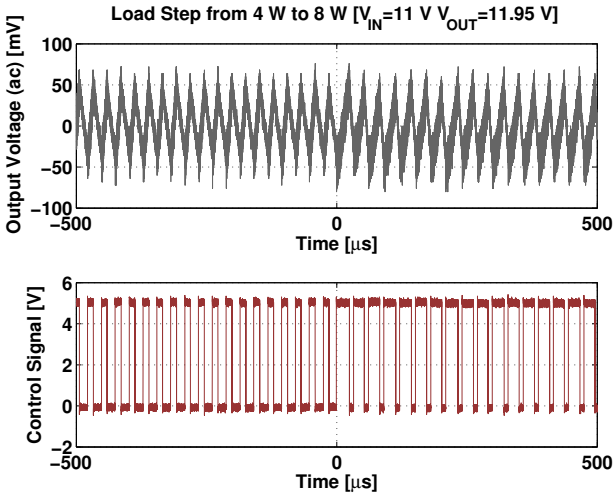


Fig. 17. Output voltage ripple and modulation control signal during a load step. P_{OUT} is changed from 4W to 8W.

regulator that provides power to the self-oscillating gate drive and start-up circuitry.

Table IV lists all the components used in the design of the controller and the auxiliary power supply which provides power to the gate drive. This auxiliary supply is a switched mode supply that is rated to provide the power for the controller and the gate drive.

As described in Section II, the on/off control scheme and the small values of the reactive components allow for fast dynamic response of the converter. This is evident in Fig. 17 which shows the output voltage during a step change in load going from 4 W to 8 W: no substantive change in output voltage is observed. The figure also shows the change in the modulation control signal due to the load change.

As described in Section III, the small sizes of the energy storage elements used in the design of the dc-dc converter allows for fast modulation rates. Figure 18 shows the modulation control signal and the drain to source voltage of the main MOSFET when the cell is switched on and off. The converter reaches steady state operation in approximately 600 ns at turn-on and also 600 ns at turn-off.

Figure 19 shows the efficiency of the dc-dc converter when operating under closed loop control. The figure plots the efficiency as the input voltage is varied over the operating range (11 V to 16 V), parameterized in output power $P_{\rm out}$. While the efficiency of this prototype design is not particularly high, our ongoing design work indicates that substantially higher efficiencies are achievable using the design methods proposed here.

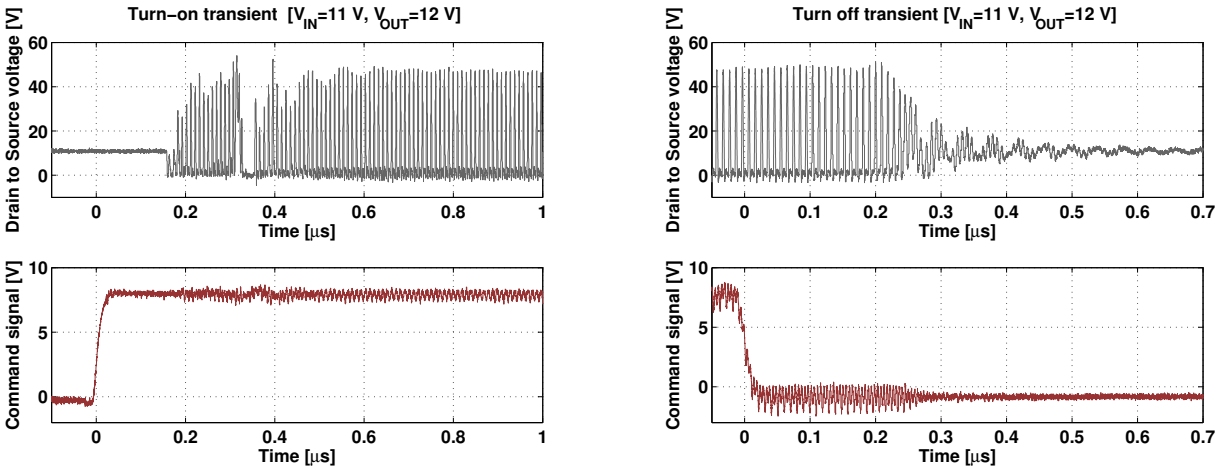
VI. Conclusion

This document describes methods and circuits suitable for the design of dc-dc converters operating at very high frequencies. These methods are applied in the design of a dc-dc a converter operating at a switching frequency of 100 MHz.

TABLE IV

COMPONENTS USED IN THE ON-OFF CONTROLLER BOARD AND AUXILIARY POWER SUPPLY OF FIG. 16.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number
R_1	510 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF5103
R_2	150 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF1503
R_3	7.5 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF7501
R_4	3.9 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF3901
R_5	100 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF1003
R_6	3 kΩ	Rohm, 0805, 1/8 W, 1 %	MCR10EZHF3001
C_1	10 μF	TDK, 1210, 16 V	C3225X5R1C106M
C_2	1 μF	TDK, 0805, 16 V	C2012X5R1C105K
C_3	0.1 μF	KEMET, 0805, 50 V	C0805C104M50AC
C_4	10 pF	KEMET, 0805, 100 V	C0805C100J1GAC
C_5	22 μF	TDK, 1210, 10 V	C3225X5R1A226M
C_6	1 μF	TDK, 0805, 16 V	C2012X5R1C105K
C_7	0.1 μF	KEMET, 0805, 50 V	C0805C104M50AC
C_8	0.1 μF	KEMET, 0805, 50 V	C0805C104M50AC
C_9	0.1 μF	KEMET, 0805, 50 V	C0805C104M50AC
C_{10}	100 pF	KEMET, 0805, 100 V	C0805C101J1GAC
C_{11}	2 pF	CDE, 0805, 100 V	MC08CA020D
U_1		Texas Instruments, QFN16	TPS6211
U_2		Texas Instruments, SOT23-6	TLV3501
U_3		Analog Devices, TSOT23-5	AD392



(a) On (b) Off

Fig. 18. Drain to source voltage and control signal during startup and shut down of the converter in on/off control. V_{IN}=11 V, V_{OUT}=12 V. The cell is fully on in 600 ns and turns off in about 600 ns.

Gate drive, rectifier and control designs are explored in detail, and experimental measurements of the complete converter are presented that verify the design approach. The gate drive, a self-oscillating multi-resonant circuit, dramatically reduces the gating power while ensuring fast on-off transitions of the semiconductor switch. The rectifier is a resonant topology that absorbs diode parasitic capacitance and is designed to appear resistive at the switching frequency. The small sizes of the energy storage elements (inductors and capacitors) in this circuit permit rapid start-up and shut-down and a correspondingly high control bandwidth. These characteristics are exploited in a high-bandwidth hysteretic control scheme that modulates the converter on and off at frequencies as high as 200 kHz. It is anticipated that the guidelines and techniques presented here will facilitate the development of power supplies with switching frequencies in the VHF range and beyond that meet the emerging demands for high performance power electronics.

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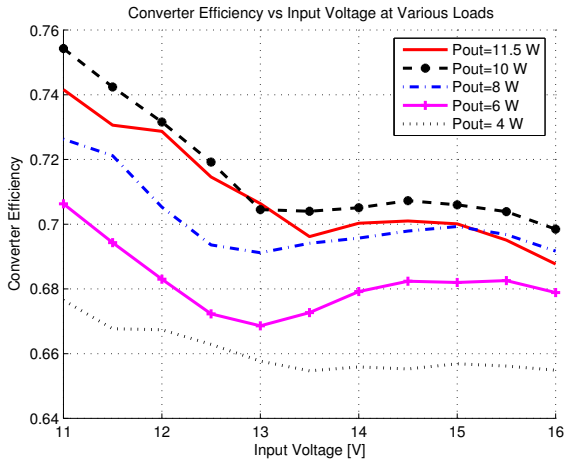

Fig. 19. Efficiency vs. input voltage at different output power levels. V_{out}=12 V.

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