Resistance Compression Networks for Resonant Power Conversion

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***Abstract*— A limitation of many high-frequency resonant inverter topologies is their high sensitivity to loading conditions. This paper introduces a new class of matching networks that greatly reduces the load sensitivity of resonant inverters and RF amplifiers. These networks, which we term resistance compression networks, serve to substantially decrease the variation in effective resistance seen by a tuned RF inverter as loading conditions change. We explore the operation, performance characteristics, and design of these networks, and present experimental results demonstrating their performance. Their combination with rectifiers to form rf-to-dc converters having narrow-range resistive input characteristics is also treated. The application of resistance compression in resonant power conversion is demonstrated in a dc/dc power converter operating at 100 MHz.**

I. BACKGROUND

A PRINCIPAL mean for improving performance and reducing the size of power electronics is through the increase in switching frequency. Resonant dc/dc power converters enable much higher switching frequencies than can be achieved with conventional pulse-width modulated circuits, due to their natural soft-switched operation and ability to absorb and utilize circuit parasitics in the conversion process. For example, efficient resonant dc/dc power conversion has been demonstrated at frequencies in excess of 100 MHz, and operation at much higher switching frequencies is clearly feasible [1], [2]. Further development of resonant power converter technology is thus of great potential value. This paper introduces a new circuit technique that overcomes one of the major limitations of resonant dc/dc converters at extremely high frequencies, and expands the range of applications for which resonant conversion is effective.

Figure 1 shows a basic structure for a high-frequency resonant dc/dc converter, comprising an inverter stage, a transformation stage, and a rectifier stage [1]–[10].

The inverter stage draws dc input power and delivers ac power to the transformation stage. Inverters suitable for extremely high frequency operate resonantly, and take advantage of the characteristics of the load to achieve zero-voltage switching (ZVS) of the semiconductor device(s) [11]–[18].

The rectifier stage takes ac power from the transformation stage and delivers dc power to the output. In addition to conventional rectifier topologies, resonant converters can take advantage of a variety of resonant rectifiers (e.g. [19], [20]). The system may be designed such that the rectifier stage appears resistive in a describing function sense (e.g., [1], [10], [19], [20]) and is matched to the inverter by the action of the transformation stage. The functions of the transformation stage are to develop this impedance match, to provide voltage and current level transformation, and in some cases to provide electrical isolation. The transformation stage can be realized using conventional transformers, "wide-band" or "transmission-line" transformers [11], [15], [21], matching networks [22], or similar means.

Power or output control of resonant converters can be achieved through a number of means, including frequency modulation [3], [5], on/off control [1], [23], and extensions of these techniques [1], [24], [25]. Fixed-frequency control techniques are preferable for circuit implementations with high-order tuned tanks or narrow-band transformation stages, and we focus on fixed-frequency operation for purposes of this paper.

A major limitation of resonant converter circuits is the sensitivity of the inverter stage to loading conditions. Switched-mode radio-frequency (RF) inverters suitable for ultra-high frequencies (e.g., classes *DE*, *E*, and *F*) exhibit high sensitivity to the effective impedance of the load. For example, class *E* inverters only operate under soft switched conditions over about a factor of two in load resistance. While acceptable in communications applications (in which the load resistance is relatively constant), this is problematic for many dc/dc power converter applications, where the effective resistance presented by the matching stage and rectifier varies greatly with output voltage and current (e.g., [10]). This problem is particularly severe in applications in which the voltage conversion ratio varies substantially; such applications include charging systems where the converter must deliver constant power over a wide output voltage range and regulating converters where the converter must operate over a wide input voltage range and/or the same converter design must be capable of supporting a range of output voltages.

This paper introduces a new class of matching/transformation networks that greatly reduce the load sensitivity of tuned RF power inverters. These networks, which we term resistance compression networks, serve to greatly reduce the variation in effective resistance seen by a tuned RF inverter as loading conditions change.

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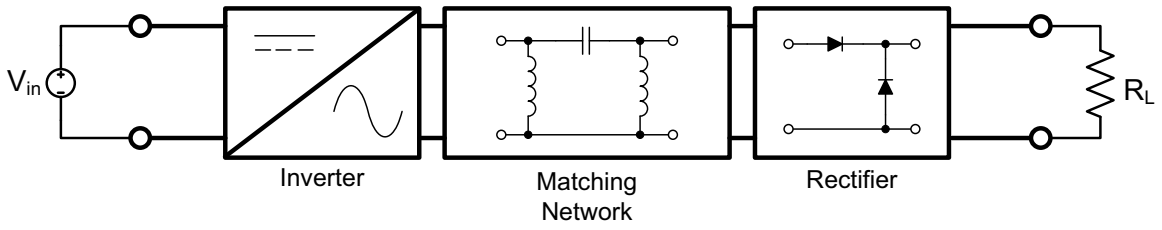


Fig. 1. Structure of the power stage of a resonant dc/dc converter. The converter comprises an inverter (dc/ac) circuit, a transformation/matching circuit, and a rectifier (ac/dc) circuit.

Compression networks ideally act without loss, such that all energy provided at the input port is transformed and transferred to the resistive load. In effect, the load resistance range appears compressed when looking through a resistance compression network. This effect can be used to overcome one of the major deficiencies of tuned radio-frequency circuits for power applications and expand the range of applications for which high-frequency resonant power conversion is viable.

Section II of the paper introduces resistance compression networks, including their fundamental principles of operation, and performance characteristics. Experimental results demonstrating their performance are also presented. Section III shows how resistance compression networks can be paired with appropriate rectifiers to yield high-performance rf-to-dc converters with resistive input characteristics. Section IV addresses design considerations for resistance compression networks and resistance compressed rectifiers. Application of this approach to the design of a 100 MHz dc/dc power converter is presented in Section V. Section VI concludes the paper.

II. Resistance Compression Networks

Here we introduce circuits that provide the previously described resistance compression effect. These circuits operate on two matched load resistances whose resistance values, while equal, may vary over a large range. As will be shown in Section III, a variety of rectifier topologies can be modelled as such a matched resistor pair.

Two simple linear circuits of this class that exhibit resistance compression characteristics are illustrated in Fig. 2. When either of these circuits is driven at resonant frequency $\omega_0 = \frac{1}{\sqrt{LC}}$, of its LC tank, it presents a resistive input impedance $\mathrm{R_{in}}$ that varies only a small amount as the *matched* load resistances R vary across a wide range. For example, for the circuit of Fig. 2(a), the input resistance is:

$$R_{in} = \frac{2R}{1 + \left(\frac{R}{Z_0}\right)^2} \tag{1}$$

in which $Z_0 = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the tank. For variations of R over a range having a geometric mean of $\mathrm{Z_0}$ (that is, $\mathrm{R} \in \left[\frac{Z_0}{c}, cZ_0\right]$, c is constant that defines the span of the resistance range) the variation in input resistance R_{in} is smaller than the variation in load resistance R. The amount of "compression" that is achieved for this case (around a center value of impedance $Z_c = Z_0$) is illustrated in Table I. For example, a $100:1$ variation in R around the center value results in only a $5.05:1$ variation in R_{in}, and a $10:1$ variation in load resistance results in a modest $1.74:1$ variation in R_{in}. Furthermore, because the reactive components are ideally lossless, all energy driven into the resistive input of the compression network is transformed in voltage and transferred to the load resistors. Thus, the compression network can efficiently function to match a source to the load resistors, despite large (but identical) variations in the load resistors.

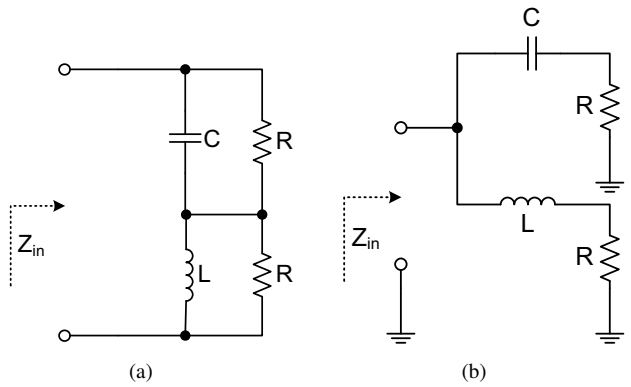


Fig. 2. Resistance compression circuits. Each of these circuits provides a compression in apparent input resistance. At the resonant frequency of the LC tank the input resistance $\mathrm{R_{in}}$ varies over a narrow range as the matched resistors R vary over a wide range (geometrically centered on the tank characteristic impedance). The circuits achieve lossless energy transfer from the input port to the resistors R.

TABLE I
Characteristics of the Resistance Compression Network of Fig. 2(a).

Ratio of R range	Range of R	Ratio of $\mathrm{R_{in}}$ range	Range of $\mathrm{R_{in}}$
100:1	$0.1\mathrm{Z_0}$ to $10\mathrm{Z_0}$	5.05:1	$0.198\mathrm{Z_0}$ to $\mathrm{Z_0}$
10:1	$0.316\mathrm{Z_0}$ to $3.16\mathrm{Z_0}$	1.74:1	$0.575\mathrm{Z_0}$ to $\mathrm{Z_0}$
4:1	$0.5\mathrm{Z_0}$ to $2\mathrm{Z_0}$	1.25:1	$0.8\mathrm{Z_0}$ to $\mathrm{Z_0}$
2:1	$0.707\mathrm{Z_0}$ to $1.41\mathrm{Z_0}$	1.06:1	$0.94\mathrm{Z_0}$ to $\mathrm{Z_0}$

For the circuit of Fig. 2(b), the input resistance at resonance is:

$$R_{in} = \frac{Z_0^2}{2R}\left[1 + \left(\frac{R}{Z_0}\right)^2\right] \tag{2}$$

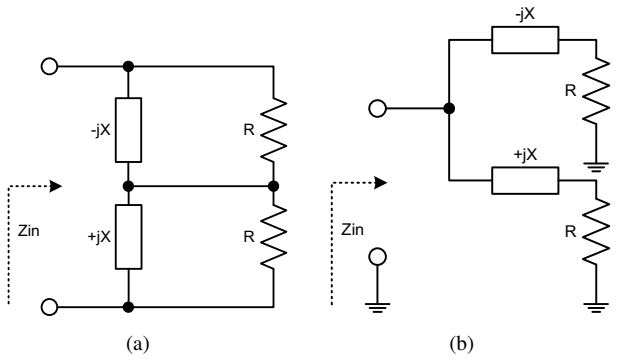


Fig. 3. Structure of some resistance compression networks. The impedance of the reactive networks is specified at the desired operating frequency. Implementation of the reactive networks may be selected to provide desired characteristics at frequencies away from the operating frequency.

More generalle, the compression networks of Fig. 2 may be designed with generalized reactive branch networks as shown in Fig. 3. The reactive branch networks in Fig. 3 are designed to have the specified reactance X at the designed operating frequency. For example, at this frequency the input impedance of the network in fig. 2(a) will be resistive with a value:

$$R_{in} = \frac{2R}{1 + \left(\frac{R}{X}\right)^2} \tag{3}$$

which provides compression of the matched load resistances about a center value of impedance $Z_c = X$. The impedances of these branches at other frequencies of interest (e.g. dc or at harmonic frequencies) can be controlled by how the branch reactances are implemented. Likewise, the resistance for the network of fig. 2(b) will be:

$$R_{in} = \frac{X^2}{2R}\left[1 + \left(\frac{R}{X}\right)^2\right] \tag{4}$$

Considerations regarding implementation of the branch networks are addressed in Section IV.

It should be noted that these networks can be cascaded to achieve even higher levels of resistance compression. For example, the resistances R in Fig. 3 can each represent the input resistance of subsequent resistance compression stage. An *"N-stage"* compression network would thus ideally have 2^N load resistances that vary in a matched fashion. However, the efficacy of multiple-stage compression is likely to be limited by a variety of practical considerations.

Figure 4 shows simulated and experimental results from a compression network of the type shown in Fig. 2(a) with component values shown in Table II. The network has a resonant frequency of 85.15 MHz and a characteristic impedance of 57.35Ω (slightly lower than nominal due to small additional parasitics) . The anticipated compression in input resistance is achieved, and in all cases the measured reactive impedance at the operating frequency is negligible.

The networks of Fig. 3 provide resistance compression about a specified value. It is also possible to achieve both resistance compression and impedance transformation in the same network. Figure 5 shows two structures of four-element compression / transformation networks. As shown in Appendix A, these networks can be designed to achieve both resistance compression and transformation of the resistance up or down by an amount only limited by efficiency requirements, component quality factor, and precision. As with the two-element networks, the input impedance remains entirely resistive over the whole load-resistance range.

TABLE II

COMPONENTS USED TO OBTAIN DATA IN FIG. 4.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number
C	33pF	CDE Chip Mica 100V	MC08FA330J
L	100nH	Coilcraft	1812SMS-R10

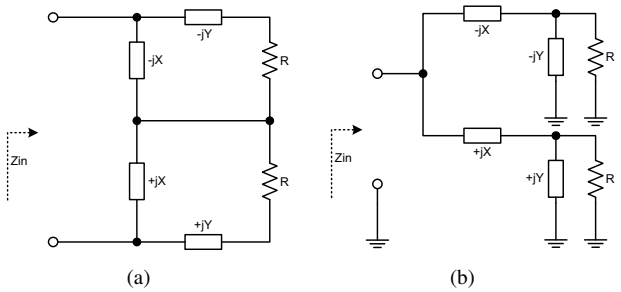


Fig. 5. Four element compression networks. These networks can provide both resistance compression and impedance transformation.

Figure 7 shows simulation and experimental measurement of a four element impedance compression network operating at a frequency of 97.4 MHz which provides both compression and transformation (Fig. 6, Table III). The load resistance is swept between 5Ω and 500Ω and presents a resistive input impedance over the whole range that varies between 50Ω and 290Ω.

The results presented in both the two element and four element resistance compression networks show the potential

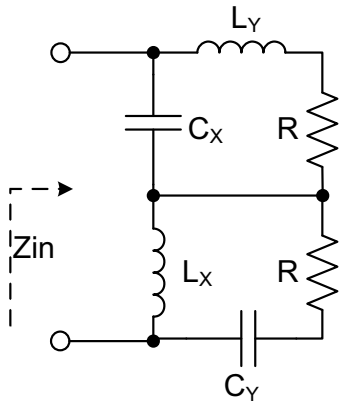
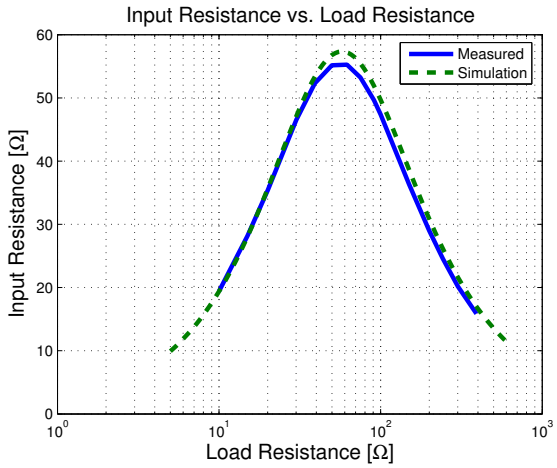
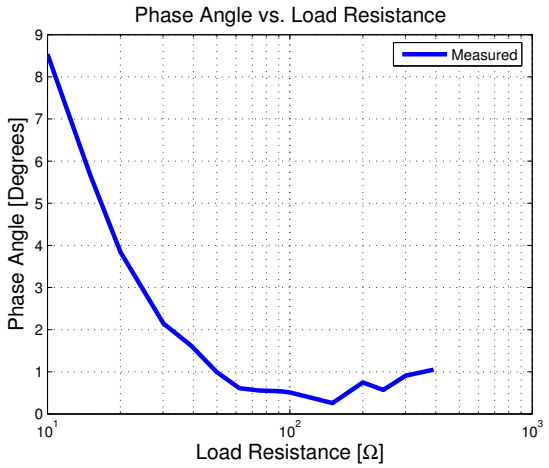


Fig. 6. Four element compression network used to obtain experimental data.

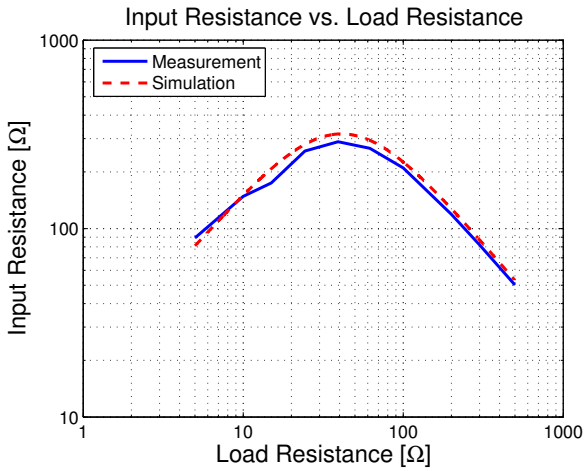


(a) Input Resistance $\Re e\{Z_{in}\}$ vs. R

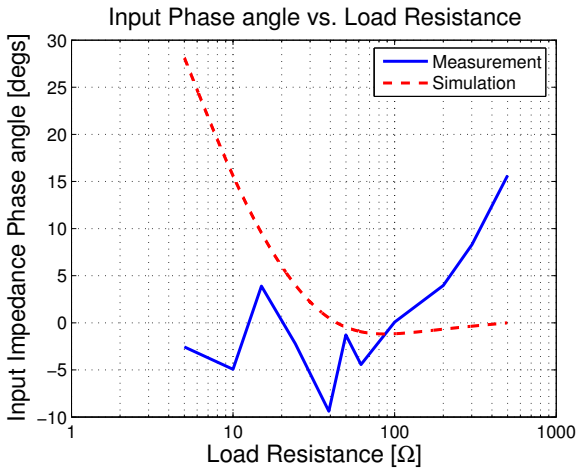


(b) Phase Angle of the Input Impedance vs. R

Fig. 4. Magnitude of the Input Resistance $\Re e\{Z_{in}\}$ and Phase of the Input Impedance (experimental and simulated) of the compression network shown in Fig. 2(a) as a function of R. L is an Coilcraft 100nH air-core inductor plus 7.2nH of parasitic inductance while C is a 33pF mica capacitor.



(a) Input Resistance ($\Re\{Z_{in}\}$) vs. R



(b) Phase Angle of the Input Impedance vs. R

Fig. 7. Input Resistance ($\Re\{Z_{in}\}$) and Impedance Phase (experimental and simulated) of the four element compression network shown in Fig. 6 as a function of R. $C_X = 15pF$, $L_X = 169nH$, $C_Y = 11pF$, $L_Y = 246nH$; measurements made at 97.4 MHz.

TABLE III
COMPONENTS USED TO OBTAIN DATA IN FIG. 7.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number
C_X	15pF	CDE Chip Mica 100V	MC08EA150J
C_Y	8pF +2pF +1pF	CDE Chip Mica 100V	MC08CA080C MC08CA020D MC08CA010D
L_X	169nH	Coilcraft	132-12SM-12
L_Y	246nH	Coilcraft	132-15SM-15

for marked improvement in the performance of load-sensitive power converters.

III. Resistance-Compressed Rectifiers

A resistance compression network can be combined with an appropriate set of rectifiers to yield an rf-to-dc converter with narrow-range resistive input characteristics. In order to obtain the desired compression effect, the rectifier circuits must effectively act as a matched pair of resistances when connected to a compression network of the kind described in Section II. A purely resistive input impedance can be achieved with a variety of rectifier structures. For example, in many diode rectifiers the fundamental ac voltage and current at the rectifier input port are in phase, though harmonics may be present [10].

One example of this kind of rectifier structure is an ideal half bridge rectifier driven by a sinusoidal current source of amplitude I_{in} and frequency ω_s, and having a constant output voltage $V_{dc,out}$, as shown in Fig. 8. The voltage at the input terminals of the rectifier $v_x(t)$ will be a square wave having a fundamental component of amplitude $V_{x1} = \frac{2V_{dc,out}}{\pi}$ in

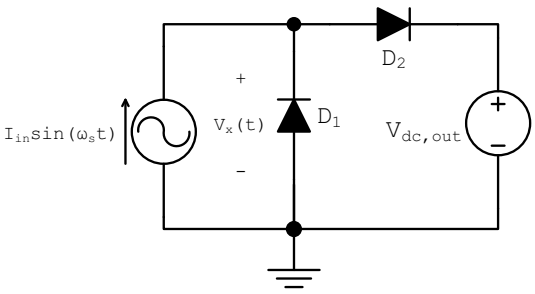


Fig. 8. Half-wave rectifier with constant voltage load and driven by a sinusoidal current source.

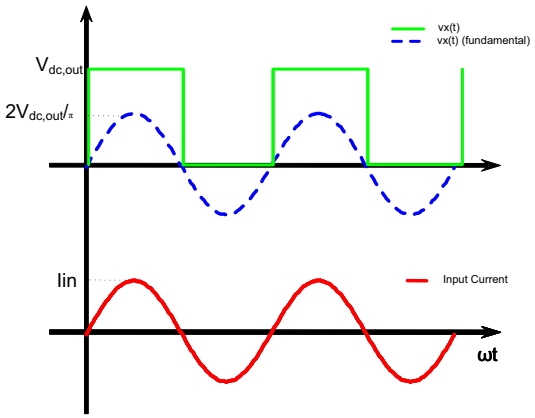


Fig. 9. Characteristic waveforms of the half-wave rectifier shown in Fig. 8. The input current and the fundamental of the input voltage are in phase.

phase with the input current $i_{\rm in}(t)$, as shown in Fig. 9. The electrical behavior at the fundamental frequency $\omega_{\rm s}$ (neglecting harmonics) can be modelled in a describing function sense as a resistor of value $\mathrm{R_{eq}} = \frac{2}{\pi}\frac{\mathrm{V_{out}}}{\mathrm{I_{in}}}$. Similarly, a full wave rectifier with a constant voltage at the output can be modelled at the fundamental frequency as a resistor $\mathrm{R_{eq}} = \frac{4}{\pi}\frac{\mathrm{V_{dc,out}}}{\mathrm{I_{in}}}$. There are many other types of rectifier topologies that present the above mentioned behavior; another example is the resonant rectifier of [19]. This rectifier also presents a resistive impedance characteristic at the fundamental frequency; furthermore it requires only a single semiconductor device and incorporates the needed harmonic filtering as part of its structure. Such a rectifier, when connected to a constant output voltage, presents a resistive equivalent impedance of the same magnitude as that of the full wave rectifier, $\mathrm{R_{eq}} = \frac{4}{\pi}\frac{\mathrm{V_{dc,out}}}{\mathrm{I_{in}}}$.

Driving this type of rectifier with a tuned network suppresses the harmonic content inherent in its operation and results in a resistive impedance characteristic at the desired frequency. This equivalent resistance can be represented by $\mathrm{R_{eq}} = \frac{k_{rect}}{|\mathrm{i_1}|}\mathrm{V_{dc,out}}$, where $\mathrm{k_{rect}}$ depends on the specific rectifier structure. As shown below, when two identical such rectifiers feed the same dc output and are driven via reactances with equal impedance magnitudes (e.g., as in the circuits of fig. 3), they act as matched resistors with values that depend on the dc output. Thus, a pair of such rectifiers can be used with a compression network to build a rectifier system having

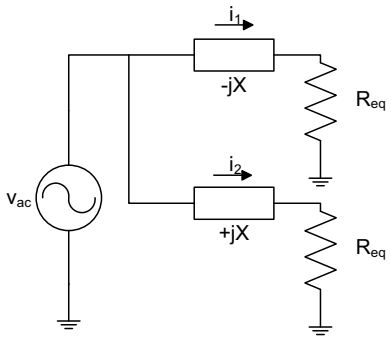


Fig. 10. A two element compression network with reactive branches represented by impedances evaluated at the operating frequency

a resistive ac-side (input) characteristic that varies little as the dc-side operating conditions change. This type of compression network/rectifier combination can be modelled as shown in Fig. 10.

We can express the magnitude of the current i_1 as:

$$|i_1| = \frac{V_{ac}}{\sqrt{X^2 + R_{eq}^2}} \tag{5}$$

By replacing $\mathrm{R_{eq}}$ with its corresponding value $\mathrm{R_{eq}} = \frac{k_{rect}}{|\mathrm{i_1}|}\mathrm{V_{dc,out}}$ we obtain

$$|i_1| = \frac{V_{ac}}{\sqrt{X^2 + \frac{k_{rect}^2}{|i_1|^2}V_{dc,out}^2}} \tag{6}$$

Rearranging:

$$|i_1|^2 X^2 + k_{rect}^2 V_{dc,out}^2 = V_{ac}^2 \tag{7}$$

Solving for $|i_1|$:

$$|i_1| = \sqrt{\frac{V_{ac}^2 - k_{rect}^2 V_{dc,out}^2}{X^2}} \tag{8}$$

From this expression we can see that the branch current magnitude $|i_1|$ depends on the dc output voltage and the reactance magnitude. The branch carrying $|i_2|$ has the same reactance magnitude and output voltage, so both branches present identical effective load resistances.

For all the rectifier structures that can be represented by an equivalent resistance of value $\mathrm{R_{eq}} = \frac{k_{rect}}{|\mathrm{i_1}|}\mathrm{V_{dc,out}}$, we can express the equivalent resistances loading each branch as:

$$R_{\rm eq} = \frac{k_{rect}V_{dc,out}}{\sqrt{\frac{V_{ac}^2 - k_{rect}^2 V_{dc,out}^2}{X^2}}} = X\sqrt{\frac{1}{\left(\frac{V_{ac}}{k_{rect}V_{dc,out}}\right)^2 - 1}} \tag{9}$$

The net input resistance of the resistance-compressed rectifier set at the specific frequency will be determined in equation (4) where $\mathrm{R_{eq}}$ for the rectifier replaces R.

Looking from the dc side of the resistance compressed rectifier we also see interesting characteristics. For a given ac-side drive, a resistance-compressed rectifier will act approximately

as a constant power source, and will drive the output voltage and/or current to a point where the appropriate amount of power is delivered.

IV. Design considerations for resistance compression networks

In designing resistance compression networks and resistance compressed rectifiers there are some subtle considerations that must be taken into account. The first consideration is how the compression network processes frequencies other than the operating frequency. When a compression network is loaded with rectifiers, the rectifiers typically generate voltage and/or current harmonics that are imposed on the compression network. It is often desirable to design the compression network to present high or low impedances to dc and to the harmonics of the operating frequency in order to block or pass them. Moreover, in some cases it may be important for the impedances of the two branches to be similar at harmonic frequencies in order to maintain balanced operation of the rectifiers. To achieve this, it is often expedient to use multiple passive components to realize each of the reactances in the network (i. e., reactances $\pm jX$ in Fig. 3.) This strategy was employed in the compression network of the system in Fig. 15 described in the following section.

A second design consideration is that of selecting a center impedance Z_C for the compression. Typically, one places the center impedance at the geometric mean of the load resistance range to maximize the amount of compression. However, in some cases one might instead choose to offset the center impedance from the middle of the range. This might be done to make the input resistance of the compression network vary in a particular direction as the power level changes. Also, in systems that incorporate impedance or voltage transformation, different placements of the compression network are possible, leading to different possible values of Z_C. For example, one might choose to place a transformation stage before the compression network, on each branch after the compression network, or both. The flexibility to choose Z_C in such cases can be quite valuable, since centering the compression network at too high or too low an impedance level can lead to component values that are either overly large or so small that they are comparable to parasitic elements.

A third major consideration is circuit quality factor and frequency sensitivity. Since compression networks operate on resonant principles, they tend to be highly frequency selective. This fact requires careful component selection and compensation for circuit parasitics in the design and layout of a compression network. Moreover, as with matching networks that realize large transformation ratios [21], compression networks realizing large degrees of compression require high quality-factor components. Component losses typically limit the practical load range over which useful compression may be achieved.

V. Motivation and Example Application: A 100 MHz dc/dc Converter

The resistance compression networks described in Section II and resistance-compressed rectifiers described in Section III have many potential applications, including radio-frequency rectifiers (e.g., for rectennas, or rectified antennas [19], [26]) and dc/dc converters operating at VHF and microwave frequencies. Here we describe some motivations for their use in resonant dc/dc converters, and provide a practical example of a resistance compressed rectifier in a 100 MHz dc/dc converter

A. Motivation

The motivation for resistance compression networks in rf-to-dc conversion applications is straightforward: The compression network allows the rectifier system to appear as an approximately constant-resistance load independent of ac drive power or dc-side conditions. In rectenna applications this can be used to improve matching between the antenna and the rectifier. As will be shown, this is also useful for preserving efficient operation of resonant dc/dc converters as operating conditions change.

As described in Section I, resonant dc/dc power converters consist of a resonant inverter, a rectifier, and a transformation stage to provide the required matching between the rectifier and the inverter. An inherent limitation of most resonant inverters suitable for VHF operation is their high sensitivity to loading conditions. This sensitivity arises because of the important role the load plays in shaping converter waveforms. Consider, for example, a class E inverter designed to operate efficiently at a nominal load resistance. As the load resistance deviates substantially from its design value, the converter waveforms rapidly begin to deteriorate. As seen in the example drain-source waveforms of Fig. 11, the peak switch voltage rises rapidly when the resistance deviates in one direction. Moreover, zero-voltage turn-on of the device is rapidly lost for deviations in either direction (*c. f.* Fig. 11, [27, fig. 5]).

There are at least three reasons why maintaining near zero-voltage switch turn on is important in very high frequency power converters. First, the turn-on loss associated with the discharge of the capacitance across the switch is undesirable and eliminating this loss is often important for achieving acceptable efficiency. Second, a rapid drain voltage transition at turn on can affect the gate drive circuit through the Miller effect, increasing gating loss and possibly increasing switching loss due to the overlap of switch voltage and current. This issue can be of particular concern in circuits employing resonant gate drives, and in cases where the gate drive transitions are a significant fraction (e.g., 5%) of the switching cycle. Finally, zero-voltage switching avoids electromagnetic interference (EMI) and capacitive noise injection generated by rapid drain voltage transitions.

In view of the above considerations, there exist substantial limits on allowable load variations. In the example of Fig. 11, even if the maximum switch off-state voltage is allowed to increase and the switch voltage magnitude at turn on is allowed to be as large as the dc input voltage (a substantial deviation

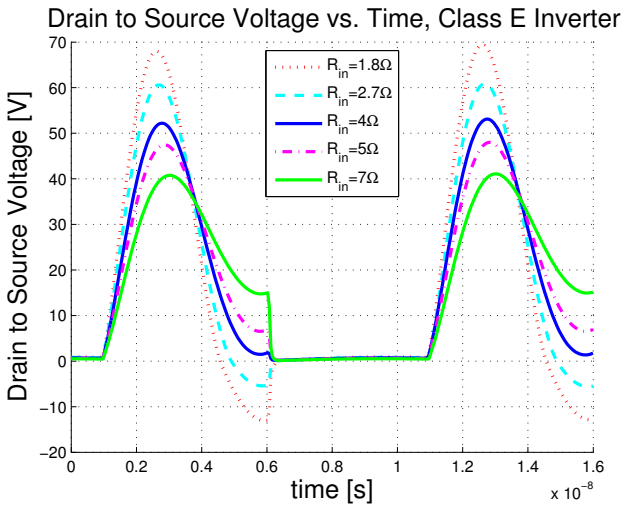


Fig. 11. Drain to source voltage for a Class E inverter for different values of resistance. Using the notation in [27] $L_1 = 538nH$, $L_2 = 24.2nH$, $C_1 = 120pF$ (non-linear), $C_2 = 163.5pF$, $1.8\Omega \leq R \leq 7\Omega$. Optimal Zero-voltage switching (ZVS) occurs at $R = 4\Omega$. When the resistor deviates from its nominal value ZVS is not achieved.

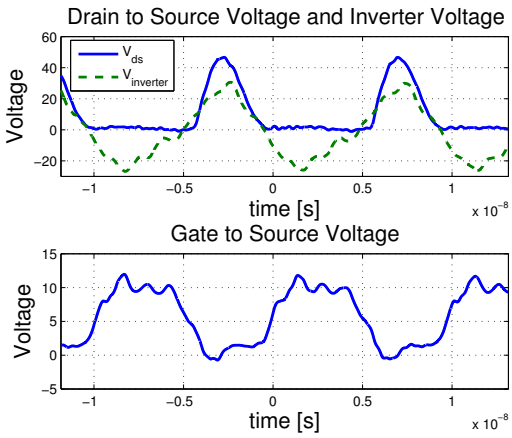


Fig. 12. Drain to source voltage, inverter output voltage, and gate to source voltage of the prototype converter

from zero-voltage switching), the permissible load resistance range is only a factor of approximately 3:1 (a range of 6Ω to 2Ω in Fig. 11). Requiring a closer approximation to zero-voltage turn on will necessitate maintaining a still narrower resistive load range.

This limitation in load range is further exacerbated in resonant dc/dc converters. As shown in Section III, the effective resistance presented to the inverter typically depends on both ac drive levels (and hence on input voltage) and on the dc output of the rectifier. These dependencies pose a challenge to the design of resonant dc/dc converters at very high frequencies.

B. Example application

The high sensitivity of radio-frequency converters such as the class E inverter to variations in load resistance is a significant limitation, and motivates the development of circuit techniques to compensate for it.

To demonstrate the use of resistance compression to benefit very high frequency dc/dc power converters, a prototype dc/dc converter operating at 100 MHz was developed. The circuit consists of a class E inverter with self-oscillating gate drive, a matching network, a resistance compression network of the type shown in Fig. 3(b), and a set of two resonant rectifiers which have a resistive characteristic at the fundamental frequency. The switching frequency for the converter is 100 MHz, the input voltage range is $11V \leq \mathrm{V_{in,dc}} \leq 16V$ and the maximum output power capability ranges from 11.4W at $\mathrm{V_{in,dc}} = 11\mathrm{V}$ to 24.5W at $\mathrm{V_{in,dc}} = 16\mathrm{V}$. The detailed schematic of the circuit implementation is shown in Fig. 15 and the components used are listed in Table IV. A photograph of the prototype converter is shown in Fig. 16.

In order to minimize the gating losses of the LDMOSFET, a self-oscillating multi-resonant gate drive was used. This gate driver is conceptually similar to the converter circuits presented in [28], resulting in a gate to source voltage with a pseudo square wave characteristic that provides fast and efficient commutation of the main semiconductor device without driving the gate-source voltage negative. The average power dissipated in the resonant driver was found to be 350mW.

Each of the two resonant rectifiers in Fig. 15 are designed to appear resistive in the sense that the fundamental ac voltage at the rectifier input is largely in phase with the drive current when the rectifier is driven from a sinusoidal current. (The compression network reactances are designed to block the voltage harmonics created by the rectifiers.) At $\mathrm{V_{dc,out}}$=12V, each rectifier is designed to present an equivalent resistance (at the fundamental) ranging from 12Ω (at an output power of 13.8W) to 27.4Ω (at an output power of 5.75W).

The compression network is designed for a nominal operating frequency of 100 MHz and a center impedance $\mathrm{Z_c} = 20\Omega$. Simulations predict a compressed resistance ranging from 21Ω down to 20Ω and back up to 22.7Ω as power ranges from minimum to maximum. Moreover, the compression network is designed to present a high impedance to dc and harmonics of the fundamental.

To enable the compression network and rectifiers to operate at a convenient impedance level, an L-section matching network is used. This network comprises shunt inductance $\mathrm{L_1}$, with the capacitive portion of the L-section network absorbed as part of the resonant capacitor $\mathrm{C_R}$.

Experimental results support the efficacy of the compression network for providing a desired narrow-range impedance to the inverter as the power level varies with input voltage. Figure 12 shows experimental waveforms for the converter running at $\mathrm{V_{in,dc}} = 11V$ and $\mathrm{V_{out,dc}} = 12V$. Shown in the figure are the voltage at the gate of the MOSFET, the drain to source voltage of the device and the voltage at the input of the compression network. It can be appreciated from the figure that zero-voltage turn-on of the LDMOSFET is achieved, indicating a proper impedance match.

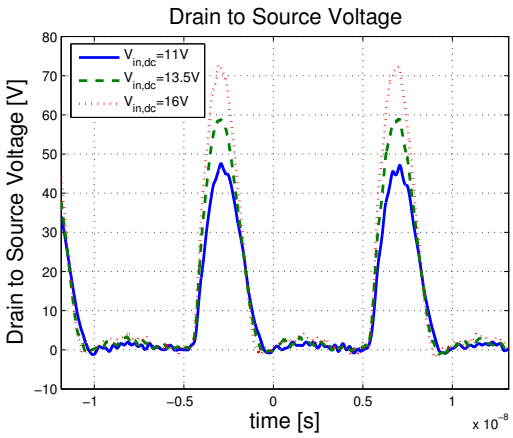


Fig. 13. Drain to source voltage for different input voltages in the range $11V \leq V_{in,dc} \leq 16V$. The inverter is seen to maintain soft switching over the full range.

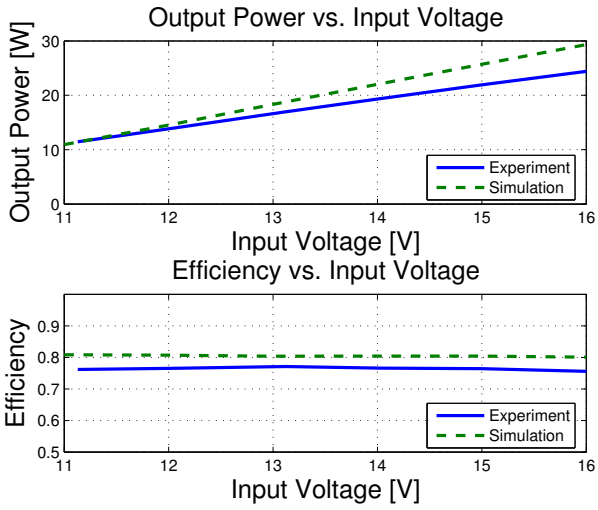


Fig. 14. Experimental and simulated output power and efficiency vs. input voltage

Figure 13 shows V_{ds} at input voltages of 11V, 13.5V, and 16V. It can be appreciated from the respective figures, the zero-voltage condition is achieved over the whole input voltage range: a situation that would not occur without the resistance compression network operating as desired.

Figure 14 shows the output power and the efficiency of the prototype converter. It can be appreciated that the output power has a characteristic proportional to the square of the input voltage, another indication that the compression network is functioning to keep the effective load resistance constant as operating conditions change.

VI. Conclusion

This document proposes a new class of matching networks that promise a significant reduction in the load sensitivity of resonant converters and RF amplifiers. These networks, which we term resistance compression networks, serve to greatly decrease the variation in effective resistance seen by a tuned RF inverter as loading conditions change. The operation, performance, and design of these networks are explored. The application of resistance compression is demonstrated in a 100 MHz dc/dc converter. Experimental results from this converter confirm the effectiveness of compression networks for reducing load sensitivity of resonant dc/dc converters. It is anticipated that the proposed approach will allow significant improvements in the performance of very high frequency power converters.

Fig. 16. Prototype dc/dc power converter.

VII. Acknowledgment

The authors would like to thank John Kassakian and Joshua Phinney, both of MIT, for the insights they provided in pursuing this work. Partial support for this work was provided by the Massachusetts Institute of Technology.

Appendix

In many applications where resistance compression is useful, a transformation in the center value of the impedance is also desirable. These functions can be combined in a higher-order compression network. This appendix describes the performance of the four-element resistance compression networks illustrated in Fig. 5.

Four element resistance compression networks provide an additional degree of design freedom that can be used to implement resistance transformation along with resistance compression. Consider the four-element compression network of Fig. 5(a), where the reactance values X and Y are the reactance of the network branches at the desired operating frequency. Straightforward analysis shows that the input impedance of this network at the specified frequency is resistive, with a value

$$R_{in} = \frac{X^2}{(X+Y)^2} \cdot \frac{2R}{1+\left(\frac{R}{X+Y}\right)^2} \tag{10}$$

Examining this equation we can identify a center impedance $Z_c = X + Y$ about which compression of the matched resistances occurs. Moreover, we can identify a transformation factor K_T, defined as:

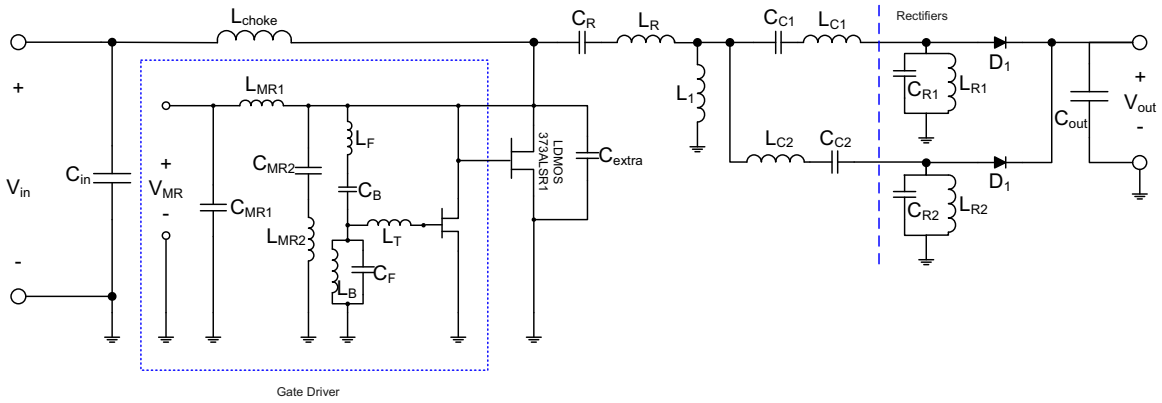


Fig. 15. A 100 MHz dc/dc power converter incorporating a resistance compression network.

TABLE IV

COMPONENTS USED IN 100 MHZ DC/DC CONVERTER OF FIG. 15.

Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value
C_{C1}	18pF +15pF	CDE Chip-Mica 100V MC08EA150J	MC08EA180J	36.22pF
C_{C2}	56pF +7pF	CDE Chip-Mica 100V MC08CA070C	MC12FA560J	66.5pF
C_{extra}	10pF × 2	CDE Chip-Mica 100V	MC08CA100D	
C_{in}	2.2μF +0.68μF +0.047μF × 12	Tantalum 35V Tantalum 35V Ceramic 50V	PCT6225CT PCT6684CT Kemet	
C_R	82pF +2pF	CDE Chip-Mica 100V MC08CA020D	MC12FA8205	
C_{R1}, C_{R2}	15pF × 2	CDE Chip-Mica 100V	MC08EA150J	C_{R1}=32.6pF C_{R2}=32pF
C_{out}	0.1μF × 19	Kemet Ceramic 50V	C0805C104M5UAC	
D_1, D_2	Schottky Power Diode	ON Semi 60V, 2.0A	MBRS260T3	
L_1	17.5nH	Coilcraft	B06T6	
L_{C1}	33nH	Coilcraft	1812SMS-33N	38.1nH
L_{C2}	68nH	Coilcraft	1812SMS-68N	69.9nH
L_{choke}	120nH × 2	Coilcraft	1812SMS-R12G	
LDMOS		Freescale 70V (max V_{ds})	MRF373ALSR1	
L_R	12.5nH + Two-turn magnet wire coil +8.9nH board parasitic	Coilcraft	A04TJ 18 AWG	Approx. 22nH
L_{R1}, L_{R2}	18.5nH	Coilcraft	A05T	L_{R1} =18.9nH L_{R2} =18.7nH

$$K_T = \frac{X^2}{(X+Y)^2} \tag{11}$$

K_T can be observed to be an additional factor by which the input impedance R_{in} is scaled (transformed) as compared to the two element matching network of Fig. 3(a). That is,

$$K_T = \left.\frac{R_{in}}{Z_c}\right|_{R=Z_c} \tag{12}$$

There are two distinct possibilities with this four element matching network. If reactances X and Y have the same sign (that is, both reactances are inductive or both are capacitive at the operating frequency) then K_T will be less than one, and there will be a downward transformation from Z_c to R_{in}. Conversely, if X and Y have opposite sign (one is inductive and the other capacitive) K_T will be greater than one, and there will be an upward impedance transformation from Z_c to R_{in}.

The four element compression network of Fig. 5(b) can similarly provide transformation along with compression. In particular the input resistance presented by this network is:

$$R_{in} = \frac{1}{2R} \cdot X^2 \cdot \left[1 + \left(\frac{R}{X \parallel Y}\right)^2\right] \tag{13}$$

The center impedance about which compression will occur is $Z_c = X \parallel Y$. The transformation ratio K_T is:

$$K_T = \frac{X^2}{(X \parallel Y)^2} \tag{14}$$

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