New Architectures for Radio-Frequency dc/dc Power Conversion

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***Abstract*— This document proposes new architectures for switched-mode dc/dc power conversion. The proposed architectures enable dramatic increases in switching frequency to be realized while preserving features critical in practice, including regulation of the output across a wide load range and high light-load efficiency. This is achieved in part by how the energy conversion and regulation functions are partitioned. The structure and control approach of the new architectures are described, along with representative implementation methods. The design and experimental evaluation of prototype systems with cells operating at 100 MHz are also described. It is anticipated that the proposed approaches will allow substantial improvements in the size of switching power converters to be achieved and, in some cases, to permit their integrated fabrication.**

***Index Terms*— RF dc/dc power converter, high frequency, integrated converter, cellular architecture, RF power amplifier, Class E inverter, self-oscillating inverter.**

I. INTRODUCTION

THE RAPID evolution of technology is generating a demand for power electronics whose capabilities greatly exceed what is presently achievable. A challenge of particular importance is the miniaturization of power electronic circuits. Miniaturization is difficult given the energy storage and loss limitations of passive components used in the conversion process. Furthermore, there is a tremendous need for new approaches that enable power circuits to be fabricated in a much more integrated fashion. Higher levels of integration can promote improved power density, and enable the use of batch fabrication techniques which are central to the cost benefits of integrated circuits and MEMS systems. Thus, design and manufacturing methods that enable power electronics to be miniaturized and/or fabricated using batch processing techniques have tremendous potential value.

Achieving miniaturization and integration of power electronic circuits will necessitate radical increases in switching frequency to reduce the required size of passive components. This paper introduces new architectures for dc/dc power conversion that enable dramatic increases in switching frequencies, potentially into the microwave/ultra-high frequency (UHF) range[1]. These new architectures promise to enable substantial miniaturization of dc/dc converters, and to permit much higher degrees of integration to be achieved. Section II provides background and highlights the principal challenges that need to be overcome to achieve these goals. Section III introduces the new conversion architectures we propose, and describes their principal operating and control characteristics. Section IV presents the design and experimental evaluation of a 100 MHz dc/dc converter "cell", and Sections V and VI demonstrate its application in two of the proposed converter architectures. Finally, Section VII concludes the paper, and points towards the emerging possibilities in this area.

[1]By architecture we mean the manner in which a power electronic system is structured and controlled. A given architecture can be realized with a range of particular converter topologies.

II. BACKGROUND

Switching power converters traditionally comprise semiconductor switching devices and controls along with passive energy storage components, including inductors and capacitors. The passive components provide intermediate energy storage in the conversion process and provide filtering to attenuate the switching ripple to acceptable levels. Inductive elements, in particular, are used to achieve near-lossless transfer of energy through the circuit and to limit the instantaneous currents generated by the switching action of the power stage. These passive energy storage elements often account for a large portion of converter size, weight, and cost, and make miniaturization difficult.

A principal means for achieving reduction in the size of power circuits is through increases in switching frequency. As is well known, the size of the energy storage elements (e.g., inductors and capacitors) required to achieve a given conversion function varies inversely with switching frequency (see, e.g., [1]). Much of the improvement in size and cost of switching power converters over time has been due to increases in switching frequency, rising from tens of kilohertz in the early 1970's into the megahertz range today. Increases in switching frequency have been achieved both through new devices and materials better suited to high-frequency operation (e.g., power MOSFETs and new ferrite magnetic materials) and through circuit and component designs that reduce losses associated with high-frequency switching (e.g., [2]–[18]).

A. Challenges of High-Frequency Power Converter Design

Despite the availability of devices capable of operating up to several gigahertz under certain conditions, power converter switching frequencies remain in the low megahertz range and below. This fact reflects some of the challenges peculiar to power electronics. Switching power converters must typically operate efficiently over a wide load range (often in excess of $100:1$) from a variable input voltage, and must regulate the output in the face of rapid and unpredictable load and input variations. However, existing circuit topologies capable of operating efficiently at high frequencies are not well matched to these requirements. These topologies use a continuous

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resonating action to achieve the zero-voltage switching that is essential to operation at high radio frequencies and beyond[2]. This approach is effective for full load conditions, where the losses associated with resonant operation are small compared to the output power. However, these resonating losses are present under all loading conditions, and are typically unacceptable in systems that must operate efficiently over a wide load range.

A second factor that has inhibited the use of higher switching frequencies in power electronics is the impact of frequency-dependent losses on magnetic component size. At high frequencies, loss limits—rather than energy storage limits—are the dominant consideration in sizing magnetics. The core loss densities of most power ferrite materials rise rapidly with frequency in the megahertz range, necessitating flux derating as frequency is increased[3]. As a result, magnetic component size does not always decrease as frequency is increased, and can even worsen [23]. Air-core magnetics designs do not suffer this limitation, but must be operated at still higher frequencies to compensate for reduced inductance resulting from the lack of permeable core material. Achieving dramatic reductions in power converter size thus requires either new passive component designs that do not suffer this loss limitation or power conversion architectures capable of operating at sufficiently high frequencies that air-core magnetics can be employed effectively.

The need to regulate the output represents a further difficulty with available power circuits capable of high frequency operation. While some degree of regulation can be achieved with such circuits (e.g., by frequency control [9]), the difficulty in realizing regulation over a wide load range is only exacerbated as switching frequency increases. Moreover, converter dynamics and control circuit implementation complexities escalate at higher operating frequencies. These factors have placed major constraints on power converter operating frequencies and, in turn, on size and performance[4]. Achieving the dramatic improvements in size, performance, and integration that are desired for future power converters thus requires new power conversion architectures that overcome these limitations.

B. Radio-Frequency Amplifiers

The proposed architectures incorporate circuit structures and principles that are employed in tuned radio-frequency power amplifiers (e.g., [15], [17], [25], [26]), but apply them in manners that overcome limitations in conventional dc/dc converter architectures. Here we review some of the characteristics of these circuits.

Switched-mode RF amplifiers (inverters) utilize resonant circuit operation to achieve zero-voltage switching of the semiconductor devices. To minimize driving losses and achieve high power gains, multistage amplifier designs are often used. In a multi-stage design, amplifiers are chained together such that each amplifier efficiently drives the gate(s) of a higher-power amplifier; the last amplifier in such a chain drives the output. Using these techniques, tuned inverters can be designed to operate with good efficiency into the gigahertz range, and in some cases can be completely integrated (e.g., [25]). Similar (including dual) circuits can be used for efficient high-frequency rectification (e.g., [8], [10], [12]).

Both inverter and rectifier circuits of this type exhibit important limitations. First, they only operate with good efficiency over a relatively narrow load range, both because of the continuous resonating losses described above and because the load greatly affects the operating waveforms. Second, the controllability of these designs (e.g., to compensate for load or input variations) is very limited, and becomes more challenging at higher frequencies and in multi-stage amplifiers. Thus, the practical use of these circuits in dc/dc power conversion (e.g., [2], [6], [9]–[11], [14]) has been limited to relatively low frequencies (<30 MHz), as previously described.

III. New Converter Architectures

As described above, conventional power converter designs are subject to a number of constraints that limit their practical operating frequency, and in turn limit the degree of miniaturization and integration that can be achieved. Here we propose new power conversion architectures that overcome these constraints. These architectures take advantage of the high-frequency performance of tuned RF amplifier circuits while circumventing their limitations through the manner in which the energy conversion and regulation functions are partitioned. Two primary architectures are introduced: a *Vernier-regulated* architecture a *time-modulation-regulated* architecture. We also consider some of the variants of these approaches.

A. Vernier-Regulated Architecture

The Vernier-regulated cellular architecture (VRCA) is a type of cellular power converter. As shown in Fig. 1, this architecture comprises a number of unregulated converter cells along with a regulating converter cell, each of which supplies the output. The unregulated cells each comprise an RF inverter, a transformation stage, and a rectifier, along with filtering and ancillary circuitry. The unregulated cells are structured such that they may be activated or deactivated (turned on or off). The regulating converter cell—or *Vernier* cell[5]—may be a switched-mode converter, a linear regulator, or some combination thereof, and need only be rated for a small fraction of the total system power.

Operation of the proposed architecture is as follows: The regulating cell is controlled to regulate the output at the desired level. As the load varies, unregulated cells are activated or deactivated to keep the regulating converter within a specified load range while ensuring that the active unregulated cells

[2]Zero-Voltage Switching (ZVS), wherein devices are switched with little or no voltage across them, is necessary to achieve the ultra-high operating frequencies considered here [18]. Likewise, at these frequencies device gating loss becomes a major consideration, and some form of resonant drive is usually required (e.g., [19]–[22]).

[3]Core loss considerations are of particular importance in magnetic elements with significant ac components of flux, such as transformers and resonant inductors.

[4]For these reasons, attempts at using greatly increased switching frequencies in conventional architectures (e.g., [24]) have not met the requirements of efficiency and ability to regulate the output.

[5]We term the regulating cell a *Vernier cell* by analogy to the Vernier scale on a caliper (named after its designer, Pierre Vernier). The Vernier scale provides incremental measurements between the discrete marks on a caliper's main scale; likewise, the Vernier cell provides the incremental power between the discrete power levels that can be sourced via the unregulated cells.

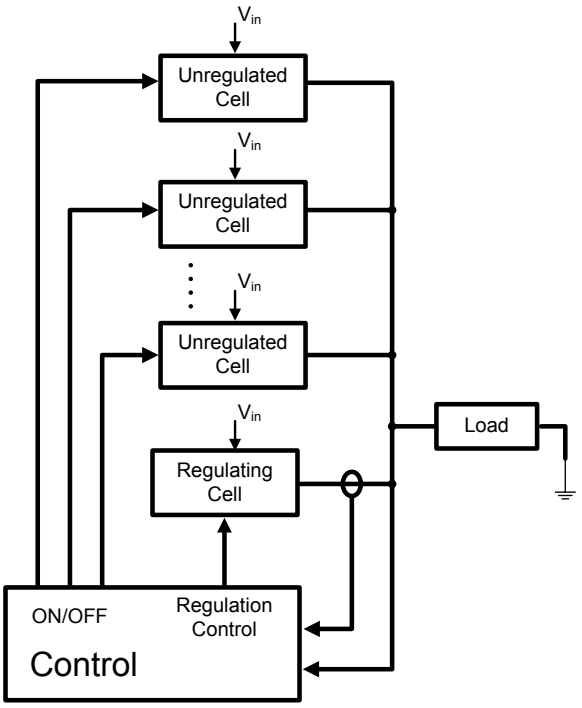

Fig. 1. A block diagram illustrating the Vernier-regulated converter architecture.

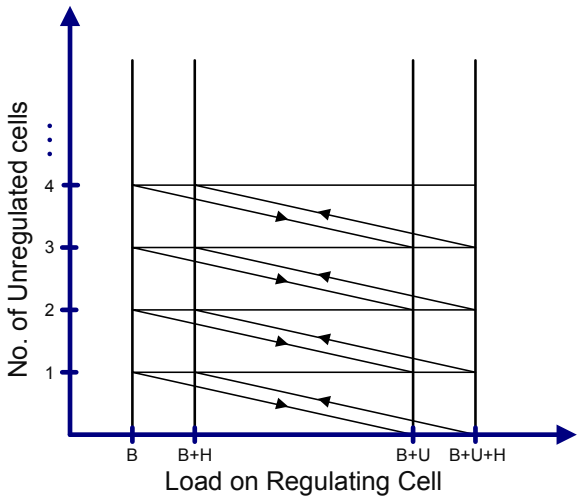

Fig. 2. An activation scheme for unregulated cells. Unregulated cells are activated or deactivated based on the load on the regulating cell. U is the incremental loading change when an unregulated cell is activated or deactivated. B is the minimum load on the regulating cell, below which an unregulated cell is deactivated. H is a hysteresis value to prevent chattering at boundaries.

run at or near their ideal operating points. One activation scheme that meets these requirements is illustrated in Fig. 2. In steady state, the unregulated cells deliver a portion of the total power (in discrete increments), while the regulating cell provides whatever remaining power is needed to regulate the load voltage.

This architecture has a number of advantages. First, the unregulated cells only run under a narrow range of loading conditions. Second, the only control required for the unregulated cells is a simple on/off command. These characteristics facilitate the use of very high frequency multi-stage amplifier designs for the unregulated cells. Furthermore, because inactive cells do not incur loss, and unregulated cells are only activated as needed to support the load, efficient light-load operation can be achieved. Finally, the proposed architecture inherits a number of advantages of more conventional cellular converter architectures, including the dispersal of heat generation in the circuitry and the potential for fault tolerance [27].

In any power converter system that processes power through multiple channels, it is important that each channel stably carry the appropriate amount of power in order to avoid circulating losses and the possible destructive overload of individual channels (see [27]–[29] and references therein). In the Vernier-regulated architecture, it is particularly important to ensure that the unregulated cells share power in the desired manner. Furthermore, the unregulated cells should not interfere with the output control function of the regulating cell.

One method of achieving these control goals is to appropriately shape the output impedances of the individual cells. For a given operating point, the cells are modelled as Thévenin equivalent voltages and impedances that drive the output filter and load [27]. For the regulating cell, the Thévenin source is equal to the reference voltage, while the Thévenin (output) impedance depends on both the power stage and control loop design. For the unregulated cells, the Thévenin model parameters depend on the input voltage, the cell power stage design, and the cell switching frequency. To achieve the desired output control, the regulating cell is designed to have low output impedance at low frequencies (down to dc), while the unregulated cells are designed to have relatively high output impedances (and thus act as current sources). High dc output impedance is achievable with appropriate rectifier design (see, e.g., [8]), and can also be used to ensure that the unregulated cells share power (and current) correctly via their "droop" characteristics [27]–[32]. Thus, through appropriate design, the control requirements of the proposed Vernier-regulated architecture can be met.

B. Time-Modulation-Regulated Architecture

The previous architecture uses a Vernier cell operating at variable load to provide the difference between the quantized power levels delivered by the unregulated cells and that needed to regulate the output. By contrast, the time-modulation-regulated architecture uses *only* unregulated cells to supply the output, as illustrated in Fig. 3. As with the previous architecture, the unregulated cells are engineered to have high output impedance (such that they may be treated as current or power sources) and to admit on/off control. To provide the proper average power to regulate the output, the number of unregulated cells that are activated is modulated over time, and an energy buffer (e.g., a capacitor, ultracapacitor, battery, etc.) at the converter output is used to filter the resulting power pulsations.

A variety of modulation strategies are compatible with this approach. Perhaps the simplest is hysteretic control of the output voltage. If the output voltage falls below a specified minimum threshold, the number of activated cells is increased (e.g., in a clocked or staggered fashion) until the output voltage

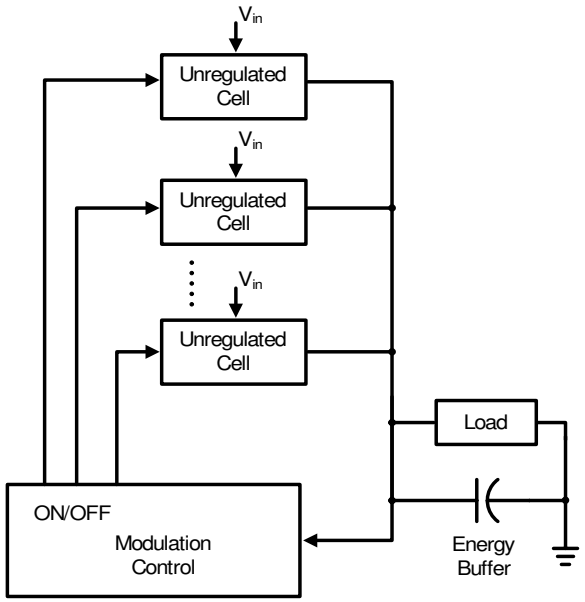

Fig. 3. A block diagram illustrating the time-modulation-regulated converter architecture.

returns above the minimum threshold (or until all cells are activated). If the output voltage rises above a specified maximum threshold, the number of activated cells is decreased until the output voltage returns below the maximum threshold (or until all cells are deactivated). In the case where a single cell is used, this corresponds to *bang-bang* control of the output. With multiple cells this approach might be considered a form of multi-level pulse-width modulation of power (or current). Clearly, there are many other similar control strategies that will likewise provide a desired average output voltage.

The time-modulation-regulated architecture exhibits a number of the advantages of the previous architecture. The unregulated cells only need to operate under on/off control over a narrow power range. This facilitates the use of UHF power converter cells having small size and high efficiency, and enables high light-load efficiency to be achieved. However, the considerations sizing input and output filters for this architecture are different than that of the previous one. In the Vernier architecture, the size of the output filter (e.g. output capacitor) needed depends primarily on the bandwidth of the regulating (Vernier) cell, and only secondarily on the startup speed of the unregulated cells if at all. By contrast, in the time-modulation-regulated architecture, the energy storage requirement and size of the output filter capacitor depends on the rate at which the unregulated cells can be modulated on and off—typically orders of magnitude slower than the switching frequency of the cells themselves. Consequently, the ultra-high frequency operation of the cells enables dramatic reductions in size of power stage components (e.g., inductors, capacitors, and transformers), but it does not benefit the input and output filter components to the same extent. Nevertheless, in many applications, substantial energy storage is provided at one or both converter ports (e.g. for holdup), so this is often acceptable[6]. It may be concluded that the time-modulation regulated architecture enables high efficiency across load and tremendous reductions in power stage component size, but does not provide the same degree of improvement for input and output filters.

C. Related Architectures

The architectures proposed above enable dramatic increases in switching frequency as compared to conventional designs, with consequent benefits. It should be appreciated that there are many variants that offer similar advantages. For example, if one is willing to accept regulation of the output to discrete levels, one can utilize a set of unregulated cells without the need for a Vernier cell or time-domain modulation to interpolate between levels. The use of unregulated cells having different power ratings (e.g., a geometric 2^N progression) would facilitate this approach, though it would perforce increase the design effort. (Note that the use of non-uniform cell sizing can benefit the above architectures as well.) The underlying characteristic of all such approaches is that they partition the energy conversion and regulation functions in manners that are compatible with the effective use of ultra-high frequency circuit designs and techniques. It is hoped that the recognition of this general strategy will lead to the emergence of additional circuit architectures having similar advantages.

IV. 100 MHz Unregulated Cell Design

The proposed architectures admit a wide range of unregulated cell designs. The principle requirements are that the cells should operate efficiently for at least a narrow specified operating range, have high output impedances, and be amenable to on/off control. These requirements are fulfilled by many RF circuit topologies, and permit cell designs having switching frequencies far higher than those reached in conventional dc/dc converters. To illustrate this, we present the design and experimental evaluation of a converter cell operating at 100 MHz that achieves $>75\%$ efficiency over its operating range.

The unregulated cell consists of a high frequency inverter, an impedance matching network, and a resonant rectifier. The inverter is driven by a self-oscillating gate driver at a free running frequency of 100 MHz.

A. Class E Resonant Inverter

The front end of the unregulated cell consists of a Class E resonant inverter (Fig. 4). In conventional RF design, the loaded Q (Q_L) of the converter is usually chosen to be large, resulting in waveforms with high spectral purity. For power conversion, however, the requirements on Q_L are different, since the goal is to maximize power transfer with minimum loss. A low value of Q_L results in less energy resonated in the tank, which further implies reduced conduction loss in the parasitic elements of the inverter[7].

[6]Many linear regulators require substantial capacitance at their input and output ports; imposing the same requirement on a more efficient switching converter design might be perfectly acceptable.

[7]Equations for the design of Class E RF inverters with low Q can be found in [33].

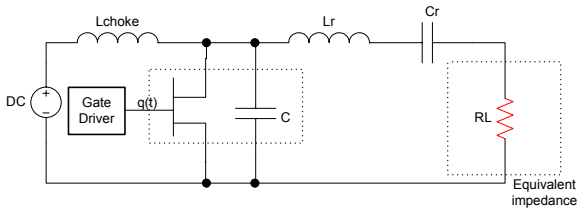

Fig. 4. Class E inverter circuit.

Under optimal ZVS conditions, inverter output power is proportional to the capacitance in parallel with the switch. For the intended range of output power in the practical cell implementation, the required capacitance was provided entirely by the parasitic drain-source capacitance associated with the switch.

The device selected for the main switching element is a Laterally Diffused MOSFET (LDMOSFET). This semiconductor device offers the required characteristics needed to operate at high frequencies: it presents an acceptable drain to source capacitance and a low gate capacitance that allows for minimum gating loss.

B. Self-Oscillating Gate Driver

In power converters, gating losses grow with switching frequency. In traditional topologies, these losses often become the limiting factor for high frequency operation. To mitigate these losses and recover some of the energy required to operate the semiconductor switch, a resonant gate driver may be used. A resonant gate drive often implies sinusoidal gate signals, a feature commonly found in cascaded power amplifiers.

A low-cost, efficient means of selectively driving the inverter is of great importance to the proposed architecture. To achieve this goal while maintaining the cell's simplicity, a self-oscillating gate driver making use of the drain-source voltage $v_{ds}(t)$ of the LDMOSFET was implemented. By properly shifting the fundamental component of the drain voltage, this resonant network generates a sinusoidal gating signal capable of sustaining oscillation at the desired frequency.

Figure 5 shows the inverter's drain to source voltage $v_{ds}(t)$ as well as its fundamental component. These waveforms are referred in phase to the required gate voltage, $v_{gs}(t)$. The phase difference between the fundamental component of $v_{ds}(t)$ and the required gate signal was found to be 163° (as depicted in Fig. 5).

1) Phase shift/feedback network: A linear circuit structure, including the internal parasitics of the LDMOS gate, provides the appropriate phase shift to attain sustained oscillations. Figure 6 shows a simplified circuit which feeds back the voltage $v_{ds}(t)$ and provides the required phase shift. The fundamental of $v_{ds}(t)$ is also attenuated to a value that ensures proper gate drive and is below the gate breakdown voltage ($v_{gs,max} = 20$ V).

Figure 7 shows the frequency response of the drain to gate transfer function $\left(\frac{V_{gs}}{V_{ds}}(\omega)\right)$; at 100 MHz the phase is the required 163°. By properly adjusting the damping resistor $\mathrm{R_{fb}}$ it is possible to set the magnitude and the precise frequency of oscillation.

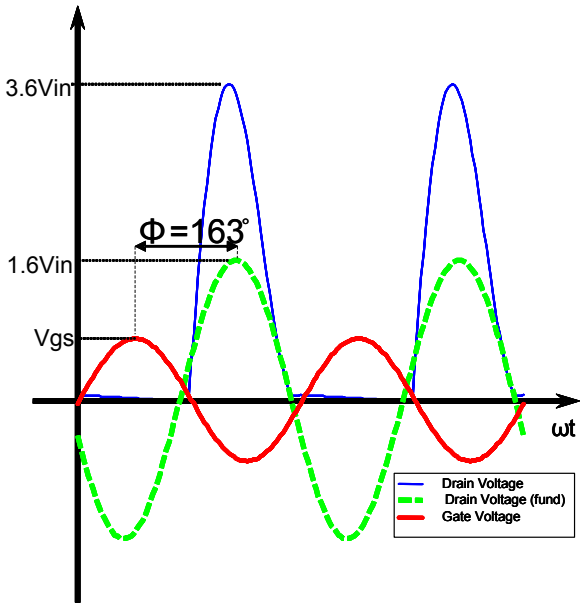

Fig. 5. Idealized $v_{ds}(t)$ and its fundamental (dotted line). The gate signal is also shown. The phase angle between the fundamental component of the drain voltage and the idealized gate signal is 163°.

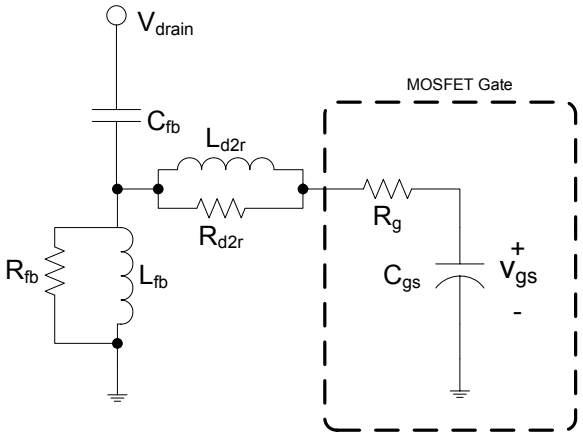

Fig. 6. Simplified feedback structure.

The function of $\mathrm{L_{d2r}}$ and $\mathrm{R_{d2r}}$ is to damp the second resonance apparent in the transfer function of Fig. 7; higher frequency oscillations (≈2 GHz) might otherwise result.

The input impedance of the self-oscillating structure is dominated by the value of the feedback capacitor $\mathrm{C_{fb}}$. This capacitor is selected such that the impedance looking into the structure is much higher than the impedance looking into the resonant tank of the Class E inverter, ensuring that the frequency characteristics of the tank circuit are not substantially altered.

2) On/off and startup circuit: The proposed architecture requires a simple control signal which starts and stops cell operation. This can be achieved with a slight modification to the phase shift/feedback network, as illustrated in Fig. 8.

When transistor $\mathrm{Q_{on/off}}$ is on, the gate is pulled low and the inverter is shut off. When $\mathrm{Q_{on/off}}$ turns off, $\mathrm{C_{dc}}$ charges through $\mathrm{R_{fb}}$. With a properly chosen logic supply voltage

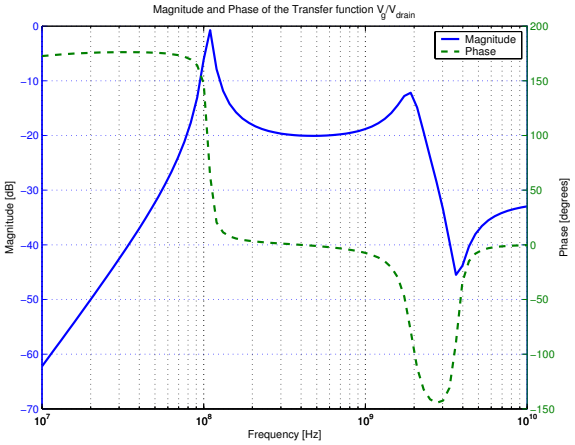

Fig. 7. Magnitude and Phase of the transfer function $\frac{V_{gs}}{V_{ds}}(\omega)$.

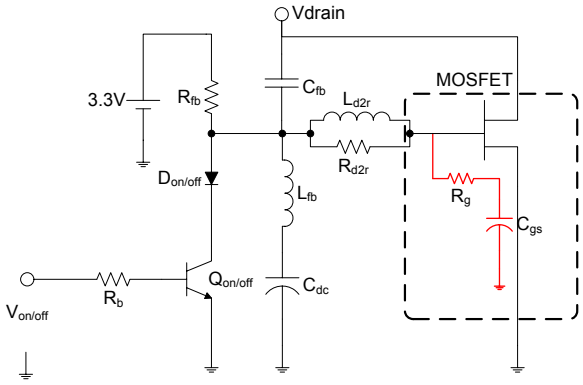

Fig. 8. Self-oscillating resonant gate driver circuit.

(3.3 V in Fig. 8), the gate is driven above threshold, turning on the MOSFET and starting oscillation through the phase shift/feedback network. A digital signal can thus be used to activate or inhibit converter operation.

During operation, C_{dc} remains biased close to the MOSFET threshold voltage, helping to keep the duty ratio near 50%. C_{dc} is selected for minimal impact on the transfer function $\frac{V_{gs}}{V_{ds}}(\omega)$. When $Q_{on/off}$ is off, the junction capacitance of $D_{on/off}$ appears in series with the output capacitance of $Q_{on/off}$; this minimizes loading on the phase shift/feedback network.

The RC circuit formed by R_{fb} and C_{dc} introduces a delay between the command signal and inverter startup; it is this delay which limits the speed at which the cell can be turned on.

C. Matching Network and Rectifier

The rectifier is implemented as a balanced pair of single-diode rectifiers. The rectifier network is structured such that it appears resistive in a describing function sense. This rectifier is connected to the inverter tank by a simple L-section matching network [34].

Figure 9 shows the implemented cell design, with component values and part numbers enumerated in Table I. Important circuit board parasitics are also described.

TABLE I
COMPONENT VALUES IN THE UNREGULATED CELL.

Circuit element	Nominal Value	Part number
L_{choke}	538 nH	Coilcraft 132-20SMJ
C_{fb}	2 pF	CDE MC08CA020C
C_{pfb}	1.15 pF	Measured circuit board parasitic
L_{fb}	27 nH	Coilcraft 1812SMS-27NG
R_{fb}	2.2 kΩ	Standard SMD
C_{dc}	2.2 nF	C0G Ceramic, 50 V
R_b	100 kΩ	Standard SMD
L_{d2r}	2.5 nH	Coilcraft A01TJ
R_{d2r}	15 Ω	Standard SMD
C_{pds}	5.9 pF	Measured circuit board parasitic
L_r	68 nH	Coilcraft 1812SMS-SMS-68N
C_r	57 pF (47 pF+10 pF)	CDE MC12FA470J CDE MC08CA100D
C_m	47 pF	CDE MC12FA470J
C_{pm}	2.4 pF	Measured circuit board parasitic
L_m	12.5 nH	Coilcraft A04TJ
C_{cn}	100 pF	CDE MC12FA101J
L_{cn}	22 nH	Coilcraft 1812SMS-22NG
L_{sh1}	12.5 nH	Coilcraft A04TJ
L_{sh2}	12.5 nH	Coilcraft A04TJ
C_{in}	4 × 47 nF	X7R Ceramic, 50 V
C_{out}	9 × 47 nF	X7R Ceramic, 50 V
$C_{3.3}$	2 × 47 nF	X7R Ceramic, 50 V
LDMOSFET		PD57018S
D_1, D_2		MBRS1540T3
$D_{on/off}$		BAS70
$Q_{on/off}$		BC847

D. Experimental Results

Cell efficiency and output power were measured over the supply voltage range 11 to 16 V with a constant-voltage load comprising fifteen 5.1 V, 1 W Zener diodes in parallel with two 15 μF Tantalum capacitors. Output power ranged from approximately 2.5 to 6 W, with an average efficiency greater than 77.5%. Figure 10 illustrates measurements from a typical cell. A photograph of one cell is shown in Fig. 11.

Figure 12 shows measured drain-source voltage under nominal conditions; turn-on and turn-off transients are depicted in Fig. 13 (the command occurs at $t = 0$ in both cases). The drain-source voltage was measured through a resistive attenuator in order to minimize loading on the drain node; as a result, the measured magnitude is approximately 38 times smaller than the voltage present at the drain.

The incremental output impedance of the unregulated cell design at V_{out} = 5 V ranged from 30 Ω (V_{in} = 11 V) to 3 Ω (V_{in} = 16 V).

The unregulated cell switching frequency, 100 MHz, is significantly higher than those found in conventional dc/dc converter designs, while maintaining an acceptable efficiency level. Nevertheless, the switching and gating losses in this design were very low, and it is anticipated that substantially higher operating frequencies could be achieved with the same switching device and circuit topology. Furthermore, there are

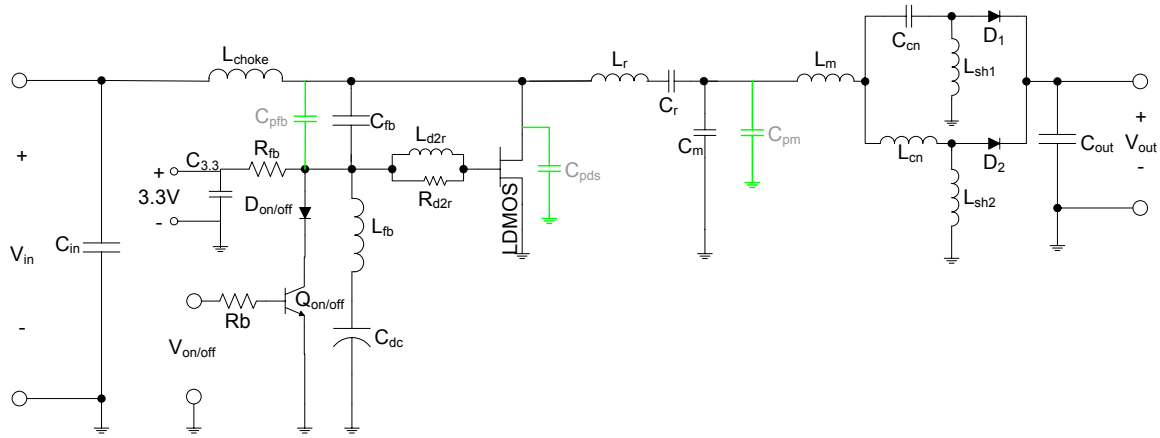

Fig. 9. Unregulated 100 MHz switching dc/dc power converter cell. Component values and important parasitics are enumerated in Table I.

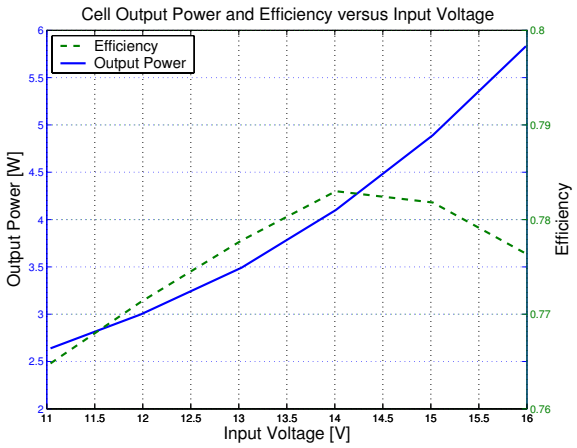

Fig. 10. Cell performance as a function of supply voltage into a 5 V load.

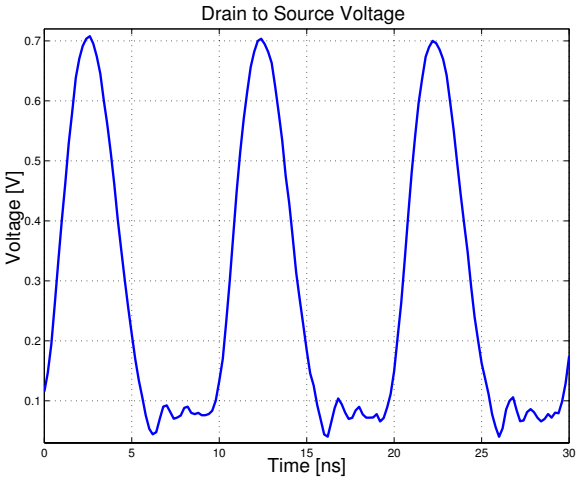

Fig. 12. Attenuated drain-source voltage under nominal conditions.

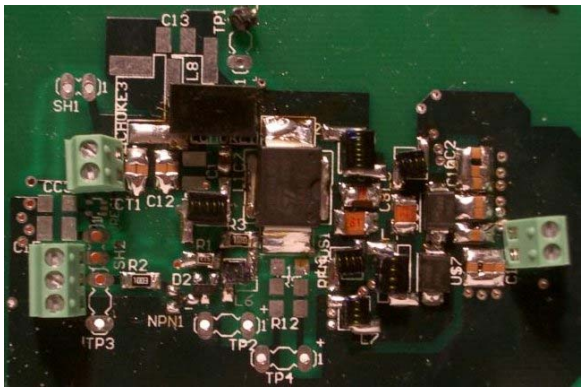

Fig. 11. A photograph of the unregulated cell circuit board.

many topological modifications that could improve power and performance levels (see e.g. [35]).

V. A Vernier-Regulated System

A. Converter Implementation

To demonstrate the fundamental operation of a Vernier-regulated converter (section III-A), we designed and constructed a prototype system comprising eight unregulated cells of the type in section IV, a Vernier cell, and a clocked controller of the type pictured in Fig. 2.

In this implementation an LM7805 was used for the Vernier cell. Chief among the reasons for this decision are its suitability to the task (as discussed in section III-A) and its simplicity. Another benefit of a linear regulator is that it maintains constant (though low) efficiency down to almost zero load. Moreover, the use of an otherwise extremely inefficient regulator in this system demonstrates the efficiency potential of the Vernier-regulated architecture despite regulating cell loss.

The controller, pictured in simplified form in Fig. 14, consists of a current sensor, two comparators, and two four-bit bi-directional shift registers. When the Vernier cell output current exceeds a predefined upper threshold, a command is sent to the shift registers which activates one additional unregulated cell. Likewise, when the lower threshold is crossed, the resulting command causes one unregulated cell to be turned off. Note that the shift register outputs are inverted to produced the appropriate active-low control signals to the unregulated cells.

To prevent oscillation, it is necessary that the difference between the upper and lower switching thresholds be larger

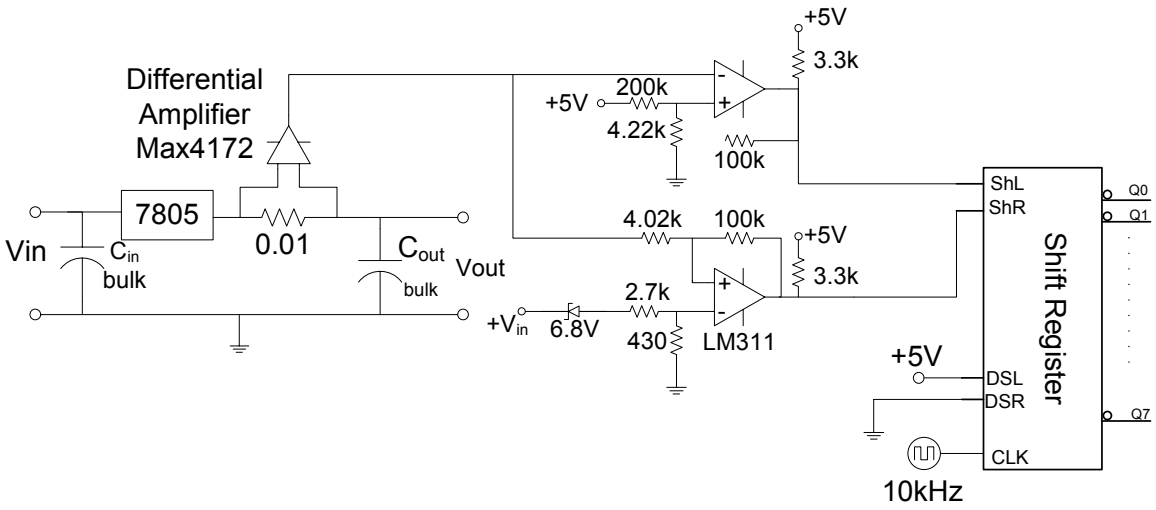

Fig. 14. Simplified schematic of the VRCA converter controller.

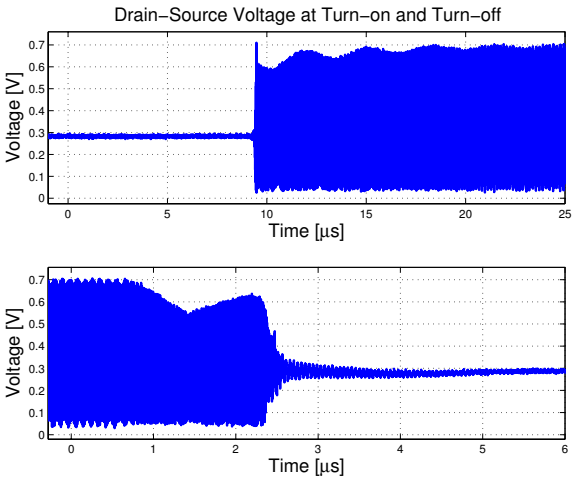

Fig. 13. Attenuated drain-source voltage during turn-on and turn-off transients. In both cases, the command occurs at $t = 0$.

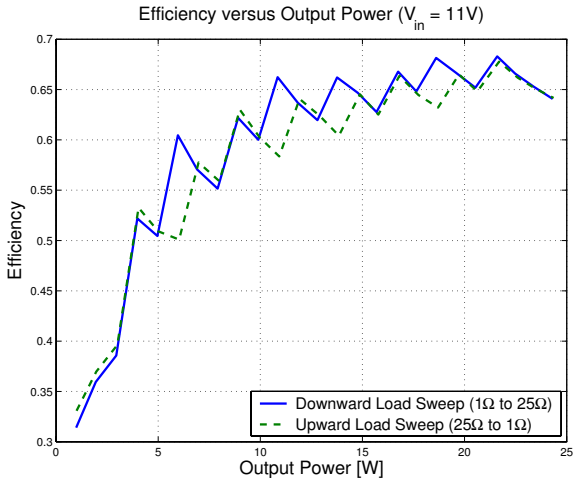

Fig. 15. Efficiency versus output power for V_{in} = 11 V. In this experiment, the load was swept from 25 Ω to 1 Ω and then back to 25 Ω, demonstrating the hysteretic characteristic of the controller.

than the maximum unregulated cell output current[8]. On the other hand, too large a hysteresis band underutilizes the unregulated cells, costing converter efficiency. As is clear from Fig. 10, unregulated cell output current is a rather strong function of input voltage. Thus, were a static upper hysteresis threshold chosen (necessarily accommodating the output current at V_{in} = 16 V), substantial underutilization of the unregulated cells would occur at lower supply voltages. To mitigate the consequent losses, the upper hysteresis threshold is instead made a function of V_{in} via a Zener diode and a resistive attenuator.

B. Experimental Results

The VRCA converter performed as expected over the full supply and load ranges, achieving over 68% peak efficiency.

[8]If this were not the case, upon exceeding the upper threshold and giving an activation command the Vernier cell output current would immediately fall below the lower threshold, causing a subsequent deactivation command and restarting the limit cycle.

Figures 15 and 16 show measured efficiency versus load at V_{in} = 11 V and V_{in} = 16 V, respectively. When an unregulated cell is switched on, power processing shifts from the low-efficiency regulating cell to the high-efficiency unregulated cell. This causes a sudden jump in converter efficiency, resulting in the sawtooth pattern apparent in both figures.

The hysteretic nature of the control strategy employed in this converter gives rise to the possibility of two distinct operating configurations for the same load condition. In the experiment of Fig. 15, the load was swept from nearly zero to maximum and then back. During the upward sweep, cell activation lagged the increasing load, resulting in the utilization of only the minimum number of cells necessary to power the load. On the downward sweep, cell *deactivation* lagged the changing load; as a result, during some portions of the downward sweep more power was processed by the high-efficiency unregulated cells than during the upward sweep.

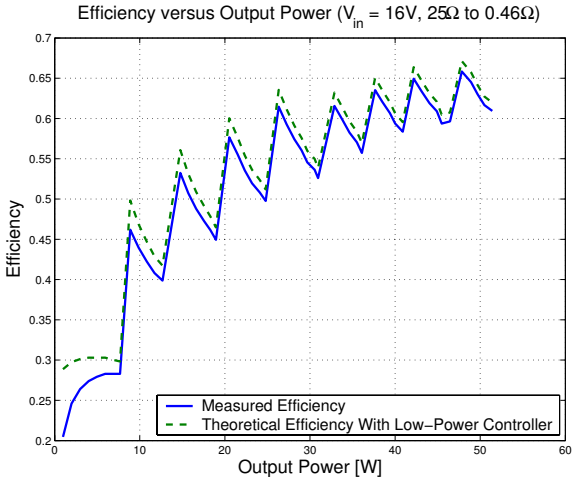

Fig. 16. Efficiency versus output power for V_{in} = 16 V, 25 Ω ≥ R_{load} ≥ 0.46 Ω. The theoretical efficiency expected under the same conditions when utilizing a low-power control circuit in place of the tested implementation is also shown.

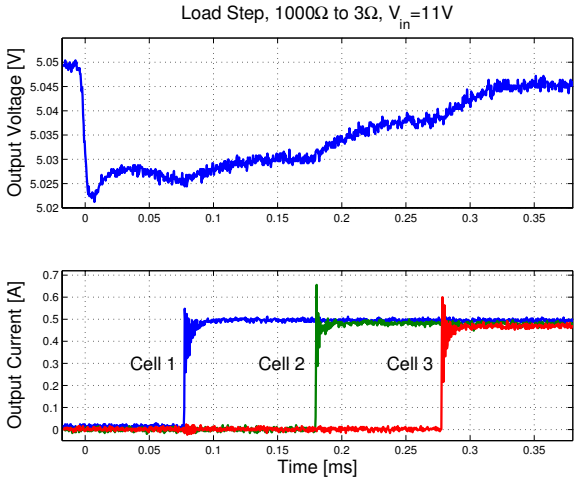

Fig. 17. Dynamic performance of the VRCA converter with V_{in} = 11 V under a load step from 1000 Ω to 3 Ω.

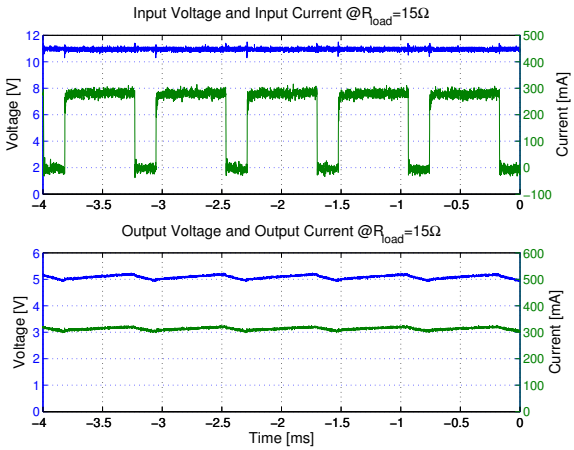

Fig. 18. Time domain waveforms under steady-state conditions (V_{in} = 11 V, C_{out} = 320 μF, R_{load} = 15 Ω).

Conversion efficiency suffers at light load because of the power drawn by the controller. In this prototype converter, the control circuitry draws 80 mA of quiescent current from the supply, resulting in substantial loss, especially under light load conditions. Figure 16 shows the theoretical efficiency impact of an implementation utilizing a low-power controller. Such a controller could be readily implemented through a variety of means.

Static line regulation was measured at 25 W across the supply range of the converter; over this range the output voltage varied by 75 mV, or less than 1.5%. Static load regulation was better than 0.8% at V_{in} = 11 V and 2.4% at V_{in} = 16 V. Measured output voltage ripple was less than 200 mV at V_{in} = 11 V, R_{load} = 1 Ω and less than 300 mV at V_{in} = 16 V, R_{load} = 0.46 Ω.

Dynamic load regulation is illustrated in Fig. 17. At V_{in} = 11 V, the load was stepped from 1000 Ω to 3 Ω, resulting in the activation of the first three unregulated cells. The delay between cell activations is determined by the controller clock frequency, 10 kHz.

In order to better match the power throughput of the unregulated cells, three of the eight cells were minimally trimmed to compensate for component variation. At maximum load with V_{in} = 16 V, individual cell output currents were matched to within ±6.5% of average. This is certainly sufficient for practical purposes, and it is expected that with tighter component tolerances or more extensive trimming much better load sharing is possible.

VI. A Time-Modulation-Regulated System

This section provides experimental verification of the architecture described in section III-B. In the prototype developed here, a single 100 MHz dc/dc cell is modulated, through its on/off control input, with a hysteretic controller which keeps the output voltage within predefined boundaries. Thus, the cell operates at an output voltage at which its efficiency is maximized. For our particular experimental implementation the hysteresis is implemented using a simple voltage comparator (LM311), and limits the voltage swing to be between 4.9 and 5.1 V. The unregulated cell is provided with an (electrolytic) output capacitance of 320 μF.

Figure 18 shows experimental measurements of the time modulated architecture system operating at an input voltage of 11 V with a 15 Ω resistive load. The figure also shows the input current of the cell, which pulsates with a frequency depending on the input voltage, the output capacitance, and output load.

Figure 19 shows the transient response of the time-domain architecture when a step change in the output load is applied. In particular, the figure shows the step change under worst-case conditions (20 Ω to 5 Ω, V_{in} = 16 V). Under such a step change, the output voltage remains within the predefined limits.

The performance of the architecture is shown in Fig. 20; the output power and efficiency are plotted as a function of the input voltage and as function of the load connected. Figure 20 shows that the overall efficiency of this architecture

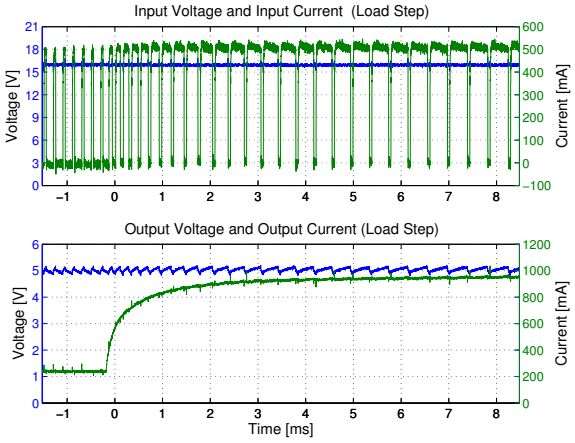

Fig. 19. Transient behavior of the time modulation scheme under a step change in output load (20 Ω to 5 Ω, V_{in} = 16 V).

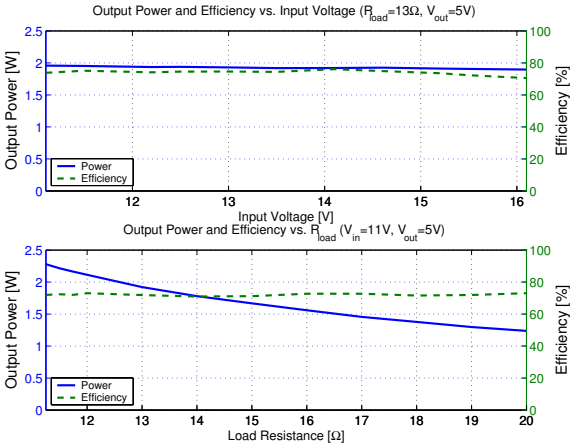

Fig. 20. (Top) Output power and efficiency vs. V_{in}. (Bottom) Output power and efficiency vs. R_{load}.

is high over the entire input voltage range. As mentioned in section IV-B.2, the converter requires a small amount of time to reach nominal operation at startup; if the time during which the converter is starting occupies an appreciable portion of the switching cycle, a small amount of loss results. Nevertheless, under rated conditions the efficiency remains quite high.

As can be seen from the prototype system and results, the high cell switching frequency allows reduction in the power stage component sizes. However the frequency of the input and output waveforms depends on the time modulation of the cell, and have much lower frequency content. Nevertheless, it is anticipated that the use of higher operating frequencies permitted by this architecture (e.g. to $>$1 GHz), the use of more cells, and design and control of cells for more rapid startup and shutdown will together enable substantial improvements in the input and output ripple performance of this architecture.

VII. Conclusion

This document proposes new architectures for switched-mode dc/dc power conversion. The proposed architectures promise to break the frequency barrier that has until now constrained the design of switched-mode power converters, while preserving features critical in practice, including regulation of the output across a wide load range and high light-load efficiency. This is achieved in part by how the energy conversion and regulation functions are partitioned in these architectures. The structure and control approach of the new architectures are described, along with representative implementation methods. The design and experimental performance of prototype systems with cells operating at 100 MHz are also described. It is anticipated that the proposed approaches will allow significant improvements in the size of switching power converters to be achieved, and, in some cases, to permit their integrated fabrication.

An underlying characteristic of the design approaches presented in this paper is that they partition the energy conversion and regulation functions in manners that are compatible with the effective use of ultra-high frequency circuit designs and techniques. It is hoped that the recognition of this general strategy will lead to the emergence of additional circuit architectures having similar advantages.

Acknowledgments

The authors would like to thank John Kassakian, Joshua Phinney, and Olivia Leitermann, all of MIT, for the insights they provided in pursuing this work.

Support for this work was provided by the member companies of the MIT/Industry Consortium on Advanced Automotive Electrical/Electronic Components and Systems, and by the Massachusetts Institute of Technology.

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