DISTRIBUTED INTERLEAVING OF POWER CONVERTERS

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Abstract. This paper introduces a distributed approach to interleaving paralleled power converter cells. Unlike conventional methods, the distributed approach requires no centralized control, automatically accommodates varying numbers of converter cells, and is highly tolerant of subsystem failures. A general methodology for achieving distributed interleaving is proposed, along with a specific implementation approach. The design and experimental verification of a 50 kHz prototype system is also presented.

Keywords. Interleaving, Ripple Cancellation, Cellular Architecture, Distributed Conversion.

INTRODUCTION

One approach to constructing a large power converter system is the use of a *cellular architecture*, in which many quasi-autonomous converters, called cells, are paralleled to create a single large converter system [1,2]. One of the primary benefits of this approach is the large degree of input and output ripple cancellation among cells which can be achieved. Consider operation of an N-cell parallel converter system. If all of the cells are clocked synchronously, then the system behaves exactly as a single large converter. However, if the cells are clocked independently (and hence operate at slightly different frequencies), it can be shown that rms input and output current ripples will be reduced by a factor of $N^{\frac{1}{2}}$ due to the passive (*stochastic*) ripple cancellation which occurs among cells. Active ripple cancellation methods can yield even higher performance benefits. The active method of *interleaving*, in which the cells are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period, is well known. (See [3] for a review.) The benefits of this technique are due to harmonic cancellation among the cells, and include low ripple amplitude and high ripple frequency in the aggregated output. For a broad class of topologies, interleaved operation of N cells yields an N-fold increase in fundamental current ripple frequency, and a reduction in peak ripple magnitude by a factor of N or more compared to synchronous operation [3-5].

To be effective in a cellular converter architecture, however, an interleaving scheme must be able to accommodate a varying number of cells and maintain operation after some cells have failed. This paper describes a new approach to interleaving parallel (or series) connected power converters. This new approach avoids some of the drawbacks of conventional methods, and is well suited for use in a cellular architecture. A means for implementing the new approach is described, and some of the major design issues are addressed. Experimental results from a 3-cell, 50 kHz prototype converter system implementing the approach are also presented.

INTERLEAVING

Interleaving N parallel (or series) connected converter cells requires that the cells be operated at the same switching frequency but phase displaced with respect to one another by $2\pi/N$ radians. This is conventionally achieved by using a centralized control circuit to supply properly phased clock or synchronization pulses to the individual cells. Typical implementations include the use of a shift register or a counter and decoder to generate the shifted clock pulses [4].

The conventional approach is effective and simple for systems with a fixed number of cells. However, it becomes less practical if there is a varying number of cells in the system, especially if interleaving is to be maintained after failure of one or more cells, as is sometimes desired [2]. The difficulty lies in the circuit and interconnection complexity required to generate the proper number of pulses and direct them to the appropriate cells. Furthermore, any failure of the centralized control circuit will cause failure of the whole system, which is undesirable if high reliability is to be achieved. These limitations have led to the development of the distributed interleaving approach described in this paper.

THE DISTRIBUTED INTERLEAVING APPROACH

In the new distributed interleaving approach, the circuitry needed to attain interleaved operation is distributed among the cells, with only minimal connections among cells. The connections among cells are non critical, i.e. failure of the connection disrupts only the interleaving function, not the basic operation of the system. Unlike the conventional approach, each cell generates its own clock pulses, and only uses intercell information to determine exact frequency and phasing of the local clock. The approach automatically accommodates varying numbers of cells. If an individual cell is removed or fails, the remaining cells automatically interleave among themselves. Any failures affecting the

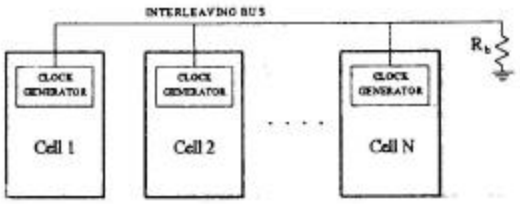

Figure 1 The distributed interleaving approach.

information-sharing connections inhibit the interleaving, but do not cause the system to fail. These attributes lead to a flexible, reliable and robust interleaving system.

To achieve distributed interleaving, all of the cells are connected by an *interleaving bus*, typically consisting of a single wire (Fig. 1). Each cell has its own clock generator, and places information about the frequency and phase of its local clock on the interleaving bus, generally in the form of signals related to the clock waveform itself. Using the aggregated information on the interleaving bus, each cell adjusts the frequency and phase of its own clock to achieve the desired interleaved effect.

A PRACTICAL IMPLEMENTATION METHOD

Consider the implementation of distributed interleaving shown in Fig. 1. Each cell contains its own clock generator. The clock generators are connected together by a single-wire interleaving bus, which is terminated in a known resistance, R_b, connected to ground. The structure of the clock generator circuit is illustrated in Fig. 2. Each clock generator contains a voltage-controlled oscillator (VCO) whose frequency (and phase) can be varied over a small range with a control voltage. The VCO generates both a sinusoidal and a square wave output voltage. The square wave output is used for the local clock. The sinusoidal output is run through a voltage-to-current converter, which drives a current proportional to the sinusoidal voltage onto the interleaving bus and through R_b. The voltage of the bus will thus be proportional to the vector sum of the sinusoidal VCO outputs of all the cells. Each clock generator senses this voltage and subtracts out its own contribution, leaving a signal which is the aggregate voltage of the other cells. A phase detector compares this signal to the output of the cell's local oscillator. A filtered version of the phase detector output is used for the control input to the VCO. This is done to drive the oscillator 180° out of phase with the aggregate output of the other cells. Each clock generator is thus designed to phase-lock out of phase with the aggregate output of the others.

When two clock generators are connected to the interleaving bus, they each phase-lock 180° out of phase with the other. When three clock generators are connected, they each phase-lock 180° out of phase with the aggregate of the other two, leading to a locked condition where each clock is 120° out of phase with the others. For situations where more than three clock generators are connected, there is more than one stable locking condition. However, they all involve sub-groups of cells interleaving among themselves.

PROTOTYPE SYSTEM DESIGN

The design of a distributed interleaving system using phase-locking techniques requires careful attention to the system dynamics. We address the system dynamics in the context of the design of a three cell prototype system operating at approximately 50 kHz. First, consider the design of the phase-locked loop (PLL) within the clock generator circuit of Fig. 2. The PLL is comprised of a phase detector, a loop filter $H(s)$, and a voltage-controlled oscillator [6]. The phase detector generates an output voltage whose average is related to the phase difference between the input waveform and the local oscillator. The multiplier phase detector employed in the prototype system yields a nonlinear relationship which can be modeled as a linear gain (K_d = 4.8 V/rad) for small perturbations away from the locked condition. The voltage-controlled oscillator converts a step in input voltage to a step in output frequency (ramping phase), and hence can be modeled (in a linearized sense) as an integrator with a gain (K_o = 6289 rad/(V-s)). The loop filter $H(s)$ serves both to remove high-frequency components from the phase detector output and to compensate the closed-loop dynamics of the PLL. To limit

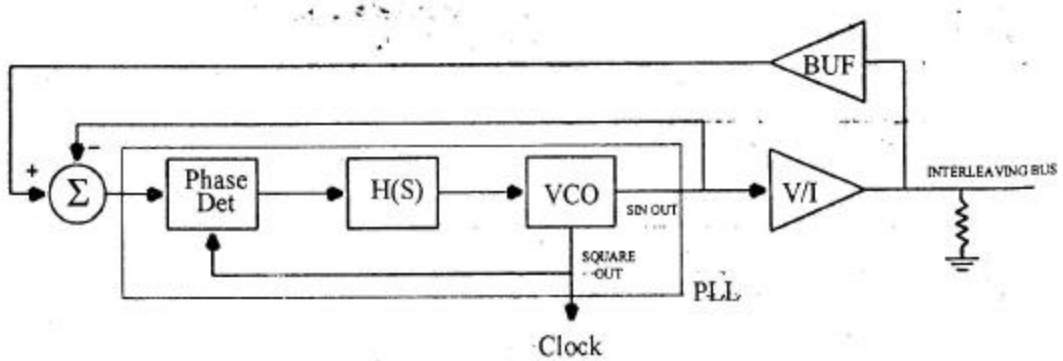

Figure 2 Structure of the clock generator for the example implementation.

the steady-state phase error of the system while allowing a limited degree of play in the phase alignment, an active loop filter of the type in Fig. 3 was selected. As described in [6], this type of loop filter yields a steady-state phase error of

$$\theta_v = \frac{\Delta\omega}{K_o K_d H(0)} \qquad (1)$$

where $\Delta\omega$ is the maximum frequency deviation of the oscillator. For the parameters of the prototype system, this yields less than 1.4° of phase error for a 5 kHz frequency deviation, which was deemed acceptable. The resulting PLL design has the (linearized) input to output phase transfer function shown in Fig. 4. This design provided sufficient lock range and tracking range for the task. Note that the 90° phase shift associated with the multiplier phase detector along with an additional 90° phase shift in the VCO sine wave output was employed to achieve the 180° phase lock position desired for the interleaving system. The additional clock generator components are simple op-amp circuits whose dynamics can be neglected in the prototype system.

It must be recognized that the individual clock generators are themselves interconnected in a feedback configuration, yielding closed-loop system dynamics which are a function of the individual clock generator dynamics. We can find the closed loop dynamics of a two-cell clock generator system using the feedback model of Fig. 5, where we have denoted the (linearized) input to output phase transfer function of the k^{th} clock generator as $P_k(s)$. For the prototype system design, this approach yields closed-loop system poles at s = -5542, -496.3, -1.05, and 0 Np/s. The pole at the origin behaves as an integrator, and may at first seem to indicate only marginal stability of the system. However, in reality, this pole merely indicates that a step input phase disturbance can cause the system to settle at a different frequency (e.g., with ramping output phase in the linearized model). Thus, the fact that the desired phase lock condition can occur over a range of frequencies yields the pole at the origin in the linearized model. The limited adjustment range of the VCO's prevents this fact from causing problems. If a disturbance brings one of the clock generators to the edge of its adjustment range, the other clock generator will lock out of phase with it at that frequency with the dynamics of a *single* clock generator. A similar feedback configuration

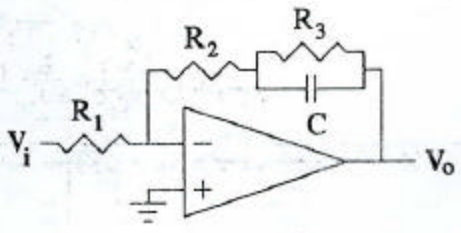

Figure 3 Loop filter structure for the prototype system. C = 0.22 μF, R_1 = 100 kΩ, R_2 = 10 kΩ, R_3 = 4.3 MΩ.

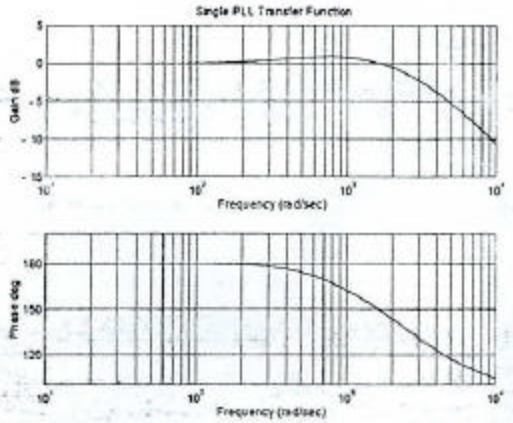

Figure 4 Input to output phase transfer function for the linearized model of a single prototype clock generator circuit.

analysis can be made for the three-cell case. This also yields a mixture of stable high- and low- frequency poles and a pole at the origin.

EXPERIMENTAL RESULTS

To validate the proposed implementation, a 3-cell discontinuous-mode boost-converter system operating at approximately 50 kHz has been constructed and used to verify the validity of the approach. Each cell employs a conventional current-mode control chip with its on-chip oscillator overridden by the local clock generator circuit. The clock generators themselves were constructed with available discrete components; an AD633 differential multiplier was used as a phase detector, while an XR2206 monolithic function generator was used as the VCO. Figure 6 shows the clock waveforms from the prototype system with 2 and 3 converter cells connected to the interleaving bus. Phase locking was found to be very stable with acceptable locking and tracking characteristics for both the two and three cell case. The correct phasing of the clock waveforms to within design specifications (1.5°) is obtained under all conditions.

To verify the ripple cancellation benefits of the approach, the output voltage ripple was measured with synchronous

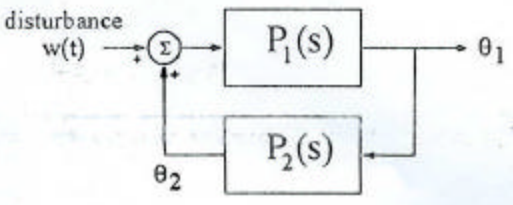

Figure 5 Feedback model for predicting the dynamics of a two-cell distributed interleaving system.

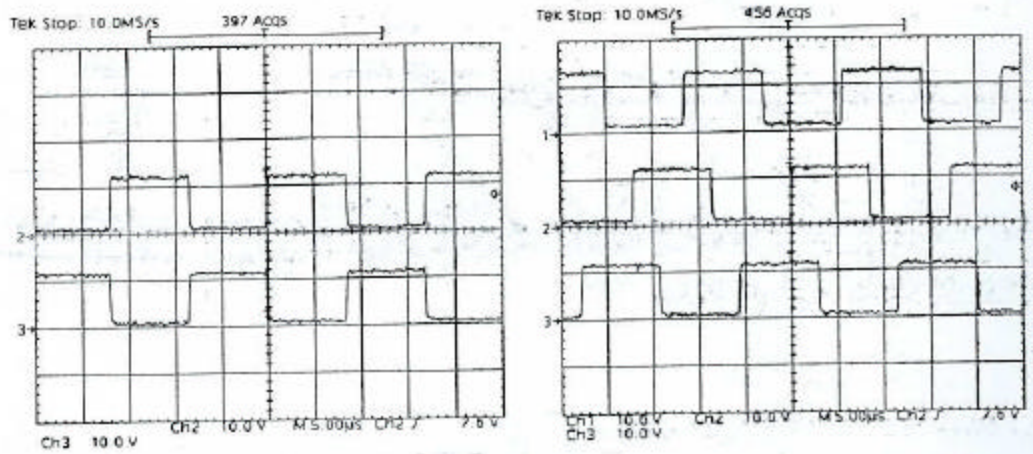

Figure 6 Experimental clock waveforms for the prototype distributed interleaving system with two and three cells.

clocking, independent clocking, and (distributed) interleaved clocking of the three cells. As shown in Fig. 7(a), synchronized clocking of the cells leads to an output voltage ripple of approximately 2.1 V_{p-p}, and 0.653 V_{rms}. As shown in Fig. 7b, independent clocking of the cells (yielding stochastic ripple cancellation) leads to a time-varying output voltage ripple, with the rms ripple reduced as expected down to $0.35 \pm 0.03 \cdot V_{rms}$. Operation under distributed interleaving, as shown in Fig. 7 (c) and (d), yields a ripple of 0.3 V_{p-p} and 0.072 V_{rms}, with the first major ripple component at three times the individual clocking frequency. This represents a factor of 7 reduction in peak-to-peak ripple over synchronized clocking. Ideally, a factor of 9 reduction should be obtained: a factor of three from the current ripple cancellation, and a factor of three from the frequency increase across the capacitive output filter. The reason for this discrepancy is shown in Fig. 7(d), where it is seen that the cancellation of the fundamental ripple frequency is not perfect due to second order effects such as phasing error, differences in the boost inductors and sense resistors, etc. Nevertheless, use of the prototype distributed interleaving circuitry yields a tremendous performance improvement over both synchronized and independent clocking of the converter system.

OTHER APPROACHES

The distributed interleaving implementation described in this paper generates $2\pi/N$ interleaving for up to 3 cells, above which the locking conditions are as yet unknown. While this may at first seem very restrictive, it should be pointed out that the benefits of interleaving cease to accrue beyond a very limited number of cells due to mismatches among cells [4]. This effect was seen in the prototype system, and is especially true for systems employing distributed current-sharing techniques (where small current mismatches inevitably exist [7-12]), and in systems operating at high frequencies (where small time delays correspond to large phase mismatches). For systems with large N, groups of three cells can be interleaved, with stochastic ripple cancellation occurring among the interleaved groups. Nevertheless, in some cases it may be desirable to generate $2\pi/N$ interleaved clock waveforms for higher numbers of cells. This is achievable through similar means as described here, but at the expense of increased complexity in the clock generator circuit structure and/or the interconnection structure.

CONCLUSION

The paper has introduced a distributed approach to interleaving converter cells in which the circuitry required to attain interleaving is distributed among the cells. Unlike conventional methods, the new approach requires no centralized control, automatically accommodates varying numbers of cells, and is highly tolerant of subsystem failures. A general methodology for achieving distributed interleaving has been proposed, along with a specific implementation approach and its experimental verification.

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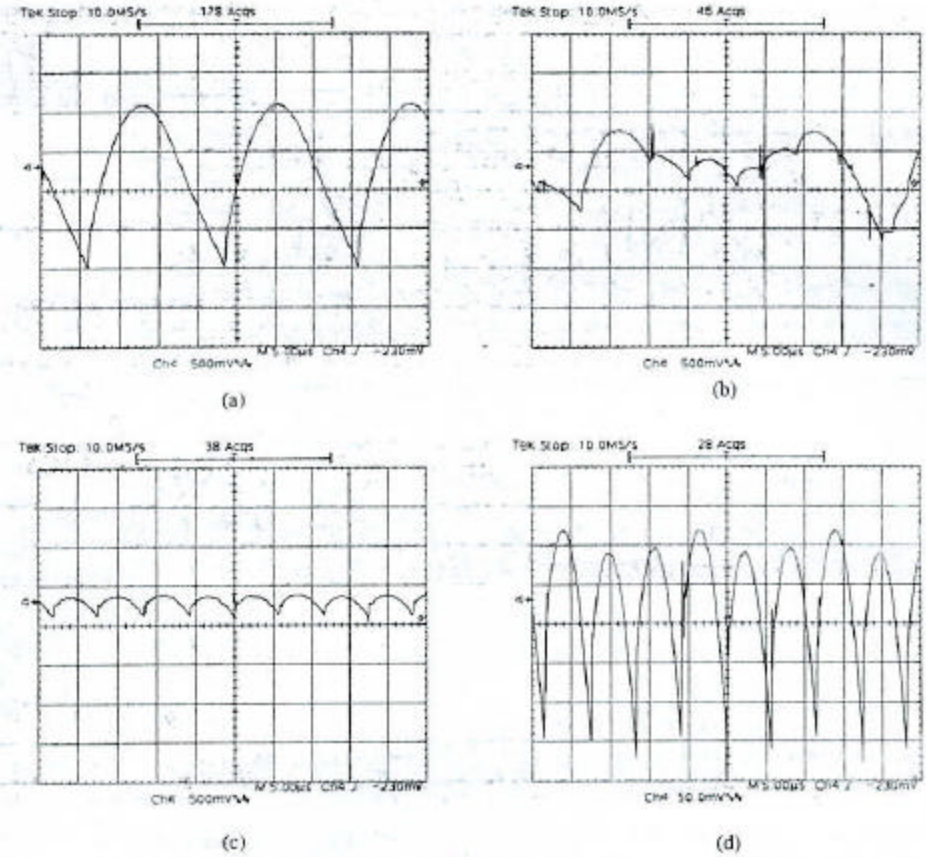

Figure 7 Output voltage ripple waveforms for the prototype system. (a) Synchronized clocking. (b) Independent clocking (stochastic ripple cancellation). (c) Interleaved clocking. (d) Interleaved clocking @ 50 mV/div.