New Architectures for Radio-Frequency DC–DC Power Conversion

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***Abstract*—This document proposes two new architectures for switched-mode dc–dc power conversion. The proposed architectures enable dramatic increases in switching frequency to be realized while preserving features critical in practice, including regulation of the output across a wide load range and high light-load efficiency. This is achieved in part by how the energy conversion and regulation functions are partitioned. The structure and control approach of the new architectures are described, along with representative implementation methods. The design and experimental evaluation of prototype systems with cells operating at 100 MHz are also described. It is anticipated that the proposed approaches and ones like them will allow substantial improvements in the size of switching power converters and, in some cases, will permit their integrated fabrication.**

***Index Terms*—Cellular architecture, class E inverter, integrated converter, radio frequency (RF) dc–dc power converter, RF power amplifier (PA), self-oscillating inverter (SOI), very high frequency (VHF).**

I. Introduction

THE RAPID evolution of technology is generating a demand for power electronic systems whose capabilities greatly exceed what is presently achievable. A challenge of particular importance is the miniaturization of power electronic circuits. Miniaturization is difficult, given the energy storage and loss limitations of passive components used in the conversion process. Furthermore, there is a need for new approaches that enable power circuits to be fabricated in a much more integrated fashion. Higher levels of integration can promote improved power density, and enable the use of the batch fabrication techniques that are central to the cost benefits of integrated circuits (ICs) and micro-electrical-mechanical systems (MEMS). Thus, design and manufacturing methods that enable power electronics to be miniaturized and/or fabricated using batch processing techniques have tremendous potential value.

Achieving miniaturization and integration of power electronic circuits will necessitate radical increases in switching frequency to reduce the required size of passive components. This paper introduces new architectures for dc–dc power conversion that enable dramatic increases in switching frequencies, potentially into the microwave/ultra-high frequency (UHF) range. By architecture, we mean the manner in which a power electronic system is structured and controlled. The architecture of most conventional systems is straightforward: a single power stage of a particular topology, regulated using a switching control technique such as pulse-width modulation (PWM) or frequency modulation. Here we expand beyond this basic architectural approach, to systems incorporating multiple power stages and new hybrid control techniques. The new system architectures relax the operating requirements on the individual power stages, enabling the sought after increase in switching frequencies. The proposed architectures can be realized with a range of particular power stage topologies; the design of power stage topologies appropriate to the proposed architectures is also addressed.

The new architectures considered here promise to enable substantial miniaturization of dc–dc converters, and to permit much higher degrees of integration to be achieved. Section II provides background and highlights the principal challenges that need to be overcome to achieve these goals. Section III introduces two new conversion architectures, and describes their principal operating and control characteristics. The general attributes of converter architectures suitable for radio frequency (RF) power conversion are also discussed, and some other closely related approaches are identified. Section IV presents the design and experimental evaluation of a 100-MHz dc–dc converter "cell," and Sections V and VI demonstrate its application in the two proposed converter architectures. Section VII discusses directions for continued development of RF power conversion systems and points toward emerging possibilities in this area. Finally, Section VIII concludes the paper.

II. Background

Switching power converters traditionally comprise semiconductor switching devices and controls along with passive energy storage components, including inductors and capacitors. The passive components provide intermediate energy storage in the conversion process and provide filtering to attenuate the switching ripple to acceptable levels. Inductive elements, in particular, are used to achieve near-lossless transfer of energy through the circuit and to limit the instantaneous currents generated by the switching action of the power stage. These passive energy storage elements often account for a large portion of converter size, weight, and cost, and make miniaturization difficult.

A principal means for achieving reduction in the size of power circuits is through increases in switching frequency. As is well known, the size of the energy storage elements (e.g., inductors and capacitors) required to achieve a given conversion

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function varies inversely with switching frequency [1, Ch. 6]. Much of the improvement in size and cost of switching power converters over time has been due to increases in switching frequency, rising from tens of kilohertz in the early 1970's into the megahertz range today. Increases in switching frequency have been achieved both through new devices and materials better suited to high-frequency operation (e.g., power metal oxide semiconductor field effect transistors (MOSFETs) and new ferrite magnetic materials) and through circuit and component designs that reduce losses associated with high-frequency switching [2]–[22].

A. Challenges of High-Frequency Power Converter Design

Despite the availability of devices capable of operating up to several gigahertz under certain conditions, power converter switching frequencies remain in the low megahertz range and below. This fact reflects some of the challenges peculiar to power electronics. Switching power converters must typically operate efficiently over a wide load range (often in excess of 100 : 1) from a variable input voltage, and must regulate the output in the face of rapid and unpredictable load and input variations. However, existing circuit topologies capable of operating efficiently at high frequencies are not well matched to these requirements. These topologies use a continuous resonating action to achieve the zero-voltage switching (ZVS) that is essential to operation at radio frequencies and beyond: wherein devices are switched with little or no voltage across them, is necessary to achieve the ultra-high operating frequencies considered here. Likewise, at these frequencies device gating loss becomes a major consideration, and some form of resonant drive is usually required [23]–[26]. This approach is effective for full load conditions, where the losses associated with resonant operation are small compared to the output power. However, these resonating losses are present under all loading conditions, and are typically unacceptable in systems that must operate efficiently over a wide load range.

A second factor that has inhibited the use of higher switching frequencies in power electronics is the impact of frequency-dependent losses on magnetic component size. At high frequencies, loss limits—rather than energy storage limits—are the dominant consideration in sizing magnetics. Core loss considerations are of particular importance in magnetic elements with significant ac components of flux, such as transformers and resonant inductors. The core loss densities of most power ferrite materials rise rapidly with frequency in the megahertz range, necessitating flux derating as frequency is increased. As a result, magnetic component size does not always decrease as frequency is increased, and can even worsen [27]. Air-core magnetics designs do not suffer this limitation, but must be operated at still higher frequencies to compensate for reduced inductance resulting from the lack of high permeability core material. Achieving dramatic reductions in power converter size thus requires either new passive component designs that do not suffer this loss limitation or power conversion architectures capable of operating at sufficiently high frequencies that air-core magnetics can be employed effectively.

The need to regulate the output represents a further difficulty with available power circuits capable of high frequency operation. While some degree of regulation can be achieved with such circuits (e.g., by frequency control [2], [9], [14]), the difficulty in realizing regulation over a wide load range is only exacerbated as switching frequency increases. Moreover, converter dynamics and control circuit implementation complexities escalate at higher operating frequencies. These factors have placed major constraints on power converter operating frequencies and, in turn, on size and performance. For these reasons, attempts at using greatly increased switching frequencies in conventional architectures [28] have not met the requirements of efficiency and ability to regulate the output. Achieving the dramatic improvements in size, performance, and integration that are desired for future power converters thus requires new power conversion architectures that overcome these limitations.

B. RF Amplifiers

The proposed architectures incorporate circuit structures and principles that are employed in tuned RF power amplifiers (PAs) [15], [17], [29], [30] but apply them in manners that overcome their limitations in conventional dc–dc converter architectures. Here, we review some of the characteristics of tuned RF power circuits.

Switched-mode RF amplifiers (inverters) utilize resonant circuit operation to achieve ZVS of the semiconductor devices. To minimize driving losses and achieve high power gains, multistage amplifier designs are often used. In a multistage design, amplifiers are chained together such that each amplifier efficiently drives the gate(s) of a higher-PA; the last amplifier in such a chain drives the output. Using these techniques, tuned inverters can be designed to operate with good efficiency into the gigahertz range, and in some cases can be completely integrated [29], [31]. Similar (including dual) circuits can be used for efficient high-frequency rectification [8], [10], [12].

Both inverter and rectifier circuits of this type exhibit important limitations. First, they only operate with good efficiency over a relatively narrow load range, both because of the continuous resonating losses described above and because the load greatly affects the operating waveforms. Second, the controllability of these designs (e.g., to compensate for load or input variations) is very limited, and becomes more challenging at higher frequencies and in multistage amplifiers. Thus, the practical use of these circuits in dc–dc power conversion [2], [6], [9]–[11], [14] has been limited to relatively low frequencies (< 30 MHz), as previously described.

III. New Converter Architectures

As described above, conventional power converter designs are subject to a number of constraints that limit their practical operating frequency, and in turn limit the degree of miniaturization and integration that can be achieved. Here we propose new power conversion architectures that overcome these constraints. These architectures take advantage of the high-frequency performance of tuned RF amplifier circuits while circumventing their limitations through the manner in which the energy conversion and regulation functions are partitioned. Two primary architectures are introduced: a Vernier-regulated architecture and a cell-modulation-regulated architecture. We also consider some of the variants of these approaches.

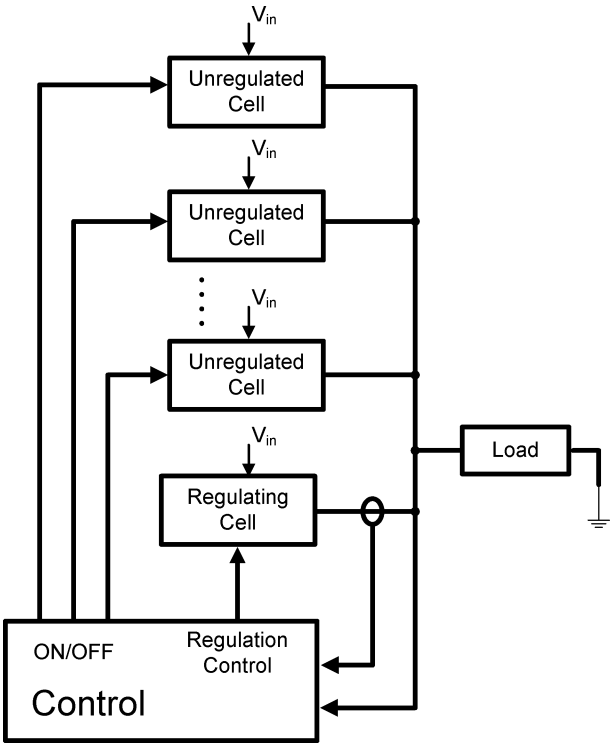

Fig. 1. Block diagram illustrating the Vernier-regulated converter architecture.

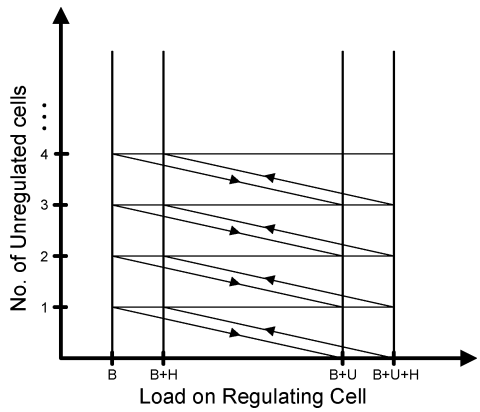

Fig. 2. Activation scheme for unregulated cells. Unregulated cells are activated or deactivated based on the load on the regulating cell. U is the incremental loading change when an unregulated cell is activated or deactivated. B is the minimum load on the regulating cell, below which an unregulated cell is deactivated. H is a hysteresis value to prevent chattering at boundaries.

A. *Vernier-Regulated Architecture*

The Vernier-regulated cellular architecture (VRCA) is a type of cellular power converter. As shown in Fig. 1, this architecture comprises a number of unregulated converter cells along with a regulating converter cell, all of which supply the output in parallel. The unregulated cells each comprise an RF inverter, a transformation stage, and a rectifier, along with filtering and ancillary circuitry. The unregulated cells are structured such that they may be activated or deactivated (turned on or off). The regulating converter cell—or Vernier cell—may be a switched-mode converter, a linear regulator, or some combination thereof, and need only be rated for a small fraction of the total system power. We term the regulating cell a Vernier cell by analogy to the Vernier scale on a caliper (named after its designer, Pierre Vernier). The Vernier scale provides incremental measurements between the discrete marks on a caliper's main scale: likewise, the Vernier cell provides the incremental power between the discrete power levels that can be sourced via the unregulated cells.

Operation of the proposed architecture is as follows. The regulating cell is controlled to regulate the output at the desired level. As the load varies, unregulated cells are activated or deactivated to keep the regulating converter within a specified load range while ensuring that the active unregulated cells run at or near their ideal operating points. One activation scheme that meets these requirements is illustrated in Fig. 2. In steady state, the unregulated cells deliver a portion of the total power (in discrete increments), while the regulating cell provides whatever remaining power is needed to regulate the load voltage.

This architecture has a number of advantages. First, the unregulated cells only run under a narrow range of loading conditions. Second, the only control required for the unregulated cells is a simple on/off command. These characteristics facilitate the use of very high frequency multistage amplifier designs for the unregulated cells. Furthermore, because inactive cells do not incur loss, and unregulated cells are only activated as needed to support the load, efficient light-load operation can be achieved[1]. Finally, the proposed architecture inherits a number of advantages of more conventional cellular converter architectures, including the dispersal of heat generation in the circuitry and the potential for fault tolerance [33].

In any power converter system that processes power through multiple channels, it is important that each channel stably carry the appropriate amount of power in order to avoid circulating losses and the possible destructive overload of individual channels (see [33]–[35] and references therein). In the Vernier-regulated architecture, it is particularly important to ensure that the unregulated cells share power in the desired manner. Furthermore, the unregulated cells should not interfere with the output control function of the regulating cell.

One method of achieving these control goals is to appropriately shape the output impedances of the individual cells. For a given operating point, the cells are modeled as Thévenin equivalent voltages and impedances that drive the output filter and load [33]. For the regulating cell, the Thévenin source is equal to the reference voltage, while the Thévenin (output) impedance depends on both the power stage and control loop design. For the unregulated cells, the Thévenin model parameters depend on the input voltage, the cell power stage design, and the cell switching frequency. To achieve the desired output control, the regulating cell is designed to have low output impedance at low frequencies (down to dc), while the unregulated cells are designed to have relatively high output impedances (and thus act as current sources) (see Fig. 3). High dc output impedance is achievable with appropriate rectifier design [8], and can also be used to ensure that the unregulated cells share power (and current) correctly via their "droop" characteristics [33]–[38]. Under these conditions, the small-signal control dynamics of the system are

[1]We note that varying the number of active cells in a parallel converter system to maintain light load efficiency has been exploited before [32], albeit in the context of very different design and control methods.

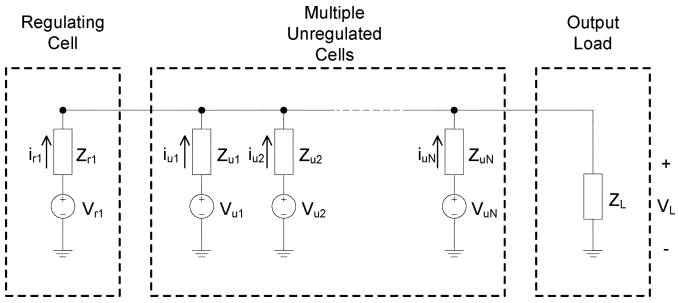

Fig. 3. Low Thévenin impedance at the regulating cell provides a tight regulation of the output. A high Thévenin impedance in the unregulated cells result in proper current sharing .

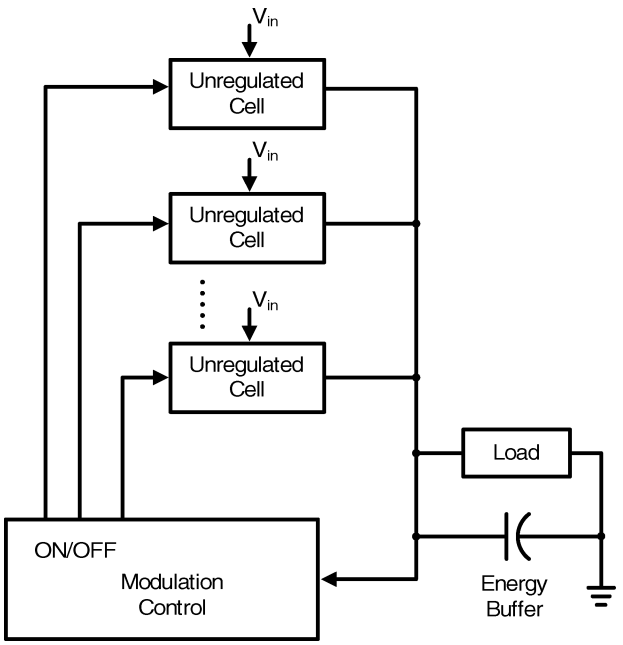

Fig. 4. Block diagram illustrating the cell-modulation-regulated converter architecture.

dominated by the regulating cell. Thus, through appropriate design, the control requirements of the proposed Vernier-regulated architecture can be met.

B. Cell-Modulation-Regulated Architecture

The previous architecture uses a Vernier cell operating at variable load to provide the difference between the quantized power levels delivered by the unregulated cells and that needed to regulate the output. By contrast, the cell-modulation-regulated architecture uses *only* unregulated cells to supply the output, as illustrated in Fig. 4. As with the previous architecture, the unregulated cells are engineered to have high output impedance (such that they may be treated as current or power sources) and to admit on/off control. To provide the proper average power to regulate the output, the number of unregulated cells that are activated is modulated over time, and an energy buffer (e.g., a capacitor, ultracapacitor, battery, etc.) at the converter output is used to filter the resulting power pulsations.

A variety of modulation strategies are compatible with this approach. Perhaps the simplest is hysteretic control of the output voltage. If the output voltage falls below a specified minimum threshold, the number of activated cells is increased (e.g., in a clocked or staggered fashion) until the output voltage returns above the minimum threshold (or until all cells are activated). If the output voltage rises above a specified maximum threshold, the number of activated cells is decreased until the output voltage returns below the maximum threshold (or until all cells are deactivated). In the case where a single cell is used, this corresponds to bang-bang control of the output [39]. With multiple cells this approach might be considered a form of multilevel PWM of power (or current). The system control can be formulated as a sigma-delta modulator [40] or other discrete pulse modulation technique. Clearly, there are many other similar control strategies that will likewise provide a desired average output voltage.

The cell-modulation-regulated architecture exhibits a number of the advantages of the previous architecture. The unregulated cells only need to operate under on/off control over a narrow power range. This facilitates the use of UHF power converter cells having small size and high efficiency, and enables high light-load efficiency to be achieved. The efficiency benefit at light loads is similar to that achieved with "burst" or "sleep" mode operation in conventional designs, e.g., [41], [42]. Moreover, because the cells can be run at fixed frequency and duty ratios, the use of high-order tuned circuits to improve efficiency and power density (e.g., Amplifer classes F, F^{-1}, E/F, etc. [43]–[45]) becomes possible. However, the considerations involved in sizing input and output filters for this architecture are different than that of the previous one. In the Vernier architecture, the size of the output filter (e.g., output capacitor) needed depends primarily on the bandwidth of the regulating (Vernier) cell, and only secondarily on the startup speed of the unregulated cells, if at all. By contrast, in the cell-modulation-regulated architecture, the energy storage requirement and size of the output filter capacitor depends on the rate at which the unregulated cells can be modulated on and off—typically orders of magnitude slower than the switching frequency of the cells themselves. Consequently, the UHF operation of the cells enables dramatic reductions in size of power stage components (e.g., inductors, capacitors, and transformers), but it does not benefit the input and output filter components to the same extent. Nevertheless, in many applications, significant energy storage is provided at one or both converter ports (e.g., for holdup), so this is often acceptable. It may be concluded that the cell-modulation regulated architecture enables high efficiency across load and tremendous reductions in power stage component size, but does not provide the same degree of improvement for input and output filters.

C. Related Architectures

The architectures proposed above enable dramatic increases in switching frequency as compared to conventional designs, with consequent benefits. It should be appreciated that there are many variants that offer similar advantages. For example, if one is willing to accept regulation of the output to discrete levels, one can utilize a set of unregulated cells without the need for a Vernier cell or time-domain modulation to interpolate between levels. The use of unregulated cells having different power ratings (e.g., a geometric 2^{N} progression) would facilitate this approach, though it would perforce increase the design

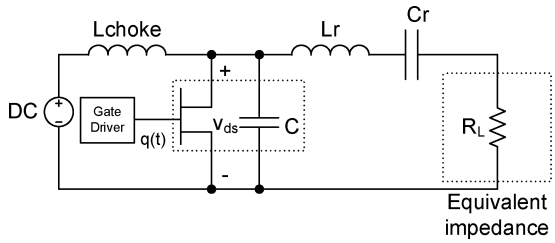

Fig. 5. Simplified model of the Class-E resonant inverter.

effort. (Note that the use of nonuniform cell sizing can benefit the above architectures as well.)

The underlying characteristic of all such approaches is that they structure the energy conversion and regulation functions in manners that are compatible with the effective use of UHF circuit designs and techniques. Limiting the drive requirements and operating conditions of activated cells by partitioning energy processing and regulation—as done here—is one means of achieving this. It is hoped that the recognition of this general strategy will lead to the emergence of additional circuit architectures having similar advantages.

IV. 100-MHz Unregulated Cell Design

The proposed architectures admit a wide range of unregulated cell designs. The principle requirements are that the cells should operate efficiently for at least a narrow specified operating range, have high output impedances, and be amenable to on/off control. These requirements are fulfilled by many RF circuit topologies, and permit cell designs having switching frequencies far higher than those reached in conventional dc–dc converters. To illustrate this, we present the design and experimental evaluation of a converter cell operating at 100 MHz that achieves $>75\%$ efficiency over its operating range.

The unregulated cell consists of a high frequency inverter, an impedance matching network, and a resonant rectifier. The inverter is driven by a self-oscillating gate driver at a free running frequency of 100 MHz.

A. Class E Resonant Inverter

The front end of the unregulated cell consists of a Class E resonant inverter (see Fig. 5). The inverter provides the desired ZVS, and admits the use of relatively slow gating waveforms without undue loss. In conventional RF design, the loaded Q (Q_L) of the converter is usually chosen to be large, resulting in waveforms with high spectral purity. For power conversion, however, the requirements on Q_L are different, since the goal is to maximize power transfer with minimum loss. A low value of Q_L results in less energy resonated in the tank, which further implies reduced conduction loss in the parasitic elements of the inverter; Equations for the design of Class E RF inverters with low Q can be found in [46]. The nominal loaded Q in the prototype design was set to $Q_L = 3.4$.

Under optimal ZVS conditions, inverter output power is proportional to the capacitance in parallel with the switch. For the intended range of output power in the prototype cell implementation, the required capacitance was provided entirely by the parasitic drain-source capacitance associated with the switch.

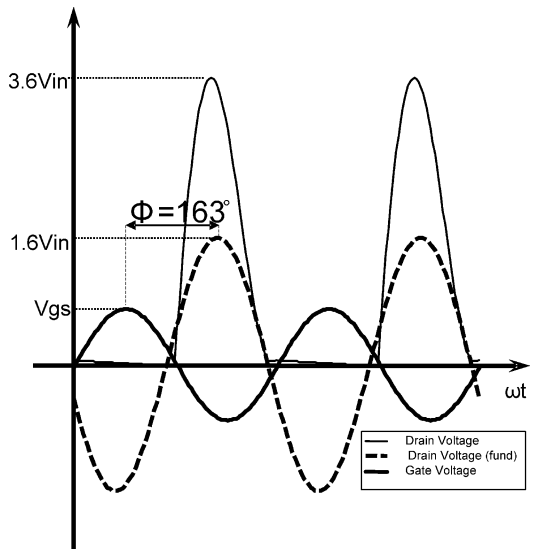

Fig. 6. Idealized $v_{ds}(t)$ and its fundamental (dotted line). The gate signal is also shown. The phase angle between the fundamental component of the drain voltage and the idealized gate signal is 163°.

The device selected for the main switching element is a silicon N-channel laterally diffused MOSFET (LDMOSFET). This semiconductor device offers the required characteristics needed to operate at high frequencies: it presents an acceptable drain to source capacitance and a low gate capacitance that allows for small gating loss.

B. Self-Oscillating Gate Driver

Gating losses in power converters grow with switching frequency. In traditional topologies, these losses often become the limiting factor for high frequency operation. To mitigate these losses and recover some of the energy required to operate the semiconductor switch, a resonant gate driver may be used. A resonant gate drive often implies sinusoidal gate signals, a feature commonly found in cascaded PAs.

A low-cost, efficient method of selectively driving the inverter is of great importance to the proposed design. To achieve this goal while maintaining the cell's simplicity, a self-oscillating gate driver making use of the drain-source voltage $v_{ds}(t)$ of the LDMOSFET was implemented. A resonant feedback network is used to extract and phase shift the fundamental component of the drain voltage to generate a sinusoidal gating signal capable of sustaining oscillation at the desired frequency.

Fig. 6 shows the inverter's drain to source voltage $v_{ds}(t)$ as well as its fundamental component. These waveforms are referred in phase to the required gate voltage, $v_{gs}(t)$. The phase difference between the fundamental component of $v_{ds}(t)$ and the required gate signal was found to be 163° (as depicted in Fig. 6).

1) Phase Shift/Feedback Network: A linear circuit structure, including the internal parasitics of the LDMOS gate, provides the appropriate frequency selection and phase shift to attain sustained oscillation at the desired frequency. Fig. 7 shows a simplified circuit which feeds back the voltage $v_{ds}(t)$ and provides the required phase shift. The fundamental of $v_{ds}(t)$ is also attenuated to a value that ensures proper gate drive while remaining below the gate breakdown voltage ($v_{gs,\max} = 20$ V).

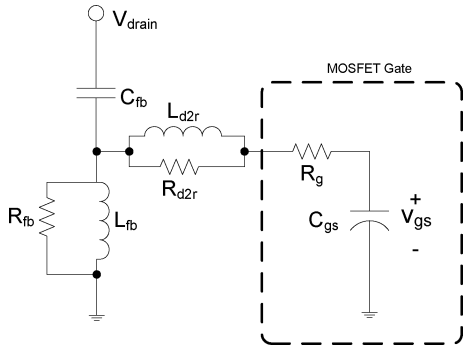

Fig. 7. Simplified phase shift/feedback network.

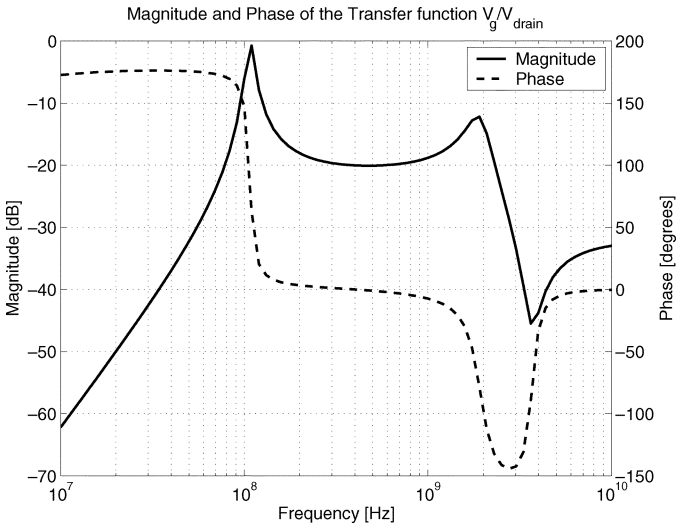

Fig. 8. Magnitude and Phase of the transfer function $(V_{gs}/V_{ds})(\omega)$ for the proposed feedback network.

Fig. 8 shows the frequency response of the drain to gate transfer function $((V_{gs}/V_{ds})(\omega))$; at 100 MHz the phase is the required 163°. By properly adjusting the damping resistor $R_{\rm fb}$ it is possible to set the magnitude and the precise frequency of oscillation by changing the Q of the resonant structure.

The function of L_{d2r} and R_{d2r} is to damp the second resonance apparent in the transfer function of Fig. 8; higher frequency oscillations (≈2 GHz) might otherwise result.

The input impedance of the self-oscillating structure is dominated by the value of the feedback capacitor $C_{\rm fb}$ at the operating frequency. This capacitor is selected such that the impedance looking into the structure is much higher than the impedance looking into the resonant tank of the Class E inverter, ensuring that the frequency characteristics of the tank circuit are not substantially altered.

2) On/Off and Startup Circuit: The proposed gate driver requires a simple method to start and stop cell operation. This can be achieved with a slight modification to the phase shift/feedback network previously described. This is illustrated in Fig. 9.

When transistor $Q_{\rm on/off}$ is on, the gate is pulled low and the inverter is shut off. When $Q_{\rm on/off}$ turns off, $C_{\rm dc}$ charges through $R_{\rm fb}$. With a properly chosen logic supply voltage (3.3 V in Fig. 9), the gate is driven above threshold, turning on the

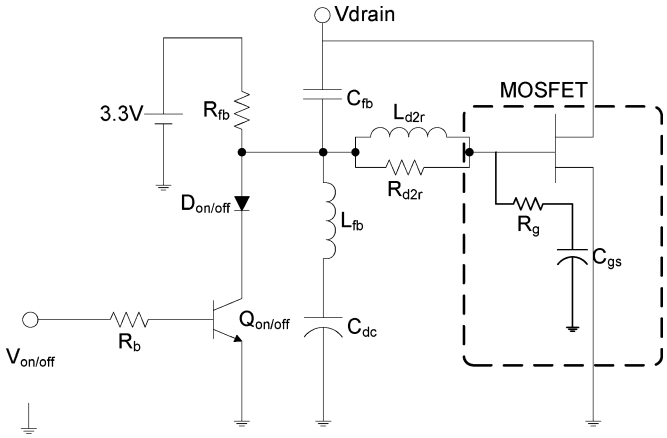

Fig. 9. Self-oscillating resonant gate driver circuit.

MOSFET and starting oscillation through the phase shift/feedback network. A digital signal can thus be used to activate or inhibit converter operation.

During operation, $C_{\rm dc}$ remains biased close to the MOSFET threshold voltage, helping to keep the duty ratio near 50%. $C_{\rm dc}$ is selected for minimal impact on the transfer function $(V_{gs}/V_{ds})(\omega)$. When $Q_{\rm on/off}$ is off, the junction capacitance of $D_{\rm on/off}$ appears in series with the output capacitance of $Q_{\rm on/off}$; this minimizes loading on the phase shift/feedback network.

The RC circuit formed by $R_{\rm fb}$ and $C_{\rm dc}$ introduces a delay between the command signal and inverter startup; it is this delay which limits the speed at which the cell can be turned on.

C. Matching Network and Rectifier

The rectifier is implemented as a balanced pair of single-diode rectifiers. The rectifier network is structured such that it appears resistive in a describing function sense. This rectifier is connected to the inverter tank by a simple L-section matching network [47].

Fig. 10 shows the implemented cell design, with component values and part numbers enumerated in Table I. Important circuit board parasitics are also described.

D. Experimental Results

Cell efficiency and output power were measured over the supply voltage range 11 to 16 V with a constant-voltage load comprising fifteen 5.1-V, 1-W Zener diodes in parallel with two 15-μF Tantalum capacitors. Output power ranged from approximately 2.5 to 6 W, with an average efficiency greater than 77.5%. Fig. 11 illustrates measurements from a typical cell. A photograph of one cell is shown in Fig. 12.

Fig. 13 shows measured drain-source voltage under nominal conditions; turn-on and turn-off transients are depicted in Fig. 14 (the command occurs at $t = 0$ in both cases).

The incremental output impedance of the unregulated cell design at $V_{\rm out} = 5$ V ranged from 30 Ω ($V_{\rm in} = 11$ V) to 3 Ω ($V_{\rm in} = 16$ V).

The unregulated cell switching frequency, 100 MHz, is significantly higher than those found in conventional dc–dc converter designs, while maintaining an acceptable efficiency level. Moreover, as discussed in Section VII, substantially

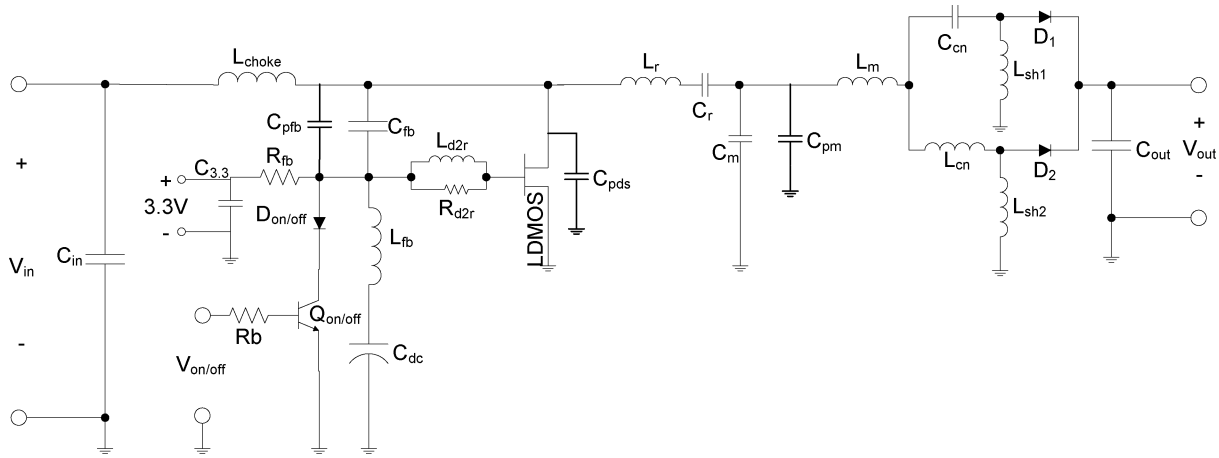

Fig. 10. Unregulated 100-MHz switching dc–dc power converter cell. Component values and important parasitics are enumerated in Table I.

TABLE I
COMPONENT VALUES IN THE UNREGULATED CELL

Circuite lement	Nominal Value	Part number
L_{choke}	538 nH	Coilcraft 132-20SMJ
C_{fb}	2 pF	CDE MC08CA020C
C_{pfb}	1.15 pF	Measured circuit board parasitic
L_{fb}	27 nH	Coilcraft 1812SMS-27NG
R_{fb}	2.2 kΩ	Standard SMD
C_{dc}	2.2 nF	C0G Ceramic, 50 V
R_b	100 kΩ	Standard SMD
L_{d2r}	2.5 nH	Coilcraft A01TJ
R_{d2r}	15 Ω	Standard SMD
C_{pds}	5.9 pF	Measured circuit board parasitic
L_r	68 nH	Coilcraft 1812SMS-SMS-68N
C_r	57 pF (47 pF+10 pF)	CDE MC12FA470J CDE MC08CA100D
C_m	47 pF	CDE MC12FA470J
C_{pm}	2.4 pF	Measured circuit board parasitic
L_m	12.5 nH	Coilcraft A04TJ
C_{cn}	100 pF	CDE MC12FA101J
L_{cn}	22 nH	Coilcraft 1812SMS-22NG
L_{sh1}	12.5 nH	Coilcraft A04TJ
L_{sh2}	12.5 nH	Coilcraft A04TJ
C_{in}	4 × 47 nF	X7R Ceramic, 50 V
C_{out}	9 × 47 nF	X7R Ceramic, 50 V
$C_{3.3}$	2 × 47 nF	X7R Ceramic, 50 V
LDMOSFET		PD57018S
D_1, D_2		MBRS1540T3
$D_{on/off}$		BAS70
$Q_{on/off}$		BC847

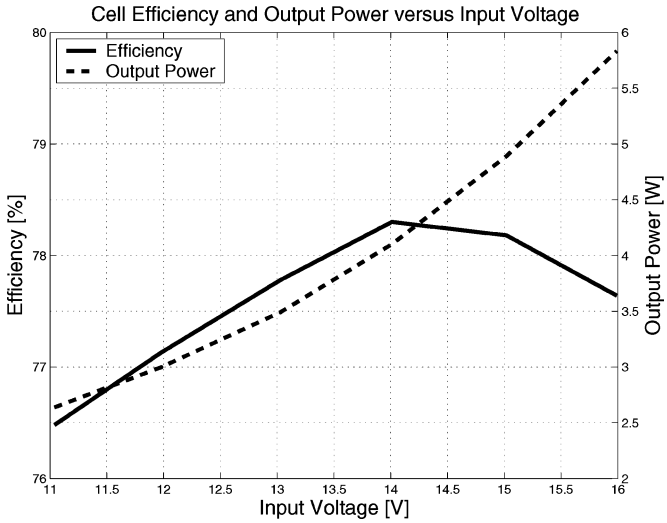

Fig. 11. Cell performance as a function of supply voltage into a 5.1-V load.

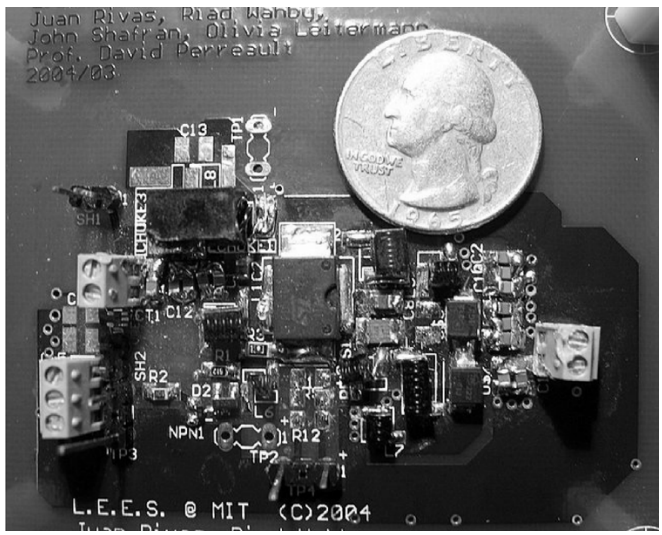

Fig. 12. Photograph of the unregulated cell circuit board.

higher switching frequencies (to several hundreds of Megahertz), power densities, and efficiencies are possible with the general approach taken here.

V. VERNIER-RREGULATED SYSTEM

A. Converter Implementation

To demonstrate the fundamental operation of a Vernier-regulated converter (Section III-A), we designed and constructed a prototype system comprising eight unregulated cells of the type in Section IV, a Vernier cell, and a clocked controller of the type pictured in Fig. 2.

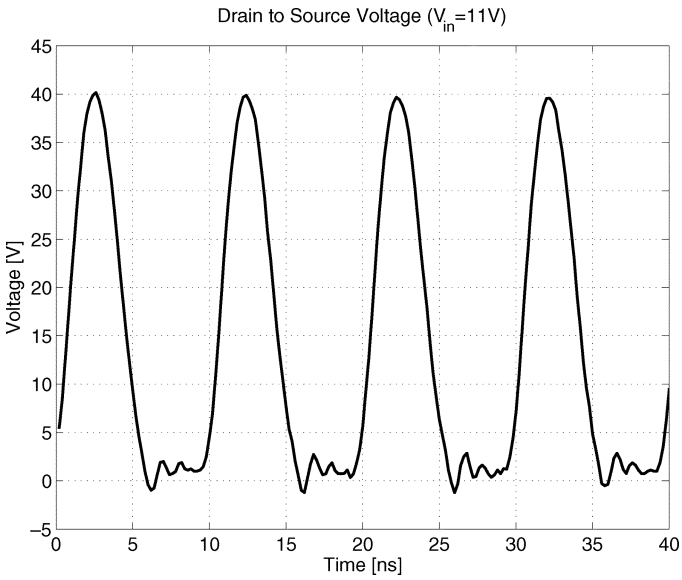

Fig. 13. Measured drain-source voltage under nominal operating conditions at $V_{\rm in} = 11$ V.

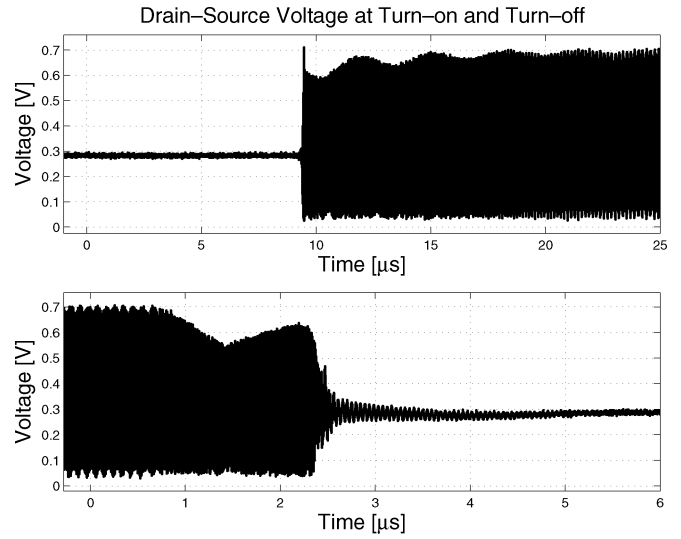

Fig. 14. Attenuated drain-source voltage during turn-on and turn-off transients. In both cases, the command occurs at $t = 0$. The drain-source voltage was measured via an attenuator network that reduced dc voltage by approximately a factor of 38; ac voltages are attenuated somewhat further.

In this implementation an LM7805 linear regulator was used for the Vernier cell. Chief among the reasons for this decision are its suitability to the task (as discussed in Section III-A) and its simplicity. Other benefits of a linear regulator are that it maintains constant (though low) efficiency down to almost zero load and that it provides well-behaved output control dynamics. Moreover, the use of an otherwise extremely inefficient regulator in this system demonstrates the efficiency potential of the Vernier-regulated architecture despite regulating cell loss.

The controller, pictured in simplified form in Fig. 15, consists of a current sensor, two comparators, and two four-bit bi-directional shift registers. When the Vernier cell output current exceeds a predefined upper threshold, a command is sent to the shift registers which activates one additional unregulated cell. Likewise, when the lower threshold is crossed, the resulting command causes one unregulated cell to be turned off. Note that

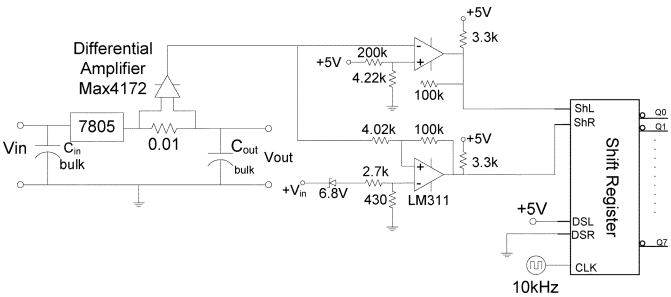

Fig. 15. Simplified schematic of the Vernier cell and system controller.

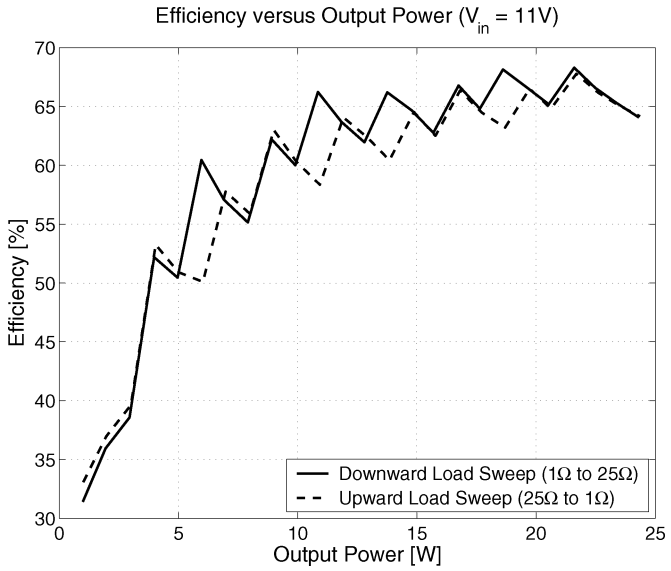

Fig. 16. Efficiency versus output power of the Vernier-regulated system for $V_{\rm in} = 11$ V. In this experiment, the load was swept from 25 Ω to 1 Ω and then back to 25 Ω, demonstrating the hysteretic characteristic of the controller.

the shift register outputs are inverted to produced the appropriate active-low control signals to the unregulated cells.

To prevent oscillation, it is necessary that the difference between the upper and lower switching thresholds be larger than the maximum unregulated cell output current. If this were not the case, upon exceeding the upper threshold and giving an activation command the Vernier cell output current would immediately fall below the lower threshold, causing a subsequent deactivation command and restarting the limit cycle. On the other hand, too large a hysteresis band underutilizes the unregulated cells, costing converter efficiency. As is clear from Fig. 11, unregulated cell output current is a rather strong function of input voltage. Thus, were a static upper hysteresis threshold chosen (necessarily accommodating the output current at $V_{\rm in} = 16$ V), substantial underutilization of the unregulated cells would occur at lower supply voltages. To mitigate the consequent losses, the upper hysteresis threshold is instead made a function of $V_{\rm in}$ via a Zener diode and a resistive attenuator.

B. Experimental Results

The Vernier architecture converter performed as expected over the full supply and load ranges, achieving over 68% peak efficiency.

Figs. 16 and 17 show measured efficiency versus load at $V_{\rm in} = 11$ V and $V_{\rm in} = 16$ V, respectively. When an unregulated

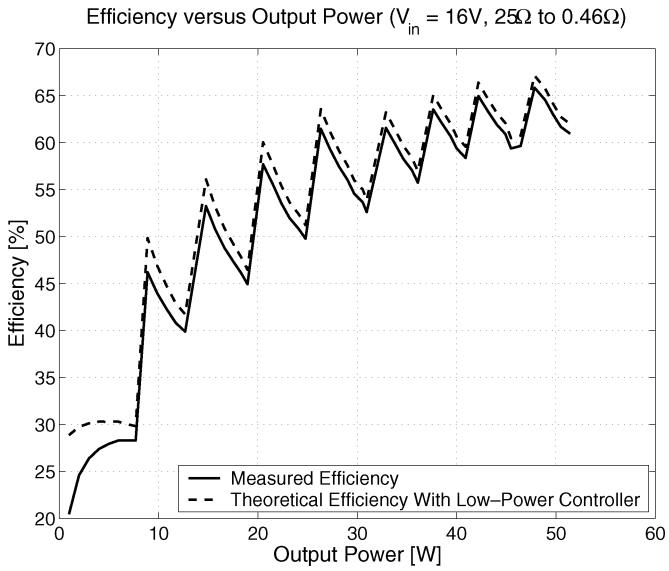

Fig. 17. Efficiency versus output power of the Vernier-regulated system for $V_{\rm in} = 16$ V, 25 $\Omega \geq R_{\rm load} \geq 0.46$ Ω. The theoretical efficiency expected under the same conditions when utilizing a low-power control circuit in place of the tested implementation is also shown.

cell is switched on, power processing shifts from the low-efficiency regulating cell to the high-efficiency unregulated cell. This causes a sudden jump in converter efficiency, resulting in the sawtooth pattern apparent in both figures.

The hysteretic nature of the control strategy employed in this converter gives rise to the possibility of two distinct operating configurations for the same load condition. In the experiment of Fig. 16, the load was swept from nearly zero to maximum and then back. During the upward sweep, cell activation lagged the increasing load, resulting in the utilization of only the minimum number of cells necessary to power the load. On the downward sweep, cell deactivation lagged the changing load; as a result, during some portions of the downward sweep more power was processed by the high-efficiency unregulated cells than during the upward sweep.

Conversion efficiency suffers at light load because of the power drawn by the controller. In this prototype converter, the control circuitry draws 80 mA of quiescent current from the supply, resulting in substantial loss, especially under light load conditions. Fig. 17 shows the theoretical efficiency impact of an implementation utilizing a low-power controller. Such a controller could be readily implemented through a variety of means.

Static line regulation was measured at 25 W across the supply range of the converter; over this range the output voltage varied by 75 mV, or less than 1.5%. Static load regulation was better than 0.8% at $V_{\rm in} = 11$ V and 2.4% at $V_{\rm in} = 16$ V. Measured output voltage ripple was less than 200 mV at $V_{\rm in} = 11$ V, $R_{\rm load} = 1$ Ω and less than 300 mV at $V_{\rm in} = 16$ V, $R_{\rm load} = 0.46$ Ω.

Dynamic performance is illustrated in Fig. 18. At $V_{\rm in} = 11$ V, the load was stepped from 1000 Ω to 3 Ω, resulting in the activation of the first three unregulated cells. The delay between cell activations is determined by the controller clock frequency, 10 kHz.

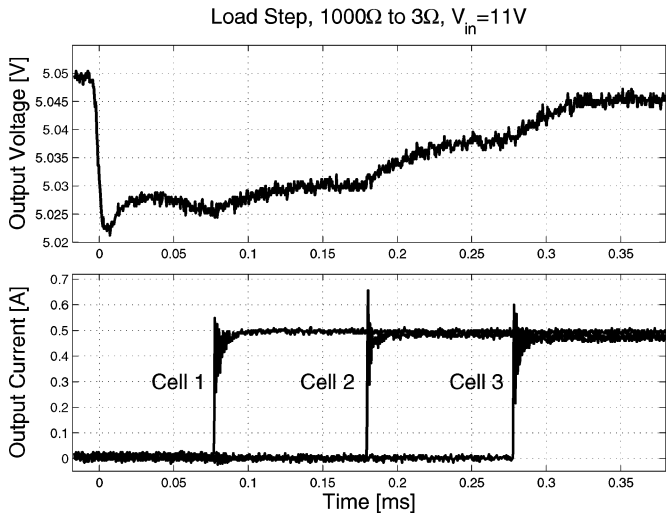

Fig. 18. Dynamic performance of the Vernier-regulated converter with $V_{\rm in} = 11$ V under a load step from 1000 Ω to 3 Ω.

In order to better match the power throughput of the unregulated cells, three of the eight cells were minimally trimmed to compensate for component variation. At maximum load with $V_{\rm in} = 16$ V, individual cell output currents were matched to within $\pm 6.5\%$ of average. This is certainly sufficient for practical purposes, and it is expected that with tighter component tolerances or more extensive trimming much better load sharing is possible.

VI. Cell-Modulation-Regulated System

This section provides experimental verification of the architecture described in Section III-B. In the prototype developed here, a single 100 MHz dc–dc cell is modulated, through its on/off control input, with a hysteretic controller which keeps the output voltage within predefined boundaries. Thus, the cell operates at an output voltage at which its efficiency is maximized. For our particular experimental implementation the hysteresis is implemented using a simple voltage comparator (LM311), and limits the voltage swing to be between 5.0 and 5.2 V. The unregulated cell is provided with an output capacitance of 16.5 μF (formed by 5 3.3 μF Tantalum capacitors in parallel).

In order to reduce the size of the capacitor needed at the output of the system, an improved self oscillating gate drive circuit was utilized. The modified self oscillating gate drive with on/off control is shown in Fig. 22. This implementation achieves faster cell turn on than the circuit described in Section IV-B and enables activation/deactivation (modulation frequency) rates in excess of 70 kHz to be obtained.

Fig. 19 shows the transient response of the time-domain architecture when a step change in the load is applied. In particular, the step change takes the converter from almost no load to half the rated output power (27 Ω to 13.5 Ω, $V_{\rm in} = 16$ V). Under such a step change, the output voltage remains within the predefined limits. The same figure shows that the input current pulsates with a frequency depending on the input voltage, the output capacitance, and load, and that it rapidly reaches steady state conditions.

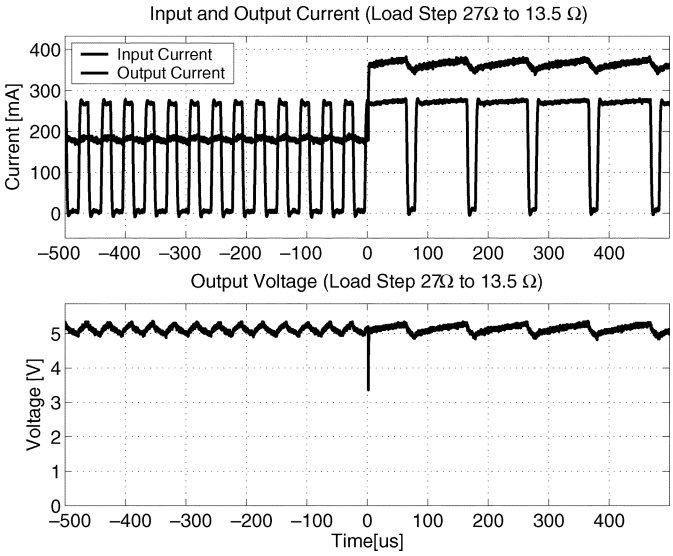

Fig. 19. Transient behavior of the cell-modulation-regulated system under a step change in load (27 Ω to 13.5 Ω, $V_{\rm in} = 16$ V).

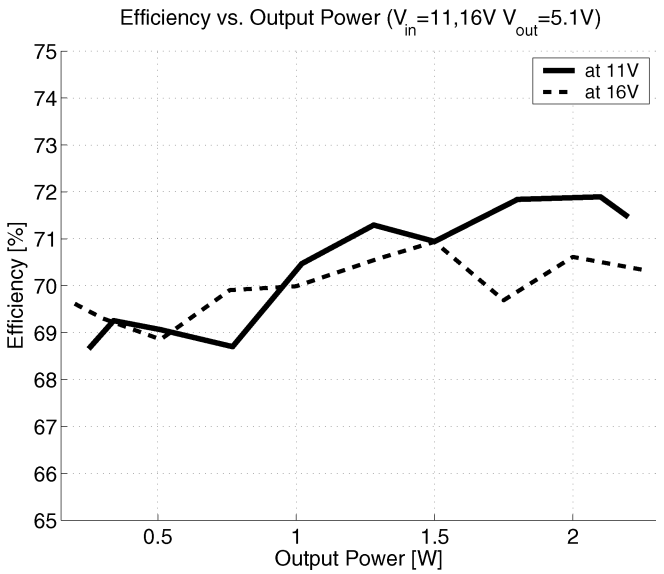

Fig. 20. Efficiency versus output power of the cell-modulation-regulated system at $V_{\rm in} = 11$ V and 16 V.

The performance of the architecture is shown in Figs. 20 and 21. Fig. 20 shows the efficiency plotted as a function of the output power and Fig. 21 the efficiency plotted as function of the input voltage. Both figures demonstrate that the overall efficiency of the system is high over the entire input voltage range and across the output power range.

As can be seen from the prototype system and results, the high cell switching frequency allows reduction in the power stage component sizes. However, the frequency of the input and output waveforms depends on the time modulation of the cell, and have much lower frequency content. Nevertheless, it is anticipated that the use of higher operating frequencies permitted by this architecture (e.g., to >1 GHz), the use of more cells, and design and control of cells for more rapid startup and shutdown will together enable substantial improvements in the input and output ripple performance of this architecture.

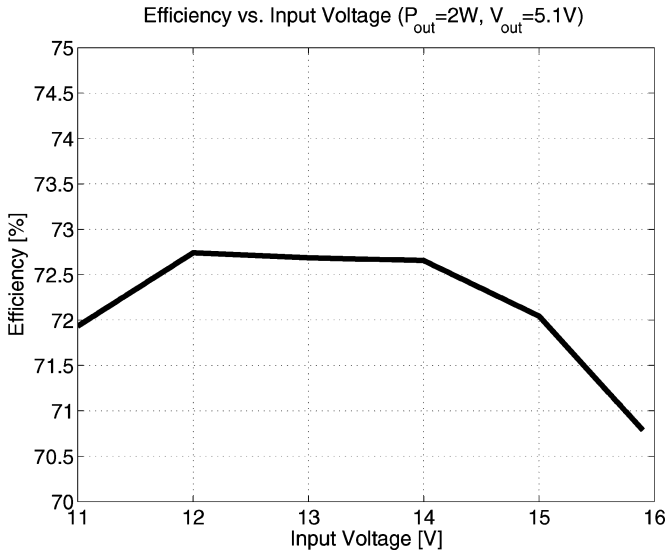

Fig. 21. Efficiency versus input voltage of the cell-modulation-regulated system at $P_{\rm out} = 2$ W.

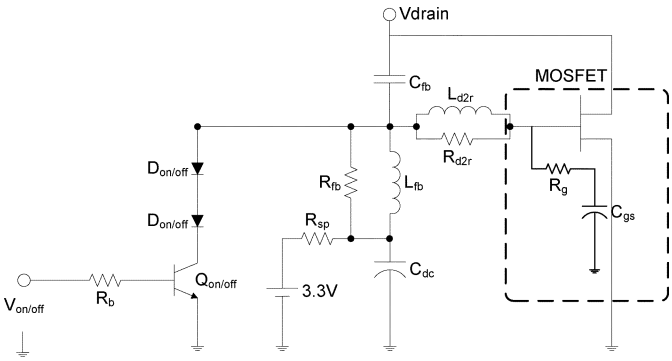

Fig. 22. Improved self oscillating gate driver with fast on/off control.

VII. Future Directions and Emerging Opportunities

The RF power converter cell design of Section IV, as applied in the architectures of the previous two sections, demonstrates the feasibility of power converters operating at very high frequencies. The dramatic reduction in passive component values and the elimination of magnetic materials also points toward the possibility of greatly increased integration (e.g., integration of the passive components as part of the printed circuit board). Nevertheless, the cell power density (∼0.5 W/cm^3) and efficiency (∼77%) of this first prototype are low compared to many conventional designs[2]. In this section we outline circuit design strategies and emerging device technologies that greatly increase the achievable power density and efficiency of RF power converters, and which will enable the benefits of the architectures described here to be more fully exploited.

A. RF Circuit Topologies

The design strategy described in this paper takes advantage of circuit topologies and techniques employed in RF PAs. While power density and efficiency are important concerns in RF PAs,

[2]Partly this is because maximizing power density and efficiency was not a focus in our first-pass design. We have subsequently developed very high frequency converters based on similar principles that provide far higher performance [48]–[50].

they are often secondary to other considerations (e.g., linearity and spectral purity). Consequently, there is substantial opportunity for developing improved RF circuits that are much better adapted to the demands of switching power electronics. Here we point out two circuit design techniques – waveshaping and parasitic absorption – that can lead to greatly improved power density and efficiency in RF power converters.

The class E inverter selected for the prototype system has many desirable attributes: it provides soft switching, is tolerant of slow gate-drive waveforms, requires only a single, ground-referenced switch, and its design is very well understood. One limitation of this topology is its very high device stresses. The waveforms of the class E inverter are treated in [15], [46], [51], and [52, Ch. 15], and reveal a peak switch voltage V_{sw} of approximately 3.6 times the dc input voltage and a peak switch current I_{sw} of approximately 1.7 times the magnitude of the ac load current. To compare the stresses of the class E inverter to other topologies, consider the per-switch stress factor PSSF, defined as

$$PSSF = \frac{V_{sw} I_{sw}}{P_{o,sw}}$$

where $P_{o,sw}$ is the output power per switch of the inverter. (This definition is the same as the stress factor defined in [1, Ch. 6] and the inverse of the normalized power handling capability defined in [52] and [53], except that we normalize to the power per switch, to better capture the limits of multiswitch topologies.) With reference to [51]–[53], the class E inverter has a PSSF $\approx$10.2, which is substantially higher than that of the class D resonant inverter, which has a PSSF $\approx$6.25.

Clearly, the power density and efficiency of the systems proposed here would benefit from RF topologies having lower device stresses. One route toward realizing such improvements is waveshaping. By designing the RF power stages with additional resonant tunings at harmonics of the fundamental, the converter waveforms can be shaped for lower stress. For example, the class F inverter [44], [52, Ch. 15], [54, Ch. 5] and its variants [45], [53] incorporate one or more additional resonances to shape the switch voltage to approximate a square wave ($V_{sw} \approx 2V_{\rm in}$), yielding a single-switch topology with a reduced PSSF $\approx$6.25 (approximately 39% below a class E inverter, and matching that of a class D inverter). The necessary multiresonant networks can be realized using lumped elements, transmission lines, or integrated LC elements [44], [45], [52, Ch. 15], [53]. The dual strategy of reshaping switch current via the resonant network is also effective for improving efficiency and power density (e.g., as accomplished in the class F^{-1} and related topologies [43], [52, Ch. 15], [55]), and there is good reason to expect that shaping both voltage and current together will be even more beneficial. Note that while achieving high efficiency with such multiresonant topologies constrains inverter operation (e.g., to fixed duty ratio and frequency), the system architectures introduced in this paper are not hampered by these constraints, as regulation is achieved through other means. We thus conclude that designs incorporating waveshaping can offer substantial improvements in performance over that demonstrated in our first prototype system.

A further means to improving efficiency and power density is through absorption of the device parasitic capacitance. While the class E topology incorporates the device capacitance as part of the resonant network (C in Fig. 5), output power is proportional to both this capacitance and to the switching frequency [51]. Consequently, for a given semiconductor device there is an upper bound on switching frequency before inverter output power – and the corresponding switch conduction losses – become too high and cause unacceptable reductions in efficiency. This coupling between device capacitance, minimum output power, and conduction loss is a limitation of the class E topology. However, some of the multiresonant topologies described above can absorb device capacitance into the network in a manner that partly decouples device capacitance from output power [43], [44]. Absorbing the parasitic capacitance in this manner allows the use of increased switching frequencies (improving power density) and/or device sizes (improving efficiency) as compared to a class E converter. Based on these considerations, it is reasonable to expect that substantial improvements in performance can be achieved by better exploiting existing RF circuit topologies and techniques. Moreover, it is apparent that there exists substantial opportunity to develop new RF circuits that are better adapted to the demands of switching power electronics, yielding further improvements in performance.

B. Devices

The attainable performance of RF power converters is also advancing quickly due to the ongoing development of improved RF power semiconductor devices. The demands of the communications sector are driving rapid improvements in RF power devices. Here we illustrate some of these ongoing developments, and describe how they impact the circuit architectures described above.

There is a close tie between the attainable performance of a RF power converter and the characteristics of its power semiconductor device(s). For example, consider the performance of a class E inverter based on a Lateral Diffused MOSFET (e.g., as utilized in the prototype system described here). If the operating frequency f is sufficiently high that the device output capacitance C_{oss} forms the entire shunt resonant capacitor (C in Fig. 5), the inverter power is approximately proportional to f and C_{oss} (optimally evaluated at the dc input voltage) [48], [51], [56]. With resonant gating, loss for this device type is heavily dominated by conduction loss[3], which is proportional to the on-state resistance $R_{ds-\rm on}$. Using these facts and following through the calculations developed in [48], [51], and [56], it can be shown that device dissipation normalized to inverter power is approximately proportional to $R_{ds-\rm on} \cdot C_{oss} \cdot f$. Thus, the product $R_{ds-\rm on} \cdot C_{oss}$ is a good measure of device performance in this circuit: a device with a lower figure of merit $R_{ds-\rm on} \cdot C_{oss}$ provides a proportionately lower device loss as a fraction of total power (yielding higher efficiency), or enables a proportionate reduction in switching period at constant loss (yielding higher frequency and power density).

Table II shows a number of recent LDMOS devices in the 65-V/70-V category (as used in the converter of Section IV)

[3]In many vertical MOSFETs, by contrast, gating loss can be a major loss mechanism even with resonant gating, making analysis somewhat more complicated [56]. Other device types can likewise have different loss considerations than the LDMOS devices considered here.

TABLE II
SOME COMMERCIAL 65-V/70-V LATERAL DIFFUSED MOSFETS AND THEIR FIGURES OF MERIT. NOTE: BECAUSE SOME OF THESE DEVICES ARE INTENDED FOR USE IN INEFFICIENT AMPLIFIER CLASSES, THEY ARE SOMETIMES PROVIDED IN RATHER UNWIELDY PACKAGES. ALSO SOME RECENT DEVICES REQUIRE MORE SOPHISTICATED GATE DRIVERS FOR SWITCHED-MODE OPERATION, SUCH AS THE MULTIRESONANT DRIVER USED IN [50]

Device	$R_{ds-on}{\cdot}C_{oss}$ ($\Omega{\cdot}$pF)
STMicroelectronicsPD57018	15.1
CreeUPF1030P	7.8
CreeUPF1010P	7.7
FreescaleMRF373ALSR1	6.7
FreescaleMRF6S9125NR1	5.0
CreeUGF9085P	4.3
FreescaleMRF6S9060NR1	4
AgereAGR09030GUM	3.9
AgereAGR09180EF	2.8

along with the figure of merit for each device. The first device, with a figure of merit of 15.1 $\Omega \cdot$ pF, is a slightly older device (datasheet from early 2003) and is the one utilized in the prototype converter demonstrated here. The remaining devices are more recent (datasheets from 2004 or 2005). As can be seen, devices providing far better figures of merit (up to a factor of 5.4 better) are presently available, indicating that similar designs having far higher power densities and efficiencies are achievable. As an example of this, we subsequently developed a converter similar to the one presented in Section IV (again without an attempt to optimize power density) using the MRF373ALSR1 MOSFET [50]. The design was of similar switching frequency, size, and efficiency, but achieved more than a factor of four increase in output power through the use of a better device (figure of merit better by a factor of 2.25). Clearly, substantial further improvements in performance are possible with presently available devices, even without resorting to improved circuit topologies.

In addition to the rapid evolution of silicon MOSFETs, the communications sector is driving development and application of other materials and device types for RF PAs. For example, GaAs, SiC, AlGaN/GaN, and InGaP material systems are all in use for RF power applications, in field effect (e.g., MOSFET, MESFET, HEMT) and bipolar (e.g., BJT, HBT) devices. (Models for some of these device types can be found in [57, Ch. 3] and references therein.) These devices can often offer improved power gain and efficiency at extreme high frequencies. While it is possible in some cases to adapt these devices to traditional switching power converters [58], their driving requirements and optimization for RF operation makes their use significantly more favorable in the type of architecture proposed here. We thus anticipate that the proposed architectures will continue to benefit from the ongoing advances in microwave semiconductor device technology.

C. Application Areas and Future Development

Reasonable questions regarding the proposed architectures are for what power and voltage ranges and for what applications spaces are these approaches most suitable? While it is too early in the development of these architectures to provide complete answers to these questions, we introduce some current thoughts on these matters here.

While the proposed architectures can be realized effectively with conventional vertical power MOSFETs [48] the use of RF power devices is particularly advantageous. It is thus reasonable to estimate that initial applications of the proposed technology will be at voltage levels for which good RF power devices are commercially available. Widely-used dc bus voltages for RF communications include 7.5, 12.5, 28, and 50 V [59], leading to RF power devices with typical rated blocking voltages of 25, 40, 65/70, and 120/125 V. (For low-power systems, discrete transistors with blocking voltages down to 3 V are available [60].) These devices are largely intended for RF PAs for communications in the VHF band (30–300 MHz) through the UHF band (300 MHz–3 GHz)[4], and can be used with high efficiency in the proposed architectures at typical factors of 3–10 lower in frequency (i. e., to several hundred megahertz.) Similarly, (vertical, metal-gate) RF power MOSFET's intended for high frequency (2–30 MHz) communications and Industrial, Scientific, and Medical (ISM) band applications (e.g., plasma generation) are commercially available. Devices of this type are available with blocking voltages in the range of 200–1000 V (see the device comparison in [53]), and can be used with acceptable efficiency to frequencies beyond 30 MHz [53], [63]–[67]. It may be concluded that the proposed architectures can be applied to applications spanning a wide range of input voltages and power levels. Based on available devices and other design considerations, higher-voltage designs will likely be implemented at lower switching frequencies and higher cell power levels.

We believe there is a wide applications space for the proposed design strategy. It is likely that the proposed approaches will find easier use in applications typically addressed with indirect [1, Ch. 6] converter topologies (e.g., Cúk, SEPIC, buck/boost, Zeta), since these topologies have relatively high stresses, and RF converter cells can easily be designed to convert both up and down in voltage [50]. Likewise, achieving isolation is relatively straightforward in typical RF topologies due to their use of high-frequency intermediate waveforms, so applications requiring isolation may be well matched to these architectures. One present application area of interest to the authors is dc–dc converters for automotive applications. This is an attractive area due to the high motivation to reduce cost (e.g., by integrating passive components as part of a printed circuit board), and the fact that available devices are well matched to the voltage requirements of automobile electrical systems [68]. It is expected that continued development will further reveal the best applications for the proposed architectures.

VIII. CONCLUSION

This document proposes new architectures for switched-mode dc–dc power conversion. The proposed architectures promise to break the frequency barrier that has until now constrained the design of switched-mode power converters, while preserving features critical in practice, including regulation of the output across a wide load range and high light-load efficiency. This is achieved in part by how the energy conversion

[4]See [61], [62] for a summary of the designation and utilization of the various frequency bands.

and regulation functions are partitioned in these architectures. The structure and control approach of the new architectures are described, along with representative implementation methods. The design and experimental performance of prototype systems with cells operating at 100 MHz are also described. It is anticipated that the proposed approaches will allow significant improvements in the size of switching power converters to be achieved, and, in some cases, to permit their integrated fabrication.

An underlying characteristic of the design approaches presented in this paper is that they structure the energy conversion and regulation functions in manners that are compatible with the effective use of UHF circuit designs and techniques. It is hoped that the recognition of this general strategy will lead to the emergence of additional circuit architectures having similar advantages.

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