Very-High-Frequency Resonant Boost Converters

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***Abstract*—This paper presents a resonant boost topology suitable for very-high-frequency (VHF, 30–300 MHz) dc–dc power conversion. The proposed design features low device voltage stress, high efficiency over a wide load range, and excellent transient performance. Two experimental prototypes have been built and evaluated. One is a 110-MHz, 23-W converter that uses a high-performance RF lateral DMOSFET. The converter achieves higher than 87% efficiency at nominal input and output voltages, and maintains good efficiency down to 5% of full load. The second implementation, aimed toward integration, is a 50-MHz, 17-W converter that uses a transistor from a 50-V integrated power process. In addition, two resonant gate drive schemes suitable for VHF operation are presented, both of which provide rapid startup and low-loss operation. Both converters regulate the output using high-bandwidth, ON–OFF hysteretic control, which enables fast transient response and efficient light-load operation. The low energy storage requirements of the converters allow the use of aircore inductors in both designs, thereby eliminating magnetic core loss and introducing the possibility of easy integration.**

***Index Terms*—Class-E inverter, class-F power amplifier, class-Φ inverter, harmonic peaking, resonant boost converter, resonant dc–dc converter, resonant gate drive, resonant rectifier, self-oscillating gate drive, very-high-frequency (VHF) integrated power converter.**

I. Introduction

THERE is an increasing demand for power electronics having reduced size, weight, and cost, as well as improved dynamic performance. Passive components (inductors and capacitors) typically dominate the size and weight of a power converter. Increased switching frequency leads to a reduction in the required energy storage and permits use of smaller passive components. Furthermore, higher frequency can substantially improve transient performance and control bandwidth. Sufficiently high frequencies permit the use of air-core magnetics, paving the way toward fully integrated power converters. Thus, many benefits can be realized by operating power converters at greatly increased switching frequencies if loss, efficiency, and control challenges can be addressed.

Soft switched resonant dc–dc power converters are able to maintain high efficiency at increased switching frequency. The nature of resonant operation, however, typically imposes high device stresses [1]–[12]. Furthermore, as can be seen in [1]–[3], [6]–[8], and [10], it is often difficult to maintain high efficiency over a wide load range with resonant converters.

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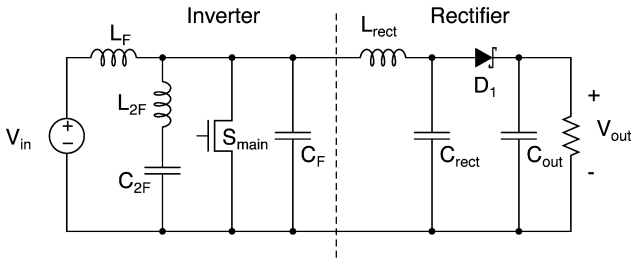

Fig. 1. Schematic of the proposed resonant boost converter topology.

This paper introduces a resonant boost converter topology and control method suitable for designs at VHF, 30–300 MHz. The topology provides low transistor voltage stress, and requires small passive components, allowing for small size and very fast transient response. Moreover, the design maintains high efficiency across a wide load range, from at least 5% to 100% of full load. Section II presents the new topology and discusses its design and operation. Two low-loss resonant gate drive schemes suitable for this topology are detailed in Section III, followed by an explanation of the converter control method in Section IV. Section V presents the design and experimental validation of two converters implementing the approach. The first is a 110-MHz, 23-W converter based on a high-performance RF lateral double-diffused MOSFET (LDMOSFET). The second is a 50-MHz, 17-W design using an LDMOSFET implemented in a 50-V integrated power process.

II. New Resonant Boost Topology

Fig. 1 shows a schematic of the new resonant boost dc–dc converter topology. The design is optimized for low device voltage stress and VHF operation at a fixed frequency and duty ratio. This enables the use of resonant gating and zero-voltage switching for high efficiency. The output is regulated by ON–OFF control of the converter (also sometimes called burst-mode control or cell modulation control [11]–[13]).

The converter can be viewed as a special version of the Class-Φ inverter,[1] described in [14]–[20], coupled with a resonant rectifier, as illustrated in Fig. 1. Here, we treat the design of each of the inverter and the rectifier, and then address their interconnection.

[1]The Class-Φ inverter uses a shorted, quarter-wave transmission line at the input to shape the drain voltage waveform. This reduces the peak voltage stress as compared to other resonant topologies, such as the Class-E converter, and eliminates the need for a "choke" or "bulk" inductor that slows the transient response during ON–OFF control.

A. Inverter

The multiresonant network comprising L_F, L_{2F}, C_F, and C_{2F} is a low-order network designed to approximate the symmetrizing properties of a quarter-wave transmission line [14]–[20]. This network is tuned to achieve zero-voltage switching while simultaneously maintaining low device voltage stress. In particular, the drain to source voltage is shaped to approximate a quasi-square or trapezoidal waveform. This reduces peak voltage stress across the switch $S_{\rm main}$ to as low as two times the input voltage as compared to other single-switch inverters such as the class-E inverter that has a peak voltage stress of 3.6 times the input voltage. To accomplish this, the components L_F, L_{2F}, C_F, and C_{2F} are chosen in the following manner [15], [19], [20].

L_{2F} and C_{2F} are tuned to resonate near the second harmonic of the switching frequency f_s to present a low drain to source impedance at the second harmonic. In addition, the components L_F and C_F are tuned in conjunction with L_{2F} and C_{2F} and the load impedance to present a high drain to source impedance near the fundamental and third harmonic of f_s. The relative impedance between the fundamental and third harmonic can be adjusted to shape the drain to source voltage to approximate a square wave, an effective means to limit the peak switch voltage stress to as low as two times the input voltage [15], [19], [20].

A complete discussion of the tuning methodology for these components is found in [20]. It is worth reiterating here that L_F, L_{2F}, and C_{2F} are all resonant elements, and can be selected relative to the component C_F in a manner that permits the parasitic output capacitance of the switch to be fully absorbed by the multiresonant network. Consequently, C_F can comprise only the parasitic switch capacitance, or if so desired, can be augmented with an additional discrete capacitor in parallel with the switch.

B. Rectifier

The inverter is coupled to a resonant rectifier, as shown in the right-hand side of Fig. 1. This rectifier is similar to that described in [21] and analyzed in [22], albeit with somewhat different operating characteristics owing to our use of ON–OFF control to regulate the output. The substitution of the properly tuned rectifier for the inverter load resistance can be accomplished with minimal effect on the inverter. The pairing is done in a way that allows dc power flow from input to output. Since the fraction of total power that is transferred at dc is subject to much lower loss in the switch or resonant elements than the ac portion, higher efficiency can be achieved as compared to a design that delivers all the power via ac coupling.

The resonant elements $L_{\rm rect}$ and $C_{\rm rect}$ of Fig. 1 are chosen so that the rectifier delivers the desired power at the specified output voltage. In the rectifier topology presented, the parasitic capacitance of the diode is absorbed by $C_{\rm rect}$. The discrete capacitor $C_{\rm rect}$ can, therefore, be reduced, and in some cases, completely eliminated, when all of the required capacitance is provided by the diode. This can be beneficial in avoiding ringing between $C_{\rm rect}$ and the parasitic inductance of the diode package.

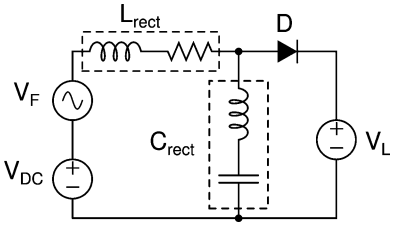

Fig. 2. Schematic of rectifier implemented in SPICE for design purposes. The equivalent series resistance of $L_{\rm rect}$ is included to aid in loss modeling. The equivalent series inductance of $C_{\rm rect}$ is included to capture dynamic behavior.

However, when precise selection of the diode's die area is possible during design, reducing loss may prove an overriding concern. Optimal diode size depends on the distribution of loss between the diode forward drop and the circulating currents in the lossy diode capacitance. Assuming the total capacitance across the diode is to be kept constant, increasing diode area decreases conduction loss, but causes an increasing fraction of the reverse current to be conducted through the diode capacitance. Since $C_{\rm rect}$ will be almost lossless by comparison, scaling the diode area evinces a die size that yields minimum loss.

Rectifier design proceeds by first creating a model for a simulation program such as SPICE. A suitable model is detailed in Fig. 2. While the bulk of the circuit is clearly the right-hand side of Fig. 1, the sources at the input and output are added. At the rectifier input, the two sources model the voltage produced by the inverter, i.e., that across the drain–source terminals of the switch. Under the assumption that nearly all the power is delivered at the fundamental and dc, this voltage can be modeled by a sinusoidal source (with an amplitude equivalent to the fundamental of the inverter drain–source voltage) and a dc offset equal to $V_{\rm IN}$. These sources are designated by V_F and $V_{\rm DC}$, respectively. The source at the output of the rectifier models the load. A constant voltage source is an appropriate representation when the output voltage is regulated by feedback, the intended control scheme for the converter.

To improve the accuracy of the model as regards circuit dynamics and loss, several additional aspects of the main rectifier components are considered. The ESR of $L_{\rm rect}$ is added to better reflect loss, while interwinding capacitance can generally be ignored, as the self-resonant frequencies of the inductors selected are typically a few orders of magnitude above the switching frequency. For $C_{\rm rect}$, ESR may be ignored because the ceramic capacitors used in these prototypes have Q's over 1000 at the switching frequency. Series inductance, however, is of the order of 1 nH, and must be considered for an accurate reflection of rectifier dynamics. Finally, to capture the large-signal dynamic and loss performance of the diode, it is modeled as a forward drop, series resistance, and ideal diode. This is in parallel with a nonlinear capacitance with an ESR that reflects its lossy nature. Diode parameters are determined by measuring the capacitance under various values of reverse bias using an impedance analyzer. The resulting set of small-signal data points is used to create a large-signal model. The forward characteristics of the diode can be measured by any number of techniques. Here, the forward drop was measured for a given drive current and

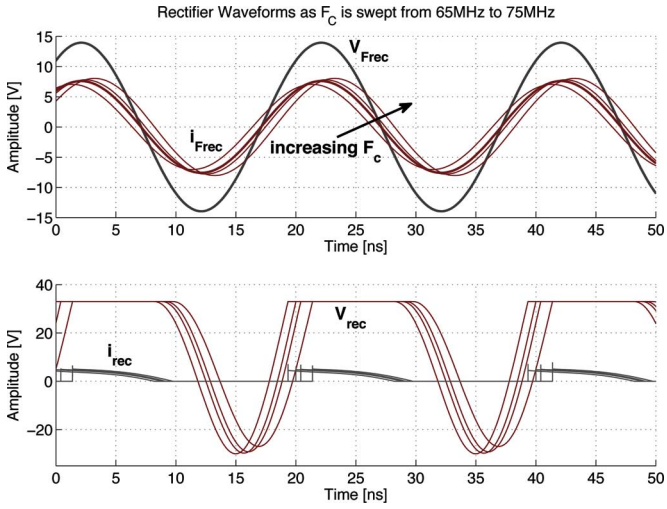

Fig. 3. Top set of curves plot the fundamentals of the voltage and current at the rectifier input port (the bottom curves are the actual voltage and current). As the value of ω_0 is swept, the phase relationship between the voltage and current fundamental changes. At some value, the rectifier can be made to look resistive.

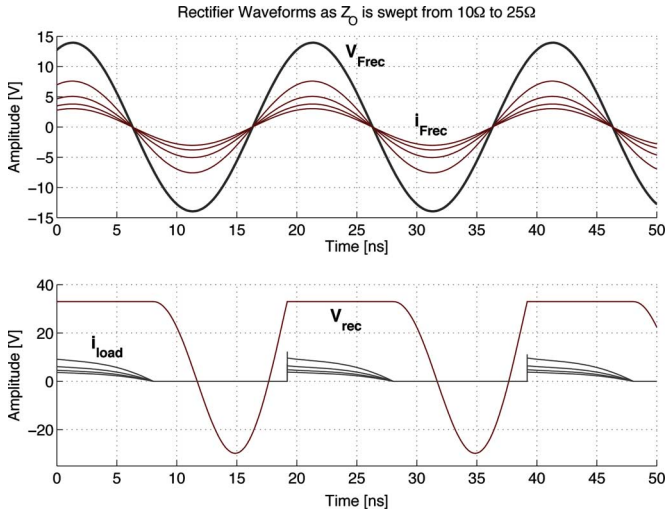

Fig. 4. This same set of curves as in Fig. 3 is plotted here, but ω_0 is held constant while Z_0 is swept. It is evident that the phase relationship between the voltage and current remains nearly constant while the amplitude of the current changes. This changes the equivalent resistance of the rectifier at the fundamental, providing a design handle for converter output power.

junction temperature. A complete SPICE model for the device we used is provided in the Appendix.

With a SPICE model, rectifier design could be accomplished in a trial and error sense by picking values for $L_{\rm rect}$ and $C_{\rm rect}$ that result in the desired output power. However, a more convenient approach to selecting component values is to define an effective center frequency and characteristic impedance. First, the total capacitance in parallel with the diode is defined as $C_{\rm tot} = C_{\rm rect} + C_D$, where C_D is the diode parasitic capacitance. Then, the effective center frequency becomes $\omega_0 = 1/\sqrt{L_{\rm rect}C_{\rm tot}}$ and the characteristic impedance is $Z_0 = \sqrt{L_{\rm rect}/C_{\rm tot}}$. The center frequency, ω_0, is used to establish resistive operation at a given rectifier input and output voltage, and the characteristic impedance Z_0 allows the output power to be set. This formulation is approximately orthogonal over a useful range of characteristic impedance, permitting one to easily tune the rectifier by sweeping ω_0 followed by Z_0. In turn, knowing the desired values of ω_0 and Z_0 readily yields component values for $L_{\rm rect}$ and $C_{\rm rect}$.

Figs. 3 and 4 illustrate the point. Fig. 3 shows simulated rectifier voltage and current waveforms and their fundamentals. As ω_0 is swept, the phase angle between the fundamental current and voltage changes. When this angle is zero, the rectifier looks like a resistor at the switching frequency. Subsequently, sweeping the value of Z_0 in the same rectifier, as in Fig. 4, changes the amplitude of the current, but not the phase angle. This sets the power level while the rectifier continues to appear resistive. The ability to control these parameters independently allows easy design.

Typically, in-phase fundamental rectifier voltage and current corresponds to the best converter operating efficiency. This is not surprising as it minimizes the circulating currents for a given level of output power. Since the phase of the rectifier voltage and current changes as both the converter input voltage and output voltage change, some care must be taken in selecting ω_0. Often the nominal operating point is a good choice. Then, when the converter is operating under its intended load and input voltage, high efficiency is achieved. However, another tuning point may be better to keep the efficiency above a minimum value over the entire operating range. This is easily accomplished by changing ω_0. Any change in power level at the desired operating point can then be compensated with a change in Z_0. It should be noted that finite diode capacitance places a lower bound on the value of $C_{\rm tot}$, limiting both the center frequency and characteristic impedance.

Using the ideas outlined earlier, a rectifier design can be realized fairly quickly. For a given input and output voltage, the values of the sources $V_F, V_{\rm DC}$, and V_L are determined. Using SPICE, ω_0 is swept until the rectifier voltage and current are in phase. Output power is then established by sweeping Z_0. At this point, the rectifier will deliver the rated power into the load when a fundamental voltage of amplitude V_F plus a dc-offset of value $V_{\rm DC}$ appears at its input. This voltage is provided by the inverter.

C. Converter Realization

To design the inverter, the ac and dc portions of the power delivered to the rectifier are treated independently. The inverter needs to deliver the required ac power into an equivalent resistance. This resistance is determined from the fundamental voltage and current at the rectifier input port.[2] Once the inverter design is accomplished, connecting the inverter to the rectifier results in a total power that is typically close to the designed power. Any difference may be adjusted via the methods outlined in [23]. It is also possible to first design the inverter and then

[2]That is, we create a describing function model for the ac impedance presented by the rectifier, which yields the load resistance for the inverter.

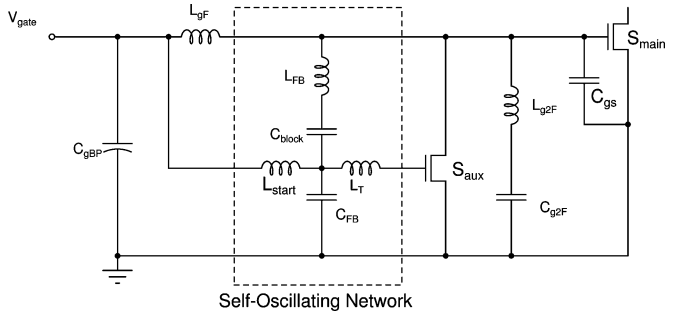

Fig. 5. Trapezoidal resonant gate drive circuit with self-oscillating network. The converter is enabled by applying the voltage $V_{\rm gate}$, and disabled by setting $V_{\rm gate}$ to zero. This gate driver is employed in the 110-MHz converter (Fig. 9).

adjust the rectifier parameters to match the inverter load. The result is a complete dc–dc power stage.

III. Gate Driver

At VHF frequencies, traditional hard-switched gating typically incurs too much loss for acceptable efficiency. Instead, with a power stage and control scheme designed to operate at a fixed frequency and duty ratio, resonant gating is advantageous. By recovering a portion of the gate energy each cycle, much lower power is required to drive the gate, minimizing the effect gating has on overall converter efficiency.

In addition to achieving low-power operation, a practical gate drive must reach steady state rapidly at startup and shutdown to maintain good converter transient response and high efficiency under ON–OFF modulation. To that end, two different low-loss gate drivers were designed, one for optimum efficiency and one for easier integration.

In the case of the 110-MHz converter, the gate terminal of the switch cannot be driven below the source due to a protection diode integrated with the switch. For this reason, a scheme similar to that presented in [12] was developed. This gate drive realizes a trapezoidal gate voltage waveform that does not drive the gate source voltage negative, and which yields near-minimum loss. The design here, depicted in Fig. 5, utilizes fewer parts and achieves a faster startup time than the design in [12]. It is based on the inverter presented in Section II, and uses a low-order lumped network to shape the main-switch gate voltage to be approximately trapezoidal. Added components provide a gate signal to the auxiliary MOSFET, $S_{\rm aux}$, such that a self-sustained oscillation is achieved. The inductor $L_{\rm start}$ helps to initiate this oscillation when the voltage $V_{\rm gate}$ is applied. Component values for this gate driver are presented in Table I.

Holding integration as a goal demands a less complicated gate drive scheme for the 50-MHz converter. A straight totem-pole driver is still too inefficient for this application, so only resonant schemes were considered. Perhaps, the simplest resonant scheme available includes a single series resonant inductor placed between a totem pole driver and the gate. This is a sinusoidal resonant gate drive. However, efficiency remains a problem with this scheme. Since all of the resonating current must pass through the totem pole driver, the output resistance of the driver is important. In this case, one can model the gate

TABLE I
Gate Drive Component Values

50 MHz Design		110 MHz Design	
R_T	2.5 kΩ	L_{gF}	5.5 nH
C_T	15 pF	L_{start}	13 nH
C_B C_P	100 nF	L_{FB}	82 nH
L_S	56 nH	C_{FB}	56 pF
L_P	47 nH	C_{block}	100 pF
R_1	100 kΩ	L_T	68 nH
Q_1	FDV303N	L_{g2F}	3.8 nH
D_1	MA27D27	C_{g2F}	139 pF
Inverter	NC7WZ04	S_{aux}	Polyfet L8821P
		C_{gBP}	5.6 nF

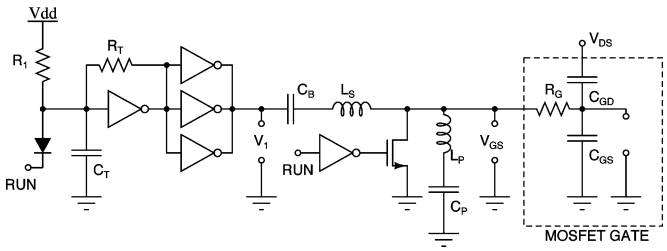

Fig. 6. Sinusoidal resonant gate drive circuit. This driver is employed in the 50-MHz converter (Fig. 19).

loss as $P_{\rm gate} = (\pi C_{\rm ISS} V_{\rm ac} f_{\rm SW})^2 (R_G + R_I)$, where R_I is the output resistance of the totem pole driver, R_G is the gate resistance, $C_{\rm ISS}$ is the gate capacitance, $V_{\rm ac}$ is the ac amplitude at the gate, and $f_{\rm SW}$ is the switching frequency. Since the totem pole devices must be small to keep their gating loss to a minimum, R_I tends to be several times larger than R_G and the total loss of this simple resonant scheme quickly exceeds that of the hard gating case.

This problem is addressed by adding a shunt leg to the basic resonant tank, as depicted in Fig. 6. The approach is similar to that in [24] and [25], though different in how the network is tuned. The shunt leg, comprising L_P and the blocking capacitor C_P, carries a portion of the resonating current, reducing the loss in the inverter bank. L_P is chosen to be resonant with $C_{\rm ISS}$ below $f_{\rm SW}$, effectively reducing the equivalent gate capacitance. L_S and C_B form the series leg, setting the transfer function from the inverter bank to the gate.

While there are many values of L_S and L_P that result in a functioning gate drive, a number of constraints define a smaller locus of useful values. First, the inverter to gate transfer function, $V_{\rm GS}/V_1$, can have a gain larger than unity. This allows the inverter bank supply voltage to be reduced, in turn, reducing loss. However, tuning the network to maximize $V_{\rm GS}/V_1$ does not result in the best efficiency. Instead, as the value of L_S starts to become smaller than L_P, an increased fraction of resonating current reaches the inverter bank. The additional loss (caused by dissipation in the inverter bank output resistance) eventually swamps improvements made by reducing the inverter bank supply voltage. On the other hand, if L_S becomes too large relative to L_P, then the inverter bank cannot effectively control the voltage, $V_{\rm GS}$, and the drain to gate transfer function $V_{\rm GS}/V_{\rm DS}$ dominates. This can cause the converter to self-oscillate at a frequency other than intended, or it may make the converter

difficult to turn OFF. A pull down switch was added to avoid the latter problem, but care is still required to ensure the inverter bank has good authority over the gate voltage. The gate drive startup time is also affected by component choice. As L_S becomes larger, startup tends to extend, which makes it harder to modulate the converter ON and OFF rapidly.

In order to find a good choice for L_P and L_S, a MATLAB script was created to calculate losses in the gate drive. The script finds the branch currents for a given set of inductors and then returns the losses based on the inductor Q, gate resistance, and inverter bank output resistance. This results in several sets of inductor values (e.g., values for L_S and L_P constitute a single set) that have approximately the same loss. From those sets, a single set is chosen that has the best startup characteristics and allows for good control over the gate voltage by the inverter bank. In particular, the inductor sets, where the phase of the transfer function $V_{\rm GS}/V_{\rm DS}$ is closest to 180°, seem to return the best efficiency and startup times. This is interpreted as having $V_{\rm GS}/V_{\rm DS}$ satisfy the phase condition for self-sustained oscillation. Since the magnitude of this transfer function is less than unity, the additional energy for continued oscillation is then supplied by the inverter bank.

The resulting component values are listed in the left half of Table I. R_T and C_T are used in conjunction with an additional CMOS inverter to create a ring oscillator that runs at 50 MHz. R_1 ensures that the oscillator will start consistently while the diode D_1 is used to kill the oscillation, thereby providing a logic-level control input. C_B and C_P are chosen to be ac short circuits at the switching frequency, serving as dc-blocks that allow the gate voltage to be biased. The bias, in turn, establishes the desired duty ratio (a negative bias will reduce the duty ratio, and positive bias does the opposite).

The design power for this gate drive was 204 mW, which is only 40% of the loss expected with hard gating. Actual measurements showed the power loss to be closer to 500 mW, the major culprit being the ring oscillator. Its output was not transitioning rapidly, likely increasing direct path losses in all the CMOS inverters. Driving the inverter bank with a signal generator results in a gate drive power of only 260 mW, including the power to drive the inverter gates. Even with larger than expected power loss, the resonant gate drive is still much better than an equivalent hard gating network, which would use over 800 mW when the gate is driven directly by an inverter bank. The gate drive design presented reaches steady state in just over 74 ns, which is sufficiently fast for this application. Further details about the two gate drives appear in [23] and [26]

IV. Control Strategy

The control strategy employed is an ON–OFF hysteretic control scheme [11]–[13], [25]. When the output voltage falls below a specified threshold, the converter is enabled and delivers power to the output, causing the output voltage to gradually increase. When the output rises above a specified threshold, the converter is disabled, and the output voltage will gradually decrease. Effectively, load power is controlled by changing the duty ratio with which the converter is modulated ON and OFF. Such a strategy is possible at VHF because the minimal energy storage required allows for rapid startup and shutdown of the entire power stage.

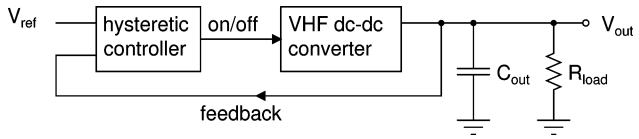

Fig. 7. Block diagram illustrating ON/OFF control of a VHF resonant dc–dc converter. This control strategy enables efficient operation over a wide load range and allows the converter to be optimized for a fixed frequency and duty ratio.

This scheme realizes the advantages of separating the control and power processing functions. When the converter is ON, it operates at a fixed high-efficiency point. When the converter is OFF, many of its loss mechanisms are removed. The result is efficient operation over a much wider load range than can be achieved with many other strategies.

Fig. 7 illustrates this approach. The bulk output capacitance $C_{\rm out}$ is sized to achieve an intended ON–OFF modulation frequency given a load range and the desired ripple voltage. Smaller capacitance will result in higher modulation frequency. Generally, converter efficiency decreases as modulation frequency increases, suggesting a tradeoff between bulk capacitor size and efficiency, though the details are somewhat complicated. It should be noted that the bulk converter input capacitance must also deal with ripple components near the modulation frequency. Nevertheless, the main power stage components are sized based on the very high switching frequency, enabling miniaturization and fast transient response.

The basic scheme presented in Fig. 7 utilizes a hysteretic comparator, a voltage reference to set the dc level, and a voltage divider to sense the output voltage. The ripple voltage is determined by the comparator and is equal to the hysteresis band times the divider ratio. Bulk capacitance is added at the output and sized according to the desired modulation frequency range and expected load. It is important to note that the transient performance of the converter is not determined by the modulation frequency, but by the delay around the control loop and the (very high) switching frequency of the converter.

V. Experimental Results

This section presents the design and experimental evaluation of two converters of the type proposed here. The first operates at 110 MHz and uses a high-performance RF LDMOSFET, while the second operates at 50 MHz using an LDMOSFET fabricated in an integrated power process.

A. 110-MHz High-Performance Implementation

A dc–dc converter based on the topology introduced in Section II and operated at 110 MHz was built and evaluated [26]. Table II lists the converter specifications. The transistor $S_{\rm main}$ is a commercially available RF MOSFET with good high-frequency characteristics. Warren *et al.* [25] describes a method for evaluating transistors for VHF soft-switching converters,

TABLE II
EXPERIMENTAL DC–DC CONVERTER SPECIFICATIONS

Nominal Input Voltage	14.4 V
Nominal Output Voltage	33 V
Input Voltage Range	8 - 16 V
Output Voltage Range	22 - 34 V
Switching Frequency	110 MHz
Nominal Output Power	23 W
Gate Drive Input Voltage	3.6 V

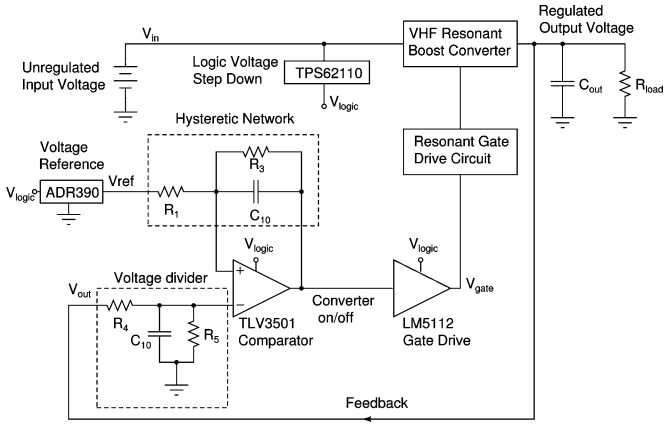

Fig. 8. Schematic drawing of the ON–OFF control circuitry for the 110-MHz converter.

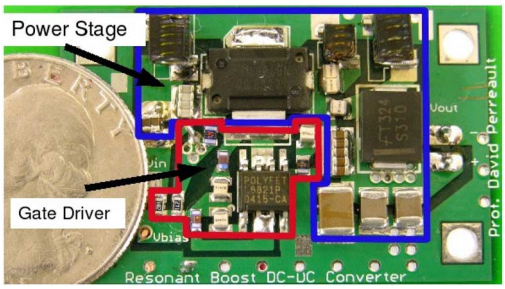

Fig. 9. Photograph of the 110-MHz prototype converter with a U.S. quarter shown for scale.

and [26] contains a detailed analysis of transistor evaluations for the study presented here.

Fig. 8 shows a schematic of the control circuitry implemented for this converter. The hysteretic network comprising R_1, R_3, and C_{10} implements frequency-dependent hysteresis to mitigate problems with the high-frequency content of the output voltage falsely triggering the comparator.

A photograph of the prototype is shown in Fig. 9. The values of the power stage components are given in Table III. Note that the capacitor C_F (as shown in Fig. 1) is provided entirely by the parasitic switch output capacitance, $C_{\rm oss}$. The control circuitry that regulates the output voltage is placed on the other side of the printed circuit board (not shown).

As can be seen in Table III, the largest inductor in the power stage is 33 nH. The small sizes of the inductors are due both to the high operating frequency of the converter (110 MHz), and to the nature of the topology introduced in Section II.

Converter waveforms are presented in Fig. 10, which show measured drain and gate voltages for $V_{\rm in} = 14.4$ V and $V_{\rm out} =$

TABLE III
POWER STAGE COMPONENT VALUES

Component	110-MHz Design	50-MHz Design
L_F	33 nH	22 nH
L_{2F}	12.5 nH	22 nH
L_{rect}	22 nH	56 nH
C_F	0 pF	56 pF
C_{2F}	39 pF	115 pF
C_{rect}	10 pF	47 pF
C_{out}	70 μF	40 μF
S_{main}	Freescale MRF6S9060	Integrated process
D_1	Fairchild S310	Fairchild S310

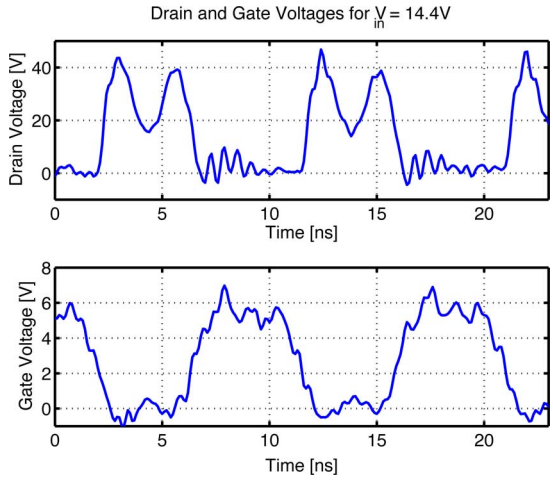

Fig. 10. Drain and gate voltages for experimental 110-MHz converter operating with $V_{\rm in} = 14.4$ V and $V_{\rm out} = 33$ V.

33 V. Switching transitions occur at least close to the zero-voltage ideal, and the peak device voltage stress is acceptable. As will be seen in the following section, peak device voltage stress can be controlled by design and traded off against other characteristics. Open-loop efficiency and power over the input voltage range are illustrated in Fig. 11, where the input voltage is swept from 8 to 16 V, and the output voltage is kept constant at 32 V. This and all following efficiency measurements include the losses of the gate driver and control circuitry, which were powered from the converter input.

Fig. 12 shows the output voltage ripple when the converter is regulating the output at 32.4 V. The approximately 200-mV ripple is set by the hysteresis band of the controller and is independent of the output capacitance of the converter. The modulation frequency at which the converter is turned ON and OFF is set by the load resistance, hysteresis band, and output capacitance, and is 50 kHz in the example of Fig. 12. If a smaller output capacitance is desired, this modulation frequency can be set as high as several hundred kilohertz with no noticeable decline in efficiency, as discussed next. The lower part of the figure shows the drain–source voltage of the main switch, and illustrates how the converter is turned ON and OFF as the output is regulated. It is important to note that while the ON–OFF modulation frequency in Fig. 12 is 50 kHz, the converter itself is switching at 110 MHz when it is turned ON. In the time scale of Fig. 12, this switching frequency is undersampled, but its effect can be seen

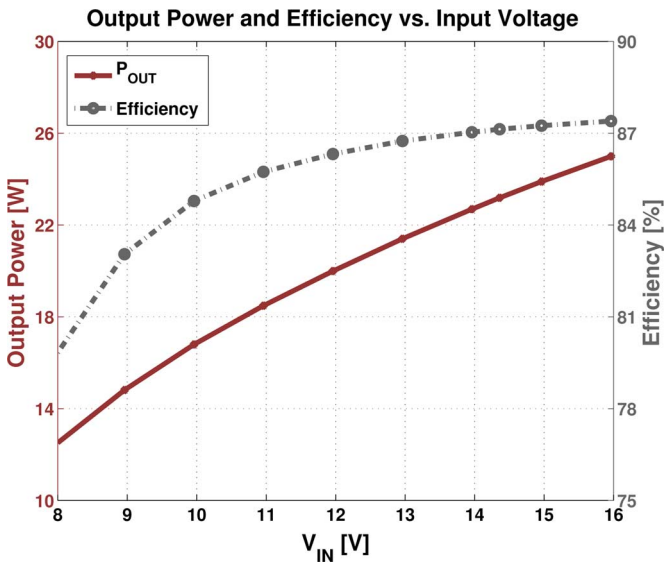

Fig. 11. Open-loop power and efficiency of the 110-MHz converter over the input voltage range, with $V_{\rm out}$ fixed at 32 V.

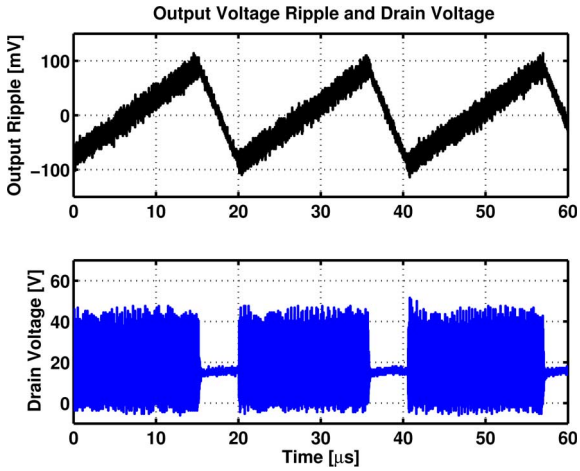

Fig. 12. (Top) Converter output voltage ripple of the 110-MHz converter for $V_{\rm in} = 14.4$ V, $V_{\rm out,dc} = 32.4$ V. (Bottom) Drain voltage illustrating ON–OFF control.

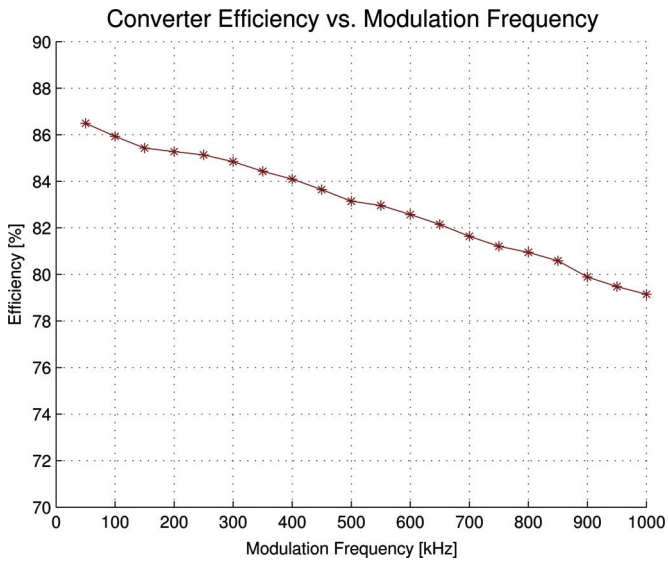

Fig. 13. Converter open-loop efficiency versus modulation frequency for 50% modulation duty ratio. The input voltage is 14.4 V and the output voltage is fixed at 33 V by the electronic load.

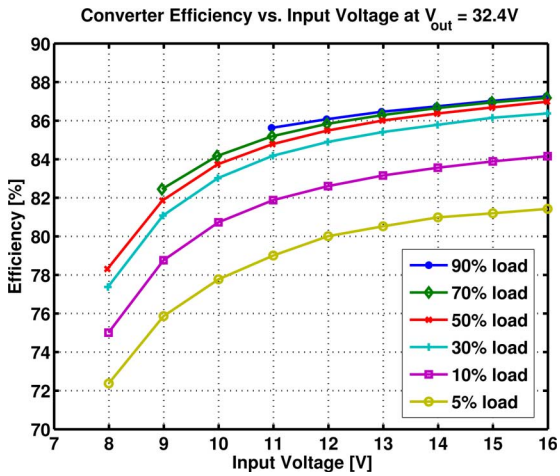

Fig. 14. Closed-loop efficiency of the 110-MHz converter over the input voltage range, parametrized by load. The output voltage is regulated at 32.4 V.

as the "hash" in the rising portion of the output voltage ripple and the drain voltage when the converter is turned ON.

The effect of modulation frequency on converter efficiency is illustrated in Fig. 13, which shows measured converter efficiency versus modulation frequency when the converter is modulated at 50% duty cycle for an input voltage of 14.4 V and an output voltage of 33 V (controlled by an electronic load). As expected, converter efficiency decreases with increasing modulation frequency, since the fixed per-cycle losses associated with startup and shutdown of the converter limit the efficiency at high modulation frequencies.

As Fig. 13 illustrates, the converter can be modulated at substantially higher frequencies than what is chosen for this study (20–100 kHz, depending on load), without a significant impact on overall efficiency. For designs where minimum output capacitance is desired, this tradeoff can greatly reduce the size of the output capacitor at a small efficiency penalty.

An important benefit of the ON–OFF control strategy is the high efficiency at light load. Fig. 14 shows the closed-loop efficiency over the input voltage range, parameterized by load. The converter regulates the output at 32.2 V and the load is varied from 5% to 90% of full load.[3] As Fig. 14 illustrates, the converter exhibits excellent light-load performance, maintaining above 81% efficiency at nominal input voltage all the way down to 5% load. This substantial improvement in light-load operation as compared to typical resonant converters can be attributed to the control strategy used, which turns the converter ON only for very small periods of time at light load. When the converter is turned OFF, it consumes no power, and for the brief time when

[3]For this measurement, full load is defined as the maximum power that the converter can deliver at an input voltage of 11 V, while still regulating the output voltage. Using this definition, 90% of full load corresponds to 16.3 W, and 5% to 0.9 W.

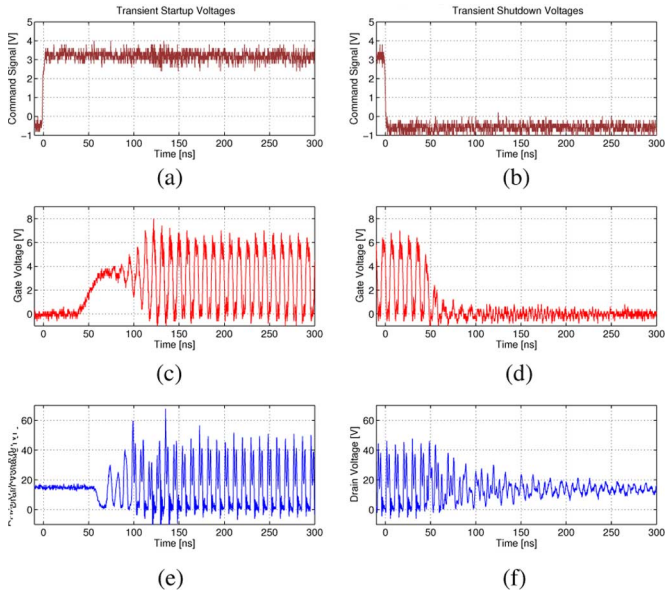

Fig. 15. Waveforms illustrating converter startup and shutdown. Operating conditions: $V_{\rm in} = 14.4$ V, $V_{\rm out} = 33$ V. (a) Startup command signal. (b) Shutdown command signal. (c) Startup gate voltage. (d) Shutdown gate voltage. (e) Startup drain voltage. (f) Shutdown drain voltage.

it is turned ON, it operates in a highly efficient state. There is quiescent loss in the control circuitry along with a small fixed power loss associated with turning the converter ON and OFF, which explains why overall efficiency still decreases with lighter load. As the delivered power is reduced, the fixed ON–OFF power loss becomes a larger fraction of the total output power, thereby reducing efficiency.

The ON/OFF control method used to regulate the output requires that the converter turn ON and OFF quickly. Rapid startup and shutdown improves transient performance, since the converter will be able to quickly respond to a change in load condition, as well as input and output voltage changes. Furthermore, the achievable modulation frequency is determined by the time needed to start up and shut down the converter. If the converter ON/OFF transitions take too long, the modulation frequency will have to be lower to maintain high efficiency. A higher modulation frequency corresponds to lower output capacitance, which is desirable as it will reduce size, weight, and cost of the converter, as well as enable faster transient performance. Fig. 15 shows measured converter waveforms during startup and shutdown. The initial delay between the change in command signal and the change in gate voltage is due to the propagation delay of the National Semiconductor LM5112 driver chip used to provide power to the gate drive. As can be seen from the figure, the converter turns ON in approximately 150 ns, and takes another 100 ns or so to reach steady state, while converter shutdown waveforms show a slightly faster response.

In addition to the size, weight, and cost benefits realized from smaller passive components, an increase in switching frequency also leads to improved transient performance. Because of the small amount of energy stored in the passive components in each switching cycle, the converter can quickly adjust to any changes in load conditions. To illustrate this, Fig. 16 shows the

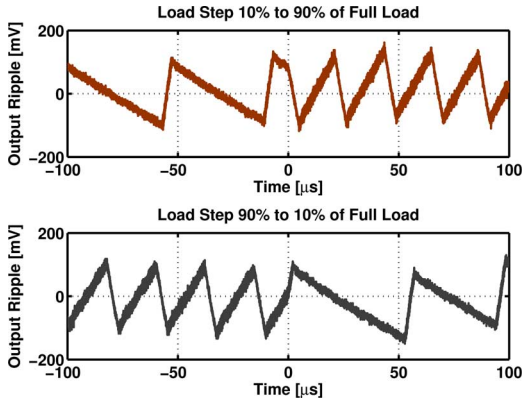

Fig. 16. Output voltage ripple of the 110-MHz converter for load steps between 10% and 90% of full load.

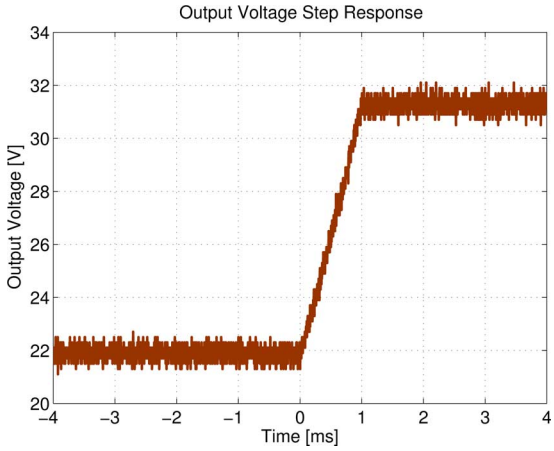

Fig. 17. Output voltage waveform when the regulated voltage was changed from 22 to 32 V (60 Ω load). Because of the small required output capacitance, the converter can quickly change the desired output voltage.

measured output voltage ripple when the load is changed from 10% to 90% of full load (top), and from 90% to 10% of full load (bottom) at time $t = 0$. It can be seen from this figure that there is an instantaneous response to the load-step transient, without any voltage deviation outside the ripple range. This formidable transient response can be attributed to the small inductors and capacitors required for operation at 110 MHz. In addition, transient performance is improved by the resonant topology introduced in Section II, which uses only small-valued resonant passive components.

In conventional dc–dc converters, the total required output capacitance is determined by the allowed voltage ripple and the desired transient performance. It is often the latter requirement that determines the minimum capacitance, calling for a larger capacitance than what output ripple requirements alone would require. The VHF resonant boost converter, with its inherently fast transient response, does not have this problem. The output capacitor is sized solely based on the desired ON–OFF modulation frequency and output ripple, not by transient response limitations.

Fig. 17 illustrates an additional advantage of having the output capacitor sized in this manner. The figure shows the measured response of the output voltage to a step change in regulation

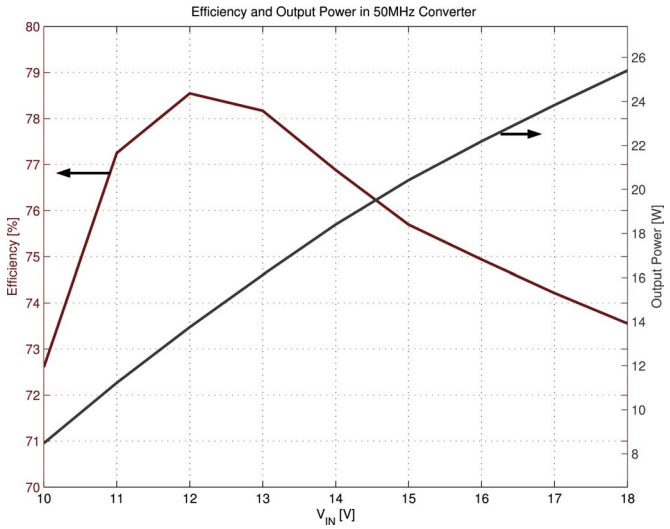

Fig. 18. Open-loop power and efficiency versus input voltage of the 50-MHz power stage for a fixed output voltage of 32 V.

voltage. In this case, the regulated output voltage was changed from 22 V to 32 V at time 0 (for a 60 Ω load), and as seen in the figure, the output voltage settles to the new value in approximately 1 ms. The slew rate of the output voltage is dependent on load, with the output voltage rising faster for a light load when the regulated output voltage is increased. Similarly, the slew rate for a command to decrease the regulated output voltage is higher for a heavy load, since the only means for removing the charge on the output capacitor is through the load resistance. It is important to realize that—for a given load—the slew rate is inversely proportional to the size of the output capacitor, which can be quite large in a conventional dc–dc converter. The proposed converter, with its small output capacitance, therefore offers an advantage in applications that require the regulated output voltage to change rapidly.

B. 50-MHz Integrated Power Process Implementation

The VHF operation of the converter described here lends itself to the possibility of integration. With this in mind, a converter was built where the main switch was fabricated in a 50-V integrated power process and the other components were discrete. The device was not optimized for RF operation or, otherwise, customized. Instead, the goal was to determine the feasibility of implementing the design in conventional power processes thereby avoiding the cost of a custom RF process. The converter was designed for an 8–18 V input range, a 22–33 V output range, and had a 17-W output power rating at the nominal input voltage of 14.4 V. Fig. 18 shows (open loop) power and efficiency versus input voltage for an output voltage of 32 V. The switching frequency was 50 MHz, which held the largest inductor value to 56 nH (a complete list of component values appears in Table III). The small-valued, air-core passive components are promising candidates to be either copackaged with a switch/controller IC or perhaps realized on-die. Fig. 19 shows a photograph of the 50-MHz converter.

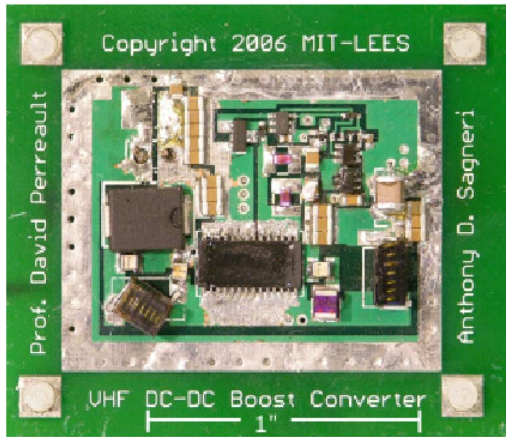

Fig. 19. Photograph of the 50-MHz resonant boost converter prototype.

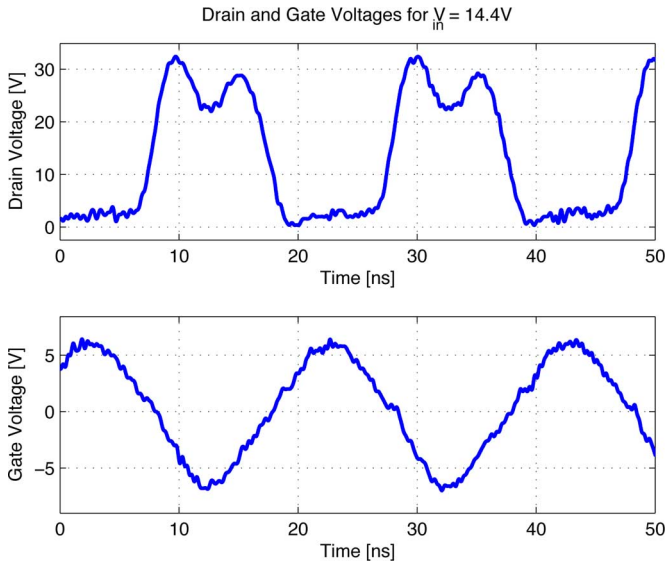

Fig. 20. Drain and gate voltages for experimental 50-MHz converter operating with $V_{\rm in} = 14.4$ V and $V_{\rm out} = 32$ V.

Fig. 20 shows the device drain and gate waveforms of the 50-MHz converter. The ability to tune the resonant boost converter to minimize peak switch voltage stress was a key factor enabling the use of the 50-V power process. The peak $V_{\rm DS}$ across the switch was 42 V at 18 V input ($< 2.4\ V_{\rm in}$). This is in contrast to the 65-V peak a class-E converter would suffer—well beyond the nominal 50-V process limit.

Careful study of the gate and drain voltage waveforms for the operating conditions shown in Fig. 20 suggests that the turn-ON transition begins when the drain voltage is below 5 V and the subsequent turn-OFF transition completes by the time the drain–source voltage reaches 5 V. This leads to small overlap and discharge switching loss.

At the nominal input voltage, the converter was better than 74% efficient over a load range from 4 to 17 W under closed-loop operation. A significant fraction of the increased loss over the high-performance design is related to the integrated device. Its gate-drive figure of merit ($R_{\rm gate} \cdot C_{\rm gate}^2$) is nearly 80-fold poorer than the RF device. Similarly a larger $C_{\rm OSS}$ and its greater

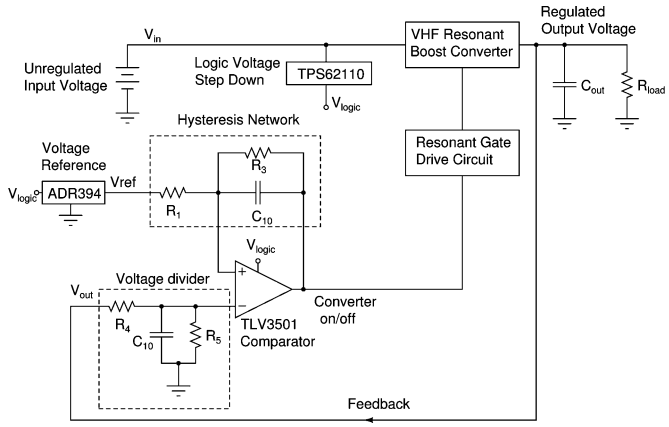

Fig. 21. Details of the ON–OFF control circuitry for the 50-MHz converter.

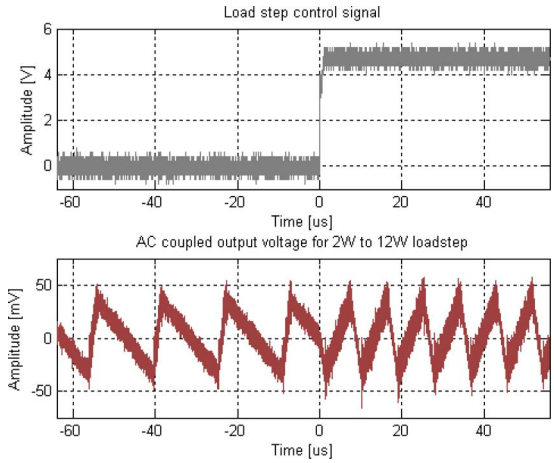

Fig. 22. Transient performance of the 50-MHz converter when the load is stepped from 2 to 12 W. The converter output remains within the ripple band.

TABLE IV
50-MHz ON–OFF CONTROL COMPONENT VALUES

Comparator	Texas Instruments TLV3501
Voltage Reference	Analog Devices ADR394
Synchronous Buck	Texas Instruments TPS62110
R1	300Ω
R3	$220k\Omega$
R4	$10.5k\Omega$
R5	$1.5k\Omega$
C10	$12pF$

equivalent series resistance contributes to increased device loss along with higher conduction loss owing to the somewhat larger 210 $\mathrm{m}\Omega$ $R_{\mathrm{DS(on)}}$. Since it was not possible to custom-design the device layout on this iteration, there is room for substantial performance enhancement by simple changes in device geometry, such as choosing a more optimum gate finger length. As a minimum, this will reduce gate resistance allowing an increase in operating frequency or greater device area and lower total loss. The detailed efficiency characteristics of the converter are qualitatively similar to those of the 110-MHz converter.

As a consequence of the small energy storage, the transient performance is excellent and the converter can be modulated at 700 kHz with only a 1% loss of efficiency. Under closed-loop operation, the modulation frequency was held to 250 kHz because of a larger than necessary 40-μF bulk capacitance.

This converter has a 100 $\mathrm{m}V_{\mathrm{pp}}$ ripple using the hysteretic voltage mode control scheme described earlier. Fig. 21 shows the detailed schematic with component values listed in Table IV. Load-step performance is excellent. The application of a load step from 2 to 12 W back to 2 W (corresponding to 13.3% load and 80% load) results in a transient response that never leaves the ripple band. That is, under load step, the output voltage is never more than 50 mV away from the reference voltage. This is illustrated in Fig. 22.

Additional detail about this design may be found in [23]. The overall good performance achieved with the integrated transistor is encouraging. Plenty of opportunity exists to optimize the device within the constraints of the process, and perhaps, realize higher efficiency, higher operating frequency, or both.

VI. CONCLUSION

This paper has presented a new resonant topology suitable for boost power conversion. The new topology addresses several shortcomings of previous designs, while maintaining all desirable properties necessary for VHF power conversion, such as zero-voltage switching and absorption of device capacitance.

The paper describes experimental implementations of two resonant boost converters. One is a 110-MHz, 23-W converter using a commercially available LDMOSFET, which achieves efficiency above 87% for nominal input and output voltages. The other is a 50-MHz, 17-W converter using a switch from a standard 50-V integrated power process. Both converters utilize a high-bandwidth control strategy that permits excellent light-load efficiency, something that is typically difficult to implement with resonant converters. In addition to greatly reducing the physical sizes of the passive components, the high operating frequency gives the converters an inherently fast transient response.

As this paper has demonstrated, it is possible to achieve miniaturization and high performance of dc–dc power converters without sacrificing efficiency. The design implementations described in this paper are expected to contribute to the development of VHF dc–dc converters, paving the way for power electronics that can satisfy the needs for improved size, cost, and performance that are demanded by modern applications.

APPENDIX
SPICE MODELS

A. *Diode Model*

```
.subckt diodenl a k
+ params:
+ Lds=1n; Series inductance
+Vdon=0.55; Diode forward drop
+Rds=0.3; Series resistance
+ Cjo=267.77p
+ Vj=0.365
```

```
+ M=0.4204
+ Rc=0.240; Rcout
+ Fs=50Meg

*Parasitic lead inductance
Lds A 101 { Lds} ic=0

*Ideal diode model
Dideal 101 102 dideal
.Model dideal D(N=0.001)

*Forward voltage drop model
Vdon 102 103 {Vdon}
Rds 103 K {Rds}

*Nonlinear capacitance
Gcnl K 104 Value={IF((V(K)-V(104))<0,Cjo*V(201)*
+ (1/Lder),V(201)*(1/Lder)
+*(Cjo/((1+((V(K)-V(104))/Vj))**M)))}
Rc 101 104 {Rc}

*Evaluate the derivative
.Param:
+ Lder=1U; Inductor for derivative circuit
+ Pi=3.14159
.Func Rder(Lder,Fs) {3000*2*Pi*Fs*Lder}

Gy 0 201 Value={V(K)-V(104)}
L1 201 0 {Lder}
R1 201 0 {Rder(Lder,Fs)}
.Ends Diodenl; Fairchild S310
```

B. Transistor Model

```
.Subckt MosfetNlc gate drain source
+ Params:
+ Rdson=0.2
+ Rg=1.7
+ Cgs=246p
+ Rcout=0.6
+ Rshunt=12Meg
+ Cjo=425.2p
+ Vj=0.177
+ M=0.252
+ Ldrain=1n
+ Lsource=200p
+ Lgate=400p
+ Crss=30p
+ Kres=1

Ldrain drain drainl {Ldrain}
Rshunt drainl sourcel {Rshunt}
Lsource sourcel source {Lsource}

Sw drainl sourcel gmain source swideal
.model swideal vswitch(Ron={Kres*Rdson}
+roff=1MEG Von=2.5 Voff=1.5)

*Nonlinear capacitance model
Gcnl N101 drainl value={if((V(drainl)-v(n101))
+<0,Cjo*V(201)*(1/Lder),V(201)*(1/Lder)*
+(Cjo/((Vdrainl)-V(n101))/Vj))**M)))}

Dideal sourcel drainl diode
.model Diode D(N=0.001)

Rcout N101 sourcel {Rcout*Kres}
Lgate gate gatel {Lgate}
Rg gatel gmain {Rg}
Cgs gmain sourcel {Cgs}
Crss drainl gmain {Crss}

*Subcircuit to evaluate the derivative
.Param:
+ Lder=0.01u
+ Pi=3.14159

.Func Rder(Lder,Fs) {100*2*Pi*Fs*Lder}
Gy 0 201 Value={V(N101)-V(drainl)}
L1 201 0 {Lder}
R1 201 0 {Rder(Lder,Fs)}
.EndS MosfetNlc
```

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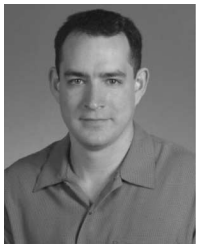

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