

Transistor Selection and Design of a VHF DC-DC Power Converter

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Abstract—This paper explores the design and performance of dc-dc power converters operating in the very high frequency (VHF, 30–300 MHz) range. Methods are presented for assessment and comparison of device losses in VHF operation under soft switching and soft gating conditions. These methods are applied to the development of a 2 W resonant boost converter operating at a switching frequency of 30 MHz. Design of the power stage, resonant gate drive, and control circuitry are treated in detail, and experimental results demonstrating the performance of the converter are presented.

Index Terms—Class E inverter, multiresonant converter, ON-OFF control, resonant converter, resonant gating, zero-voltage switching.

I. INTRODUCTION

THE COST, SIZE, and performance of dc-dc power converters are heavily dependent on the required size of passive components such as inductors and capacitors. The sizes of passive components often dominate over the switching devices and control circuits, constraining power density. Likewise, the achievable converter transient performance (essentially, the rate at which the converter can adapt its operating condition) is limited by the energy stored in the passive components. Because required component values and energy storage decrease as frequency increases [1], there is a motivation to operate switching power converters at as high a frequency as possible commensurate with practical constraints such as efficiency.

Important frequency-dependent device loss mechanisms include switching loss and gating loss. Zero-voltage switching (e.g., [2]–[12]) can be used to mitigate the voltage/current overlap and capacitive discharge losses associated with device switching. Similarly, soft (resonant) gating [3], [13]–[20] can be employed to reduce the loss associated with charging and discharging MOS device gates. Used together, these techniques enable dramatic increases in the achievable switching frequencies of dc-dc converters [3], [16]–[20].

This document explores the design of dc-dc converters operating in the VHF frequency range (30–300 MHz). Section II presents a method for evaluating transistors and selecting operating frequencies for class-E-based power converters employing sinusoidal resonant gating. Section III applies this approach to

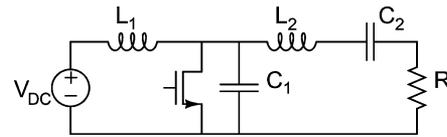


Fig. 1. Class E inverter topology [21], [22]. L_1 is an RF choke, while the remaining components are selected as described in [21], [22]. This topology provides zero voltage switching which allows for high frequency operation.

the design of a resonant boost converter operating at 30 MHz. Design of the power stage, resonant gate drive, and control circuitry are treated in detail. Section IV presents a summary of the experimental evaluation of this converter and a comparison to the performance of a commercially available alternative. It is demonstrated that small size and fast transient performance are achieved with the proposed approach. Finally, Section V concludes the paper.

II. TRANSISTOR EVALUATION

The performance of power converters operating in the VHF range depends greatly on the characteristics of the power semiconductor devices. In this section, methods are introduced for assessment and comparison of MOS devices in VHF operation under soft switching and soft gating conditions. These comparisons are made on the basis of their calculated performance (especially efficiency) in the well-known class E RF inverter topology of Fig. 1 [21], [22]. Device performance in this topology is a useful metric because closed-form expressions are available for it [18], [22], and the underlying loss mechanisms remain the same in other circuit topologies. Performance of a given device will differ in other topologies (and may be considerably better), but the relative performance of different devices is likely to remain unchanged.¹ As such, the following derivations apply specifically to the class E topology of Fig. 1, but it is reasonable to utilize the results for transistor evaluation purposes.

As a basic measure of device merit, device loss is normalized to ideal output power as a function of switching frequency f . The device with the highest frequency capability for a given allowed efficiency penalty may be considered the best device. Normalized device loss may be calculated in terms of device parameters, providing a simple evaluation of device merit as a function of frequency. Alternatively, one may compute the lowest loss device for a given desired power and frequency. This evaluation metric is developed in the following subsections.

¹Note that the detailed loss equations may be different even in other class E topologies [23], [24].

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A. Approximate Class E Operating Characteristics

1) *Output Power*: Starting from the design equations in [22] and neglecting losses, the input or output power of a class E inverter of Fig. 1 with high loaded Q can be approximated as [18]

$$P \approx 19.76 \cdot f \cdot C_1 \cdot V_{dc}^2 \quad (1)$$

where P is power in W, f is switching frequency in Hz, V_{dc} is dc input voltage in V, and C_1 is the total capacitance in parallel with the switch, measured in Farads. Note that C_{oss} of the switching device should be included as part of C_1 , with C_{oss} evaluated at a device voltage of $V_{ds} = V_{dc}$ to best model the effect of the non-linear device capacitance on circuit operation. Since the peak device voltage reaches approximately 3.6 times the dc input voltage, a reasonable approximation is to require a device breakdown voltage (e.g., for a MOSFET) of $V_{ds,max} \geq 4 \cdot V_{dc}$ [22].

A further consequence of the power relation in (1) is that there is a *minimum* achievable output power for a converter using this topology under class E operation at a given frequency, obtained when C_1 comprises only the device output capacitance C_{oss}

$$P_{min} \approx 19.76 \cdot f \cdot V_{dc}^2 \cdot C_{oss}|_{V_{ds}=V_{dc}} \quad (2)$$

For a specified output power and input voltage this translates into a maximum switching frequency guideline f_{max} for a class E design

$$f_{max} \approx \frac{P}{19.76 \cdot V_{dc}^2 \cdot C_{oss}|_{V_{ds}=V_{dc}}} \quad (3)$$

Frequencies higher than f_{max} may be used if the converter power delivered is controlled by means such as adjustment of the input voltage or by cell modulation [25]. However, it is desirable to match the maximum converter output (at the maximum permissible voltage) to the power output specification. For purposes of device to device comparison, fixing an output power and determining f_{max} provides a metric for evaluating switching devices for high frequency applications. A device with a higher f_{max} will allow for reducing the numerical values and sizes of passive components in the class E converter, increasing power density relative to a switching device with a lower f_{max} .

2) *Losses*: The frequency limitations of practical devices depend directly on the loss mechanisms. Because the class E inverter ideally provides zero voltage switching at both transitions, there is no capacitive discharge loss at switch turn ON. Moreover, the voltage/current overlap loss at switch turn OFF can be neglected as it is small compared to other loss components. The dominant losses, considered here, are device conduction loss and gating loss.

For a MOSFET, the device conduction loss normalized to inverter power P above can be approximated as [18], [22]

$$P_{Cond, Norm} \approx 2.363 \cdot \frac{P}{V_{dc}^2} R_{DS, on} \quad (4)$$

where $R_{DS, on}$ is the device on-state resistance in Ω , and the other values are as defined above.²

We consider gating loss for a MOSFET in the case where a sinusoidal current drive is used to charge and discharge the gate (soft gating). This may be realized with a number of resonant drive strategies (see, e.g., [3], [16], [18], and Section III-B), and leads to lower loss levels than hard-switched gating when the required switching time is much longer than the gate time constant ($t_{sw} \gg R_G \cdot C_{iss}$). Power dissipation due to gating loss, normalized to inverter power P , may be computed as

$$P_{Gate, Norm} \approx \frac{2\pi^2 \cdot f^2 \cdot C_{iss}^2 \cdot R_G \cdot V_{G, ac}^2}{P} \quad (5)$$

where C_{iss} is the input capacitance, R_G is the gate resistance, and $V_{G, ac}$ is the magnitude of the sinusoidal voltage swing at the gate (e.g., neglecting Miller effect, with the ac voltage swing being about a desired dc value such as the MOSFET threshold voltage V_{TH} .) $V_{G, ac}$ should be selected large enough to fully enhance the device during the ‘‘on’’ time, without exceeding the gate voltage rating. Note that lower gate drive losses are possible with other waveforms (e.g., ‘‘constant current’’ charge and discharge of the gate, resulting in a trapezoidal gate voltage [19], [20]) but are less simple to realize, and so are not further considered here.

B. Semiconductor Device Evaluation

Here the above operating characteristics are applied to evaluate devices for VHF power conversion. Evaluation is based on computing the fractional power loss $P_{switch, norm}$ introduced by the semiconductor switch in a class E inverter as a function of frequency. For a given allowed fractional loss (e.g., 0.1 for 10% power loss in the transistor) this approach reveals an upper bound on operating frequency for a specific device in a class E converter. When comparing devices, a device having a higher operating frequency limit may be considered more desirable. The switching frequency limit may be significantly higher in other converter topologies, but the relative performance of different devices is likely to remain unchanged.

Two variants of this evaluation procedure are introduced. The first variant is based on selecting an optimal output power for each candidate frequency to maximize efficiency with the specified transistor. This is useful for general transistor evaluation. The second variant is based on evaluating the transistor across frequency for a specified output power level (i.e., to meet a desired application target). This is useful when comparing transistors for a target application.

1) *General Transistor Evaluation*: To evaluate a transistor for VHF operation, consider the total normalized power loss in the transistor

$$P_{Sw, Norm} \approx \underbrace{2.36 \cdot \frac{P}{V_{dc}^2} R_{DS, on}}_{\text{Conduction Loss}} + \underbrace{\frac{2\pi^2 f^2 C_{iss}^2 R_G V_{G, ac}^2}{P}}_{\text{Gating Loss}} \quad (6)$$

²In designs where C_1 is mostly or entirely composed of device capacitance, conduction through the lossy device capacitance may also represent a significant loss mechanism. R_{oss} , the equivalent resistance of the device output capacitance, is shown in Table III for a number of devices.

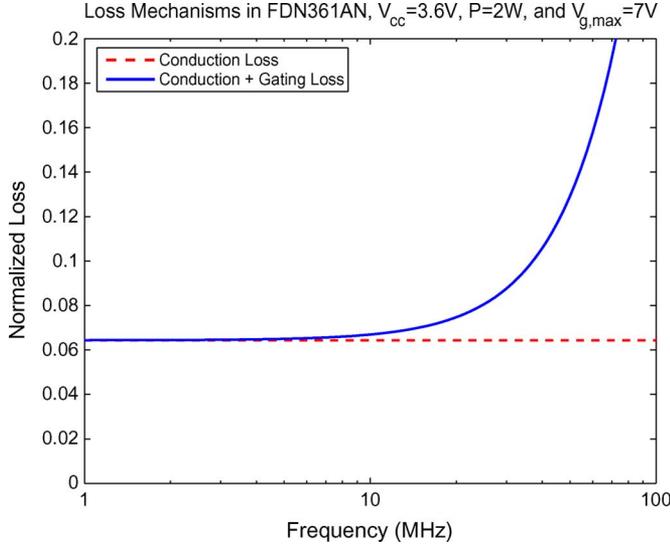


Fig. 2. Normalized device loss for the FDN361AN MOSFET versus frequency for a class E inverter with sinusoidal gate drive. Conduction loss is a constant independent of frequency, providing the base level. Gating loss varies with the square of frequency as in (5), providing the frequency dependence for the normalized device loss.

This is the loss in the transistor (due to gating and conduction) normalized to total system power P .

For a given switching frequency f there is an operating power P_{OPT} (in W) that maximizes efficiency subject to the minimum power constraint of the class E inverter

$$P_{OPT} = \max \left\{ P_{\min}, 2.89 \sqrt{\frac{R_G}{R_{DS,on}}} C_{iss} V_{dc} V_{G,ac} f \right\} \quad (7)$$

in which P_{\min} is calculated as in (2) and $V_{dc} = V_{ds,max}/4$. Plotting $P_{Switch, Norm}$ from (6) where P is selected at P_{OPT} from (7) at each frequency yields the appropriate transistor loss versus frequency curve. This curve shows the minimum loss achievable with the specified transistor (in class E operation) and sinusoidal resonant gate drive as a function of frequency. This result may be considered a lower bound for what is achievable with available VHF converter topologies.

2) *Evaluation for a Target Output Power:* To evaluate a given transistor across frequency for a particular target power level P , one can plot $P_{Switch, Norm}$ from (6) for this power level and a specified input voltage $V_{dc} < V_{ds,max}/4$. This curve can be used to select a maximum permissible operating frequency for class E operation based on allowed loss in the transistor. Note that the allowable operating frequency for this calculation is only for class E operation with sinusoidal gate drive, and is bounded by the limits of (3). As above, this result may be considered a lower bound on the performance achievable across topologies and operating methods.

As an example of this second variant, consider the evaluation of a transistor for application in a 2 W converter with $V_{dc} = 3.6$ V. (6) can be evaluated as a function of frequency for the device in order to determine maximum operating frequency. From device to device, this maximum frequency can be used to rank their relative performance, with the objective of identifying the highest frequency possible. $V_{G,ac}$ must be chosen to

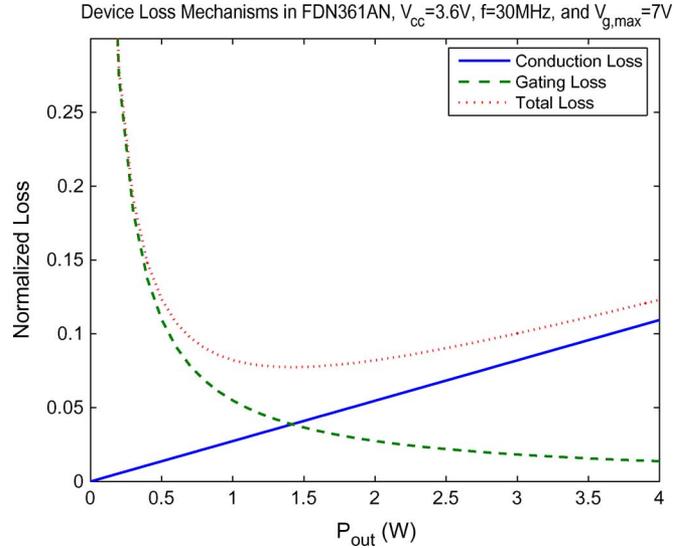


Fig. 3. Normalized device loss for the FDN361AN versus P_{out} for a class E inverter with sinusoidal gate drive. Conduction loss varies linearly with P_{out} as shown in (4). Gating loss is independent of P_{out} , so the normalized gating loss falls with increasing output power.

ensure the device is fully enhanced at turn on. Fig. 2 illustrates the performance of the FDN361AN MOSFET identified by the selection metrics as a good device for high frequency.³ From the chart, an operating frequency of 30 MHz was selected for the converter design described in the following section for a target $P_{Switch, Norm} \leq 10\%$. Fig. 3 illustrates the device loss for a general application at a fixed frequency of 30 MHz as a function of output power. This helps evaluate how close the realized target application is to ideal application for the device at 30 MHz.

III. CONVERTER SPECIFICATION AND DESIGN

A resonant boost converter was designed using the transistor selected in Section II. The converter was designed to meet the following specifications: The input voltage ranges from 3.6 V to 7.2 V, while the output voltage is to be regulated at 7 V. The output power range is from 1 W to 2 W.

The resonant boost converter is based on a soft gated class E inverter combined with a single diode rectifier operating at 30 MHz. This frequency was selected above as the target frequency for $P_{Switch, Norm} \leq 10\%$. The output is regulated using cell modulation control (also called ON-OFF control or burst mode control) [20], [25], [26].

In this control scheme, the converter operates at a fixed switching frequency and duty ratio. To regulate the power delivered to the output, the converter operation is gated ON and OFF over time at a rate that is much slower than the switching frequency. By appropriately modulating the fraction of the time that the converter delivers power (at a modulating frequency far below the switching frequency) the output voltage can be maintained at a desired level.

A significant advantage of this control scheme is that the converter only runs at fixed switching frequency and duty ratio, facilitating implementation of soft switching and soft gating.

³A selected list of commercially available devices deemed suitable for high frequency operation is provided in the Appendix along with some important device parameters.

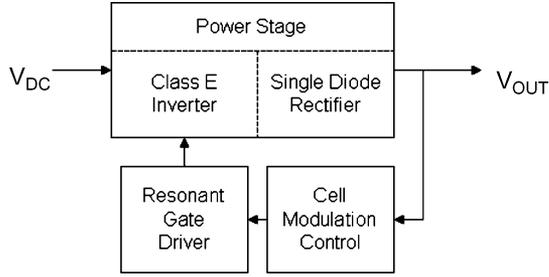


Fig. 4. Block diagram for 2 W dc-dc converter operating at 30 MHz using cell modulation control. The dc-dc conversion is accomplished by the class E based inverter and single diode rectifier. The resonant gate drive circuit provides the drive signal for the inverter. The cell modulation control turns the converter ON and OFF over time in order to maintain a regulated output voltage.

TABLE I

COMPONENT VALUES FOR A CLASS E BASED RESONANT BOOST CONVERTER OPERATING AT 30 MHz USING CELL MODULATION CONTROL. INPUT VOLTAGE RANGES FROM 3.6 V TO 7.2 V, WITH OUTPUT VOLTAGE REGULATED TO 7 V. OUTPUT POWER RANGES FROM 1 W TO 2 W

Part	Value	Part	Value
C1	220p	L3	75n
C2	220p	L4	180n
C3	15p	L5	120n
C4	0.022u	M1	FDN361AN
C5	0.022u	R1	11.8k
D1	MBR0520L	R2	8.87k
D2	MA27D2700	R3	510
Comparator	LMV7235	R4	202k
Dual Inverter	NC7WZ04	R5	1k
Dual Inverter	NC7WZ04	R6	10k
5V Regulator	TPS76950	R7	15.4k
L1	120n	R8	990k
L2	58n	REF1	ADR530

Moreover, all of the power stage components can be sized based on the very high switching frequency, yielding small size and fast transient performance. Only the input and output filter capacitors need be sized for the ripple at the lower modulation frequency. The practical implications of this strategy will be presented in Section IV.

A block diagram of the converter is presented in Fig. 4. The three main components of the converter are the power stage, resonant gate drive circuit, and the cell modulation control. The design and performance of the individual subsystems follow, including a schematic for each block in Fig. 4. All component values are specified in Table I. Experimental results for the full converter are presented in Section IV.

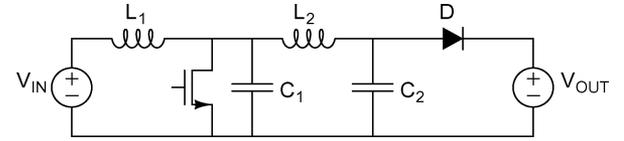


Fig. 5. Schematic of the prototype resonant converter power stage. The converter is based on a class E inverter whose tank is parallel loaded with a single diode rectifier. It is also topologically equivalent to the ZVS multiresonant boost converter proposed in [27], but utilizes a different control method. Component values are listed in Table I.

A. Power Stage

The power stage of the resonant boost converter can be developed from the class E inverter as follows [18]: The series resistive load is transformed to an equivalent resistance in parallel with the tank capacitor. The resistor is then replaced by a resonant single-diode rectifier (which siphons energy out of the tank), yielding the topology of Fig. 5. The tank may be retuned if needed to account for the nonlinear impact of the diode, such that near ZVS is maintained over the input voltage range. A benefit of the topology of Fig. 5 is that it absorbs the device parasitic capacitances to the extent that package inductances are not large (a valid approximation in the developed prototype).

Note that the transformation from a load in series with the tank to a load in parallel with the tank capacitor means that a fraction of the total power (equal to V_{IN}/V_{OUT}) is transferred directly as dc current from the input to the output; this reduces loss as compared to processing all power through ac waveforms. A further advantage of the topology of Fig. 5 is that it absorbs the parasitic capacitances of both the switch and the diode to the extent that device package inductances can be ignored. (If C_1 and C_2 in Fig. 5 entirely comprise device capacitance, then the package inductances can be effectively absorbed into L_1 and L_2 as well.)

It should also be noted that, component value selection aside, the circuit of Fig. 5 is topologically equivalent to the ZVS “multiresonant” boost converter of [27]. The principle differences between the design introduced here and the approach elucidated in [27] arise from how the circuit is controlled. Because we focus on operation at fixed switching frequency and duty ratio (with on/off control for regulation) rather than constant-off-time/variable-frequency control as in [27], we can employ sinusoidal resonant gating for efficient operation at VHF frequencies. Likewise, we need not rely on the switch body diode to preserve ZVS operation across operating conditions. Finally, the use of ON/OFF control offers the possibility of greatly improved light-load operation.

It should be noted that the concept of a steady state conversion ratio (e.g., “ M ”) is not relevant for the proposed converter design. This is because output power and voltage are controlled by modulating the converter ON and OFF over time, and not by running continuously at an operating point that provides the requisite conversion ratio or output power.

In developing the power stage, simulations in SPICE were carried out. Detailed simulation models used in this development may be found in [18]. Manufacturer-provided models were used for the semiconductor devices. There has also been great success in utilizing simple “ideal switch plus drop” models of

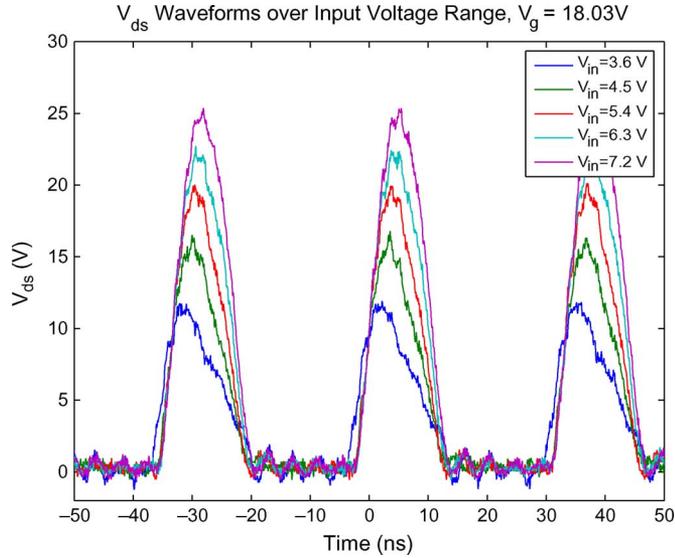


Fig. 6. Laboratory measurements of drain to source voltage (V_{ds}) waveforms across the input voltage range 3.6 V to 7.2 V for the converter power stage prototype whose schematic is presented in Fig. 5. The transistor is driven using a sinusoidal signal provided by a power amplifier with $V_{G,ac} = 18.03$ V.

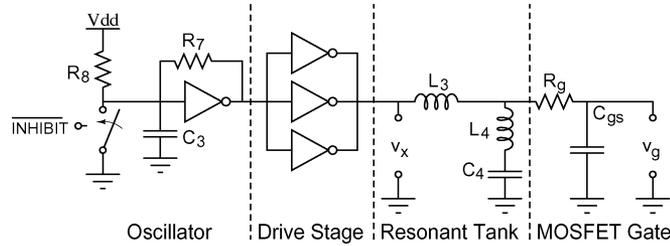


Fig. 7. Multistage resonant gate drive circuit schematic for class E based dc-dc converter. A relaxation oscillator provides a fixed frequency and duty ratio drive signal. Three inverters in parallel form a drive stage for the resonant tank. The resonant tank also develops a dc offset voltage at the gate, allowing the sinusoidal drive to be centered closer to V_{th} of the switching device. Component values are listed in Table I.

the semiconductor devices, augmented with nonlinear capacitances. This approach has also been found to be adequate to frequencies in excess of 100 MHz. At the highest frequencies, device package inductance and printed circuit board capacitance also need to be carefully modeled for high accuracy, along with passive component parasitics such as capacitor ESR and ESL (e.g., see [17].)

A prototype of the power stage illustrated in Fig. 5 was developed prior to the full system design to validate the power stage behavior. The transistor was gated with a 30 MHz sinusoidal drive signal via an external power amplifier. The resultant converter was then exercised over the full input voltage range while driving a fixed voltage load. Fig. 6 shows the v_{ds} waveforms for the transistor, demonstrating the ZVS behavior across the input voltage range.

B. Resonant Gate Drive

A multistage resonant gate drive circuit was designed to operate the power stage transistor. The design combines the features of a self oscillating resonant driver [3], [16], [20] and the tapered hard-switched driver designs sometimes found in

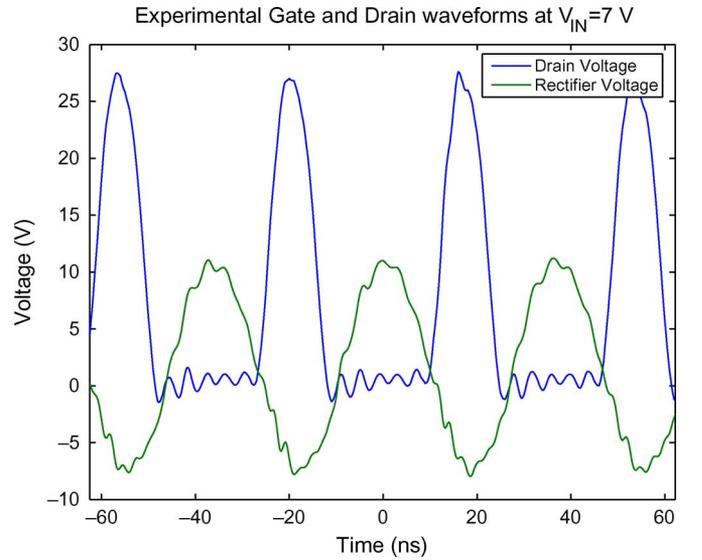


Fig. 8. Example laboratory measurements of drain to source (V_{ds}) and gate to source (V_{gs}) waveforms for $V_{in} = 7$ V for the full converter prototype. The power stage of the converter is that whose schematic is presented in Fig. 5, with the gate drive signal provided by the circuit illustrated in Fig. 7.

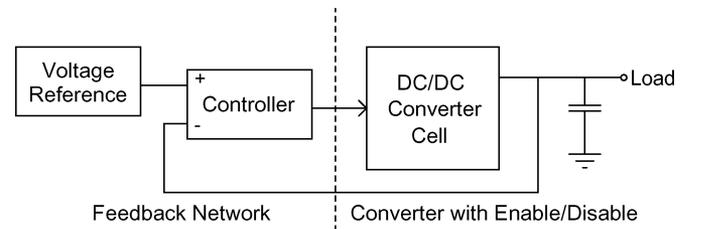


Fig. 9. Cell modulation architecture block diagram. The output voltage is compared to a reference; the result enables or disables the converter power stage. The output filter capacitor buffers the converter output while the power stage is OFF.

low-power integrated converters [28], [29]. The drive circuit is illustrated in Fig. 7. An example gate drive waveform, V_{gs} , for the resonant gate drive circuit of the final converter prototype is presented in Fig. 8. The accompanying drain waveform, V_{ds} , is also included.

The gate drive circuit is made up of two stages of inverters. The first stage is designed as a low current oscillator source, and the second stage is designed as a higher current drive stage. Simple inverters can be used for the drive current stage as well as adapted to a relaxation oscillator with relatively few components.

The first stage of the drive structure was designed to be self oscillating, eliminating the need for a separate oscillator. The converter is controlled by alternately disabling the gate drive and allowing it to run freely.

The second stage consists of three parallel inverters designed to deliver sufficient power to the resonant tank. The inverters are utilized for their suitable current drive capability, as well as their benefit of eliminating the external circuitry a traditional push/pull stage would require to mitigate shoot through. This drive stage has three times the current capacity as the oscillator stage, taking advantage of a tapered multistage design.

The final component of the gate drive circuit is the resonant tank network which operates resonantly to reduce gate drive

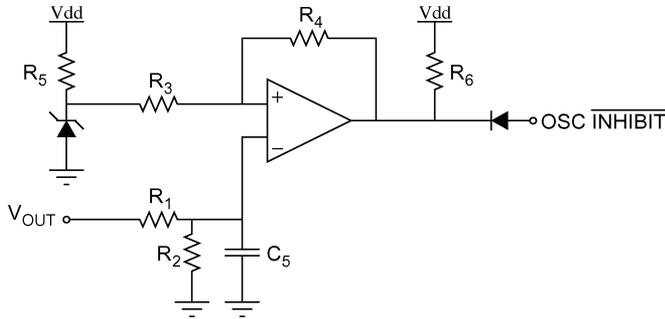


Fig. 10. Cell modulation control schematic for the block diagram in Fig. 9. A Zener diode provides a voltage reference that is constant across the input voltage range. An isolation diode allows the oscillator to run while the comparator output is high, but will pull the oscillator down to ground when the comparator output falls. The hysteresis band influences the magnitude of the output ripple. Component values are listed in Table I.

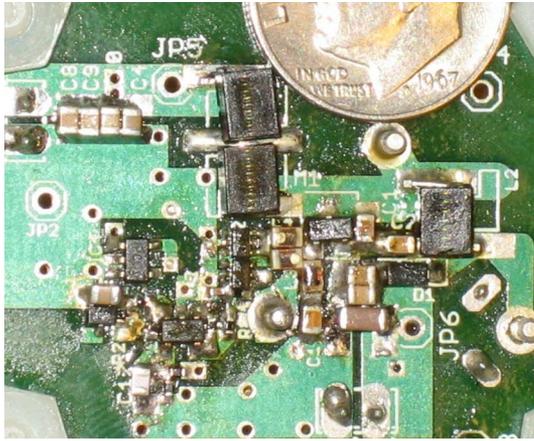


Fig. 11. Image of prototype converter cell (edge of US dime for scale). The converter operates with an input voltage of 3.6 V to 7.2 V, and provides a regulated 7 V output. The power requirement ranges from 1 W to 2 W; the converter can supply up to 3 W across its input voltage range.

loss. The inductively-tuned shunt leg L_4C_4 is designed to resonate with the gate capacitance at a frequency slightly below the switching frequency, such that it provides much of the reactive power needed to drive the gate (reducing the current requirement and output capacitance of the drive stage). The resulting network is capacitive at the switching frequency, and is driven from the square-wave output of the drive stage via inductor L_3 , thus providing approximately sinusoidal drive waveforms and reducing the capacitive switching loss of the drive stage.

A limitation of this reactive drive network is the potential for undesired self driving of the gate from the drain voltage via C_{rss} when the oscillator is inhibited. This is a possibility (especially at high input voltages) since the resonant tank network peaks the gate impedance near the switching frequency, and the drive stage holds the gate low only through the tank network. In the design presented here, a compromise was made between optimizing the forward drive (from the drive stage) when driving the power stage and mitigating the reverse drive (from the drain) when holding the power stage OFF. The need for this compromise could be eliminated (improving drive performance) by adding an additional small semiconductor switch directly across the gate which is closed when the power stage is inhibited.

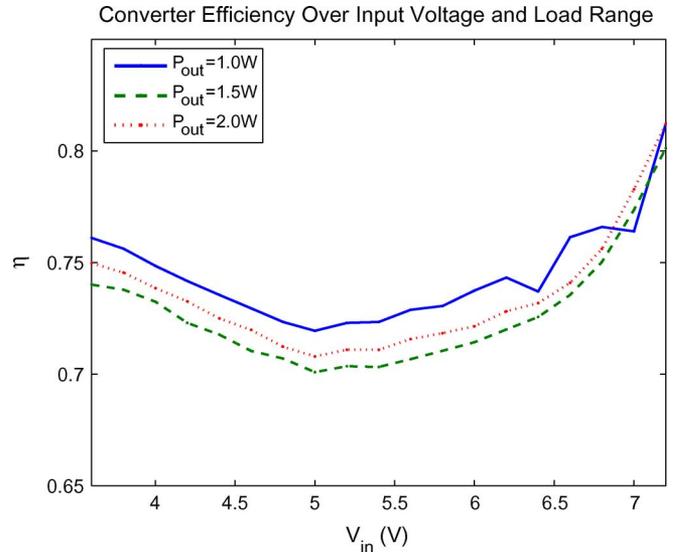


Fig. 12. Full converter efficiency over input voltage range of 3.6 V to 7.2 V. Efficiency is plotted for P_{out} equal to 1 W, 1.5 W, and 2 W, spanning the specified output range.

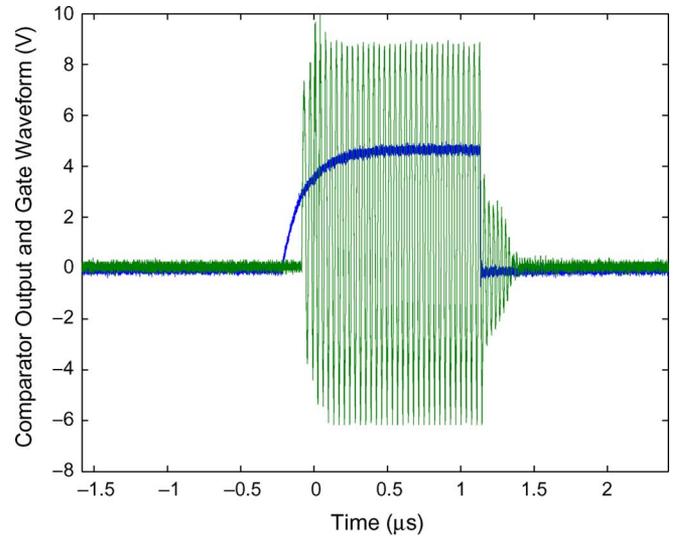


Fig. 13. Experimental measurement of the turn On and turn OFF transient performance of the prototype converter. The power stage requires approximately $0.25 \mu s$ to transition from OFF to ON or vice versa. This response is enabled by very high frequency design as the passive components store less energy than converters operating at lower frequencies. Short ON/OFF transients allow the cell modulation control architecture to tightly regulate output voltage by quickly responding to load requirements.

A resonant tank circuit with an added shunt branch helps to overcome the tradeoff between the drive stage resistance and its hard switched output capacitance. The second LC tank provides reactive power to the gate, reducing the dissipation in the drive stage. This allows for the size of the drive switches to be reduced, with less output capacitance.

The capacitor C_4 in the shunt branch also helps improve the switching behavior. In steady state, the capacitor has a voltage of $V_{dd}/2$ across it that biases the drive signal closer to the device threshold voltage. However, under cell modulation control, the charge on C_4 will be hard switched as the converter is enabled and disabled. This occurs at the cell modulation frequency,

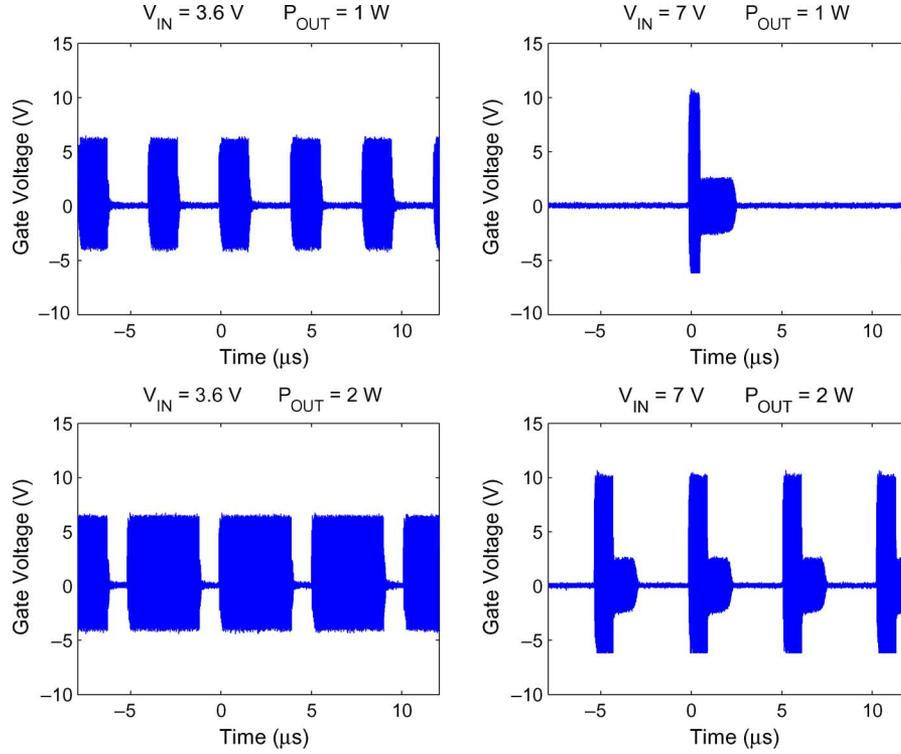


Fig. 14. Cell modulation behavior over input voltage and load range. The illustrated waveform is gate voltage of the converter cell on a long time scale to illustrate the cell modulation frequency.

which is significantly lower than the converter frequency of 30 MHz. This results in losses of

$$P_{\text{shunt}} = C_4 \left(\frac{V_{dd}}{2} \right)^2 f_{\text{mod}} \quad (8)$$

where V_{dd} is the inverter rail voltage, and f_{mod} is the rate at which the converter is modulated ON and OFF to regulate the output.

C. Cell Modulation Control

Fig. 9 contains a simplified block diagram for a cell modulated (ON-OFF) control architecture. The main components are the rf dc-dc converter, an output filter, and a feedback network to enable or disable the converter. The output filter averages the power delivered by the converter over time, while the feedback network enables the converter for an appropriate fraction of time to meet the load requirement.

A feedback network is needed to monitor the output voltage and provide the modulation (ON/OFF) control signals for the converter. The controller schematic is shown in Fig. 10.

A voltage divider network scales the output voltage down for comparison to a 3 V reference, chosen to be valid over the full input voltage range. A hysteresis band is set around the comparator to provide noise rejection and control the magnitude of the output ripple.

The output of the control network is designed to directly enable or inhibit the converter's gate drive oscillator. A low output from the comparator pulls the relaxation oscillator input down, disabling the drive circuit, while a high output from the comparator isolates the comparator from the oscillator, allowing it to run freely.

IV. CONVERTER PERFORMANCE

A prototype dc-dc converter was built using the converter cell, resonant gate circuit, and cell modulation control architecture described in the previous section. The converter is presented in Fig. 11 along with the edge of a U.S. dime for scale. The converter area is approximately 0.75 in^2 . The height, including PCB, is approximately 0.25 in. Full experimental results for this converter and a comparison to a commercially available device follow.

A. Experimental Results of Full Converter

Efficiency over load and input voltage range is presented in Fig. 12. The converter efficiency ranges from 71% to 81% over the load range of the converter.

The converter cell transient response is illustrated in Fig. 13. Both the cell turn ON and turn OFF time is approximately $0.25 \mu\text{s}$ in response to the gate driver enable signal. The cell modulation characteristics of the converter are illustrated over input voltage and load range in Fig. 14. The modulation frequency range (far below the switching frequency of 30 MHz) is enumerated in Table II.

Fig. 15 demonstrates the band limited output voltage ripple as well as the converter load transient response. At time $t = 0$, the converter load is stepped from 1 W to 2 W, the entire load range of the converter. The cell modulation duty cycle of the converter changes to meet the load requirement, and the transient response of the circuit does not exceed the output ripple of the converter operating in steady state. (The visible noise spike is from the load switching circuit.) The cell modulation control architecture easily adapts to changing load conditions.

TABLE II
CELL MODULATION FREQUENCIES FOR A 2 WATT RESONANT BOOST CONVERTER. THE MODULATION FREQUENCIES ARE PRESENTED AT THE FOUR CORNER POINTS OF INPUT VOLTAGE RANGE AND LOAD. INPUT VOLTAGE RANGES FROM 3.6 V TO 7.2 V, AND THE LOAD RANGES FROM 1 W TO 2 W

V_{in}	$P_{out} = 1W$		$P_{out} = 2W$	
	$T_{mod} (\mu s)$	$f_{mod} (kHz)$	$T_{mod} (\mu s)$	$f_{mod} (kHz)$
3.6	4	250	11	91
7.2	5	200	5	200

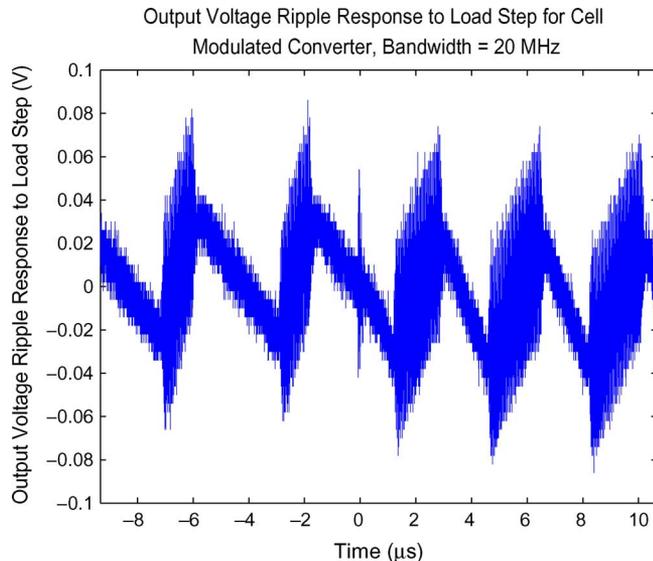


Fig. 15. AC output ripple measurement for the cell modulated converter prototype around the regulated dc output voltage, 7 V. The power stage is turned ON during the positive slope portions, and shut down during the negative portions. The 30 MHz switching ripple is highly undersampled in this photograph leaving the modulation frequency component visible. This figure also illustrates the transient response to a load step from 1 W to 2 W at time $t = 0$. The spike seen at $t = 0$ is from the load switching circuit.

B. Relative Performance of a Commercial Converter

A commercial boost converter design was used as a benchmark for comparison to the new design. The LM7231Y boost converter from National Semiconductor was selected for comparison. It is an integrated switch boost converter operating at a switching frequency of 600 kHz. An evaluation board from the manufacturer, having similar output capacitance (10 μF) to the VHF design and configured to match the 7 V output specification of the prototype, was used for the comparison. The evaluation board uses a 4.7 μH boost inductor.

The prototype converter was compared to the LM7231Y in terms of ripple performance and load transient behavior. Circuit area was comparable, though further integration work on the prototype could reduce its size while the LM7231Y is already a fully integrated part except for external passive components.

The ripple performance of the LM7231Y is presented in Fig. 16. It is appropriate to compare this to Fig. 15 for the prototype converter. The static switching ripple of the conventional converter is approximately one third that due to the VHF design. This is not surprising, given that the two designs use

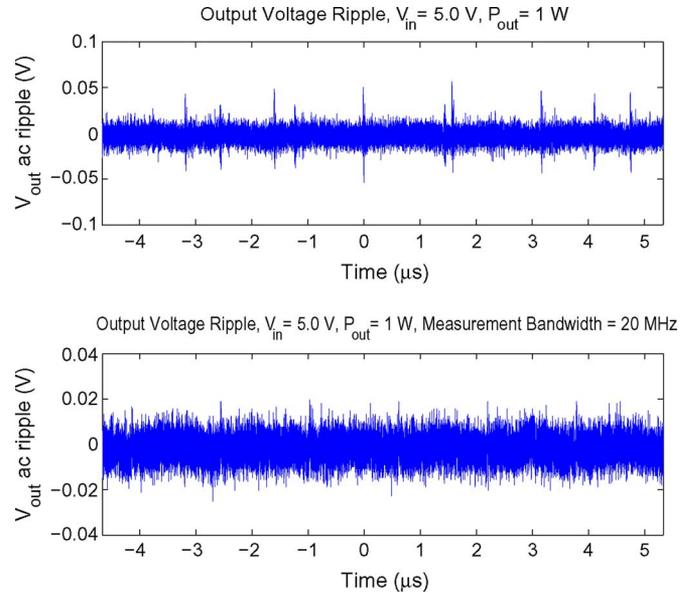


Fig. 16. National Semiconductor LM7231Y ripple response measurement input voltage is 5 V and output voltage is configured for 7 V. The load is 1 W. The top graph presents the full bandwidth measurement, and the bottom graph presents the measurement with a 20 MHz measurement bandwidth.

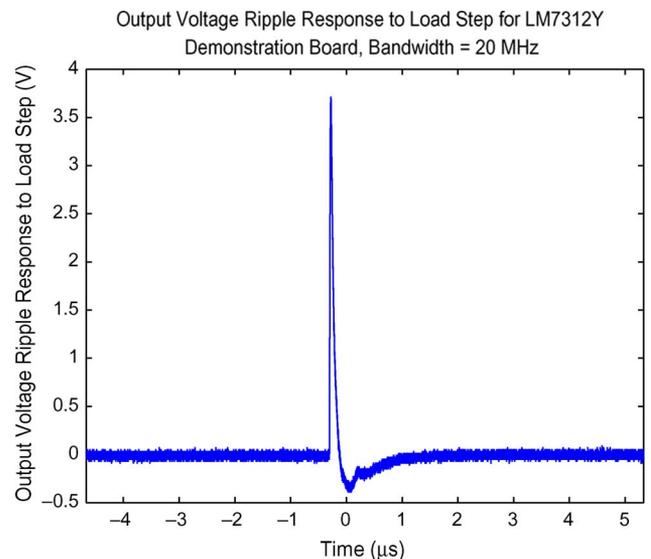


Fig. 17. National Semiconductor LM7231Y load transient response. The measurement is ac coupled and bandlimited to 20 MHz. The load steps from 2 W to 1 W, resulting in a transient response of up to 50% overshoot.

similar levels of output capacitance and the highest modulation frequency of the VHF design is roughly one third the switching frequency of the conventional design.

It is also important to consider the transient performance of the two designs. The ac coupled response of the LM7231Y evaluation board output voltage to a load transient is illustrated in Fig. 17. The load is stepped from 2 W to 1 W, resulting in a 3.5 volt overshoot and 0.5 volt undershoot around the 7 V operation voltage.

The main benefit of the resonant boost converter is revealed by comparing Fig. 17 and Fig. 15. The transient response of the VHF resonant boost converter does not even exceed its nominal

TABLE III
 REPRESENTATIVE DEVICES SUITABLE FOR HIGH-FREQUENCY OPERATION UNDER SOFT-SWITCHING AND SOFT-GATING OPERATION.
 LISTED PARAMETERS ARE A MIXTURE OF DATASHEET VALUES AND MEASURED PARAMETERS

Device	$V_{DS,Max}$ (V)	R_{gate} (Ω)	C_{ISS} (pF) (@ $V_{DS} = 0$)	$R_{DS,ON}$ (Ω) (@ $V_{GS} = 4.5V$)	C_{OSS} (pF) (@ $V_{DS} = V_{DS,Max}/4$)	R_{OSS} (m Ω) (@ $V_{DS} = V_{DS,Max}/4$)
IRF1902	20	0.8	480	0.085 (@ $V_{GS} = 4.5V$)	190	N/A
Si4346DY	30	0.5	1100	0.025 (@ $V_{GS} = 4.5V$)	175	577.16
FDN361AN	30	1.2	280	0.15 (@ $V_{GS} = 4.5V$)	60	404.86
Si4940	40	1	550	0.059 (@ $V_{GS} = 4.5V$) 0.036 (@ $V_{GS} = 10V$)	150	519.23
IRFL014N	55	0.7	290	0.16 (@ $V_{GS} = 10V$)	100	255.57
IRFZ24NS	55	0.9	560	0.07 (@ $V_{GS} = 10V$)	190	444.15
FDS5672	60	0.12	2900	0.012 (@ $V_{GS} = 6V$) 0.0088 (@ $V_{GS} = 10V$)	500	194.13
PD57060	65	0.19	190	0.233 (@ $V_{GS} = 10V$)	65	638.44
DE150-201N09A	200	1.1	1200	0.2 (@ $V_{GS} = 15V$)	190	N/A
ARF449A	450	0.07	1100	0.8 (@ $V_{GS} = 10V$)	95	N/A
ARF521	500	<0.1	1000	0.56 (@ $V_{GS} = 10V$)	85	300

steady state output voltage ripple. In comparison, the LM7231Y overshoots its operating point by 50%. The cell modulated resonant boost converter provides a tightly regulated output voltage over any transient within its load range specification using only small passive components. Achieving a similar level of ripple and transient performance from the conventional design would require dramatic increases in output capacitance, with commensurate increases in circuit size.

This comparison underscores an important difference between the proposed approach and conventional low-frequency PWM designs. In a VHF design with ON/OFF control, the bulk output capacitance is selected based on a specified ripple. One way to reduce ripple is to increase the bulk capacitance. Alternatively, however, the modulation ripple of a VHF design can be reduced without increasing bulk capacitance and with very little efficiency penalty through the use of low dropout

linear post regulation or active ripple filtering (e.g., [30]–[34]). A conventional converter, by contrast, requires a large bulk capacitor to meet transient requirements, independent of ripple considerations. (Linear post regulation and active filtering are not typically effective for large-signal transient variations, especially for voltage undershoot.) The reduction in bulk energy storage in the power stage due to VHF operation thus provides different constraints on the design of input and output filters which can be of significant advantage in many cases.

V. CONCLUSION

The desire to reduce passive component size and improve dynamic performance of dc-dc converters motivates the development of designs operating at very high switching frequencies. Practical operation at these frequencies requires circuit designs, control methods, and semiconductor devices that provide low-loss switching and gating of the devices. This paper explores transistor selection and design of very high frequency dc-dc converters.

Methods for evaluating MOSFET transistors and selecting operating frequencies for VHF power converters are presented. The selection metrics are for class-E based converters employing sinusoidal resonant gating, but may be expected to be useful on a qualitative level for a broader range of VHF topologies. These methods are applied to the design of a resonant boost converter operating at 30 MHz using a conventional vertical power MOSFET. Design of the power stage, resonant gate drive, and control circuitry are treated in detail. Experimental results demonstrating the performance of the converter are presented along with a comparison to a conventional design. It is shown that the VHF design achieves a combination of size and dynamic performance that is far better than the conventional design.

APPENDIX

This appendix provides a representative list of MOSFETs that the authors have identified as good candidates for high-frequency operation under soft-switching and soft-gating conditions. Parameters provided are a mixture of datasheet values and measured parameters of sample devices. (Gate resistance in particular is often not provided in datasheets, as it is not of primary importance in hard-gated converters.) Table III presents the data.

It should be noted that the authors and their colleagues have used a subset of the devices listed here to realize designs operating at frequencies up to 110 MHz at tens of Volts and Watts (e.g., [17], [19], [20], and [35]) and up to 30 MHz at hundreds of Volts and Watts (e.g., [36] and [37]). Moreover, additional increases in power at a given frequency can be obtained through the use of a cellular converter architecture, as described in [16], [25].

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