Resistance Compression Networks for Radio-Frequency Power Conversion

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***Abstract*—A limitation of many high-frequency resonant inverter topologies is their high sensitivity to loading conditions. This paper introduces a new class of matching networks that greatly reduces the load sensitivity of resonant inverters and radio frequency (RF) power amplifiers. These networks, which we term resistance compression networks, serve to substantially decrease the variation in effective resistance seen by a tuned RF inverter as loading conditions change. We explore the operation, performance characteristics, and design of these networks, and present experimental results demonstrating their performance. Their combination with rectifiers to form RF-to-dc converters having narrow-range resistive input characteristics is also treated. The application of resistance compression in resonant power conversion is demonstrated in a dc–dc power converter operating at 100 MHz.**

***Index Terms*—Class E inverter, high frequency, integrated converter, matching network, radio frequency (RF) dc–dc resonant converter, RF power amplifier (RF PA), rectenna, resonant rectifier, self-oscillating inverter, very high frequency (VHF).**

I. Background

A PRINCIPAL means for improving performance and reducing the size of power electronics is through increasing the switching frequency. Resonant dc–dc power converters enable much higher switching frequencies than can be achieved with conventional pulsewidth modulated circuits, due to their natural soft-switched operation and ability to absorb and utilize circuit parasitics in the conversion process. For example, efficient resonant dc–dc power conversion has been demonstrated at frequencies in excess of 100 MHz, and operation at much higher switching frequencies is clearly feasible [1], [2]. Further development of resonant power converter technology is thus of great potential value. This paper introduces a new circuit technique that overcomes one of the major limitations of resonant dc–dc converters at extremely high frequencies, and expands the range of applications for which resonant conversion is effective.

Fig. 1 shows a basic structure for a high-frequency resonant dc–dc converter, comprising an inverter stage, a transformation stage, and a rectifier stage [1]–[10].

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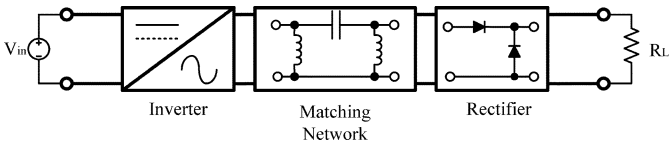

Fig. 1. Structure of the power stage of a resonant dc–dc converter. The converter comprises an inverter (dc–ac) circuit, a transformation/matching circuit, and a rectifier (ac–dc) circuit.

The inverter stage draws dc input power and delivers ac power to the transformation stage. Inverters suitable for extremely high frequencies operate resonantly, and take advantage of the characteristics of the load to achieve zero-voltage switching (ZVS) of the semiconductor device(s) [11]–[18].

The rectifier stage takes ac power from the transformation stage and delivers dc power to the output. In addition to conventional rectifier topologies, resonant converters can take advantage of a variety of resonant rectifiers [19], [20]. The system may be designed such that the rectifier stage appears resistive in a describing function sense [1], [10], [19], [20] and is matched to the inverter by the action of the transformation stage. The functions of the transformation stage are to develop this impedance match, to provide voltage and current level transformation, and in some cases to provide electrical isolation. The transformation stage can be realized using conventional transformers, "wide-band" or "transmission-line" transformers [11], [15], [21], matching networks [22], or similar means.

Power or output control of resonant converters can be achieved through a number of means, including frequency modulation [3], [5], on/off control [1], [23], and extensions of these techniques [1], [24], [25]. Fixed-frequency control techniques are preferable for circuit implementations with high-order tuned tanks or narrow-band transformation stages, and we focus on fixed-frequency operation for purposes of this paper.

A major limitation of resonant converter circuits is the sensitivity of the inverter stage to loading conditions. Switched-mode radio frequency (RF) inverters suitable for ultra-high frequencies (e.g., classes DE, E, and F) exhibit high sensitivity to the effective impedance of the load. For example, class E inverters only operate under soft switched conditions over about a factor of two in load resistance. While acceptable in communications applications (in which the load resistance is relatively constant), this is problematic for many dc–dc power converter applications, where the effective resistance presented by the matching stage and rectifier varies greatly with output voltage and current [10]. This problem is particularly severe in applications in which the voltage conversion ratio varies substantially; such applications include charging systems where the converter must deliver

constant power over a wide output voltage range and regulating converters where the converter must operate over a wide input voltage range and/or the same converter design must be capable of supporting a range of output voltages.

This paper introduces a new class of matching/transformation networks that greatly reduce the load sensitivity of tuned RF power inverters. These networks, which we term resistance compression networks, serve to greatly reduce the variation in effective resistance seen by a tuned RF inverter as loading conditions change.

Compression networks ideally act without loss, such that all energy provided at the input port is transformed and transferred to the resistive load. In effect, the load resistance range appears compressed when looking through a resistance compression network. This effect can be used to overcome one of the major deficiencies of tuned RF circuits for power applications and expand the range of applications for which high-frequency resonant power conversion is viable.

Section II of the paper introduces resistance compression networks, including their fundamental principles of operation and performance characteristics. Experimental results demonstrating their performance are also presented. Section III shows how resistance compression networks can be paired with appropriate rectifiers to yield high-performance RF-to-dc converters with resistive input characteristics. Section IV addresses design considerations for resistance compression networks and resistance compressed rectifiers. Application of this approach to the design of a 100-MHz dc–dc power converter is presented in Section V. Section VI concludes the paper.

II. Resistance Compression Networks

Here we introduce circuits that provide the previously described resistance compression effect. These circuits operate on two matched load resistances whose resistance values, while equal, may vary over a large range. As will be shown in Section III, a variety of rectifier topologies can be modeled as such a matched resistor pair.

Two simple linear circuits of this class that exhibit resistance compression characteristics are illustrated in Fig. 2. When either of these circuits is driven at the resonant frequency $\omega_0 = 1/\sqrt{LC}$, of its LC tank, it presents a resistive input impedance R_{in} that varies only a small amount as the matched load resistances R vary across a wide range. For example, for the circuit of Fig. 2(a), the input resistance is:

$$R_{\text{in}} = \frac{2R}{1 + \left(\frac{R}{Z_0}\right)^2} \tag{1}$$

in which $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the tank. For variations of R over a range having a geometric mean of Z_0 (that is, $R \in [(Z_0/c), cZ_0]$, where c is a constant that defines the span of the resistance range) the variation in input resistance R_{in} is smaller than the variation in load resistance R. The amount of "compression" that is achieved for this case (around a center value of impedance $Z_c = Z_0$) is illustrated in Table I. For example, a 100:1 variation in R around the center value results in only a 5.05:1 variation in R_{in}, and a 10:1 variation in load resistance results in a modest 1.74:1 variation in R_{in}. Furthermore, because the reactive components are ideally lossless, all energy driven into the resistive input of the compression network is transformed in voltage and transferred to the load resistors. Thus, the compression network can efficiently function to match a source to the load resistors, despite large (but identical) variations in the load resistors.

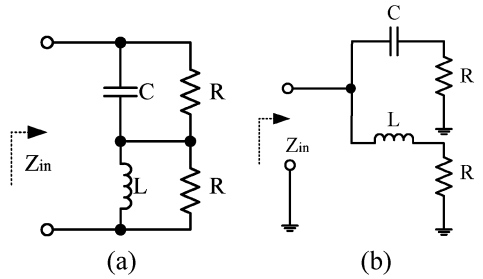

Fig. 2. Resistance compression circuits. Each of these circuits provides a compression in apparent input resistance. At the resonant frequency of the LC tank the input resistance R_{in} varies over a narrow range as the matched resistors R vary over a wide range (geometrically centered on the tank characteristic impedance). The circuits achieve lossless energy transfer from the input port to the resistors R.

TABLE I
Characteristics of the Resistance Compression Network of Fig. 2(a)

Ratio of R range	Range of R	Ratio of R_{in} range	Range of R_{in}
100:1	$0.1Z_0$ to $10Z_0$	5.05:1	$0.198Z_0$ to Z_0
10:1	$0.316Z_0$ to $3.16Z_0$	1.74:1	$0.575Z_0$ to Z_0
4:1	$0.5Z_0$ to $2Z_0$	1.25:1	$0.8Z_0$ to Z_0
2:1	$0.707Z_0$ to $1.41Z_0$	1.06:1	$0.94Z_0$ to Z_0

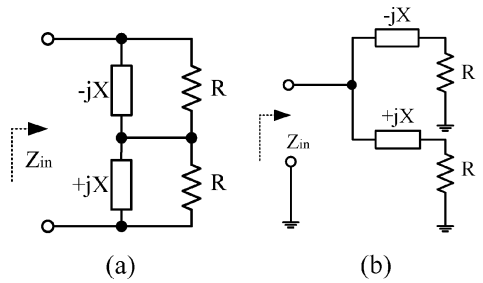

Fig. 3. Structure of the two basic resistance compression networks introduced in the paper. The impedance of the reactive networks is specified at the desired operating frequency. Implementation of the reactive networks may be selected to provide desired characteristics at frequencies away from the operating frequency.

For the circuit of Fig. 2(b), the input resistance at resonance is

$$R_{\text{in}} = \frac{Z_0^2}{2R}\left[1 + \left(\frac{R}{Z_0}\right)^2\right] \tag{2}$$

which represents the same degree of compression as R varies about Z_0.

More generally, the compression networks of Fig. 2 may be designed with generalized reactive branch networks as shown in Fig. 3. The reactive branch networks in Fig. 3 are designed

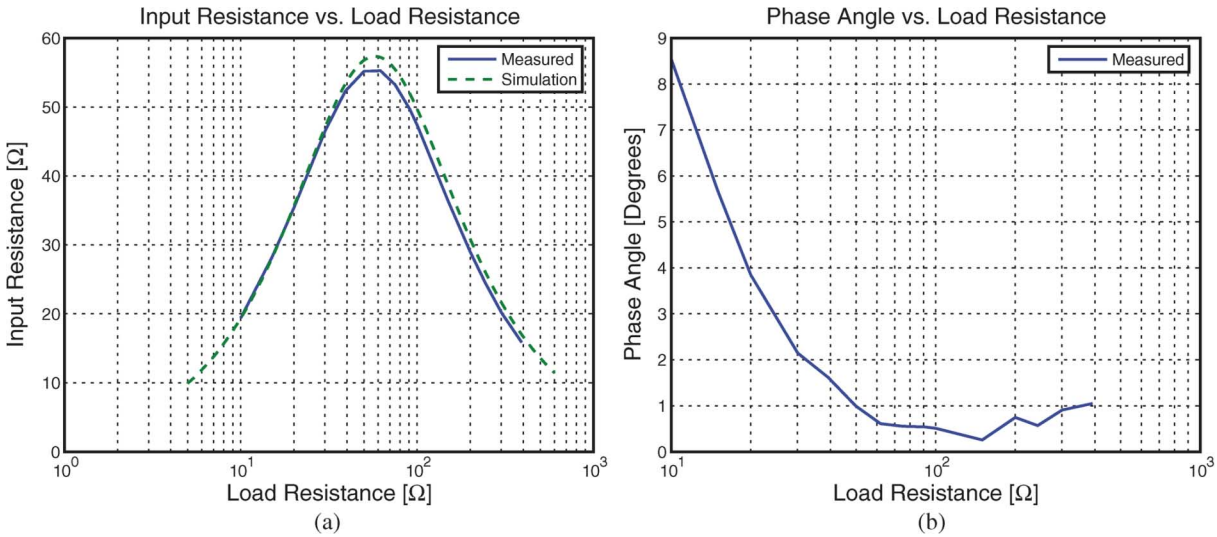

Fig. 4. Magnitude of the input resistance $\Re e\{Z_{\rm in}\}$ and phase of the input impedance (experimental and simulated) of the compression network shown in Fig. 2(a) as a function of R. L is a Coilcraft 100 nH air-core inductor plus 7.2 nH of parasitic inductance while C is a 33-pF mica capacitor. Measurements made at 85.15 MHz. (a) Input resistance $\Re e\{Z_{\rm in}\}$ versus R; (b) Phase Angle of the Input Impedance vs. R.

TABLE II
COMPONENTS USED TO OBTAIN DATA IN FIG. 4

Component Name	Nominal Value	Manufacturer and Part Style	Part Number
C	33 pF	CDE Chip Mica 100V	MC08FA330J
L	100 nH	Coilcraft	1812SMS-R10

to have the specified reactance X at the designed operating frequency. For example, at this frequency the input impedance of the network in Fig. 2(a) will be resistive with a value

$$R_{\rm in} = \frac{2R}{1+\left(\frac{R}{X}\right)^2} \tag{3}$$

which provides compression of the matched load resistances about a center value of impedance $Z_c = X$. The impedances of these branches at other frequencies of interest (e.g., dc or at harmonic frequencies) can be controlled by how the branch reactances are implemented. Likewise, the resistance for the network of Fig. 2(b) will be

$$R_{\rm in} = \frac{X^2}{2R}\left[1+\left(\frac{R}{X}\right)^2\right]. \tag{4}$$

Considerations regarding implementation of the branch networks are addressed in Section IV.

It should be noted that these networks can be cascaded to achieve even higher levels of resistance compression. For example, the resistances R in Fig. 3 can each represent the input resistance of subsequent resistance compression stage. An "N-stage" compression network would thus ideally have 2^N load resistances that vary in a matched fashion. However, the efficacy of multiple-stage compression is likely to be limited by a variety of practical considerations.

Fig. 4 shows simulated and experimental results from a compression network of the type shown in Fig. 2(a) with component values shown in Table II. The network has a resonant frequency of 85.15 MHz and a characteristic impedance of 57.35 Ω (slightly lower than nominal due to small additional parasitics). The anticipated compression in input resistance is achieved, and in all cases the measured reactive impedance at the operating frequency is negligible. The compression network of Fig. 3(b) is the network dual of that shown in Fig. 3(a). In the network of Fig. 3(b), the input and load resistors share a common ground, which can be useful in applications such as the one developed in Section V.

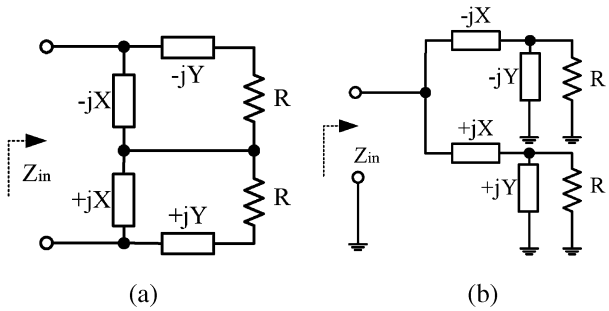

Fig. 5. Four-element compression networks. These networks can provide both resistance compression and impedance transformation.

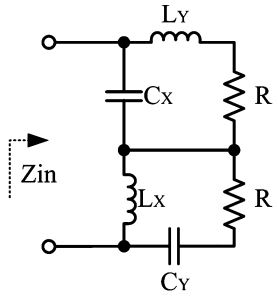

Fig. 6. Four-element compression network used to obtain experimental data. Layout of this circuit is illustrated in Appendix A.

The networks of Fig. 3 provide resistance compression about a specified value. It is also possible to achieve both resistance compression and impedance transformation in the same network. Fig. 5 shows two structures of four-element compression/transformation networks. As shown in Appendix B, these networks can be designed to achieve both resistance

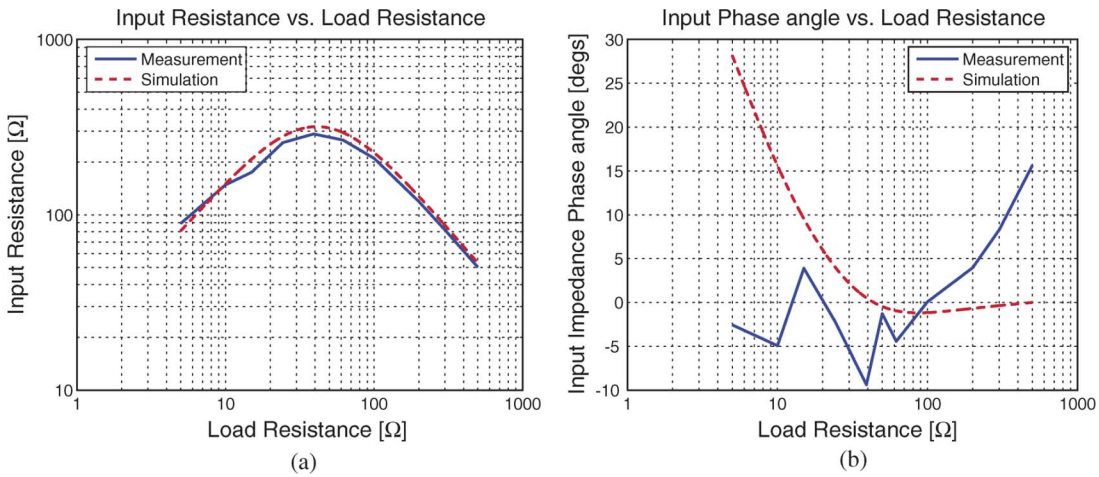

Fig. 7. Input resistance ($\Re\{Z_{\rm in}\}$) and impedance phase (experimental and simulated) of the four-element compression network shown in Fig. 6 as a function of R. $C_X = 15$ pF, $L_X = 169$ nH, $C_Y = 11$ pF, $L_Y = 246$ nH; measurements made at 97.4 MHz: (a) input resistance ($\Re\{Z_{\rm in}\}$) versus R and (b) phase angle of the input impedance versus R.

TABLE III
COMPONENTS USED TO OBTAIN DATA IN FIG. 7

Component Name	Nominal Value	Manufacturer and Part Style	Part Number
C_X	15 pF	CDE Chip Mica 100V	MC08EA150J
C_Y	8 pF +2 pF +1 pF	CDE Chip Mica 100V	MC08CA080C MC08CA020D MC08CA010D
L_X	169 nH	Coilcraft	132-12SM-12
L_Y	246 nH	Coilcraft	132-15SM-15

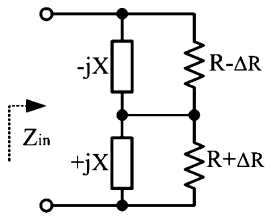

Fig. 8. Resistance compression network with unequal loads. The load resistors are mismatched by $2\Delta R$, assuming $\Delta R \ll R$.

compression and transformation of the resistance up or down by an amount only limited by efficiency requirements, component quality factor, and precision. As with the two-element networks, the input impedance remains entirely resistive over the whole load-resistance range.

Fig. 7 shows simulation and experimental measurement of a four-element impedance compression network operating at a frequency of 97.4 MHz which provides both compression and transformation (Fig. 6 and Table III). The load resistance is swept between 5 Ω and 500 Ω and presents a resistive input impedance over the whole range that varies between 50 Ω and 290 Ω.

In practice, the load resistors of compression network may not be perfectly matched. Consider the resistance compression network circuit in Fig. 8. The load resistors are mismatched by $2\Delta R$. Assuming $\Delta R \ll R$ and ignoring higher order ΔR terms, the input impedance $Z_{\rm in}$ is

$$Z_{\rm in} = |Z_{\rm in}|\angle\theta = \frac{2R}{1+\left(\frac{R}{X}\right)^2} + j\frac{4RX^3}{(R^2+X^2)^2}\Delta R. \quad (5)$$

The magnitude and phase of the input impedance $Z_{\rm in}$ are

$$|Z_{\rm in}| = \frac{2R}{1+\left(\frac{R}{X}\right)^2}\left[1+\frac{2X^2}{(R^2+X^2)^2}\Delta R^2\right] \quad (6)$$

$$\theta = \arctan\left(\frac{2X}{R^2+X^2}\Delta R\right) \approx \frac{2X}{R^2+X^2}\Delta R. \quad (7)$$

As can be seen from (6) and (7), the resulting deviation in impedance magnitude is proportional to ΔR^2, while the deviation in phase is proportional to ΔR. So for small deviations ΔR the phase of the input impedance is more sensitive to load resistance mismatch than is the magnitude. This is also true for four-element compression networks. It can be seen in Figs. 4 and 7 that the match between theory and experiment is better for magnitude than for phase. Moreover, in Fig. 7, the network achieves impedance compression and transformation through resonant action, working at high quality factor over some of the operating range. As with other high-quality factor networks operated near resonance, the phase is more sensitive to both deviations in frequency and in component values (e.g., parasitics) than is the magnitude. Thus, small unmodeled parasitics can easily lead to the observed differences in phase. Nevertheless, the performance observed is quite acceptable for many practical applications.

The compression networks of Fig. 3 also have an interesting effect when the matched load impedances are not perfectly resistive. In fact, as shown in Appendix C, these networks can provide substantial "phase compression" of the input impedance (towards zero phase) for matched loads having an impedance magnitude near X but varying phase.

The results presented in both the two-element and four-element resistance compression networks show the potential for marked improvement in the performance of load-sensitive power converters.

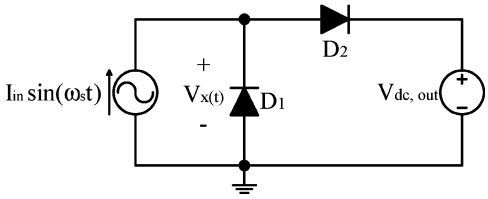

Fig. 9. Half-wave rectifier with constant voltage load and driven by a sinusoidal current source.

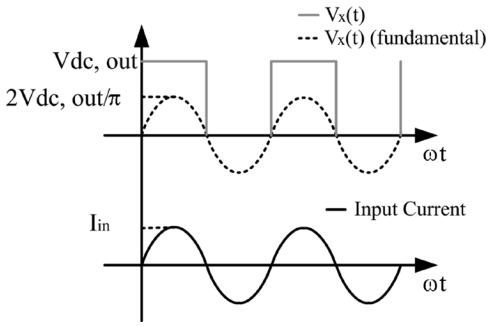

Fig. 10. Characteristic waveforms of the half-wave rectifier shown in Fig. 9. The input current and the fundamental of the input voltage are in phase.

III. Resistance-Compressed Rectifiers

A resistance compression network can be combined with an appropriate set of rectifiers to yield an RF-to-dc converter with narrow-range resistive input characteristics. In order to obtain the desired compression effect, the rectifier circuits must effectively act as a matched pair of resistances when connected to a compression network of the kind described in Section II. A purely resistive input impedance can be achieved with a variety of rectifier structures. For example, in many diode rectifiers the fundamental ac voltage and current at the rectifier input port are in phase, though harmonics may be present [10].

One example of this kind of rectifier structure is an ideal half bridge rectifier driven by a sinusoidal current source of amplitude $I_{\rm in}$ and frequency $\omega_{\rm s}$, and having a constant output voltage $V_{\rm dc,out}$, as shown in Fig. 9. The voltage at the input terminals of the rectifier $v_x(t)$ will be a square wave having a fundamental component of amplitude $V_{x1} = (2V_{\rm dc,out}/\pi)$ in phase with the input current $i_{\rm in}(t)$, as shown in Fig. 10. The electrical behavior at the fundamental frequency $\omega_{\rm s}$ (neglecting harmonics) can be modelled as a resistor of value $R_{\rm eq} = (2/\pi)(V_{\rm out}/I_{\rm in})$. Similarly, a full wave rectifier with a constant voltage at the output can be modelled at the fundamental frequency as a resistor $R_{\rm eq} = (4/\pi)(V_{\rm dc,out}/I_{\rm in})$. There are many other types of rectifier topologies that present the above mentioned behavior; another example is the resonant rectifier of [19]. This rectifier also presents a resistive impedance characteristic at the fundamental frequency; furthermore, it requires only a single semiconductor device and incorporates the necessary harmonic filtering as part of its structure. Such a rectifier, when connected to a constant output voltage, presents a resistive equivalent impedance of the same magnitude as that of the full wave rectifier, $R_{\rm eq} = (4/\pi)(V_{\rm dc,out}/I_{\rm in})$. Still another type of rectifier providing this type of behavior is the resonant rectifier used in the dc–dc converter of Fig. 16 [19].

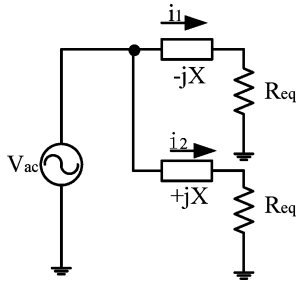

Fig. 11. Two-element compression network with reactive branches represented by impedances evaluated at the operating frequency.

Driving this type of rectifier with a tuned network suppresses the harmonic content inherent in its operation and results in a resistive impedance characteristic at the desired frequency. This equivalent resistance can be represented by $R_{\rm eq} = (k_{\rm rect}/|I_1|)V_{\rm dc,out}$, where $k_{\rm rect}$ depends on the specific rectifier structure and $|I_1|$ is the fundamental component of the drive current. As shown below, when two identical such rectifiers feed the same dc output and are driven via reactances with equal impedance magnitudes (e.g., as in the circuits of Fig. 3), they act as matched resistors with values that depend on the dc output. Thus, a pair of such rectifiers can be used with a compression network to build a rectifier system having a resistive ac-side (input) characteristic that varies little as the dc-side operating conditions change. This type of compression network/rectifier combination can be modelled as shown in Fig. 11.

We can express the magnitude of the current i_1 as

$$|i_1| = \frac{V_{\rm ac}}{\sqrt{X^2 + R_{eq}^2}}. \tag{8}$$

By replacing $R_{\rm eq}$ with its corresponding value $R_{\rm eq} = (k_{\rm rect}/|I_1|)V_{\rm dc,out}$ we obtain

$$|i_1| = \frac{V_{\rm ac}}{\sqrt{X^2 + \frac{k_{\rm rect}^2}{|i_1|^2}V_{\rm dc,out}^2}}. \tag{9}$$

Rearranging

$$|i_1|^2 X^2 + k_{\rm rect}^2 V_{\rm dc,out}^2 = V_{\rm ac}^2. \tag{10}$$

Solving for $|i_1|$

$$|i_1| = \sqrt{\frac{V_{\rm ac}^2 - k_{\rm rect}^2 V_{\rm dc,out}^2}{X^2}}. \tag{11}$$

From this expression we can see that the branch current magnitude $|i_1|$ depends on the dc output voltage and the reactance magnitude. The branch carrying $|i_2|$ has the same reactance magnitude and output voltage, so both branches present identical effective load resistances.

For all the rectifier structures that can be represented by an equivalent resistance of value $R_{\rm eq} = (k_{\rm rect}/|i_1|)V_{\rm dc,out}$, we can express the equivalent resistances loading each branch as

$$R_{\rm eq} = \frac{k_{\rm rect}V_{\rm dc,out}}{\sqrt{\frac{V_{\rm ac}^2 - k_{\rm rect}^2 V_{\rm dc,out}^2}{X^2}}} = X\sqrt{\frac{1}{\left(\frac{V_{\rm ac}}{k_{\rm rect}V_{\rm dc,out}}\right)^2 - 1}}. \tag{12}$$

The net input resistance of the resistance-compressed rectifier set at the specific frequency will be determined in (4) where $R_{\rm eq}$ for the rectifier replaces R.

Looking from the dc side of the resistance compressed rectifier we also see interesting characteristics. For a given ac-side drive, a resistance-compressed rectifier will act approximately as a constant power source, and will drive the output voltage and/or current to a point where the appropriate amount of power is delivered.

IV. Design Considerations for Resistance Compression Networks

In designing resistance compression networks and resistance compressed rectifiers there are some subtle considerations that must be taken into account. The first consideration is how the compression network processes frequencies other than the operating frequency. When a compression network is loaded with rectifiers, the rectifiers typically generate voltage and/or current harmonics that are imposed on the compression network. It is often desirable to design the compression network to present high or low impedances to dc and to the harmonics of the operating frequency in order to block or pass them. Moreover, in some cases it may be important for the impedances of the two branches to be similar at harmonic frequencies in order to maintain balanced operation of the rectifiers. To achieve this, it is often expedient to use multiple passive components to realize each of the reactances in the network (i.e., reactances $\pm jX$ in Fig. 3.) This strategy was employed in the compression network of the system in Fig. 16 described in the following section.

A second design consideration is that of selecting a center impedance Z_C for the compression. Typically, one places the center impedance at the geometric mean of the load resistance range to maximize the amount of compression. However, in some cases one might instead choose to offset the center impedance from the middle of the range. This might be done to make the input resistance of the compression network vary in a particular direction as the power level changes. Also, in systems that incorporate impedance or voltage transformation, different placements of the compression network are possible, leading to different possible values of Z_C. For example, one might choose to place a transformation stage before the compression network, on each branch after the compression network, or both. The flexibility to choose Z_C in such cases can be quite valuable, since centering the compression network at too high or too low an impedance level can lead to component values that are either overly large or so small that they are comparable to parasitic elements.

A third major consideration is circuit quality factor and frequency sensitivity. Since compression networks operate on resonant principles, they tend to be highly frequency selective. This fact requires careful component selection and compensation for circuit parasitics in the design and layout of a compression network. Moreover, as with matching networks that realize large transformation ratios [22], compression networks realizing large degrees of compression require high quality-factor components. Component losses typically limit the practical load range over which useful compression may be achieved.

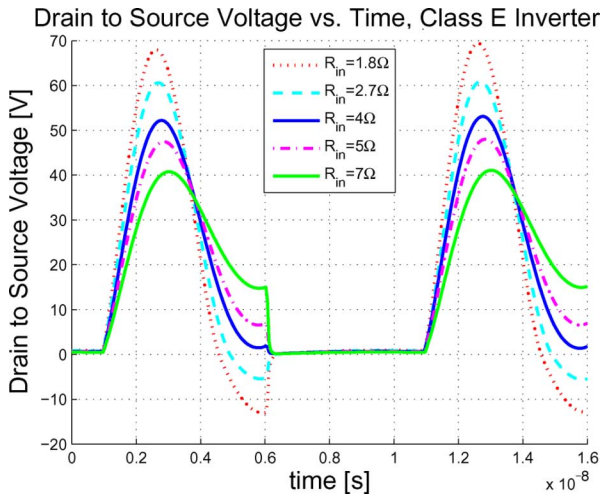

Fig. 12. Drain to source voltage for a class E inverter for different values of resistance. Using the notation in [27] $L_1 = 538$ nH, $L_2 = 24.2$ nH, $C_1 = 120$ pF (nonlinear), $C_2 = 163.5$ pF, $1.8\ \Omega \leq R \leq 7\ \Omega$. Optimal ZVS occurs at $R = 4\ \Omega$. When the resistor deviates from its nominal value ZVS is not achieved.

V. Motivation and Example Application: A 100-MHz dc–dc Converter

The resistance compression networks described in Section II and resistance-compressed rectifiers described in Section III have many potential applications, including RF rectifiers (e.g., for rectennas, or rectified antennas [19], [26]) and dc–dc converters operating at VHF and microwave frequencies. Here, we describe some motivations for their use in resonant dc–dc converters, and provide a practical example of a resistance compressed rectifier in a 100-MHz dc–dc converter.

A. Motivation

The motivation for resistance compression networks in RF-to-dc conversion applications is straightforward. The compression network allows the rectifier system to appear as an approximately constant-resistance load independent of ac drive power or dc-side conditions. In rectenna applications this can be used to improve matching between the antenna and the rectifier. As will be shown, this is also useful for preserving efficient operation of resonant dc–dc converters as operating conditions change.

As described in Section I, resonant dc–dc power converters consist of a resonant inverter, a rectifier, and a transformation stage to provide the required matching between the rectifier and the inverter. An inherent limitation of most resonant inverters suitable for VHF operation is their high sensitivity to loading conditions. This sensitivity arises because of the important role the load plays in shaping converter waveforms. Consider, for example, a class E inverter designed to operate efficiently at a nominal load resistance. As the load resistance deviates substantially from its design value, the converter waveforms rapidly begin to deteriorate. As seen in the example drain-source waveforms of Fig. 12, the peak switch voltage rises rapidly when the resistance deviates in one direction.[1] Moreover, zero-voltage turn-on

[1]This effect is somewhat mitigated in circuits where the switch has an intrinsic or external antiparallel diode. However, the diode introduces loss and parasitic effects of its own, so such operation is still not desirable.

of the device is rapidly lost for deviations in either direction (see Fig. 12 and [27, Fig. 5]).

There are at least three reasons why maintaining near zero-voltage switch turn on is important in very high frequency power converters. First, the turn-on loss associated with the discharge of the capacitance across the switch is undesirable and eliminating this loss is often important for achieving acceptable efficiency. Second, a rapid drain voltage transition at turn on can affect the gate drive circuit through the Miller effect, increasing gating loss and possibly increasing switching loss due to the overlap of switch voltage and current. This issue can be of particular concern in circuits employing resonant gate drives, and in cases where the gate drive transitions are a significant fraction (e.g., 5%) of the switching cycle. Finally, ZVS avoids electromagnetic interference (EMI) and capacitive noise injection generated by rapid drain voltage transitions.

In view of the above considerations, there exist substantial limits on allowable load variations. In the example of Fig. 12, even if the maximum switch off-state voltage is allowed to increase and the switch voltage magnitude at turn on is allowed to be as large as the dc input voltage (a substantial deviation from ZVS), the permissible load resistance range is only a factor of approximately 3:1 (a range of 6 Ω to 2 Ω in Fig. 12). Requiring a closer approximation to zero-voltage turn on will necessitate maintaining a still narrower resistive load range.

This limitation in load range is further exacerbated in resonant dc–dc converters. As shown in Section III, the effective resistance presented to the inverter typically depends on both ac drive levels (and hence on input voltage) and on the dc output of the rectifier. These dependencies pose a challenge to the design of resonant dc–dc converters at very high frequencies.

B. Example Application

The high sensitivity of RF converters such as the class E inverter to variations in load resistance is a significant limitation, and motivates the development of circuit techniques to compensate for it.

To demonstrate the use of resistance compression to benefit very high frequency dc–dc power converters, a prototype dc–dc converter operating at 100 MHz was developed. The circuit consists of a class E inverter with self-oscillating gate drive, a matching network, a resistance compression network of the type shown in Fig. 3(b), and a set of two resonant rectifiers which have a resistive characteristic at the fundamental frequency. The switching frequency for the converter is 100 MHz, the input voltage range is 11 V $\leq V_{\mathrm{in,dc}} \leq$16 V and the maximum output power capability ranges from 11.4 W at $V_{\mathrm{in,dc}} = 11$ V to 24.5 W at $V_{\mathrm{in,dc}} = 16$ V. The detailed schematic of the circuit implementation is shown in Fig. 16 and the components used are listed in Table IV. A photograph of the prototype converter is shown in Fig. 17, and detailed layout information for the resistance compressed rectifier is provided in Fig. 19 and Appendix A.

In order to minimize the gating losses of the LDMOSFET, a self-oscillating multiresonant gate drive was used. This gate driver is conceptually similar to the converter circuits presented in [28], resulting in a gate to source voltage with a pseudosquare wave characteristic that provides fast and efficient commutation of the main semiconductor device without driving the gate-source voltage negative. The average power dissipated in the resonant driver was found to be 350 mW; through subsequent work we have been able to reduce this substantially [29].

TABLE IV
COMPONENTS USED IN 100 MHz DC–DC CONVERTER OF FIG. 16

Component Name	Nominal Value	Manufacturer and Part Style	Part Number	Measured Value
C_{C1}	18 pF +15 pF	CDE Chip-Mica 100V	MC08EA180J MC08EA150J	36.22 pF
C_{C2}	56 pF +7 pF	CDE Chip-Mica 100V	MC12FA560J MC08CA070C	66.5 pF
C_{extra}	10 pF × 2	CDE Chip-Mica 100V	MC08CA100D	
C_{in}	2.2 μF +0.68 μF +0.047 μF × 12	Tantalum 35V Tantalum 35V Ceramic 50V	PCT6225CT PCT6684CT Kemet	
C_R	82 pF +2 pF	CDE Chip-Mica 100V	MC12FA8205 MC08CA020D	
C_{R1}, C_{R2}	15 pF × 2	CDE Chip-Mica 100V	MC08EA150J	C_{R1}=32.6 pF C_{R2}=32 pF
C_{out}	0.1 μF × 19	Kemet Ceramic 50V	C0805C104M5UAC	
D_1, D_2	Schottky Power Diode	ON Semi 60V, 2.0A	MBRS260T3	
L_1	17.5 nH	Coilcraft	B06T6	
L_{C1}	33 nH	Coilcraft	1812SMS-33N	38.1 nH
L_{C2}	68 nH	Coilcraft	1812SMS-68N	69.9 nH
L_{choke}	120 nH × 2	Coilcraft	1812SMS-R12G	
LDMOS		Freescale 70V (max V_{ds})	MRF373ALSR1	
L_R	12.5 nH + Two-turn magnet wire coil +8.9nH board parasitic	Coilcraft	A04TJ 18 AWG	Approx. 22 nH
L_{R1}, L_{R2}	18.5 nH	Coilcraft	A05T	L_{R1} =18.9 nH L_{R2} =18.7 nH

Each of the two resonant rectifiers in Fig. 16 are designed to appear resistive in the sense that the fundamental ac voltage at the rectifier input is largely in phase with the drive current when the rectifier is driven from a sinusoidal current. (The compression network reactances are designed to block the voltage harmonics created by the rectifiers.) The instantaneous power level of the converter varies with input voltage (as expected for a class E inverter). At $V_{\mathrm{dc,out}} = 12$ V, each rectifier is designed to present an equivalent resistance (at the fundamental) ranging from 12 Ω (at an output power of 13.8 W) to 27.4 Ω (at an output power of 5.75 W). These values were arrived at through simulations of the rectifier network over a range corresponding to the approximate instantaneous power levels expected (see Fig. 15) [29], [30]. The rectifier impedance is determined by rectifier output voltage, instantaneous rectifier power (as determined by the input voltage) and resonant components. In this design, we only need to consider operation for an output voltage of 12 V, independent of load resistance. This is because the converter is designed to run under on/off control [1], [23]. In this approach, the entire converter is modulated on and off (at frequencies orders of magnitude lower than the switching frequency) such that the output is always maintained at 12 V. Hence, the rectifier input impedance depends on the input voltage (and instantaneous power as illustrated in Fig. 15), but not on the converter load.

The compression network is designed for a nominal operating frequency of 100 MHz and a center impedance $Z_c = 20$ Ω. Simulations predict a compressed resistance ranging from 21 Ω down to 20 Ω and back up to 22.7 Ω as power ranges from minimum to maximum. Moreover, the compression network is

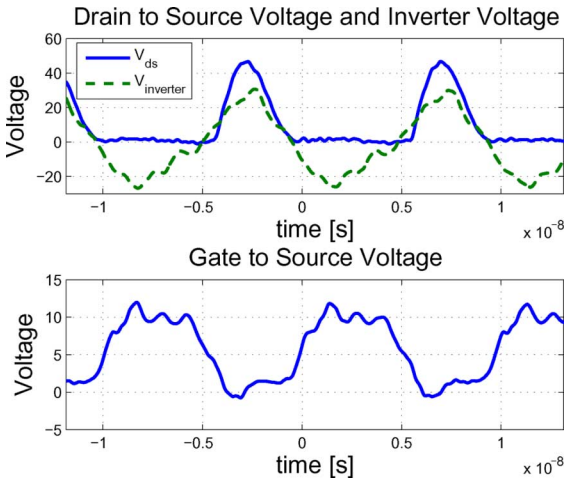

Fig. 13. Drain to source voltage, inverter output voltage, and gate to source voltage of the prototype converter.

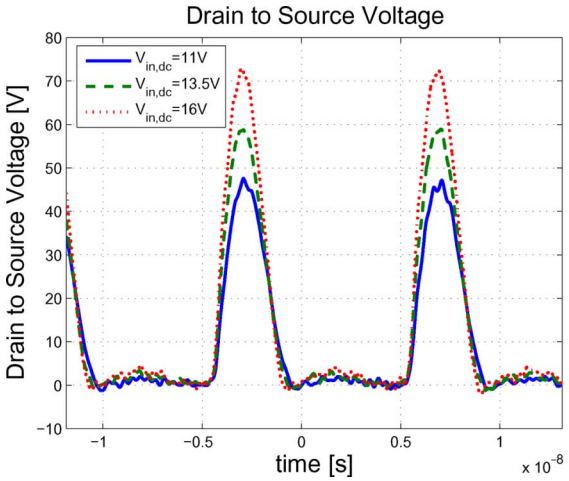

Fig. 14. Drain to source voltage for different input voltages in the range 11 V $\leq V_{in,dc} \leq$ 16 V. The inverter is seen to maintain soft switching over the full range.

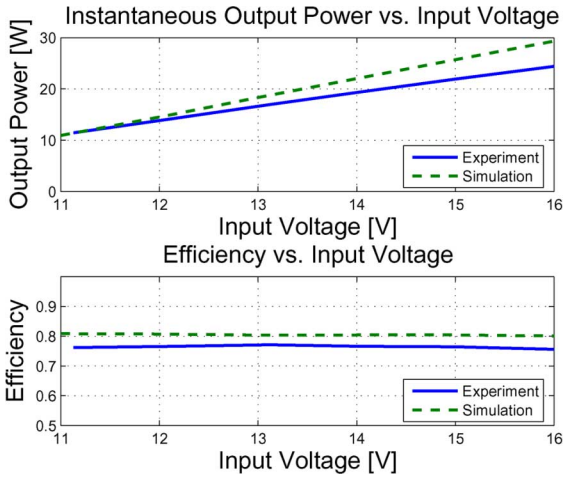

Fig. 15. Experimental and simulated output power and efficiency versus input voltage. Simulations were carried out using PSPICE. The MOSFET was modeled as switched resistor in parallel with a nonlinear capacitor, and the on-state of the diode was modeled with a constant voltage drop plus a series of resistance. Inductor ac and dc ESR values were modeled, while capacitors were treated as ideal.

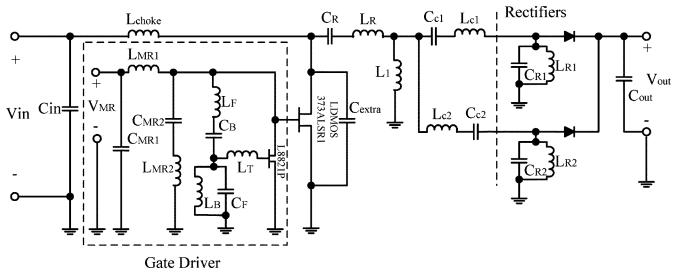

Fig. 16. 100-MHz dc–dc power converter incorporating a resistance compression network.

designed to present a high impedance to dc and harmonics of the fundamental.

To enable the compression network and rectifiers to operate at a convenient impedance level, an L-section matching network is used. This network comprises shunt inductance L_1, with the capacitive portion of the L-section network absorbed as part of the resonant capacitor C_R.

Experimental results support the efficacy of the compression network for providing a desired narrow-range impedance to the inverter as the power level varies with input voltage. Fig. 13 shows experimental waveforms for the converter running at $V_{\mathrm{in,dc}} = 11$ V and $V_{\mathrm{out,dc}} = 12$ V. Shown in the figure are the voltage at the gate of the MOSFET, the drain to source voltage of the device and the voltage at the input of the compression network. It can be appreciated from the figure that zero-voltage turn-on of the LDMOSFET is achieved, indicating a proper impedance match.

Fig. 14 shows V_{ds} at input voltages of 11, 13.5, and 16 V. As can be appreciated from the respective figures, the zero-voltage condition is achieved over the whole input voltage range: a situation that would not occur without the resistance compression network operating as desired.

Fig. 15 shows the output power and the efficiency of the prototype converter. It can be appreciated that the output power has a characteristic roughly proportional to the square of the input voltage, another indication that the compression network is functioning to keep the effective load resistance constant as operating conditions change.

The simulation results for output power match the experimental results well at low input voltage, but depart somewhat as input voltage is increased. We attribute this to the parasitic components and coupling which are not fully modeled in our simulations and which are difficult to measure with sufficient precision to model appropriately. The nonlinear device drain capacitance and resonant inductance (and parasitics at those locations) seem to be particularly important in this regard. It is not surprising that the deviation increases at high voltage, given that both the modeled and actual power behavior are approximately proportional to V_{in}^2. (In the ideal class E inverter, power is proportional to V_{in}^2, with a proportionality constant depending on frequency, duty ratio, resonant component values and load impedance [31].) The effects of any deviations thus scale up rapidly with voltage. Likewise, the simple simulation model

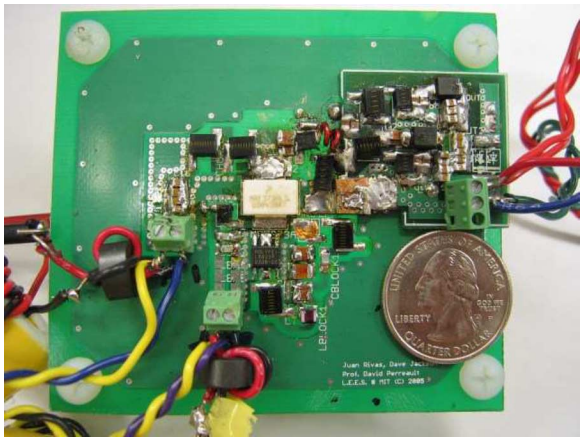

Fig. 17. Prototype dc–dc power converter.

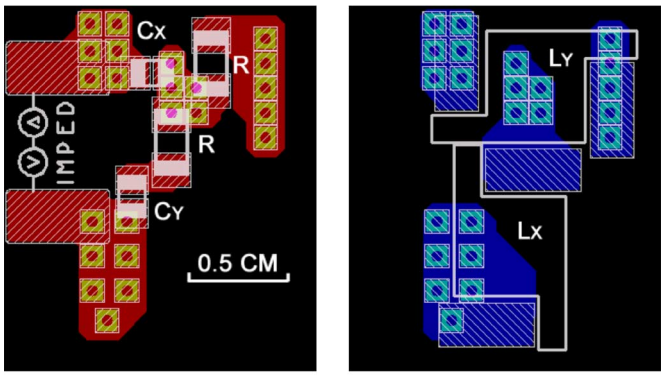

Fig. 18. Layout of four-element compression network test board: (a) top and (b) bottom. This layout is associated with Figs. 6 and 7.

does not account for some loss mechanisms (e.g., conduction losses in traces and interconnects) and so slightly overestimates converter efficiency. Nevertheless, the observed behavior is consistent with proper operation of the compression network, and acceptable for practical purposes.

VI. Conclusion

This document proposes a new class of matching networks that promise a significant reduction in the load sensitivity of resonant converters and RF amplifiers. These networks, which we term resistance compression networks, serve to greatly decrease the variation in effective resistance seen by a tuned RF inverter as loading conditions change. The operation, performance, and design of these networks are explored. The application of resistance compression is demonstrated in a 100-MHz dc–dc converter. Experimental results from this converter confirm the effectiveness of compression networks for reducing load sensitivity of resonant dc–dc converters. It is anticipated that the proposed approach will allow significant improvements in the performance of very high frequency power converters.

Appendix A

Fig. 18 shows the layout of the test board for four-element compression networks associated with Figs. 6 and 7. Capacitors and resistors are soldered on the top side of the printed

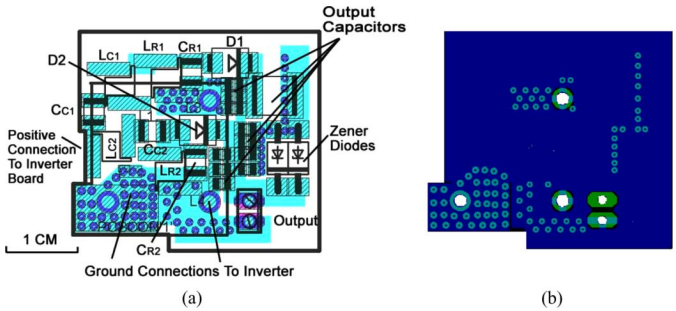

Fig. 19. Compression network and rectifier PCB layout: (a) top and (b) bottom. This layout associated with Figs. 16 and 17 [30].

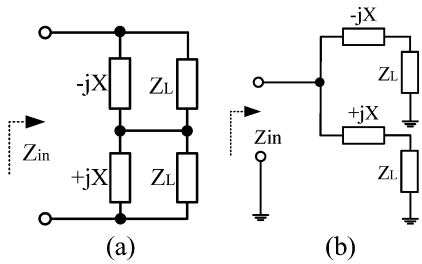

Fig. 20. Impedance compression networks terminated in matched nonresistive loads.

circuit board (PCB) and inductors are soldered on the bottom side. Fig. 19 shows the layout of the resistance compression network and rectifiers for the system demonstrated in Section V. The compression network and rectifier are laid out on a separate board (two-sided 0.064″ thick FR4) from the Class E inverter and control circuits. More details about this design and layout may be found in reference [30].

Appendix B

In many applications where resistance compression is useful, a transformation in the center value of the impedance is also desirable. These functions can be combined in a higher-order compression network. This appendix describes the performance of the four-element resistance compression networks illustrated in Fig. 5.

Four-element resistance compression networks provide an additional degree of design freedom that can be used to implement resistance transformation along with resistance compression. Consider the four-element compression network of Fig. 5(a), where the values X and Y are the reactances of the network branches at the desired operating frequency. Straightforward analysis shows that the input impedance of this network at the specified frequency is resistive, with a value

$$R_{\text{in}} = \frac{X^2}{(X+Y)^2} \cdot \frac{2R}{1+\left(\frac{R}{X+Y}\right)^2}. \tag{13}$$

Examining this equation we can identify a center impedance $Z_c = X + Y$ about which compression of the matched resistances occurs. Moreover, we can identify a transformation factor K_T, defined as

$$K_T = \frac{X^2}{(X+Y)^2}. \tag{14}$$

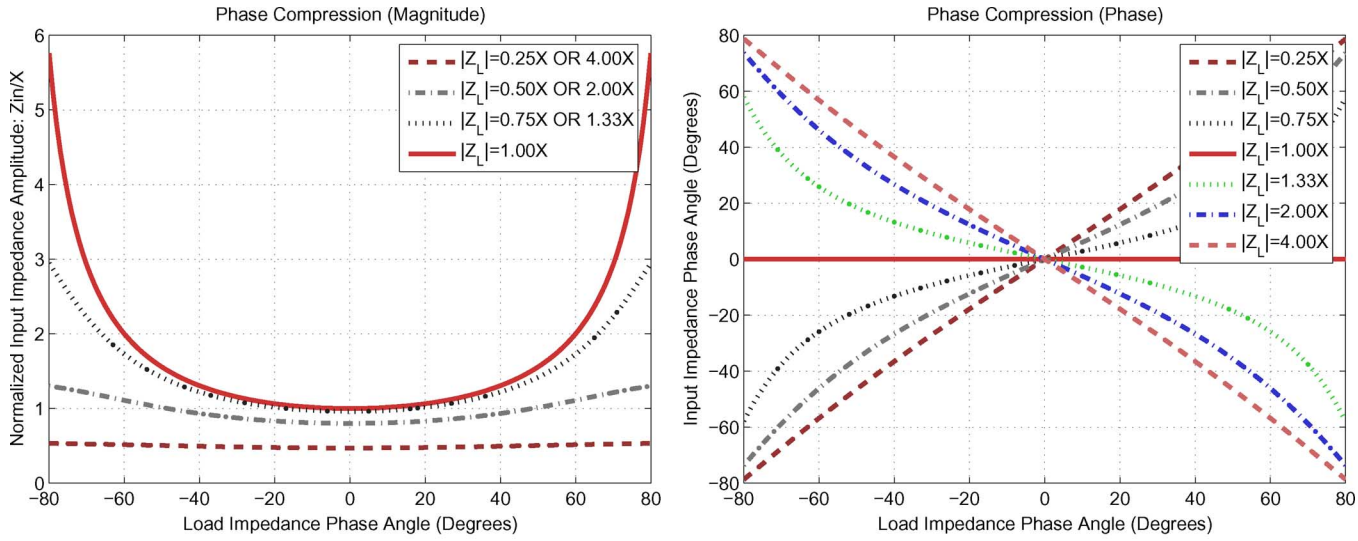

Fig. 21. Z_{in} versus load impedance phase α, parameterized in load impedance magnitude $|Z_L|$ for the topology of Fig. 20(a).

K_T can be observed to be an additional factor by which the input impedance R_{in} is scaled (transformed) as compared to the two-element matching network of Fig. 3(a). That is

$$K_T = \left.\frac{R_{\text{in}}}{Z_c}\right|_{R=Z_c}. \tag{15}$$

There are two distinct possibilities with this four-element matching network. If reactances X and Y have the same sign (that is, both reactances are inductive or both are capacitive at the operating frequency) then K_T will be less than one, and there will be a downward transformation from Z_c to R_{in}. Conversely, if X and Y have opposite sign (one is inductive and the other capacitive) K_T will be greater than one, and there will be an upward impedance transformation from Z_c to R_{in}.

The four-element compression network of Fig. 5(b) can similarly provide transformation along with compression. In particular, the input resistance presented by this network is

$$R_{\text{in}} = \frac{1}{2R}\cdot X^2 \cdot \left[1+\left(\frac{R}{X||Y}\right)^2\right]. \tag{16}$$

The center impedance about which compression will occur is $Z_c = X||Y$. The transformation ratio K_T is

$$K_T = \frac{X^2}{(X||Y)^2}. \tag{17}$$

Appendix C

This appendix considers the behavior of the compression networks of Fig. 3 when the (matched) load impedances are not purely resistive.

As will be shown, if the matched loads are both resistive and reactive, the resistance compression network can serve to transform the load impedances in a manner that makes the network impedance more resistive than the loads, thus providing "phase compression" of the load impedance.

Fig. 20 shows the compression networks of Fig. 3, with the load resistances replaced by complex impedances.

For example, in Fig. 20(a), the load impedance can be expressed as

$$Z_L = R_L + jX_L = |Z_L|\angle\alpha \quad \text{at} \quad \omega = \omega_0 \tag{18}$$

$$|Z_L| = \sqrt{R_L^2 + X_L^2} \quad \text{and} \quad \tan\alpha = \frac{X_L}{R_L}. \tag{19}$$

The input impedance at $\omega = \omega_0$ can be expressed as

$$\begin{aligned} Z_{\text{in}} &= |Z_{\text{in}}|\angle\theta \\ &= \frac{2X^2\left[R_L\left(X^2+|Z_L|^2\right)+jX_L\left(X^2-|Z_L|^2\right)\right]}{\left[R_L^2+(X_L+X)^2\right]\left[R_L^2+(X_L-X)^2\right]} \end{aligned} \tag{20}$$

$$\tan\theta = \frac{X_L}{R_L}\left[\frac{X^2-|Z_L|^2}{X^2+|Z_L|^2}\right] = \tan\alpha\left[\frac{X^2-|Z_L|^2}{X^2+|Z_L|^2}\right]. \tag{21}$$

Since $|(X^2 - |Z_L|^2/(X^2 + |Z_L|^2)| < 1$, we find $|\theta| < |\alpha|$. That is, the magnitude of the input impedance phase angle θ is less than the magnitude of the load phase angle α, thus providing "phase compression"

$$\frac{\tan\theta}{\tan\alpha} = \frac{X^2-|Z_L|^2}{X^2+|Z_L|^2}. \tag{22}$$

If the magnitude of the matched load impedances equals that of the compression network reactances ($|Z_L| = X$), the input impedance is totally resistive for any load phase angle, which means the load reactive component is eliminated. As the magnitude of the matched load impedances deviates from those of the compression network, the compression effect decreases. The amount of phase angle compression achieved for several load impedances is illustrated in Table V.

Fig. 21 plots the normalized magnitude and phase of Z_{in} as a function of load impedance phase α for the circuit of Fig. 20(a). The compression in input impedance magnitude and phase achieved with different load impedance magnitudes can be observed.

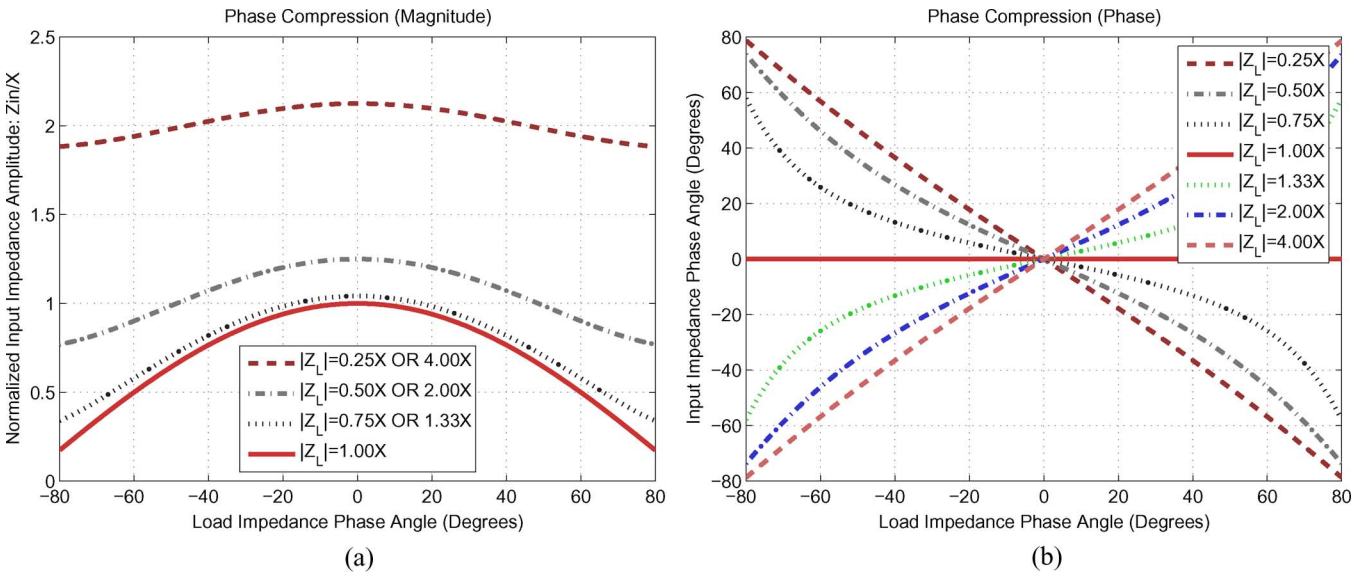

Fig. 22. Z_{in} versus load impedance phase α, parameterized in load impedance magnitude $|Z_L|$ for the topology of Fig. 20(b).

TABLE V
THE θ RANGES FOR DIFFERENT $|Z_L|$ VALUES AND α RANGES

	$-30° \le \alpha \le 30°$	$-45° \le \alpha \le 45°$	$-60° \le \alpha \le 60°$
$\lvert Z_L\rvert = X$	$\theta = 0°$	$\theta = 0°$	$\theta = 0°$
$\lvert Z_L\rvert = 0.75X$ or $1.33X$	$-9.2° \le \theta \le 9.2°$	$-15.6° \le \theta \le 15.6°$	$-25.9° \le \theta \le 25.9°$
$\lvert Z_L\rvert = 0.5X$ or $2X$	$-19.1° \le \theta \le 19.1°$	$-31.0° \le \theta \le 31.0°$	$-46.1° \le \theta \le 46.1°$

The input impedance for the compression network of Fig. 20(b) is:

$$Z_{\text{in}} = |Z_{\text{in}}|\angle\theta = \frac{R_L\left(|Z_L|^2 + X^2\right) + jX_L\left(|Z_L|^2 - X^2\right)}{2|Z_L|^2}. \tag{23}$$

This circuit likewise provides compression of the input impedance angle, with a measure of compression given by

$$\frac{\tan\theta}{\tan\alpha} = \frac{|Z_L|^2 - X^2}{X^2 + |Z_L|^2}. \tag{24}$$

Fig. 22 shows the normalized magnitude and phase of Fig. 20(b) as load impedance angle varies. The anticipated compression in load phase angle is achieved with different loads.

As detailed above, the compression networks of Fig. 20 can provide a limited degree of compensation for nonresistive characteristics of the matched loads. The input impedance of the compression network will be more closely resistive than that of the loads. This effect is quite pronounced for load impedance magnitudes near the impedance magnitude of the compression network.

In order to verify the phase compression calculation of (23) and (24), measurements were carried out using the compression network type in Fig. 20(b). The tested compression networks have the topologies indicated in Fig. 23 and are implemented on PCBs. The loads are purely resistive in Fig. 23(a). The complex load impedance Z_{L1} and Z_{L2} in Fig. 23(b) and (c) are achieved via parallel combinations of resistors and reactive components. Table VI shows component values corresponding

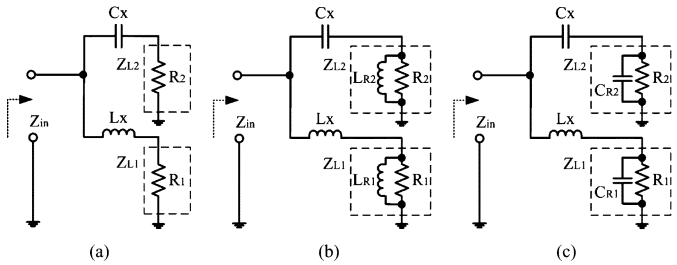

Fig. 23. Topologies of experimental compression networks for testing phase compression effects. The load impedances are purely resistive in (a). Complex load impedances Z_{L1} and Z_{L2} in (b) and (c) are achieved by parallel combinations of resistors and reactive components.

TABLE VI
VALUES OF COMPONENTS USED TO OBTAIN DATA IN TABLE

	L_X	C_X	L_{R1} or C_{R1}	L_{R2} or C_{R2}	R_1	R_2
Fig. 23(a)	47.4 nH	54.0 pF			$29.9\angle 1.7°\ \Omega$	$29.9\angle 1.9°\ \Omega$
Fig. 23(b)	47.4 nH	54.0 pF	56.5 nH	56.2 nH	$54.5\angle 1.4°\ \Omega$	$54.5\angle 1.1°\ \Omega$
Fig. 23(c)	47.4 nH	54.0 pF	45.7 pF	45.5 pF	$54.5\angle 1.4°\ \Omega$	$54.5\angle 1.1°\ \Omega$

TABLE VII
CALCULATED AND MEASURED IMPEDANCES AT A FREQUENCY OF 100 MHz

	X_{LX}	X_{CX}	Z_{L1}	Z_{L2}	Z_{in}	$Z_{in}(Cal)$
Fig. 23(a)	$29.8\ \Omega$	$29.5\ \Omega$	$29.9\angle 1.7°\ \Omega$	$29.9\angle 1.9°\ \Omega$	$30.5\angle 0°\ \Omega$	$29.6\angle 0.1°\ \Omega$
Fig. 23(b)	$29.8\ \Omega$	$29.5\ \Omega$	$29.4\angle 57.3°\ \Omega$	$29.4\angle 57.4°\ \Omega$	$17.1\angle 7.6°\ \Omega$	$15.9\angle -0.4°\ \Omega$
Fig. 23(c)	$29.8\ \Omega$	$29.5\ \Omega$	$29.7\angle -57.0°\ \Omega$	$29.7\angle -57.0°\ \Omega$	$17.9\angle 8.9°\ \Omega$	$16.2\angle 0.2°\ \Omega$

to the topologies in Fig. 23. All these values were measured with an impedance analyzer at a frequency of 100 MHz. The pairs of components such as C_X and L_X, L_{R1} and L_{R2}, C_{R1} and C_{R2}, R_1 and R_2 are carefully selected to make them as matched as possible.

Table VII shows calculated and measured input impedances at a frequency of 100 MHz. The values of X_{LX} and X_{CX} are the reactances of L_X and C_X in Table VI. Z_{L1} and Z_{L2} are load impedances. The load phase angles are approximately 0°, 57°, and $-57°$ in Fig. 23(a)–(c). $Z_{\text{in}}(Cal)$ is the input impedance

calculated by (23), letting $X \approx X_{LX} \approx X_{CX}$ and $Z_L \approx Z_{L1} \approx Z_{L2}$. Because $X \approx |Z_L|$ in Table VII, the calculated input impedance $Z_{\rm in}(Cal)$ has approximate zero phase angle by (24). $Z_{\rm in}$ is the input impedance measured with an impedance analyzer. $Z_{\rm in}$ is close to $Z_{\rm in}(Cal)$. The measured input impedance phases are within approximately 9° of the predicted values, successfully demonstrating the predicted phase compression. The small differences of magnitude and phase between $Z_{\rm in}$ and $Z_{\rm in}(Cal)$ are believed to arise mainly due to parasitic components of the PCB and the limited precision with which we were able to model the components.

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