Switching-Ripple-Based Current Sharing for Paralleled Power Converters

David J. Perreault, *Member, IEEE*, Kenji Sato, *Member, IEEE*, Robert L. Selders, Jr., and John G. Kassakian, *Fellow, IEEE*

Abstract— This paper presents the implementation and experimental evaluation of a new current-sharing technique for paralleled power converters. This technique uses information naturally encoded in the switching ripple to achieve current sharing and requires no intercell connections for communicating this information. Practical implementation of the approach is addressed and an experimental evaluation, based on a three-cell prototype system, is also presented. It is shown that accurate and stable load sharing is obtained over a wide load range. Finally, an alternate implementation of this current-sharing technique is described and evaluated.

Index Terms—Cellular, current sharing, load sharing, modular, parallel.

I. INTRODUCTION

OWER conversion systems are sometimes constructed by paralleling many quasiautonomous power converter cells (Fig. 1). Advantages of such a parallel, or cellular, converter architecture include high performance and reliability, modularity, and the ability to attain large system ratings [1], [2]. One important characteristic of a parallel converter architecture is that the converter cells share the load current equally and stably. Good current-sharing behavior is important for reducing system losses and stresses, for improving system reliability, and for achieving desirable control characteristics. Current sharing is sometimes achieved using a centralized control scheme in which a single (possibly redundant) controller regulates the current balance among cells [3]-[10]. Another approach, often preferred for modularity and reliability reasons, is distributed current-sharing control, in which the cells share information and work together to maintain current sharing.

To implement distributed current-sharing control, only a limited amount of information needs to be shared among cells. If all of the cells are provided with information about the average cell output current, for example, then each cell can adjust its own output current to be close to the average, thereby achieving current sharing with the other cells [11]-[19]. Other quantities can also be used to implement

Manuscript received November 25, 1997; revised November 2, 1998. This work was supported in part by the Bose Foundation and in part by the Office of Naval Research under Grant number N00014-96-1-0524 and in part by equipment grants from the Intel and Tektronix Corporations. The work of K. Sato was supported in part by the Central Japan Railway Company. The work of R. Selders was supported in part by Delco Electronics through the Delco Electronics Scholarship Program. This paper was recommended by Associate Editor M. K. Kazimierczkuk.

The authors are with the Massachusetts Institute of Technology, Laboratory for Electromagnetic and Electronic Systems, Cambridge, MA 02139 USA. Publisher Item Identifier S 1057-7122(99)08100-3.

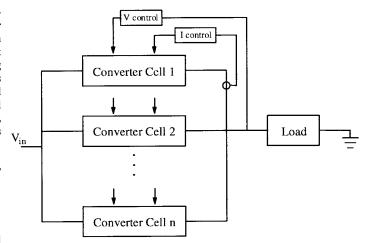


Fig. 1. A cellular converter architecture supplying a single load.

current sharing, including root-mean-square (rms) cell current [20], weighted cell current stress [21], and maximum cell current [22]. The current-sharing information is most often generated and shared across a single interconnection among cells [11]–[19], [21]–[23]. For example, the interconnection circuit may be designed such that if each cell generates a voltage proportional to its output current, then the voltage on the interconnection wire is proportional to the average (or maximum, etc.) of all of the output currents.

The single interconnection approach to generating and distributing current-sharing information is both simple and effective and is widely used. However, a desire to improve the reliability of parallel converter systems has led to the development of distributed current-sharing techniques which do not require direct interconnection of control circuits. Droop methods, in which the voltage drops across the cell output impedances are used to enforce a degree of current sharing and are sometimes used in dc-output applications for this reason [10], [24], [25]. Similarly, in fixed-frequency inverter applications, both voltage and frequency droop are sometimes used to achieve current sharing [26]. Unfortunately, by their nature, droop methods suffer from high-output voltage regulation if accurate current sharing is to be achieved, which is unacceptable in many applications. For example, consider the case of a two-converter system using droop- based current sharing in which each converter has a voltage reference with $\pm 1\%$ tolerance. If a voltage droop of 5% is allowed over the load range, the two converters are only guaranteed to share current to within $\pm 20\%$ of the average at full load, and $\pm 39\%$

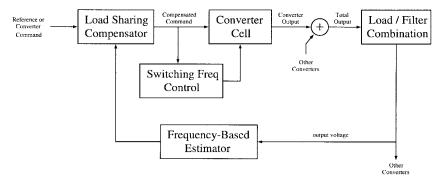


Fig. 2. Schematic representation of the switching-ripple method of current-sharing control.

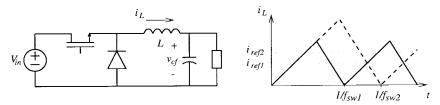


Fig. 3. A buck converter cell operating at the edge of discontinuous conduction. The switching frequency is inversely proportional to the average output current.

at half load. Improving the current sharing requires the use of either a larger voltage droop in the output or more accurate references. The situation does not improve as more converters are paralleled, because the load impedance to be supplied is reduced at the same rate as the net output impedance of the paralleled converter system (droop-based current sharing in the many-converter case is addressed in [24]). What may be concluded is that, despite their reliability advantages, droop methods have limitations which make them unacceptable in many applications.

In this paper, we present a new current-sharing method which requires no additional interconnections among cells and which does not rely on output droop characteristics. It can thus achieve the reliability advantages of the droop approach, without its performance limitations. The new method, which was proposed but not explored in [27] and [28], uses information naturally encoded in the frequency content of the output switching ripple to achieve current sharing among converter cells. The use of the switching ripple to encode current-sharing information falls into the category of frequency-based current-sharing methods proposed in [27]–[29]. The approach described here has a number of performance advantages over the frequency-based approaches explored in [27]–[29], and is quite different from an implementation point of view.

Section II of the paper describes the operation of the new current-sharing method. Section III details one implementation of this method and presents the design of a low-power prototype system. An experimental evaluation of the current-sharing method using the prototype system is presented in Section IV. Section V discusses the application of the approach to systems with different power levels, numbers of converters, and operating frequencies. Section VI describes an alternate implementation of the current-sharing approach and presents an experimental evaluation of it. The final section summarizes the findings of the paper.

II. THE SWITCHING RIPPLE METHOD

This paper considers the switching-ripple method of current-sharing control proposed in [27] and [28] and illustrated in Fig. 2. In this approach, each converter cell is controlled such that its average output current is directly related to its switching frequency. As a result, the frequency content of the aggregate output ripple voltage contains information about the individual cell output currents. Each cell measures the output ripple voltage and uses this information to achieve current balance with the other cells.

Implementing a relationship between the cell output current and the switching frequency is typically straightforward, as many conversion approaches yield a natural relationship between them. For example, controlling the buck converter of Fig. 3 to operate at the edge of discontinuous conduction results in an inverse relationship between the switching frequency and the average output current (equal to the reference current). Conversion approaches which do not exhibit a relationship between the output current and the switching frequency can often be modified to do so. For example, such a relationship could be achieved in a clocked PWM converter by adjusting the clock frequency (and PWM ramp slope) as a function of the output current.

There are many methods by which the information in the aggregate output ripple voltage can be extracted and used to achieve current sharing. In the implementation considered here, each cell employs a frequency estimator which generates a positive (differential) signal when any other cell is operating at a lower switching frequency. Each cell uses this information to adjust its output such that no other cell is operating at a lower switching frequency. The cells thus converge to operate at the same switching frequency and achieve current balance as a result. This approach is simple and robust, and is insensitive to the switching-ripple harmonic content and waveform shape.

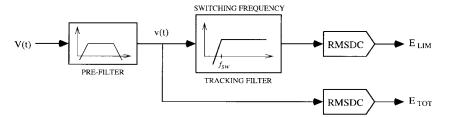


Fig. 4. Structure of the frequency estimator used in the prototype system. $E_{\rm lim}$ is the rms of the filtered ripple, $E_{\rm tot}$ is the rms of the total ripple. These signals are used by the current-sharing controller.

III. PROTOTYPE SYSTEM IMPLEMENTATION

The current-sharing approach is demonstrated using a lowpower three-cell prototype system composed of buck converter cells operating at the edge of discontinuous conduction. Each cell has an inner current control loop, a middle voltage-control loop, and an outer current-sharing control loop. The inner current control loop maintains operation of the cell at the edge of discontinuous conduction and enforces a relationship between the cell switching frequency and the average output current. Current-sharing control is achieved in the prototype system by having each cell adjust its local reference voltage (used by the voltage-control loop) if any other cell is operating at a lower switching frequency. Methods and circuits will be described for controlling cell switching patterns, making estimates of switching-ripple frequency content based on output voltage measurements, and controlling the output voltage and current balance among cells. A more detailed discussion of the design and implementation of the system can be found in [30] and [31].

A. Prototype System Power Stage

The prototype system uses low-power buck converter cells operating at the edge of discontinuous conduction under peak current control. Each cell has an inner current control loop which causes the cell output current to ramp between zero and twice the reference current $i_{\rm ref}$ with an average value of $i_{\rm ref}$ and is designed to handle a peak current of 20 mA, yielding a per-cell load range of 1–10 mA. The system has a total output capacitance C_f of 45 $\mu{\rm F}$ and is resistively loaded.

Operation at the edge of discontinuous conduction yields an average output current (equal to one half of the peak output current) that is inversely proportional to the switching frequency, with the maximum switching frequency set by the minimum load specification of the system. Specifically, for the parameters shown in Fig. 3 and an approximately constant output voltage v_{cf} , we find

$$f_{\rm sw} = \frac{v_{cf}(V_{\rm in} - v_{cf})}{2V_{\rm in}Li_{\rm ref}}.$$
 (1)

For example, in the prototype system, with $L=125~\mathrm{mH}$, $V_{\mathrm{in}}=10~\mathrm{V}$, and $v_{cf}=5~\mathrm{V}$, full load for a cell corresponds to a 1-kHz switching frequency, while a minimum 10% load corresponds to a maximum 10-kHz switching frequency. The cell output current switching ripple causes a very small (<2%) ripple in the output voltage at the same fundamental frequency. It is the frequency content of this output voltage ripple which carries information about the average cell output current.

B. Frequency Estimation

To decode the current-sharing information contained in the output voltage ripple, each cell employs a frequency estimator which detects whether any other cell is operating at a lower switching frequency. The estimator structure used in the prototype system, shown in Fig. 4, is composed of three stages: 1) a prefilter stage, 2) a frequency-tracking filter stage, and 3) an rms-to-dc conversion stage. The prefilter stage removes the low-frequency and high-frequency (noise) components of the output voltage, while amplifying the switching-ripple component. The frequency-tracking filter is a high-pass filter whose cutoff frequency is continuously adjusted to fall just below the local cell switching frequency in order to attenuate switching-ripple components at frequencies below that of the local cell. The rms-to-dc conversion stage measures the rms of the switching-ripple signals before and after the tracking filter. If the rms of the filtered switching ripple is lower than that of the unfiltered ripple, it indicates that one or more cells are operating at switching frequencies below that of the local cell and, therefore, are supplying more current. Thus, the estimator structure of Fig. 4 provides enough information to implement the current-sharing approach described previously.

The prefilter stage is a cascade of a second-order Butterworth high-pass filter ($f_c=500~{\rm Hz}$), a second-order Butterworth low-pass filter ($f_c=40~{\rm kHz}$), and a high-gain frequency-dependent amplifier. The frequency-dependent amplifier compensates for the fact that the magnitude of the voltage ripple across the capacitive output filter decreases with increasing frequency. For frequencies below 20 kHz, it acts as a differentiator to amplify ripple components by an amount proportional to their frequency. Above 20 kHz, it acts as an integrator to attenuate high-frequency noise. The output of the prefilter stage is thus an amplified and frequency-compensated version of the output switching ripple, with high-order switching harmonics (and high-frequency noise) attenuated.

The frequency-tracking filter stage is a fourth-order Butterworth high-pass filter whose cutoff frequency is continuously adjusted to 0.8 times the local switching frequency. A Butterworth filter is selected because it exhibits no peaking in its response near the cutoff frequency. The tracking filter is implemented using an LMF100 switched- capacitor filter whose clock frequency is derived from the local switching frequency.

To achieve the desired tracking filter cutoff frequency, the LMF100 clock frequency must be 80 times the local switching frequency. A frequency multiplier based on the

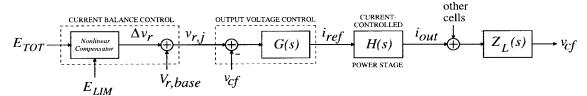


Fig. 5. Block diagram of the cell control structure used in the prototype system.

74VHC4046 phase-locked loop (PLL) IC is used to generate the LMF100 clock from the local gate drive waveform. A divide-by-eighty counter in the feedback path of the PLL yields a switched-capacitor filter clock frequency of 80 times the (input) switching frequency. This results in a tracking filter cutoff frequency of 0.8 times the switching frequency.

The rms-to-dc conversion stage of the frequency estimator measures the rms of the switching-ripple signals before and after the tracking filter. It is implemented using AD637 integrated circuit rms-to-dc converters connected in the two-pole Sallen–Key filter arrangement. The averaging and filter capacitor values ($C_{\rm AV}=0.022~\mu{\rm F},~C_2=C_3=0.047~\mu{\rm F})$ are selected to yield a 1% settling time of 8 ms. This is considered fast enough to track the variations in switching-ripple frequency content, while still suppressing ripple in the rms-to-dc converter outputs. The two rms-to-dc converter outputs form the output of the frequency estimator stage. Any difference between these signals indicates that another cell is operating at a lower switching frequency. This information is used by the current-sharing controller to achieve load balance with the other cells.

C. Control Design

This section describes the design of the control circuitry used in the prototype converter system. A block diagram of the cell control structure used in the prototype system is shown in Fig. 5. In simplest terms, each cell can be viewed as having an inner current control loop, a middle voltage-control loop, and an outer load-sharing control loop. The inner current loop, which maintains cell operation at the edge of discontinuous conduction, causes the average output current $i_{\rm out}$ to accurately track a current reference $i_{\rm ref}$ and allows the cell power stage to be modeled as a controlled current source of value $i_{\rm ref}$ (yielding H(s)=1 in Fig. 5). It also inherently enforces a relationship between the cell switching frequency and average output current, thus encoding current-sharing information on the output switching ripple.

To regulate the output voltage, each cell has a middle voltage-control loop which generates the current reference for its inner loop, based on the difference between a local voltage reference and the output voltage. The prototype system employs a lag compensator ($\tau_p=0.0159, \tau_z=0.00159$, dc gain = 50 mA/V) for this purpose. This yields a voltage-control bandwidth on the order of 100 Hz, with less than 5% load regulation over the load range of the cell. The output of the voltage-control circuit has a clamp to keep the commanded reference current within the specified load range of 1–10 mA.

To achieve load balance among cells, each cell has a slow outer current-sharing loop which operates by adjusting the local reference voltage $v_{\rm ref}$ over a limited range about a base value $v_{r,{\rm base}}$. The individual converter references are shifted via integral control, based on the difference between the two frequency estimator outputs minus a small offset. That is, the system uses the difference between the rms of the total switching ripple and the rms of the switching-ripple components at frequencies of the local cell and higher, minus an additional offset, i.e.,

$$\frac{dv_{r,j}}{dt} = K_j [E_{\text{tot}} - E_{\text{lim}} - \Delta E]$$
 (2)

where K_j is the (integral) control gain, $E_{\rm tot}$ and $E_{\rm lim}$ are the two frequency estimator outputs, and ΔE is the offset. The jth reference is adjustable over a small range from a base value $v_{r,j,{\rm base}}$ to a maximum value $v_{r,j,{\rm max}}$ (which is about 5% larger than the base value) and is prevented from going outside this range. The offset ΔE guarantees that the reference of the lowest switching frequency (highest current) cell will always be driven down toward its base value, so that current sharing can be achieved.

To implement this outer-loop control structure, the prototype system uses the reference adjustment circuitry provided in the UC3907 load-sharing IC. The UC3907 is designed to implement a single-wire current-sharing scheme in which the local voltage reference is adjusted based on the difference between the highest cell current and the local cell current minus a small offset [22]. By properly scaling and shifting the two outputs of the frequency estimator and using them in place of the local and highest current inputs to the UC3907, the UC3907 can instead be caused to adjust its local reference voltage as described above. The integrating compensator implemented in the UC3907 yields a current-sharing control bandwidth on the order of 1 Hz.

The three control loops operate together to properly regulate the output voltage of the system while maintaining current sharing among cells. While other design approaches are possible, this multilayered control strategy has been found to be both simple and effective.

IV. EXPERIMENTAL EVALUATION

This section presents an evaluation of the switching-ripple method of current-sharing control using the three-cell prototype system design presented in the previous section. Additional results can be found in [30]. It should be noted that the approach is independent of the number of cells in the system and can be applied to systems with an arbitrary number of cells. Fig. 6 shows operation of the prototype system

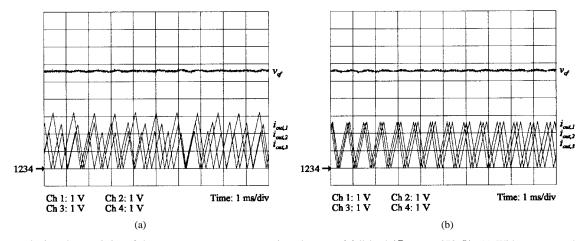


Fig. 6. Current-sharing characteristics of the prototype system at approximately 66% of full load ($R_{\rm load} = 278~\Omega$). (a) Without current-sharing control. (b) With current-sharing control. Current signals are represented at a scale factor of 200 V/A.

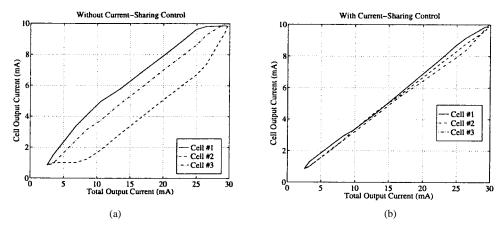


Fig. 7. The static current-sharing characteristic of the prototype system. (a) Without current-sharing control. (b) With current-sharing control.

at approximately 66% of full load, both with and without current-sharing control. Without current-sharing control, there is a significant imbalance in average output current among the three cells. The inverse relationship between switching frequency and average output current is also apparent. With current-sharing control, the switching frequencies and average cell output currents are almost precisely equal. This high degree of current sharing is achieved by using the information encoded in the frequency content of the output switching ripple, without additional interconnections.

Fig. 7 shows the static current-sharing characteristic over the load range of the system both with and without current-sharing control. Without current sharing, there are significant current imbalances over much of the load range, while with current sharing the cells share current to within 5% of the average over the entire load range. This high degree of active current sharing is obtained with less than 5% load regulation over the entire load range.

Current-sharing behavior was also investigated under transient conditions. Fig. 8 shows the current-sharing behavior for load steps between 673 and 224 Ω , corresponding to approximately 27 and 83% of full load. The current-sharing behavior is seen to be stable for even large load steps. Fig. 9 shows the reference current transient response for two cells

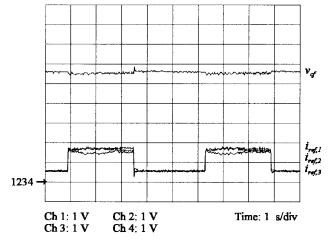


Fig. 8. Transient response for load steps between 224 and 673 Ω (approximately 27 and 83% of full load). Currents are represented at 200 V/A.

when current-sharing control is turned on. Again, accurate current sharing is rapidly achieved with stable dynamics. What may be concluded from these results is that the switching-ripple method can be used to achieve accurate static and dynamic current sharing without the need for additional interconnections among cells.

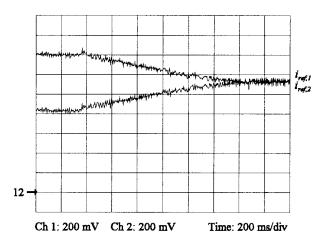


Fig. 9. Current reference transient response for two cells when current sharing is turned on with $R_L = 500 \Omega$. Currents are represented at 200 V/A.

V. SCALING OF THE APPROACH

The new current-sharing approach described in this paper has been evaluated using a low-power prototype converter system operating at switching frequencies in the 1–10 kHz range. In this section, we describe how the implementation and effectiveness of the new current-sharing method is expected to scale for systems operating at higher voltage and current levels, at higher switching frequencies, and for different numbers of paralleled converters.

We first address how the new current-sharing approach scales to systems operating at higher voltage and/or current levels than the prototype system. Beginning with the lowpower prototype converter system described in the previous sections, we consider scaling the design in the following manner. First, consider scaling the inverse of the converter inductances, the inverse of the current sensor gains, the output capacitances, and the inverse of the load resistance by a factor k. This will yield a system in which all the waveform shapes and frequencies remain identical to those in the prototype system. The voltages will remain exactly the same as those in the prototype system, while the current levels will be exactly a factor k larger. (That is, the current waveforms will be scaled in magnitude by a factor of k, while all the other waveforms and sensed signals remain invariant to this transformation.) From the standpoint of the control circuitry (including the current-sharing controller), this scaled system is identical to the prototype system and should exhibit precisely the same behavior. Similarly, if the input voltage, the inductances, the inverse of the capacitances, the inverse of the voltage sensor gains, and the load resistance are all scaled by a factor of k, we will again obtain a system which has the same waveform shapes and frequencies as the prototype system. In this case, however, the current waveforms will remain the same as the prototype system, and the voltage waveforms will be scaled by a factor of k. Again, all the waveforms sensed by the control circuitry remain invariant to the scaling, and the scaled system will exhibit the same current-sharing behavior as the prototype system. In principle, therefore, the new current-sharing method is directly applicable to systems operating at much higher voltage and/or current levels than the prototype system. The

main practical limiting factor is the higher noise levels seen by the control circuitry as the power level increases. However, the control circuitry used to implement the new current-sharing method does not appear to be significantly more susceptible to noise than that used in many widely employed current-sharing techniques. We thus conclude that the new current-sharing method is directly applicable to systems operating at a wide range of voltage and current levels.

A second issue is how the approach scales with increases in the switching frequency. It is straightforward to develop a system scaling similar to the previous ones, which preserves signal magnitudes and waveform shapes, but increases the operating frequency by a factor k. The primary question to be answered is whether the control circuitry can be modified to accommodate this increase in frequency. For switching frequencies of up to several hundred kilohertz, appropriate modifications of the voltage control and current-balancing control compensators (Fig. 5) and the first and last stages of the frequency estimator (Fig. 4) are easily accommodated through simple component changes. However, modification of the frequency-tracking filter stage of the frequency estimator does require additional consideration. The frequency-tracking filter in the prototype system is implemented using a switchedcapacitor filter circuit, whose cutoff frequency is continuously adjusted to track the cells switching frequency. For switching frequencies of up to several tens of kilohertz, this is an effective approach. At higher switching frequencies, however, it becomes difficult to implement the tracking filter function in this manner due to the lack of appropriate switched-capacitor filter IC's. Nevertheless, the tracking filter function (a highpass filter with a voltage-controlled cutoff frequency) can easily be implemented for higher frequencies through other means. It is straightforward to construct filters with voltagecontrolled cutoff frequencies by combining fixed elements with voltage-controlled impedances (see [33] and the references therein). For example, a voltage-controlled resistance [34], [35] can be used with a fixed capacitor to create a controlled first-order Butterworth filter. Thus, we conclude that the new current-sharing approach can be directly employed for switching frequencies of up to several tens of kilohertz and is useful for switching frequencies of up to at least several hundred kilohertz, with only minor implementation modifications.

A final issue is how the approach will scale with different numbers of converters in parallel, particularly with respect to the magnitude of the feedback signals. We assume that each cell is provided with its own output capacitor, so that the output capacitance of the system is proportional to the number of cells paralleled. In this case, the output voltage ripple would be entirely invariant to the number of cells paralleled if the ripple signals were at the same fundamental frequency and synchronized in time. However, in practice, the switching frequencies are never quite synchronized in frequency or phase, even when the desired degree of current sharing is established. Nevertheless, using the ripple analysis techniques for paralleled converters developed in [36] and [37], it can be shown that even though the frequencies and phases of the individual ripple signals are not identical, the peak ripple

magnitude will remain constant as the number of converters changes, while the rms ripple magnitude will be proportional to $N^{-1/2}$, where N is the number of cells in parallel. Therefore, if the number of paralleled converters paralleled is changed by a factor of ten, the peak ripple-signal magnitude will stay constant, and the rms ripple-signal magnitude will vary only by a factor of about 3.2. We thus conclude that the magnitude of the ripple signal used to implement the current-sharing control is relatively insensitive to the number of converters paralleled and that it is feasible to use this current-sharing approach even in systems where the number of cells in parallel can vary widely.

From the results of this section we draw three conclusions. First, the new current-sharing method is directly applicable to paralleled converter systems operating at many different voltage, current, and power levels. Second, the current-sharing method is applicable to systems with switching frequencies of up to at least several hundred kilohertz, and perhaps higher. Finally, the signal levels used to implement the current-sharing scheme are relatively insensitive to the number of converters paralleled, so the approach is applicable even when the number of paralleled converters can vary widely.

VI. AN ALTERNATE IMPLEMENTATION

The simple and effective current-sharing control implementation described in the previous sections operates by indirectly extracting current-sharing information from the switching-ripple frequency content and using it to enforce current sharing. However, given that the output voltage harmonic content contains information about the individual cell currents, it is reasonable to ask if quantities such as the average or rms cell currents can be directly extracted from the output voltage harmonic content for use in current-sharing control. This section explores that possibility and examines the advantages and disadvantages of such an approach. For simplicity and consistency, a cellular system composed of buck converter cells operating at the edge of discontinuous conduction will again be considered.

A. An Rms Current Estimator

The switching frequency and ripple current harmonic content of a converter cell operating at the edge of discontinuous conduction is uniquely related to its average output current. Thus, the aggregate voltage ripple due to paralleled cells operating at the edge of discontinuous conduction contains information about the individual cell output currents. Here we present a method for estimating the rms of the cell reference currents for such a system directly from the output voltage ripple. The rms of the cell reference currents for an N-cell converter system is defined as

$$i_{\rm rms}(t) = \sqrt{\frac{\sum_{k=1}^{N} i_{{\rm ref},k}^2}{N}}$$
 (3)

where $i_{{\rm ref},k}$ is the reference current (or equivalently, the average output current) of the kth cell. Knowledge of the

rms of the cell currents can be used by the individual cells to implement a current-sharing control scheme.

Consider the relationship between the reference current, switching frequency, and harmonic content of a buck converter cell operating at the edge of discontinuous conduction. The output current of the kth cell can be written as a Fourier series

$$I_{k} = \sum_{n=-\infty}^{\infty} C_{n,k} \delta(\omega - n\omega_{k})$$
 (4)

where ω_k is given by

$$\omega_k = \frac{\pi v_{cf} (V_{\text{in}} - v_{cf})}{V_{\text{in}} L i_{\text{ref},k}}.$$
 (5)

Approximating the output current as a piecewise-linear function (i.e., a triangle wave), the nth Fourier coefficient for the output current of the kth cell can be expressed as

$$C_{n,k} = \frac{m_2}{2\pi n^2 \omega_k} (1 - e^{jn\omega_k \Delta t_2}) - \frac{m_2 \Delta t_2}{2\pi j n} e^{jn\omega_k \Delta t_2} + \frac{m_1}{2\pi n^2 \omega_k} (e^{-jn\omega_k \Delta t_1} - 1) - \frac{m_1 \Delta t_1}{2\pi j n} e^{-jn\omega_k \Delta t_1}$$
(6)

where $m_1 = (V_{\rm in} - v_{cf})/L, m_2 = -v_{cf}/L, \Delta t_1 = 2i_{{\rm ref},k}/m_1$, and $\Delta t_2 = -2i_{{\rm ref},k}/m_2$ [32]. For the ripple component of $i_k, C_{0,k} = 0$, while all other terms are given by (6).

Careful examination of (5) and (6) reveals that the values $C_{n,k}$ are proportional to $i_{\text{ref},k}$, while ω_k is inversely proportional to $i_{\text{ref},k}$. This is due to the fact that the shape of $i_k(t)$ is invariant to the value of $i_{\text{ref},k}$; the waveform is merely scaled in time and magnitude for different values of $i_{\text{ref},k}$, as illustrated in Fig. 3. Recognizing this, we can define normalized variables which are independent of $i_{\text{ref},k}$:

$$\hat{C}_n = \frac{C_{n,k}}{i_{\text{ref},k}} \tag{7}$$

and

$$\hat{\omega} = \omega_k \cdot i_{\text{ref},k}. \tag{8}$$

Because the normalized variables are independent of $i_{\text{ref},k}$, they are the same for every converter cell, provided that the cells are identical.

Using this normalized variable representation and employing power spectral analysis, the rms values of some important circuit waveforms and their derivatives can be computed to be

$$rms\{\tilde{i}_k(t)\} = \sqrt{i_{ref,k}^2 \sum_n |\hat{C}_n|^2}$$
 (9)

$$\operatorname{rms}\{\tilde{i}'_k(t)\} = \sqrt{\hat{\omega}^2 \sum_n |n\hat{C}_n|^2}$$
 (10)

$$\operatorname{rms}\{\tilde{v}_{cf}'(t)\} = \sqrt{\left[\frac{1}{C_f^2} \sum_{n} |\hat{C}_n|^2\right] \cdot \sum_{k=1}^{n} i_{\operatorname{ref},k}^2}$$
 (11)

$$\operatorname{rms}\{\tilde{v}_{cf}''(t)\} = \sqrt{\left[\frac{\hat{\omega}^2}{C_f^2} \sum_{n} |n\hat{C}_n|^2\right] \cdot N}$$
 (12)

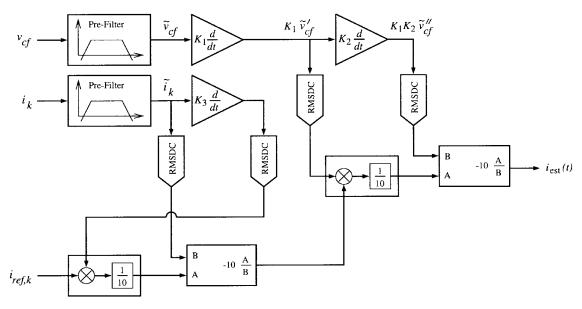


Fig. 10. Functional block diagram of the prototype rms reference current estimator.

where we denote the ac components of waveforms with a tilde and assume that the load impedance is much greater than the filter capacitor impedance for the switching frequency and above. These computations can be used for the purpose of calculating the rms of the cell currents. Taking the ratio of (11) to (12) yields a quantity that is proportional to the rms of the cell currents

$$\frac{\text{rms}\{\tilde{v}'_{cf}(t)\}}{\text{rms}\{\tilde{v}''_{cf}(t)\}} = \sqrt{\left[\frac{\sum_{n} |\hat{C}_{n}|^{2}}{\hat{\omega}^{2} \sum_{n} |n\hat{C}_{n}|^{2}}\right] \cdot \frac{\sum_{k=1}^{n} i_{\text{ref},k}^{2}}{N}}.$$
 (13)

To cancel the proportionality constant in (13), we multiply by the ratio of (10) to (9) and also multiply each side by $i_{\text{ref},k}$. This yields the desired estimate of the rms of the cell currents

$$i_{\text{est}} = \frac{\text{rms}\{\tilde{v}'_{cf}(t)\} \text{ rms}\{\tilde{i}'_{k}(t)\}i_{\text{ref},k}}{\text{rms}\{\tilde{v}''_{cf}(t)\} \text{ rms}\{\tilde{i}_{k}(t)\}}$$
$$= \sqrt{\frac{\sum_{k=1}^{n} i_{\text{ref},k}^{2}}{N}}.$$
 (14)

This result means that by properly combining the rms values of the ac components of i_k and v_{cf} and their derivatives, the rms of the cell currents can be computed. The value of this result is that while all of the quantities on the top line of (14) can be measured or computed locally at each cell, their combination computes the rms of all of the cell output currents. This is possible because the output voltage ripple and its derivatives contain information about all of the cell currents, as seen in (11) and (12). The additional factors in (14) compute needed proportionality constants in an in-line fashion, without requiring a priori knowledge of the circuit parameters or operating point. Also note that the computation does not require a priori knowledge of the number of cells, since this

information is implicitly contained in (12). In summary, (14) allows computation of the rms of the cell reference currents using only information locally measurable at each cell, without requiring *a priori* knowledge of the number of cells, circuit parameters, or operating point. This information can, in turn, be used to implement current-sharing control.

B. Rms Current Estimator Implementation

The implementation of an rms estimator based on (14) is significantly more complicated than that of the estimator structure presented in Section III. Nevertheless, a direct implementation of the estimator in analog circuitry is quite possible, as is an equivalent microprocessor-based implementation. Here, we briefly describe an analog implementation of an rms cell current estimator based on (14).

The estimator implements the following rms current estimation equation

$$i_{\text{est}}(t) = \frac{\text{rmsdc}\{K_1 \tilde{v}'_{cf}(t)\} \text{ rmsdc}\{K_3 \tilde{i}'_k(t)\} i_{\text{ref},k}}{\text{rmsdc}\{K_1 K_2 \tilde{v}''_{cf}(t)\} \text{ rmsdc}\{\tilde{i}_k(t)\}}$$
(15)

where rmsdc denotes operation of a conventional integrated circuit rms-to-dc converter and K_1, K_2 , and K_3 are scaling constants used to keep intermediate computations in range. A functional block diagram of the implemented estimator circuit is shown in Fig. 10. Detailed circuit diagrams for the estimator may be found in [31], [32]. The estimator of Fig. 10 is composed of four stages: 1) a prefilter stage, 2) a gain and differentiation stage, 3) an rms-to-dc conversion stage, and 4) a multiplication and division stage. The estimator is designed to be used with converter cells of the type described in Section III operating within a load current range of 1–10 mA (which corresponds to a 1–10 kHz switching frequency range).

The prefilter stage comprises a pair of bandpass filters which isolate the ripple components of the output voltage and local-cell current signals, respectively. The bandpass filters attenuate both the low-frequency and high-frequency

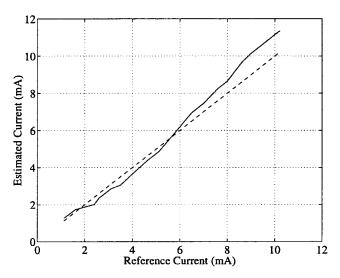


Fig. 11. Estimation performance of the rms reference current estimator with a single cell. The dashed line is the actual output current of the cell, while the solid line is the estimated current.

(noise) components of the measured signals, while passing the ripple-frequency components. The gain and differentiation stage computes the required derivatives of \tilde{v}_{cf} and \tilde{i}_k and provides the proper signal scaling for the remaining stages. Band-limited differentiator circuits are used which act as differentiators for the frequency range of interest, but whose gains roll off at high frequencies in order to attenuate high-frequency noise. The rms-to-dc conversion stage computes local-time approximations to the rms values of the required signals. The effects of using such local-time approximations to the rms (in terms of frequency resolution and response speed) are addressed in [28] and [31]. The multiplication and division stage computes the final estimate from the different factors in (15).

C. Experimental Results and Evaluation

An rms current estimator of the described design was constructed and used with a single converter cell of the type described in Section III. The estimator was tested by using it to estimate the cell's own reference current over the load range. [For a single cell, the rms reference current of all cells equals the cell's own reference current, as per (3)]. As illustrated in Fig. 11, the results of this test indicate that while the rms current estimator does track the reference current, estimation errors as high as 10% occur over the load range.

Careful examination of the operation of the circuit revealed two primary sources of estimation error. The first source of error is the inaccuracies and approximations in modeling the converter waveforms. Second-order ripple effects, filter capacitor ESR, and semiconductor device drops all contribute to the circuit waveforms deviating from the idealized approximations used to design the estimator and result in the shape of $i_k(t)$ not being quite invariant to the value of $i_{\mathrm{ref},k}$. This leads to significant estimation errors, especially at high reference current levels. In general, it may be concluded that the accuracy of this type of estimation approach depends heavily on the modeling assumptions used in its development.

This contrasts markedly with the estimation approach taken in Section III, which is insensitive to waveform shape and harmonic content.

Perhaps a more significant source of error is the susceptibility of the estimator to noise. The estimator structure uses a cascade of differentiators to extract information about the cell currents from the voltage ripple waveform (Fig. 10). It was found that the differentiator cascade heavily amplifies the inevitable switching noise. This heavily-amplified noise component is captured by the rms-to-dc conversion stage and affects the final estimate. This estimator structure is thus unlikely to be practical in the high-noise environment of a full-power switching converter system.

The presented method for estimating the rms of the cell currents is thus not viable in this particular case. It is the relationship between the output current and the output switching ripple in this converter that makes the estimation task especially difficult; estimation of other quantities or with a control strategy yielding a different output current/switching-ripple relationship may produce very different results. Thus, while the approach we have presented for deriving and implementing the estimator may not be advantageous in this case, it may be quite useful in the development of estimators for other quantities, or for use with other converter types.

VII. CONCLUSIONS

This paper presents the implementation and experimental evaluation of a new current-sharing approach for paralleled power converters. This approach, which is based on encoding the current-sharing information in the switching ripple of the converter cells, eliminates the need for additional currentsharing interconnections among converters. One practical implementation of the approach is addressed, including methods for controlling the cell switching patterns, decoding the current-sharing information from the output switching ripple, and controlling the output voltage and current sharing. An experimental evaluation of the new current-sharing approach based on a three-cell prototype system is also presented. It is shown that accurate and stable current sharing is obtainable over a wide load range using this approach. It is also argued that the implemented approach is applicable to converters in many voltage, current, and switching frequency regimes, and that it is practical even if the number of paralleled converters can vary widely. Finally, an alternative method for extracting current-sharing information from the switching ripple is described and evaluated.

ACKNOWLEDGMENT

The authors thank the anonymous reviewers for their useful comments and suggestions.

REFERENCES

- J. G. Kassakian, "High frequency switching and distributed conversion in power electronic systems," in *Proc. Sixth Conf. Power Electronics Motion Control (PEMC 90)*. Budanest, Hungary, 1990.
- Motion Control (PEMC 90), Budapest, Hungary, 1990.
 [2] J. G. Kassakian and D. J. Perreault, "An assessment of cellular architectures for large converter systems," in Proc. First Int. Conf. Power Electronics Motion Control, Beijing, China, 1994, pp. 70–79.

- [3] H. Huisman and B. Gravendeel, "A modular and versatile control method for phase-staggering multiple power converters," in Proc. European Power Electronics Conf., 1989, pp. 959-963.
- [4] K. Siri, C. Lee, and T. Wu, "Current distribution control for parallel connected converters: Part I," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 28, pp. 829-840, July, 1992.
- F. Petruzziello, P. Ziogas, and G. Joos, "A novel approach to paralleling of power converter units with true redundancy," in Proc. IEEE Power Electronics Specialists Conf., 1990, pp. 808–813. [6] J. Holtz, W. Lokzat, and K. Werner, "A high-power multitransistor-
- inverter uninterruptible power supply system," IEEE Trans. Power Electron., vol. 3, pp. 278-285, July 1988.
- [7] J. Holtz and K. Werner, "Multi-inverter UPS system with redundant load sharing control," IEEE Trans. Power Electron., vol. 37, pp. 506-513, Dec. 1990.
- [8] J. Chen and C. Chu, "Combination voltage-controlled and currentcontrolled PWM inverters for UPS parallel operation," IEEE Trans. Power Electron., vol. 10, Sept. 1995.
- [9] S. J. Chiang, C. M. Liaw, W. C. Chang, and W. Y. Chang, "Multimodule parallel small battery energy storage system," IEEE Trans. Energy Conversion, vol. 11, pp. 146-154, Mar. 1996.
- [10] J. Dixon and B. Ooi, "Series and parallel operation of hysteresis currentcontrolled PWM rectifiers," IEEE Trans. Ind. Applicat., vol. 25, pp. 644-645, July/Aug. 1989.
- [11] L. Walker, "Parallel redundant operation of static power converters," in Proc. IEEE Industry Applications Society Ann. Meeting, 1973, pp.
- [12] T. Kawabata and S. Higashino, "Parallel operation of voltage source inverters," IEEE Trans. Ind. Applicat., vol. 24, pp. 281-287, Mar./Apr.
- K. T. Small, "Single wire current share paralleling of power supplies," U.S. Patent 4717833, 1988.
- [14] R. Wu, T. Kohama, Y. Kodera, T. Ninomiya, and F. Ihara, "Loadcurrent-sharing control for parallel operation of DC-to-DC converters," in Proc. IEEE Power Electronics Specialists Conf., 1993, pp. 101-107.
- [15] T. Kohama, T. Ninomiya, M. Shoyama, and F. Ihara, "Dynamic analysis of parallel module converter system with current balance controllers," in 1994 IEEE Telecommunications Energy Conf. Rec., 1994, pp. 190-195.
- [16] T. Kohama, T. Ninomiya, M. Wakamatsu, and M. Shoyama, "Static and dynamic response of a parallel-module high power-factor converter system with current-balancing controllers," in Proc. IEEE Power Electronics Specialists Conf., 1996, pp. 1198-1203.
- [17] M. Jovanovic, D. Crow, and L. Fang-Yi, "A novel, low-cost implementation of 'Democratic' load-current sharing of paralleled converter modules," IEEE Trans. Power Electron., vol. 11, pp. 604-611, July
- [18] V. J. Thottuvelil and G. C. Verghese, "Stability analysis of paralleled DC/DC converters with active current sharing," in Proc. IEEE Power Electronics Specialists Conf., 1996, pp. 1080-1086.
- ., "Analysis and control design of paralleled DC/DC converters with current sharing," IEEE Trans. Power Electron., vol. 13, pp. 635-644, July 1998.
- [20] M. Youn and R. Hoft, "Analysis of parallel operation of inverters," in Proc. IEEE Industry Applications Society Ann. Meeting, 1976, pp. 951-958.
- [21] D. Maliniak, "Dense DC-DC converters actively share stress," Electron. Design, pp. 39-44, Jan. 21, 1993.
- [22] M. Jordan, "UC3907 load share IC simplifies parallel power supply design," Unitrode Corp., Merrimack, NH, Unitrode Application Note
- [23] Y. Panov, J. Rajagopalan, and F. C. Lee, "Analysis and design of Nparalleled DC-DC converters with master-slave current-sharing control," in Proc. 1997 IEEE Applied Power Electronics Conf., Feb. 1997, pp. 436-442.
- [24] J. Bocek and C. Liu, "Determining current sharing criterion for parallel operation of power converters in multi-module bus systems," in Proc. IEEE Power Electronics Specialists Conf., 1990, pp. 870-879.
- [25] J. Glaser and A. Witulski, "Output plane analysis of load-sharing in multiple-module converter systems," IEEE Trans. Power Electron., vol. 9, pp. 43-50, Jan. 1994.
- [26] M. Chandorkar, D. Divan, and R. Adapa, "Control of parallel connected inverters in stand-alone AC supply systems," in Proc. IEEE Industry Application Society Ann. Meeting, 1991, pp. 1003-1009.
- [27] D. J. Perreault, R. Selders, and J. G. Kassakian, "Frequency-based current-sharing techniques for paralleled power converters," in Proc. 1996 IEEE Power Electronics Specialists Conf., Baveno, Italy, June

- power converters," IEEE Trans. Power Electron., vol. 13, pp. 626-634, July 1998.
- _, "Implementation and evaluation of a frequency-based currentsharing technique for cellular converter systems," in Proc. IEEE Africon '96, Matieland, South Africa, Sept. 1996, pp. 682-686.
- [30] K. Sato, "A switching ripple based current sharing control system for cellular converters," S.M. thesis, Massachusetts Inst. Technol. Dept. Electrical Eng. Computer Sci., June 1997.
- [31] D. Perreault, "Design and evaluation of cellular power converter ar-chitectures," Ph.D. dissertation, Massachusetts Inst. Technol. Dept. Electrical Eng. Computer Sci., June 1997.
- R. L. Selders, "A current-balancing control system for cellular power converters," S.M. thesis, Massachusetts Inst. Technol. Dept. Electrical Eng. Computer Sci., Feb. 1996.
- [33] A. Leuciuc and L. Goras, "New general immittance converter JFET voltage-controlled impedances and their applications to controlled biquads synthesis," IEEE Trans. Circuits Syst. I, vol. 45, pp. 678-682, June 1998.
- J. L. Huertas, J. I. Acha, and A. Gago, "Design of general voltageor current-controlled resistive elements and their applications to the synthesis of nonlinear networks," IEEE Trans. Circuits Syst., vol. CAS-27, pp. 92-103, Feb. 1980.
- [35] K. Nay and A. Budak, "A voltage-controlled resistance with wide dynamic range and low distortion," IEEE Trans. Circuits Syst., vol. CAS-30, pp. 770-772, Oct. 1983.
- [36] D. J. Perreault and J. G. Kassakian, "Analysis and control of a cellular converter system with stochastic ripple cancellation and minimal magnetics," IEEE Trans. Power Electron., vol. 11, pp. 145-152, Nov.
- , "Distributed interleaving of paralleled power converters," IEEE Trans. Circuits Syst. I, vol. 44, pp. 728-734, Aug. 1997.
- [38] D. J. Perreault, K. Sato, and J. G. Kassakian, "Switching-ripple-based current sharing for paralleled power converters," in Proc. Power Conversion Conf.—Nagaoka, Nagaoka, Japan, 1997, pp. 473-478.



David J. Perreault (S'91-M'97) was born in North Providence, RI, on January 22, 1967. He received the B.S. degree in electrical engineering from Boston University, Boston, MA, in 1989, and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1991 and 1997.

He is currently a Research Scientist in the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, where his work includes the investigation of new

methods for the design and control of power electronic systems.

Dr. Perreault is a member of Tau Beta Pi, Sigma Xi, and the National Society of Professional Engineers.



Kenji Sato (S'97-M'98) was born in Tokyo, Japan, on May 8, 1966. He received the B.S. and M.E. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1989 and 1991, respectively, and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1997.

In 1991 he joined the Central Japan Railway Company (JR Central), Tokyo, Japan, where he has been engaged in the development and design of the power conversion systems of the Shinkansen

Train (or "bullet train"). From 1995 to 1997 he was involved in research on paralleled power converters at the Massachusetts Institute of Technology. He currently works on a next-generation high-speed train project at JR Central.

Mr. Sato is a member of the Institute of Electrical Engineers of Japan.



Robert L. Selders, Jr. was born in Tacoma, WA, in 1970. He received the B.S. degree in electrical engineering from Southern University and A & M College, Baton Rouge, LA, in 1993 and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology in 1996.

He is presently with Delphi Delco Electronics Systems, Kokomo, IN, where he is engaged in the development and design of adaptive restraint technologies and systems for the Restraint System Electronics (RSE), Electrical Competency Group

and leading electrical design activities to bring these new technologies to production readiness.



John G. Kassakian (S'65-M'73-SM'80-F'89) received the Sc.D degree from the Massachusetts Institute of Technology (MIT), Cambridge, in 1973.

He is a professor of Electrical Engineering and Director for the MIT Laboratory for Electromagnetic and Electronic Systems. His fields of expertise are power electronics and automotive electrical systems, and he serves as a consultant to government and industry. He has published extensively in the area of power electronics, and is a coauthor of the textbook Principles of Power Electronics.

Dr. Kassakian was the Founding President of the IEEE Power Electronics Society and serves as the U.S. representative to the European Power Electronics Society. He is the recipient of the IEEE Centennial Medal, the IEEE William E. Newell Award, the IEEE Distinguished Lectureship Award, and the Distinguished Service Award. In 1993, he was elected to the National Academy of Engineering.