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A CMOS-Based Energy Harvesting Approach for Laterally-Arrayed Multi-Bandgap Concentrated Photovoltaic Systems

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***Abstract*—This paper presents an energy harvesting approach for a Concentrated Photovoltaic (CPV) system based on cell-block-level integrated CMOS converters. The CPV system, built upon the Laterally-Arrayed Multi-Bandgap (LAMB) cell structure, is a potentially higher-efficiency and lower-cost alternative to traditional Tandem-based systems. The individual cells within a sub-module block are connected for approximate voltage matching, and a Multi-Input Single-Output (MISO) buck converter harvests and combines the energy while performing Maximum Power Point Tracking (MPPT) locally for each cell type. A miniaturized MISO dc-dc prototype converter operating at 10MHz is developed in a 130nm CMOS process. For 45-160mW power levels, the prototype converter achieves >92% nominal and >95% peak efficiency in a small (4.8 mm^2) form factor designed to fit within available space in a LAMB PV cell block. The results demonstrate the potential of the LAMB CPV architecture for enhanced solar energy capture.**

***Index Terms*—MISO dc-dc converter, energy harvesting, concentrated photovoltaic systems, maximum power point tracking, CMOS dc-dc power converters**

I. Introduction

MULTI-JUNCTION cells with concentration are adopted where high conversion efficiency exceeding the Schockley-Queisser limit of a single-junction solar cell is desired [2], [3]. However, the Tandem structures, i.e. the conventional two-terminal vertical multi-junction cell structures commonly used in Concentrated Photovoltaic (CPV) systems, have the disadvantage that all cells are physically stacked and electrically connected in series, such that the extractable energy will be negatively affected with cell mismatches and solar spectral variations [3]. In addition, lattice-matching requirements in tandem structures often demand complex and expensive growth processes [4]. The LAMB cell structure illustrated in Fig. 1, in which incident light is spectrally split and concentrated on multiple independently grown and optimized cells placed on a common substrate, is a promising alternative to the tandem structure with potentially higher conversion efficiency and lower fabrication costs [4], [5].

One of the key benefits of CPV systems is that under high concentration ratio, the area of the underlying cells can be greatly reduced, thus lowering raw material costs for the cells [6]. However, this presents a power management challenge where interconnection losses and complexity scales super-linearly as the module size increases, especially for systems with multi-junction cells where the I-V characteristic of individual cells are different and separate power buses are often required. Therefore, a cell-block level power management approach would be beneficial in terms of reducing interconnection complexity and improving system robustness against cell mismatches, as is the case in [7], [8]. In addition, since MPPT capability can be integrated with the cell-block level energy harvester, a Distributed Maximum Power Point Tracking (DMPPT) architecture can be readily achieved, which, as compared with centralized MPPT, can yield substantially more energy under partial-shading or other conditions that lead to cell mismatches such as aging, dirt accumulation, etc [9], [10].

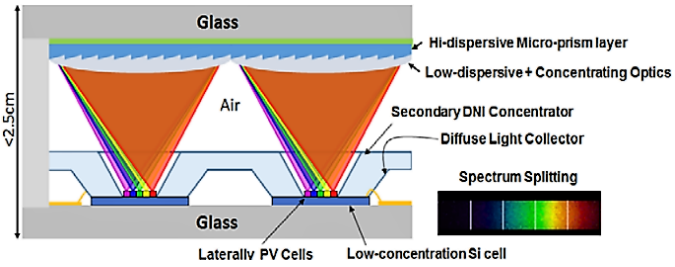

Fig. 1: Structure of a LAMB cell unit. The optical layer splits and focuses the direct solar spectrum onto multiple III-V cells, and a large-area Si cell is used for diffuse light collection.

A variety of approaches are possible for distributed power conversion and DMPPT. Some designs - including the one developed here - process the full power generated by individual cells or cell blocks (e.g. [10]); others utilize differential power converters, or "Δ-converters", where only the power imbalance between adjacent cell modules [11] or cells [12] is processed by the converters. While advantageous in some cases, such differential power processing approach requires inter-module communication to accurately track the global Maximum Power Point (MPP). Other approaches have sought to improve power extraction without a power converter, such as with reconfigurable interconnections through a switching matrix [13] or with only passive voltage-matching [14]. However, for terrestrial power generation applications, it is desirable for the power management system to be robust against spectral

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variations and other non-idealities, limiting the value of such relatively crude "converterless" techniques.

To take best advantage of the LAMB CPV approach of Fig. 1, a power conversion system is needed that can efficiently extract and combine power from the multiple laterally-arrayed cells, across solar spectral, cell fabrication and environmental variations, and deliver it to a single output port. The individual converters for realizing this distributed power conversion function should be footprint-minimized, and have a profile that enables them to be co-packaged within the physical envelope of the LAMB-cell optics at mm scale.

This work explores a power management approach in which several LAMB cell units are interconnected to form a closely voltage-matched cell block, and a CMOS-based Multiple-Input Single-Output (MISO) converter harvests and combines power from the cell arrays while tracking the cell-block-level MPP for each cell type. This is intended as a subsystem for the panel-level architecture of Fig. 2, in which many of these MISO converters are stacked in series across the panel before interfacing with the AC grid through a micro-inverter. A similar panel-level architecture is employed for sub-modules with a single cell type, for example in [10].

In terms of cost, while converter-less approaches, which often assume a constant operating voltage, have lowest power management overhead, the loss of overall energy capture could significantly increase the Levelized Cost of Energy (LCOE) [15]. The centralized, panel-array-level and distributed, cell-module level MPPT approaches greatly improve overall energy capture and lower the LCOE, although they require addition of power electronic components. The approach being explored in this work, with cell-block level CMOS-based converters, also achieves DMPPT. However, with the demonstrated system-level efficiency and potential of full integration, it can leverage the low-cost integrated-CMOS production and further reduce the LCOE.

This paper focuses on the development of the cell-block-level power management system (labeled "Cell Block with DMPPT" in Fig. 2), and is organized as follows: in Section II, the LAMB cell structure is introduced and an overview of the power management scheme is given. Section III describes the CMOS-based power converter design. The test environment setup and experimental results are discussed in Section IV and conclusions are presented in Section V. Details of a model comparing estimated performances of the LAMB and the tandem cell structure can be found in Appendix A, and some CMOS-level circuit design is discussed in Appendis B.

II. System Overview

This section gives an overview of both the photovoltaic (PV) system and the power management system. The PV system discussed here mainly focuses on the LAMB cell structure, and the power management system involves a cell-block level MISO energy harvesting converter and an accompanying MPPT algorithm.

A. LAMB Cell Structure

The size and power levels of individual LAMB cell units shown in Fig. 1 are dictated by optical considerations. For interconnection loss minimization as well as to maintain an appropriate power level for the MISO converter, a LAMB cell block is formed with four individual cell units, each with 1.1cm×1.1cm input lens aperture. A LAMB cell unit includes four cells: InGaAs, GaAs, InGaP and Si. Some cell parameters are given in Table I. The III-V cells receive concentrated direct light while the Si cell absorbs diffused light.

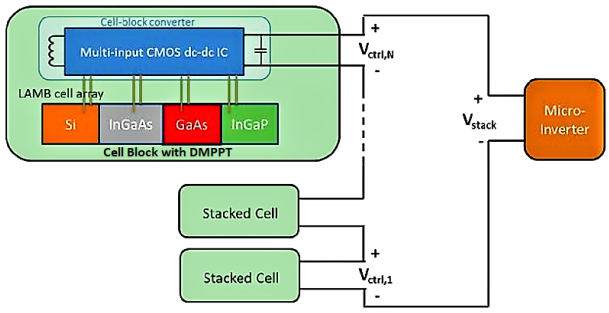


Fig. 2: The proposed power management structure. Each cell block has a MISO dc-dc converter that tracks local MPPT and converts energy from multiple cells into a single output. The power from individual converters can then be combined, e.g., by stacking outputs in series.

	InGaAs	GaAs	InGaP	Si
Bandgap (eV)	1	1.45	1.9	1.14
Refractive Index [16]	3.2	3.8	4.5	3.6
EQE [3]	0.85	0.85	0.85	0.9
Cell Area (mm^2)	2.64	0.66	5.5	112.2

TABLE I: Parameters of PV cells in a LAMB cell unit.

	InGaAs	GaAs	InGaP	Si
V_{oc} (V)	0.61	1.05	1.31	0.65
I_{sc} (mA)	16.8	13.0	14.9	9.5
V_{mpp} (V)	0.53	0.95	1.21	0.57
P_{mpp} (mW)	8.5	12.1	17.7	5.2
η_{ind} (%)	6.35	9.07	13.28	3.92
η_{tot} (%)		32.62		

TABLE II: Modeled I-V parameters of individual PV cells.

The modeled I-V parameters of the cells are listed in Table II, where η_{ind} refers to the individual cell's conversion efficiency with reference to the solar input power received by the LAMB cell unit, and η_{ov} is the overall conversion efficiency of the cell unit. To improve converter performance, the cells within a LAMB cell block are interconnected in the following manner: First, groups of like cells are connected in series or in parallel to achieve approximate open-circuit voltage (or to the same effect, MPP voltage) matching, then multiple such interconnected cell-branches are paralleled in to the LAMB cell block which provides a power level suitable for effective power conversion and DMPPT at the cell block level. Fig. 3 illustrates the interconnected LAMB block with 4 LAMB units and 16 individual cells in total.

As shown in Appendix A, it is estimated that with a properly designed power management system where each cell branch's MPP is accurately tracked, the LAMB cell structure can offer as high as 35.44% more extractable energy over a Tandem

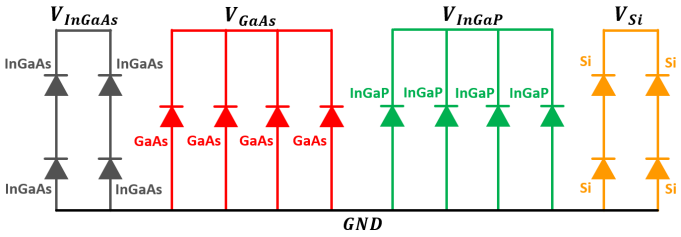


Fig. 3: A LAMB cell block with approximate voltage matching of the cell branches achieved through local interconnections.

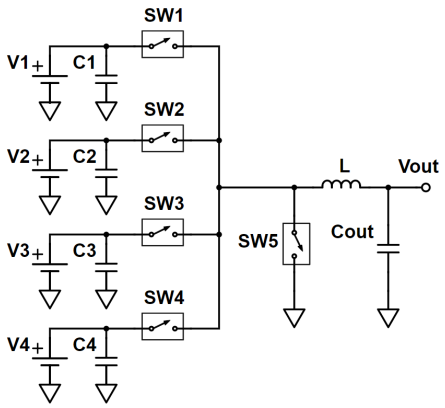
configuration under AM1.5 and diffused light, and on average an increment of 19.04% more energy harvesting capability based on estimations made with measured spectrum over a day-long period. This indicates that so long as the power management scheme is reasonably efficient, the LAMB cell structure can offer significant energy harvesting benefits.

B. MISO Energy Harvesting Converter

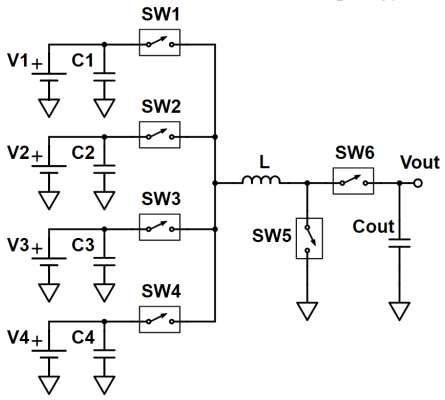
As shown in Table I, the total III-V cell area is on the order of 10 mm^2, and the Si cell takes up more than 10× this area for diffuse light collection. However, the MISO converter shall be co-packaged with the cell blocks on the same substrate, which means the Si cell area might be reduced to accommodate the converter footprint. Though it can be assumed that diffuse-light power collection will not be significantly affected with the slightly reduced Si cell area due to the presence of a diffused light concentrator, the converter footprint should not be so large as to mandate the removal of a Si cell. Also, the co-packaged converters should draw power for its controls from the PV input.

Therefore, the MISO converter should have a small footprint, high conversion efficiency and MPP tracking efficiency, and be self-powered from the cells. Converters built with integrated CMOS processes can offer very high power density with a small physical profile, and are particularly attractive for the power management system.

Here we present a brief exploration into several possible MISO converter topologies for this application, and discuss their suitability for meeting the design objectives. Since magnetic components inherently do not scale down well with size [17], desirable topologies should involve few such components and/or have low magnetic component stress. Switched-capacitor circuits require no inductors in general and can achieve high power density, yet the efficiency generally declines as the input and output voltage ratio deviates from a topology-determined rational number [18]. Hence they seem inappropriate for PV cell inputs which are subject to constantly varying light intensities and mandate variable conversion ratios. Hybrid magnetic switched-capacitor topologies such as in [19]–[22] reduce magnetic component requirements while enabling variable conversion ratios. However, they typically have high component counts and are thus less advantageous for this specific application. Therefore, it is desirable to adopt a direct converter which draws power from multiple inputs and combines them into a single output, while employing a single inductor, and operating in strict Continuous Conduction Mode



(a) A MISO buck converter topology.



(b) A MISO boost converter topology.

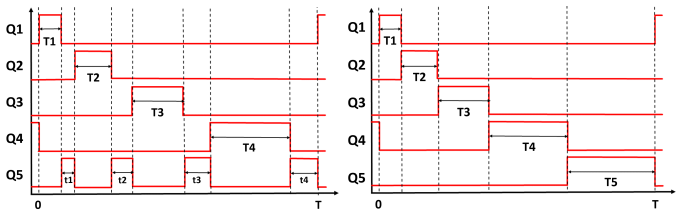
Fig. 4: Two multi-input single-inductor single-output direct converter topologies identified to be potentially suitable for this application. The MISO buck topology is selected based on its lower device loss and resulting higher efficiency.

(CCM) in order to achieve device stress reduction, component count minimization and magnetic energy storage diminution.

Two possible direct converter topologies, a MISO buck and a MISO boost converter respectively, are shown in Fig. 4a and Fig. 4b respectively. The four inputs come from the four voltage-matched cell-branches in the LAMB structure, and a single shared inductor helps combine the input power and deliver it to the single output. For low-voltage CMOS implementations, the major loss components in each of these converters include the switch conduction and gating losses, and the inductor conduction loss. The boost design has the potential advantage of requiring less series-stacked converters in a string if a certain cell-module voltage level is desired. However, the voltage gain benefit is greatly out-weighed by the additional device losses from the series output switch (SW6 in Fig. 4b). Consequently, we focus on the MISO buck design of Fig. 4a.

C. MPPT Control

In order to achieve DMPPT of the PV system, a feedback control scheme aiming at maximizing the output power of each cell-block-level MISO energy harvester is developed. The first requirement of such a system is a PWM control pattern that



(a) Distributed SW5 on-time. (b) Lumped SW5 on-time.

Fig. 5: Two possible MISO buck switching sequences, with ground switch (SW5) turning on multiple times during a period (a) or only once in a period (b).

enables efficient modulation of the power from each input. Two switching sequences of the MISO buck converter are discussed here, the ground switch (SW5) in one sequence turns on four times during one cycle, once after each input switch (Fig. 5a), and in another turns on only once for a lumped period (Fig. 5b). The latter sequence results in higher inductor current ripple but greatly reduces transistor gating losses and control complexity, and is therefore selected for converter operation. Fig. 6 shows a special analog Pulse-Width Modulation (PWM) waveform generation mechanism, expanding upon that in [23], to realize the switch control sequence. A sawtooth voltage ramp (V_{ramp}) is compared against a set of four synthesized switch duty cycle control voltage levels ($V_{d,1-4}$), and produces overlapping square waveforms (K_{1-4}). The non-overlapping waveforms for gate driving (q_{1-5}) can then be generated through combinational logic operations on K_{1-4}, as listed in (1). The MPPT algorithm described below modulates the four duty cycle control signals to maximize overall power extraction.

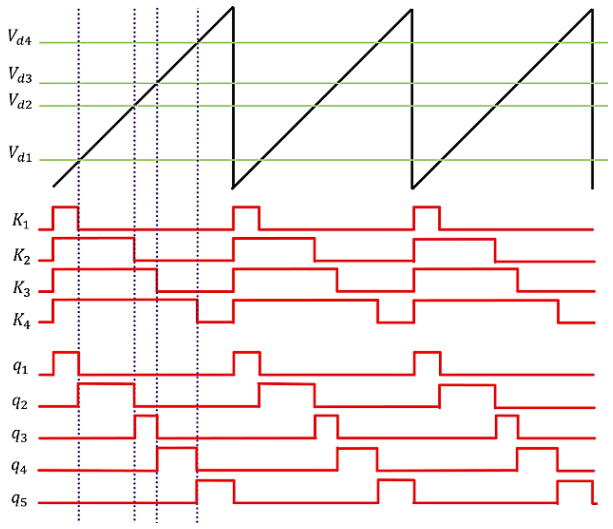


Fig. 6: The proposed PWM gate-drive waveform generation scheme. This approach is based on comparing multiple reference voltages ($V_{d,1-4}$) to a single sawtooth waveform.

$$\begin{cases} q_1 = K_1 \\ q_2 = \overline{K_1} \cdot K_2 \\ q_3 = \overline{K_1} \cdot \overline{K_2} \cdot K_3 \\ q_4 = \overline{K_1} \cdot \overline{K_2} \cdot \overline{K_3} \cdot K_4 \\ q_5 = \overline{K_1} \cdot \overline{K_2} \cdot \overline{K_3} \cdot \overline{K_4} \end{cases} \quad (1)$$

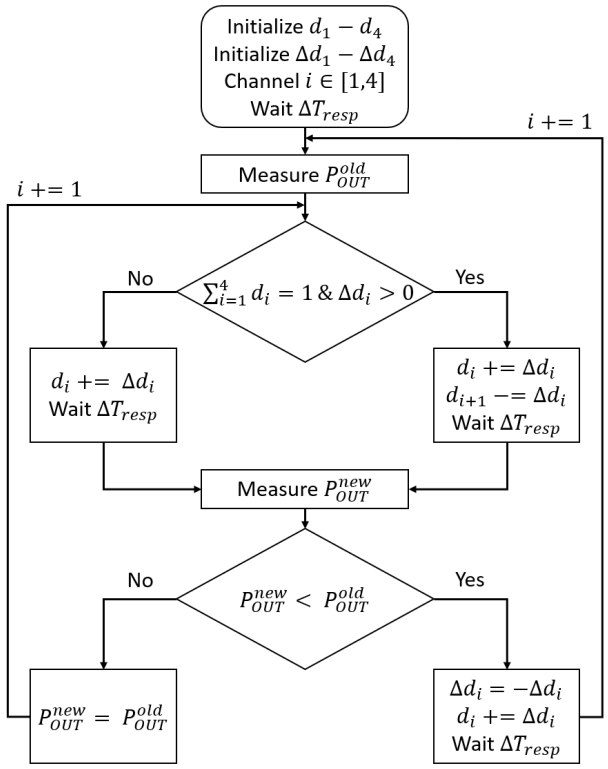


Fig. 7: Multi-input perturb-and-observe MPPT algorithm.

Some MPPT algorithms for similar applications are described in [4], [24], yet they either depend on current sensors for power estimation or measure input power from each individual input. For control loss minimization, a perturb-and-observe (P&O) algorithm is developed here that enables perturbation of each of the input duty cycles for MPPT while only requiring power sensing at the output, without explicit current measurements. This technique generalizes upon the approach introduced in [25] to handle multiple-input MPPT as required here. Fig. 7 illustrates the multi-input P&O algorithm, where d_{1-4} and Δd_{1-4} refer to the duty cycles of and perturbations to the four input channels respectively. Each observation is taken at ΔT_{resp} after the perturbation, and P_{out}^{new} and P_{out}^{old} refer to the sensed output power levels. Note that with the analog PWM generation scheme, the duty cycles are equivalent to the voltage differences in the control voltage $V_{d,1-4}$, and thus perturbations to a pair of adjacent duty cycles can be realized by simply changing one control voltage level.

The MPPT algorithm has in general two operating cases. The first is when the sum of the four input duty cycles is smaller than one, i.e. $\sum_{i=1}^{4} d_i < 1$; in this case, the ground switch SW5 turns on in each cycle and it is possible to independently change each input duty cycle. The second case is when the input duty cycles sum to unity, i.e. $\sum_{i=1}^{4} d_i = 1$,

where one switch duty cycle cannot be changed without affecting another. Both cases may be encountered, as the duty cycles depend on the ratio of output (inductor) current and each PV input current ($d_i = \frac{I_i}{I_L}$). Thus in the former case, the duty cycle of one input is perturbed at the expense of the ground switch duty cycle d_5, while in the latter case, the algorithm applies perturbations Δd_i to d_i and $-\Delta d_{i+1}$ to d_{i+1} for each i sequentially (d_4 changes with d_1), to keep the unity sum of input duty cycles. A numerical simulation of the algorithm and further experimental validation of the proposed approach can be found in [26].

III. MISO Buck Converter Design

This section introduces in more detail the prototype CMOS-based MISO energy harvester and discusses a technique that simplifies MPPT power sensing, the CMOS-level transistor sizing optimization, and the chip packaging design.

The presence of the converter relieves the demand of perfect voltage-matching between large-scale parallel-connected cell branches across various operating points, as would be required in an interconnection-only environment [14]. The voltage-matching cell interconnection structure reduces the voltage differences between the multiple inputs, which facilitates improved performance of the power converter. Consequently, as opposed to bi-directional blocking switches (Fig. 8 right) typically required in multi-input converters [27], single MOSFET devices (Fig. 8 left) can be employed, which simultaneously reduces device count, simplifies gate-driving, and lowers switch-associated losses. Moreover, the relatively close input voltages also lowers the inductor current ripple, permitting the use of a smaller and/or lower-loss inductor.

The converter is designed to operate in deep CCM for the benefit of reduced device conduction loss, a simpler control scheme and for compatibility with the lossless power sensing technique discussed later in this section. Based on the modeled PV input of the converter ($V_i \in$ [0.95V, 1.30V], $I_i \in$ [18.24mA, 59.60mA]), a TSMC 130nm process is selected to leverage its low $R_{ds,on} \times Q_g$ figure-of-merit of the core devices and its appropriate voltage ratings. The switching frequency is chosen to be around 10MHz for the sake of footprint minimization, and at the same time keeping inductor current ripple small in order to reduce ac conduction losses and power sensing errors.

A block diagram of the CMOS-based MISO converter is given in Fig. 9. The power stage includes the multiple inputs from solar cells, the power switches and their drivers, on-chip low-pass-filters for voltage sensing, an off-chip inductor, and several off-chip input and output buffering capacitors. The

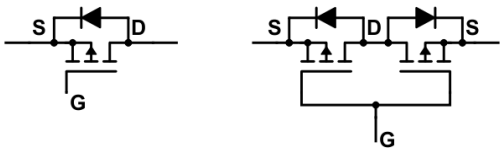


Fig. 8: Single and bi-directional blocking p-type MOSFET as MISO buck converter input switches.

control stage comprises a bandgap voltage reference, an LDO, a sawtooth ramp generator, several comparators, combinational logic gates, and a set of Digitally-Controlled Delay-Elements (DCDEs) for dead-time tuning and level-shifters for logic and power stage voltage interfacing. For prototyping and measurement purposes, some of the high-level MPPT control logic of the prototype is realized off-chip in a micro-controller, though it could be added on die for full integration without significant increase in footprint or energy consumption.

Some of the core CMOS functional blocks used to realize the MISO converter, including the sawtooth wave generator and the bandgap reference, are discussed in Appendix B. For the rest of this section, we focus on the higher-level aspects of converter design, on the lossless sensing scheme for effective MPPT control, the transistor sizing optimization for loss reduction, and also on the overall converter system packaging and implementation.

A. Lossless Power Sensing

For sensing loss minimization, instead of measuring voltage and currents at every input port, only the output power is measured and used in the MPPT algorithm. However, even measuring a single current can incur loss, as it typically requires sensing the voltage across a known resistance inserted into the current path. A technique is thus selected for equivalent current sensing without extra losses, leveraging the parasitic equivalent series resistance of the inductor (R_{ESL}), similar to the approach proposed in [25]. As shown in Fig. 9, two R-C low-pass filtered and hence time-domain averaged voltage levels v_L and v_O are taken at the switching node v_{sw} and the output v_{out}. The averaged output power $\langle P_{out} \rangle$ satisfies

$$\begin{aligned} \langle P_{out} \rangle = \langle v_{out} \rangle \cdot \langle i_L \rangle = \langle v_{out} \rangle \cdot \langle \frac{v_{sw} - v_{out}}{R_{ESL}} \rangle \\ \propto v_O \cdot (v_L - v_O) \end{aligned} \tag{2}$$

where $\langle\ \rangle$ denotes time-averages in periodic steady-state. The relative magnitude of output power and the direction of change in P_{out} needed in the perturb-and-observe MPPT algorithm can thus be determined with only sensed voltages. Note that this technique is more suitable for deep CCM with small inductor current ripple.

B. CMOS Transistor Sizing Optimization

Transistor sizing optimization of the power stage is performed in order to meet the anticipated solar cell input profile, e.g. to maximize averaged performance over time.

The CMOS process permits design flexibility in both gate width and length for each of the power MOSFETs (Q1-5 in Fig. 9). Typically the product of the ith switch's on-state resistance and gate-associated capacitance, $R_{sw,i} \times C_{sw,i}$, is a process-dependent constant [28], which is denoted γ. Therefore, an optimization of power stage losses, expressed in (3), can be achieved, assuming other parameters such as $V_{g,i}^2 f$, denoted as α, and $P_{in} \cdot I_i / V_{out}$, denoted as β, are known constants. To reduce both $R_{sw,i}$ and $C_{sw,i}$, the

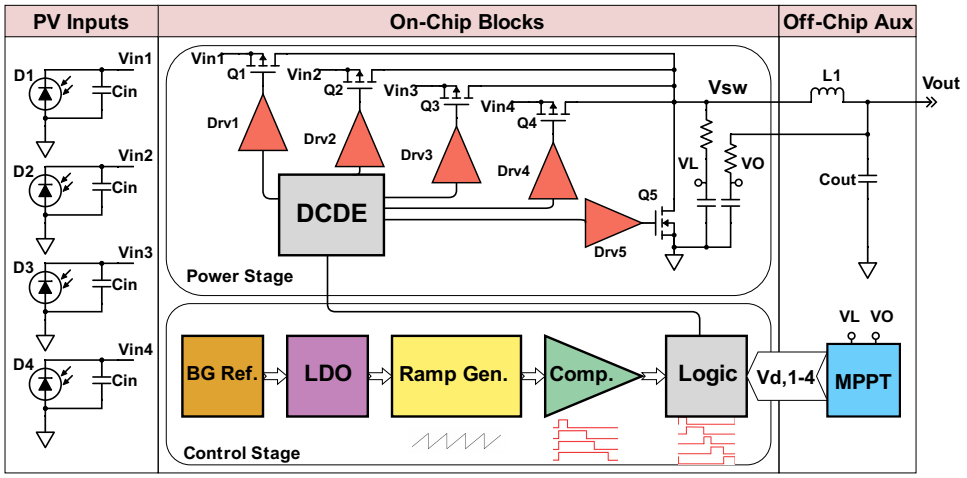


Fig. 9: A block diagram of the CMOS-based MISO energy harvester. The on-chip blocks are self-powered from V_{in2}, the input from diffuse-light collecting Si cells that are active during daytime. Consequently an external power supply is not needed for the on-die converter system (except for the MPPT-related micro-controller and DAC in the off-chip auxiliaries).

physical gate length of the switch (L_i) is fixed at the CMOS-process minimum, and from the expression of power stage losses related to the ith switch in (4), an optimized on-state switch resistance $R_{sw,i}$ and corresponding width (W_i) can be selected. The optimized resistance $R_{sw,i,opt} = \sqrt{\frac{\alpha\gamma}{\beta}}$, capacitance $C_{sw,i,opt} = \sqrt{\frac{\beta\gamma}{\alpha}}$, and the minimized loss of the ith switch is $P_{loss,i,min} = 2\sqrt{\alpha\beta\gamma}$.

$$P_{loss}^{buck} = (\frac{P_{in}}{V_{out}})^2 R_L + \sum_{i=4}^{4}(C_{sw,i}V_{g,i}^2 f + \frac{P_{in}}{V_{out}} I_i R_{sw,i}) + [C_{sw,5}V_{g,5}^2 f + \frac{P_{in}}{V_{out}}(\frac{P_{in}}{V_{out}} - I_{in})R_{sw,5}] \quad (3)$$

$$P_{loss,i} = \frac{\alpha\gamma}{R_{sw,i}} + \beta R_{sw,i} \quad (4)$$

The aforementioned optimization technique employs one pair of parameters α and β, however, with varying solar intensities, the converter will not operate with constant output power, voltage, or input current. Therefore, the optimization parameters should reflect the time-averaged annual operation. A set of weights provided by Californian Energy Commission [29], shown in Table III, is one of several location-specific regulatory standards that capture the effect of solar intensity variations. The respective quantities in parameters α and β can thus be computed with a standard spectrum (ASTM-G173 AM1.5 with added diffuse light in this case), a PV circuit model presented in Appendix A, and the selected set of weights. Table IV gives the optimized device widths and simulated on-state resistances for the power transistors.

Intensity	10%	20%	30%	50%	75%	100%
Weights	0.04	0.05	0.12	0.21	0.53	0.05

TABLE III: CEC weighting factors [29].

	Q1	Q2	Q3	Q4	Q5
Width (mm)	24	12	15	18	10
$R_{ds,on}$ ($m\Omega$)	101	152	129	99	40
γ ($\Omega \cdot pF$)		2.563			0.704

TABLE IV: Transistor parameters after optimization. The widths are rounded to the nearest mm for layout purposes.

C. Converter Footprint and Packaging Design

Due to footprint constraints and conversion efficiency concerns with relatively low total input power, flip-chip bumping chip-scale packaging (or equivalently, Ball Grid Array, BGA) is preferred over wire-bonding, since the latter typically require wire landing pads in excess to the chip area, and multiple wires must be paralleled to reduce parasitic resistive losses. To demonstrate that a converter footprint on the same order of the cells is feasible, and at the same time to accommodate the prototype's testing requirements, a 200 μm bump pitch is selected, and in total 48 I/O bumps, arranged as 8 rows by 6 columns, are fitted onto a 1.3 mm wide by 1.7 mm long chip. Fig. 10 shows a converter chip photo with overlaid layout design and annotations. The bumps are numbered 1-48 starting from the top left corner and incrementing left-to-right and then top-to-bottom. The detailed usage of the bumps are listed in Table V. Note that many of these bumps are for testing purposes only, and most of the chip area is not used by active devices but to accommodate the bumps. Hence, a production system could be expected to utilize less die area and interconnects.

IV. Test Environment Setup and Experimental Results

This section presents the test setup and experimental results for the prototype MISO dc-dc converter. For evaluation purposes, the converter is tested with a custom-designed LAMB PV simulator as its input and a R-I Norton-equivalent circuit as its load.

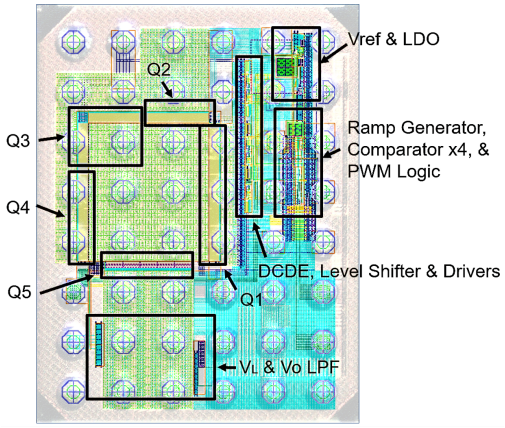


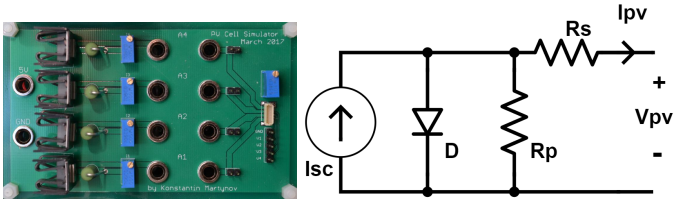
Fig. 10: Die photo overlaid with layout design and annotations. The die is 1.3 mm by 1.7 mm, and utilizes a minimum bump pitch of 200 μm.

Bump No.	Usage	Bump No.	Usage
1,6,43,48	Dummy Bumps	16,22,28	V_{in1}
2	$V_{g,Q3}$	17	Ramp Frequency V_{ctrl}
7,8,13	V_{in3}	18	V_{ramp}
3,9	V_{in2}	23,24,29,30	$V_{d,1-4}$
4	$V_{g,Q2}$	19,25	V_{in4}
10	$V_{g,Q1}$	31	$V_{g,Q4}$
5	V_{ref}	34	$V_{g,Q5}$
11	LDO V_{reg}	37,40,46	Averaged V_L&V_O
12	V_e	36,42	DCDE Programming
14,15,20, 21,26,27	V_{sw}	32,33,38, 39,44,45, 35,41,47	GND

TABLE V: Assigned purposes of each bump

A. PV Simulator

For comprehensive testing of the MISO converter, a PV simulator was developed to realize in hardware the single-diode detailed-balance cell circuit model discussed in Appendix A; it generates the expected I-V characteristics of the four inputs under a variety of test scenarios. A general non-ideal cell model is shown in Fig. 11b, and a picture of the simulator is given in Fig. 11a. Detailed design of the simulator can be found in [30].



(a) PV Simulator Board (b) Single Diode Model

Fig. 11: The PV simulator and the cell circuit model.

Series resistances R_s are inserted in the single-diode circuit models to account for non-idealities introduced by discrete diode components. The measured results, ideal model predictions and adjusted model predictions under AM1.5G (ASTM-G173 and scaled diffused spectrum) condition are given in Fig. 12. It can be seen that the adjusted model prediction matches closely with the measured data points. All subsequent experiments and MPP tracking efficiency determination are hence based on this adjusted model.

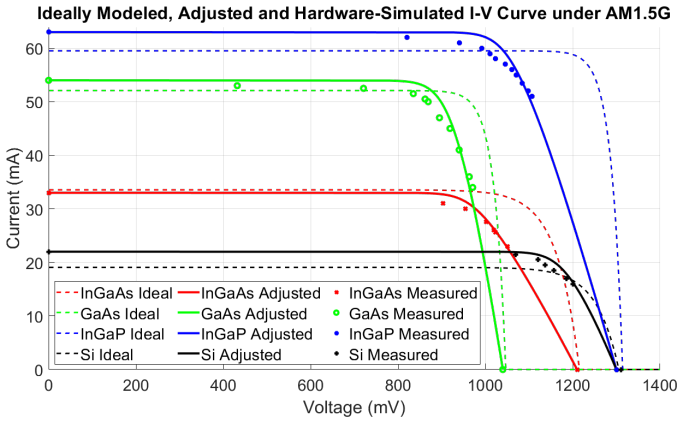


Fig. 12: Ideally modeled, adjusted, and hardware simulated cell-block level I-V curves under AM1.5G conditions.

B. Testbench Assembly

The chip is mounted on an HDI daughter board for ease of pin breakout and lab testing, whereas it will be co-packaged on the same substrate with the LAMB cell blocks in the eventual CPV system. The complete converter also includes six 4.7μF input and output capacitors in 0201 packages (CGB2A1JB) and a 0.55μH inductor in an 0603 package (GLFR1608). The daughter board is connected to the mother board via through-hole pins for minimization of parasitics. The assembled testbench with annotations and a U.S. dime for size reference is shown in Fig. 13, where a white box, 2.8 mm by 3.5 mm in size, encircles the chip and discrete power stage components. The CMOS die is 1.3 mm by 1.7mm, and the total component footprint is approximately 4.80 mm^2, less than 4% of the LAMB unit cell module area. The off-chip auxiliary components include a micro-controller that handles the P&O algorithm, and a DAC for duty-cycle control voltage (V_{d1-4}) interface. The power consumption of these components are not included in the subsequent measurements, although these functionalities could be added on-chip for full integration without significant increase in energy consumption or footprint.

C. Test with R-I Norton Equivalent Load

To mimic the string-connected cell-block level converters' load profile, a R-I Norton equivalent load is implemented. The PV simulator is tuned to reflect expected LAMB cells' I-V profiles with respect to different time-points in a day-long outdoor-measured spectrum as well as the AM1.5G scenario.

Assuming the cell-block level converter string is controlled by a resistive-loaded panel-level inverter with a global MPPT algorithm, a fixed load resistance (R_L) is set and the load current level (I_l) is swept across a certain range. In order to keep I_l within a certain reasonable range, a 30 Ω resistor is chosen. The output power can be expressed as

$$P_{out} = \frac{V_{out}^2}{R_L} + V_{out} \cdot I_l \tag{5}$$

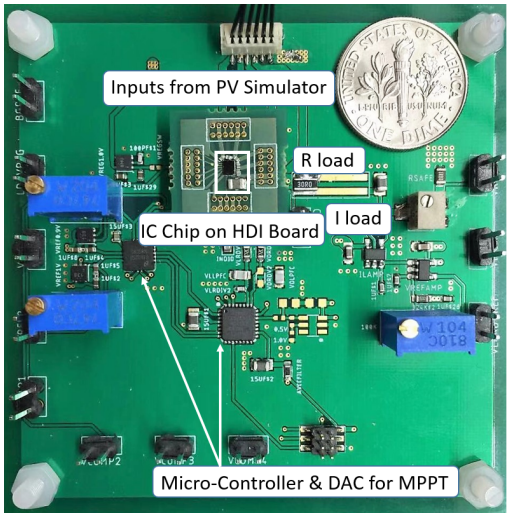


Fig. 13: The testbench assembly with annotations.

An optimal load current, I_{l-max}, exists which delivers maximum power to the load. This can be seen as a trade-off between the MPP tracking efficiency and conversion efficiency. If $I_l < I_{l-max}$, the load is not extracting the full potential from the input, while if $I_l > I_{l-max}$, the increased conduction losses negatively affects the conversion efficiency and hence the extractable power. In each test scenario, I_l is swept across a certain range near the predicted MPP current in order to experimentally determine the maximum extractable output power $P_{out-max}$.

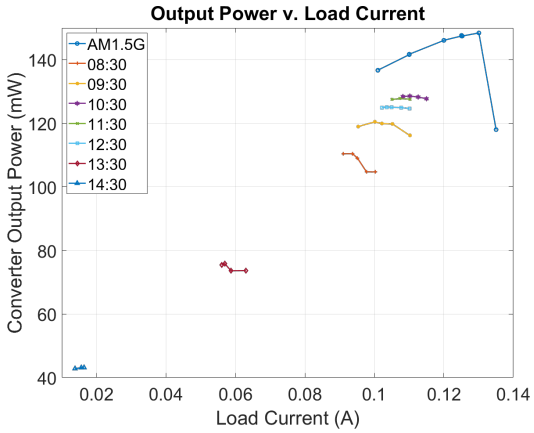
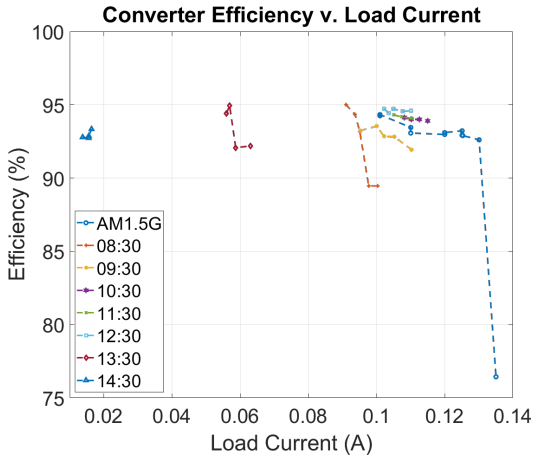
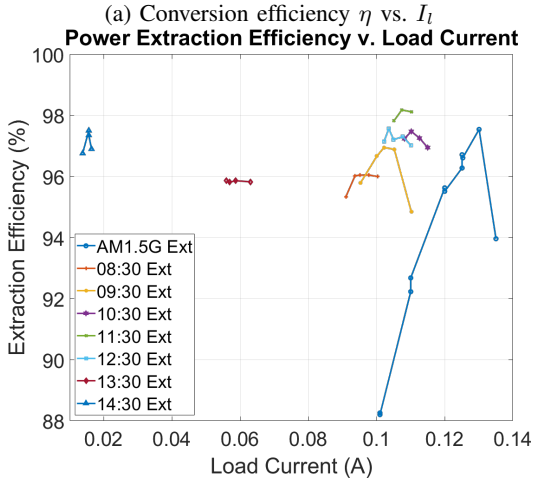


Fig. 14: P_{out} vs. I_l for each input scenario.

In Fig. 14, measured P_{out} is plotted against I_l for each input scenario as represented in Table VII. We define the conversion efficiency η and MPP tracking (or extraction) efficiency η_{ext} as in $P_{out} = \eta \cdot P_{in} = \eta \cdot \eta_{ext} \cdot P_{max}$, where P_{max} is the sum of individual cell's maximum power in a LAMB cell-block. With the load current at I_{l-max}, the $\eta \cdot \eta_{ext}$ product is maximized. η and η_{ext} for all input scenarios are plotted against I_l and given in Fig. 15a and Fig. 15b. It can be seen that η generally decreases as I_l increases, and peak conversion efficiencies of >95% can be achieved. Also, η_{ext} rises as I_l to a certain extent, after which it starts to drop as the input can no longer accommodate this artificially high current demand.



(a) Conversion efficiency η vs. I_l



(b) MPP extraction efficiency η_{ext} vs. I_l

Fig. 15: Efficiency plots vs. load current. Conversion efficiency $\eta = P_{out}/P_{in}$ captures the converter performance, while MPP extraction efficiency $\eta_{ext} = P_{in}/P_{max}$ quantifies how close the converter tracks the maximum available input power and reflects the efficacy of the MPPT algorithm.

The theoretical maximum power from the PV simulator, P_{max}, the actual output power from the simulator, i.e. the input power to the converter P_{in}, and the maximum power delivered to the load $P_{out-max}$ for each input scenario are plotted in Fig. 16. The typical conversion efficiency is in the range of 92% to 95%, which is sufficiently high to validate the comparative advantage of LAMB cell structure with cell-block level MISO energy harvester against that of series-connected two-port multi-junction tandem cell structures. Furthermore, the MPP extraction efficiency is in the range of 95% to 98.2%, demonstrating the effectiveness of the MPPT algorithm.

Fig. 17 shows two waveforms (with a dc offset) of the switching node voltage, when the ground switch (SW5 or Q5 in Fig. 9) is turned once in a period (Fig. 17b) or is never turned on (Fig. 17a), corresponding to the two MPPT algorithm operation cases. Generally, the ground switch is turned on when the load current I_l is set at a higher level, although this can negatively affect the efficiency since it incurs additional gating and conduction losses. Nevertheless, in each

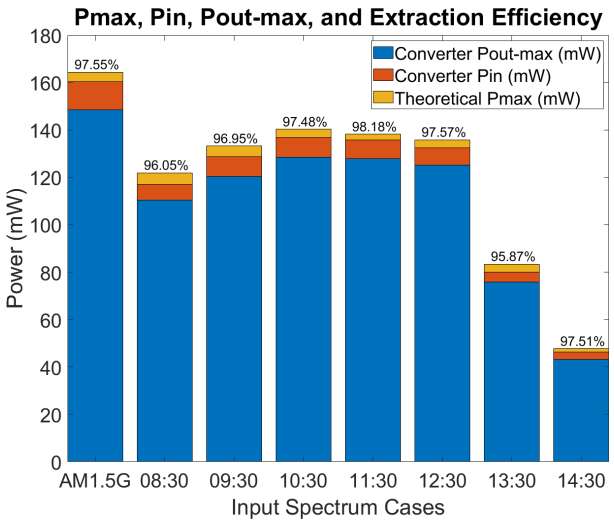


Fig. 16: Theoretically maximum available power from PV simulator P_{max}, converter input power P_{in} and maximum power delivered to the load $P_{out-max}$ for each input scenario with annotated peak MPP extraction efficiency η_{ext}.

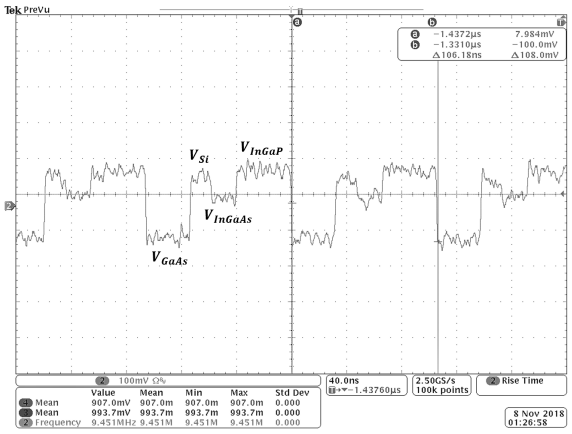
case the control algorithm is able to converge at a stationary set of duty cycles for the five switches and deliver an output power level as set by the input and load profile.

Table VI presents a comparison between some PV power management approaches reported in the literature. The PV cell type, energy harvesting approach and MPPT granularity, implementation method, power level, peak converter efficiency, reported system efficiency under mismatches or spectrum variations, and estimated cost are listed. SJ and MJ stand for single- and multi-junction respectively, and FPP and DPP represent full- and differential-power processing approaches. It can be seen that approaches employing MPPT-enabling converters generally have a higher system efficiency considering cell mismatches or spectrum variations, and our work in particular achieves low estimated cost with good system efficiency.

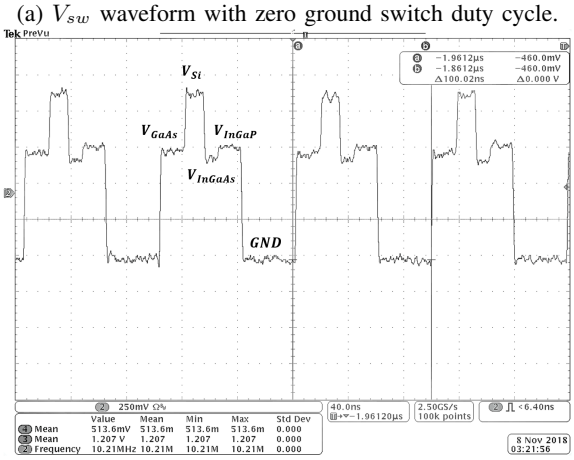
A reasonable question is how the proposed LAMB cell configuration performs without any power electronic conversion, e.g. in a pseudo-tandem approach in which all cells are electrically stacked in series and voltage-matched in parallel tandem branches. This is treated in detail in Appendix A, where it is shown that even if MPPT were provided to the pseudo-tandem stacks, elimination of the MISO converter would result in much lower energy extraction.

V. Conclusion

Compared to traditional tandem, two-terminal multi-junction cell structures, the LAMB-based multi-junction CPV system is predicted to offer significant energy extraction benefits, especially under spectrum variations, due to it parallel arrangements of individually optimizable cells and independent MPPT operation. To enable such systems, a power management approach is developed with close voltage-matching at the cell-block level, and features a small-footprint 130nm CMOS-based energy harvesting converter with multiple inputs, a single inductor and a single output. High conversion efficiencies in the 90+% range and MPPT tracking efficiencies above 95%, which are sufficient to establish the considerable long-term energy harvesting advantages of the LAMB architecture, have been experimentally demonstrated.



(a) V_{sw} waveform with zero ground switch duty cycle.



(b) V_{sw} waveform with non-zero ground switch duty cycle.

Fig. 17: Switching node voltage waveforms. Each plot has 40ns/div. Plot (a) is at 100mV/div and plot (b) is at 250mV/div.

Acknowledgment

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Appendix A
Cell Modeling and Comparison

To compare the achievable performance of LAMB and tandem cell structures, and to guide the design of a CMOS power converter for LAMB CPV systems, a detailed-balance model is developed to characterize the I-V profile of the two cell structures under spectrum variations.

The diode equation used in the detailed-balance model is

$$J = J_0 \cdot (e^{qV/kT} - 1) - J_{ph} \tag{6}$$

where the saturation current density J_0 can be calculated as

$$J_0 = \frac{q(n^2+1)E_g^2 kT}{4\pi^2 \hbar^3 c^2} \cdot e^{-E_g/kT} \tag{7}$$

	[9]	[10]	[11]	[12]	[13]	This work
PV Cell Type	SJ	SJ	SJ	CPV-MJ	SJ	CPV-MJ
MPPT Approach	DMPPT	DMPPT	DMPPT	DMPPT	switch matrix	DMPPT
Granularity	sub-module	sub-module	sub-module	cell-block	cell-block	cell-block
Power Processing	FPP	FPP	DPP	DPP	FPP	FPP
Implementation	GaN-based discrete	Si-based discrete	simulation	1um CMOS	180nm CMOS	130nm CMOS
Power Level (W)	∼100 W	∼80 W	∼70 mW	∼7.5 W	0.3 μW-0.3 mW	45 mW-160 mW
Converter efficiency	99%	98%	assumed 90%	90%	95%	95%
System efficiency	>90%	97.7%*	simulated >92%	>90%	>78%	>92%
Estimated Cost	high	medium	N/A	low	low (potentially high LCOE)	low

TABLE VI: Comparison of various converter designs with different power management approaches. Note that the power management architectures are disparate in terms of compatible PV systems.
*: reported system efficiency without partial shading or introduced mismatches.

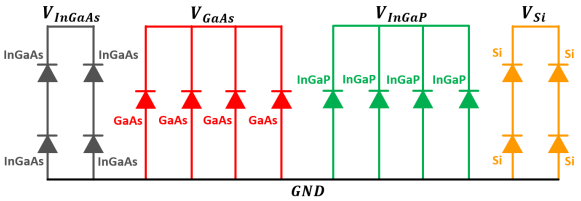
and the photo-current J_{ph} given by

$$J_{ph} = C \cdot EQE \cdot \int_{\lambda_{min}}^{\lambda_{max}} \frac{S(\lambda) \cdot \lambda}{hc} d\lambda \tag{8}$$

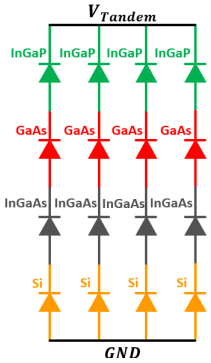
where C is the concentration ratio, EQE is the external quantum efficiency, λ_{min} and λ_{max} are the cell's cut-off wavelengths from the solar spectral irradiance $S(\lambda)$, based on their bandgaps and assuming perfect spectrum-splitting. The diffused light portion is modeled as a scaled AM1.5G with total spectral power density of $200W/m^2$ based on outdoor diffused light measurements. Similar to the approach adopted in [14], a saturation current degradation factor in the range of $200\times$ through $10000\times$ is applied to J_0 so as to match a typical PV cell's open-circuit voltage V_{oc} and conversion efficiency [31], [32].

To compare the modeled energy extraction from LAMB cell blocks with that of the tandem structure, a configuration using the same number and types of cells is constructed as shown in Fig. 18b. The 4 cells within a tandem unit are series-connected, and then 4 tandem units are paralleled into a block. To better approximate the typical tandem cell structure with uniform cross-sectional area, the area (A) of each III-V cell is equally set to be the average of the original total area, i.e. $A_{InGaAs,tandem} = A_{GaAs,tandem} = A_{InGaP,tandem} = \sum A_{III-V,LAMB} \,/\, 3$. The Si cells (used to collect diffused light) remain unchanged for both structures.

The model presumes perfect MPPT for each cell branch in the LAMB and tandem structures, and neglects optical penetration losses in the tandem vertical cell stack. This model is used to compare the maximum available power under both ASTM-G173 AM1.5 (incl. diffused) and a measured solar irradiance profile collected with a 2-axis tracker from 08:30 until 14:30 at 1 hour intervals (plus the same diffused light component) on a clear day in November in Cambridge MA. The results are given in Table VII, where the LAMB cell structure offers on average 19.04% more energy harvested over a day long period. This indicates that so long as the power management scheme for the LAMB CPV system is reasonably efficient, the LAMB structure has significant benefits in terms of energy capture. While cells in a tandem structure would typically be optimized for current density matching, this comparison nevertheless highlights the possible detrimental current-mismatching effects.



(a) A LAMB cell block.



(b) A Tandem cell block.

Fig. 18: Cell connection within LAMB and Tandem blocks.

Appendix B
CMOS Control Stage Function Blocks

The on-chip control stage comprises a bandgap reference circuitry (designed to be insensitive to both temperature and supply voltage variations), an LDO which regulates a stable voltage from the varying photovoltaic input, a sawtooth waveform generator that sets the frequency, and a set of comparators and logic that compares the sawtooth ramps with control voltage levels $V_{d.1-4}$ and produces non-overlapping PWM square waves q_{1-5}, as shown in Fig. 6. In addition, a set of Digitally-Controlled Delay-Elements (DCDE) are inserted between the driver input and logic output for dead-time regulation and chip fabrication variation adjustments. This appendix discusses the CMOS-level implementation of some important control blocks.

1) Bandgap Reference: The input voltage from the photovoltaic sources fluctuates due to solar spectral composition and intensity variations, however, a steady supply voltage for the control stage is desired to maintain a stable switching frequency. Therefore, the bandgap reference circuit shown in Fig. 19 is implemented. Current mirror devices M1, 2 and 3

	AM1.5	08:30	09:30	10:30	11:30	12:30	13:30	14:30
$P_{max,Tandem}$ (mW)	128.33	119.36	126.45	127.28	127.17	126.85	81.11	30.33
$P_{max,LAMB}$ (mW)	173.81	132.74	147.34	156.04	154.71	151.03	89.54	47.78
Increment (%)	35.44	11.21	16.52	22.60	21.66	19.06	10.39	57.53
Avg. Incr. (%)	35.44				19.04			

TABLE VII: Extractable power comparison between Tandem and LAMB structure.

have the same geometry for branch current matching, resistors $R_1+R_2=R_4$ for symmetry, and assuming an ideal Op-Amp, the reference voltage V_{ref} can be expressed as

$$V_{ref} = \frac{R_5}{R_4} \cdot V_{BE,1} + \frac{R_5}{R_3} \cdot ln(N) \cdot \frac{kT}{q} \tag{9}$$

where $V_{BE,1}$ is the base-to-emitter voltage of BJT Q1, N is the BJT saturation current ratio $I_{S,Q2}/I_{S,Q1}$ and hence approximately the footprint area ratio, and T is the temperature. The Op-Amp output controls M4, which regulates the $V_{dd-decoupled}$ rail, connected to the supply voltage through another current mirror M5, and M6, and decouples the rail voltage from variations in V_{dd}. The noise on the decoupled rail is further isolated from the reference voltage output by adopting a self-biasing voltage divided by R_1 and R_2. Adding additional capacitance to ground on nodes V_{ref} and $V_{dd-decoupled}$ can further enhance the power-supply noise immunity. This circuitry is designed to generate a 750mV V_{ref} with V_{dd} varying from 1.0V to 1.3V with less than 1mV deviation, and temperature (for prototyping purposes selected to be around room temperature) from -20°C to 50°C with <0.05mV/°C drift. Further design, analysis and simulation results can be found in [30].

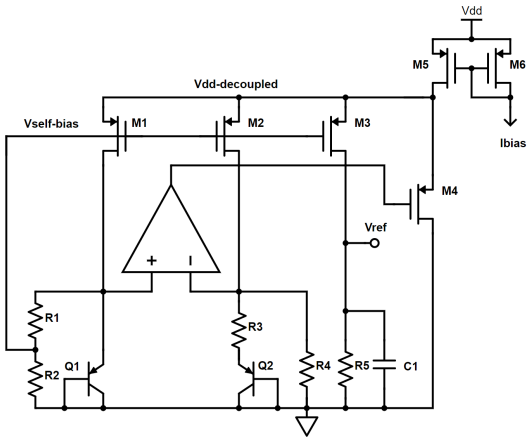


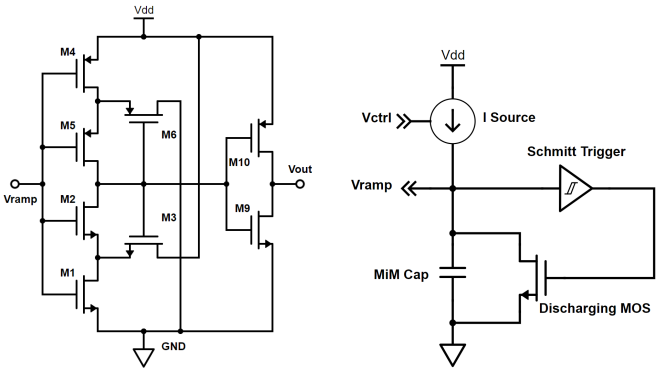
Fig. 19: The employed bandgap reference circuit with enhanced supply voltage insensitivity.

2) Sawtooth Wave Generator: A sawtooth signal is generated on-chip for PWM control, and a CMOS Schmitt trigger, with customizable hysteresis triggering threshold levels, is employed as shown Fig. 20b, where the input to the Schmitt trigger is the desired sawtooth voltage V_{ramp} across a linear capacitor, and the output controls a discharging switch. A current source controlled by an external voltage level is used to realize frequency fine-tuning. Fig. 20a illustrates a CMOS Schmitt trigger with a cascaded inverter, and the input low-to-high and high-to-low transition thresholds (V_{LH} and V_{HL}) can be expressed as

$$V_{LH} = \frac{V_{dd} + \sqrt{\frac{k_1}{k_3}} \cdot V_{th,n}}{1 + \sqrt{\frac{k_1}{k_3}}} \tag{10}$$

$$V_{HL} = \frac{\sqrt{\frac{k_4}{k_6}} \cdot (V_{dd} - |V_{th,p}|)}{1 + \sqrt{\frac{k_4}{k_6}}} \tag{11}$$

where $k_n = \frac{1}{2}\frac{W_n}{L_n}\mu_e C_{ox}$ is a transistor-dependent parameter, and $V_{th,n}$ and $V_{th,p}$ are the threshold voltages of the n- and p-type MOSFETs respectively. To achieve a large swing, V_{LH} should be set close to V_{dd} and V_{HL} close to 0, hence the device widths are designed such that $W_3 \gg W_1$ and $W_6 \gg W_4$.



(a) CMOS Schmitt Trigger (b) Sawtooth Generator

Fig. 20: The Schmitt Trigger (with a cascaded inverter) and the sawtooth generator.

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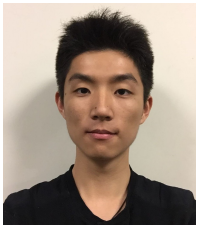

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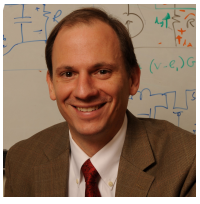

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