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DC-DC Converter Implementations Based on Piezoelectric Transformers

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***Abstract*—The drive to miniaturize power electronics motivates investigation into alternative passive component technologies such as piezoelectrics, which offer fundamentally higher power density and efficiency capabilities at small scales compared to magnetics. Piezoelectric transformers (PTs) have seen application in dc-dc converters, but these designs typically require additional magnetics for competitive efficiency. In this work, we systematically enumerate isolated and non-isolated dc-dc converter topologies and switching sequences capable of efficiently utilizing PTs as their only energy storage components. The proposed switching sequences maintain high-efficiency behaviors (e.g., zero voltage switching (ZVS), all-positive instantaneous power transfer, and minimal charge circulation) across wide voltage gain and load ranges. We present techniques for deriving these switching sequences' ZVS regions, estimating PT efficiency, and solving for periodic steady state switching times; these offer insights for comparing and implementing design options. We then verify our analyses in a 180-500 V experimental prototype based on a commercially-available PT, which demonstrates significant efficiency gain through a proposed implementation.**

***Index Terms*—dc-dc converter topologies, piezoelectric transformers, switching sequences, zero voltage switching**

I. Introduction

Demand for power electronics having smaller volume, lighter weight, and improved manufacturability motivates exploration of alternative converter energy storage mechanisms. Miniaturization tends to be limited by the sizes and performance capabilities of passive components, particularly magnetic elements including inductors and transformers. The achievable power densities of magnetic components fundamentally decrease with volume [3], [4], which inhibits miniaturization, and even switched-capacitor converter architectures require auxiliary magnetics for efficient voltage regulation. This creates an opportunity in power conversion for alternative passive component technologies that can offer major advances in achievable power density, or power handling capability per volume, without the presence of magnetics.

One promising alternative passive component technology is piezoelectrics, which can be utilized as single-port piezoelectric resonators (PRs) or multi-port piezoelectric transformers (PTs). Piezoelectrics, which store energy in the mechanical compliance and inertia of a piezoelectric material, have higher performance and power density capabilities at small volumes compared to magnetics [5]–[7]. Piezoelectrics likewise offer planar form factors, batch fabrication, and the potential for integration. PTs in particular can provide voltage transformation as well as galvanic isolation.

TABLE I
Demonstrated Power-Stage Efficiencies for Magnetic-less DC-DC Converters Based on Piezoelectric Transformers

Reference	[23]	[25]	[26]	[24]	This work
Efficiency	70 %	62 %	78 %	68 %	90 %

Although piezoelectrics have been used extensively for energy harvesting, sensing, actuation, and transduction, the widespread use of PTs in power conversion has been primarily limited to fluorescent backlight drivers [8]. These designs, along with variations proposed for dc-dc power conversion, typically include auxiliary magnetic component(s) to help achieve zero voltage switching (ZVS) despite the detriment to potential power density.

Magnetic-less converter designs capable of ZVS and high efficiency have been realized with PRs in [9]–[13]. PR-based converter topologies and switching sequences are enumerated in [9], with one such implementation achieving >99% efficiency. Topologies in [11] and [13] provide step-up/step-down capabilities and improved efficiency for high step-down ratios, respectively, and [12] demonstrates use of a high-frequency lithium niobate PR to achieve high power density. Although such PR-based converter designs are promising, they exhibit decreasing efficiencies for high voltage conversion ratios and are not inherently capable of galvanic isolation.

PT-based converter designs capable of ZVS without magnetics have been explored in [6], [14]–[29]. ZVS conditions and operating regions have been analyzed for PT-based half-bridge inverters in [14]–[18] and demonstrated using frequency modulation [19], dead time control [22], and phase-locked loops [29]. Dc-dc converters based on PTs have likewise achieved ZVS with frequency modulation [24], [25], phase-locked loops [20], and burst-mode control [26]. ZVS for bidirectional operation of dc-dc converters has been analyzed in [21], [23].

Despite such progress, these magnetic-less PT-based converters report limited efficiency capabilities. PTs are understood to be capable of efficiencies >95% with sinusoidal drives [16], [19], [25], but PT-based dc-dc converter power-stage efficiencies tend to be drastically lower as summarized in Table I. Notably, however, most of these designs rely on standard resonant converter architectures and operating techniques; there has been little investigation into alternative converter implementations dedicated to maximizing PT efficiency.

The authors are with the Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA, USA (email: jboles@mit.edu, elaineng@mit.edu, lang@mit.edu, djperrea@mit.edu). This material is an extension of [1] and [2] and is based upon work supported by Texas Instruments, the National Science Foundation Graduate Research Fellowship Program under Grant No. 1122374, and the MIT Undergraduate Research Opportunities Program.

In this paper, we conduct a systematic enumeration and downselection process in search of isolated and non-isolated dc-dc converter implementations that efficiently utilize PTs as their only energy storage components. This process focuses on periodic steady state switching sequences for PT-based converters; the resulting topologies are mechanisms for realizing these switching sequences. This search is confined to practical switching sequences capable of high-efficiency behaviors including ZVS, all-positive instantaneous power transfer, and minimal charge circulation across wide operating ranges. To analyze and compare implementations, we provide tools for deriving their ZVS operating regions, estimating PT efficiency, and solving for periodic steady state to calculate switching times. We then validate these analyses with an experimental prototype of one proposed implementation using a commercially-available PT.

II. Isolated Converter Implementations

f We first identify isolated PT-based converter implementations in which the PT serves as a 2-port, 4-terminal device. For this enumeration process, we assume an isolated dc-dc system with a constant-voltage load as shown in Fig. 1. The PT is modeled using a reduced form of the Mason model, which includes physical terminal capacitances, an ideal transformer, and an LCR branch modeling the PT's mechanical resonance properties [30]–[32]. The parameters of this model are assumed to be constant throughout this work, though we discuss their sensitivities in Appendix E. While this work focuses on a PT oriented for step-up operation, the presented analyses can be similarly applied to step-down PTs [1].

A. Stages

We begin enumerating converter implementations by first identifying possible *stages* of a switching cycle. Each distinct way the terminals of the PT can be connected in the source-load system of Fig. 1 constitutes a possible stage. We refer to stages independently for each port, labeled by the voltage imposed on v_{pA} or v_{pB}. Moreover, we constrain the polarity of i_L in each stage for high-efficiency behaviors including ZVS, all-positive instantaneous power transfer, and minimal charge circulation. Thus, stages can be classified as follows:

- Connected stages: the PT port is connected to the source-load system such that $v_{pA} = \pm V_{in}$ or $v_{pB} = \pm V_{out}$. The polarity of i_L is constrained for all-positive instantaneous power transfer.
- Zero stages: the PT port is short-circuited, requiring v_{pA} or v_{pB} to equal zero. The polarity of i_L may be either positive (denoted *Zero+*) or negative (denoted *Zero-*), constrained for unidirectionality to avoid excess charge circulation.
- Open stages: the PT port is open-circuited, allowing v_{pA} or v_{pB} to increase or decrease through resonance. The polarity of i_L is constrained for charging/discharging C_{pA} or C_{pB} as required for ZVS. One or both terminals may transition in this stage, either simultaneously or sequentially.

Connected stages transfer energy between the PT and the source-load system, while zero and open stages redistribute energy within the PT. The set of all potential stages is summarized along with i_L polarity constraints in Table II.

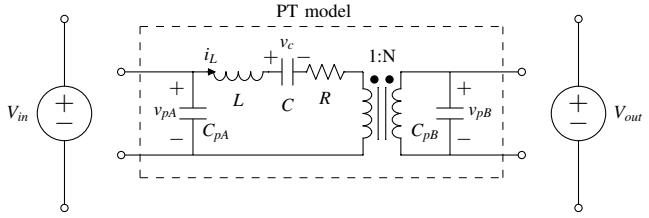


Fig. 1. Isolated source-load system assumed for switching sequence enumeration, with the PT represented by the reduced Mason circuit model [30]. Other terminal capacitances are neglected.

TABLE II
Potential Isolated Stages by Port and i_L Polarity

Polarity	Input Stages (v_{pA} =)	Output Stages (v_{pB} =)
$i_L > 0$	V_{in}; *Zero+*; $\frac{dv_{pA}}{dt} < 0$	V_{out}; *Zero+*; $\frac{dv_{pB}}{dt} > 0$
$i_L < 0$	-V_{in}; *Zero-*; $\frac{dv_{pA}}{dt} > 0$	-V_{out}; *Zero-*; $\frac{dv_{pB}}{dt} < 0$

B. Switching Sequences

We permute these potential stages to create *switching sequences*, defined as order-specific arrangements of stages across a switching cycle. In the case of isolated PTs, we first identify sub-sequences for each PT port and then combine them to create full PT-wide switching sequences. Assuming the stages and i_L constraints in Table II, we enumerate possible sub-sequences with:

1) A minimum number of stages (for control simplicity).
2) At least one connected stage (for transferring energy to/from the PT).
3) Alternating connected/zero stages and open stages (for ZVS between connected/zero stages).
4) No repetition of the same connected/zero stage.
5) At least one connected/zero stage each for positive and negative i_L (for charge balance on C across the cycle).
6) One sequential span each of positive and negative i_L (for completion in one PT resonant cycle) [9].

Enumerating all possible sub-sequences and filtering according to these criteria yields two distinct[1] 4-stage sub-sequences and two distinct 6-stage sub-sequences each for the input and output ports of the PT. Multiplied together between the two ports, the enumerated sub-sequences create 16 full switching sequences that enable ZVS and all-positive instantaneous power transfer in isolated PT-based dc-dc converters. These sequences are further downselected in Section II-C.

Throughout this work, we refer to a sub-sequence by the order of its connected/zero stage voltages (e.g., V_{out}, -V_{out}, *Zero+* for a six-stage sub-sequence), assuming the open stages between each. Full switching sequences are then denoted by "input-port sub-sequence | output-port sub-sequence" (e.g., V_{in}, -V_{in} | V_{out}, -V_{out}, *Zero+*).

[1]Similar-stage sub-sequences are distinct only if the *order* of their stages is different, regardless of which stage is listed "first". Also, the inverted version of a sub-sequence (i.e., all stages having inverted voltage but in the same order) is considered the same sub-sequence.

TABLE III
PROPOSED ISOLATED SWITCHING SEQUENCES, TOPOLOGIES, AND CONSTRAINTS

Switching Sequence (Input | Output)	Topology	Ideal V_{out}/V_{in} Range	Charge Transfer Utilization Factors (K)	C_{pA}, C_{pB} Voltage Ranges (V_{ppA}, V_{ppB})
V_{in}, -V_{in} | V_{out}, *Zero+*, *Zero-*	FB-HB	$2N < \frac{V_{out}}{V_{in}} < \infty$	$K_A = 1$, $0 < K_B < \frac{1}{2}$	$2V_{in}$, V_{out}
V_{in}, -V_{in} | V_{out}, -V_{out}, *Zero+*	FB-FB	$N < \frac{V_{out}}{V_{in}} < 2N$	$K_A = 1$, $\frac{1}{2} < K_B < 1$	$2V_{in}$, $2V_{out}$
V_{in}, *Zero-* | V_{out}, *Zero+*, *Zero-*	HB-HB	$N < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $0 < K_B < \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero-* | V_{out}, -V_{out}, *Zero+*	HB-FB	$\frac{N}{2} < \frac{V_{out}}{V_{in}} < N$	$K_A = \frac{1}{2}$, $\frac{1}{2} < K_B < 1$	V_{in}, $2V_{out}$
V_{in}, -V_{in}, *Zero-* | V_{out}, *Zero-*	FB-HB	$N < \frac{V_{out}}{V_{in}} < 2N$	$\frac{1}{2} < K_A < 1$, $K_B = \frac{1}{2}$	$2V_{in}$, V_{out}
V_{in}, -V_{in}, *Zero-* | V_{out}, -V_{out}	FB-FB	$\frac{N}{2} < \frac{V_{out}}{V_{in}} < N$	$\frac{1}{2} < K_A < 1$, $K_B = 1$	$2V_{in}$, $2V_{out}$
V_{in}, *Zero+*, *Zero-* | V_{out}, *Zero-*	HB-HB	$0 < \frac{V_{out}}{V_{in}} < N$	$0 < K_A < \frac{1}{2}$, $K_B = \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero+*, *Zero-* | V_{out}, -V_{out}	HB-FB	$0 < \frac{V_{out}}{V_{in}} < \frac{N}{2}$	$0 < K_A < \frac{1}{2}$, $K_B = 1$	V_{in}, $2V_{out}$

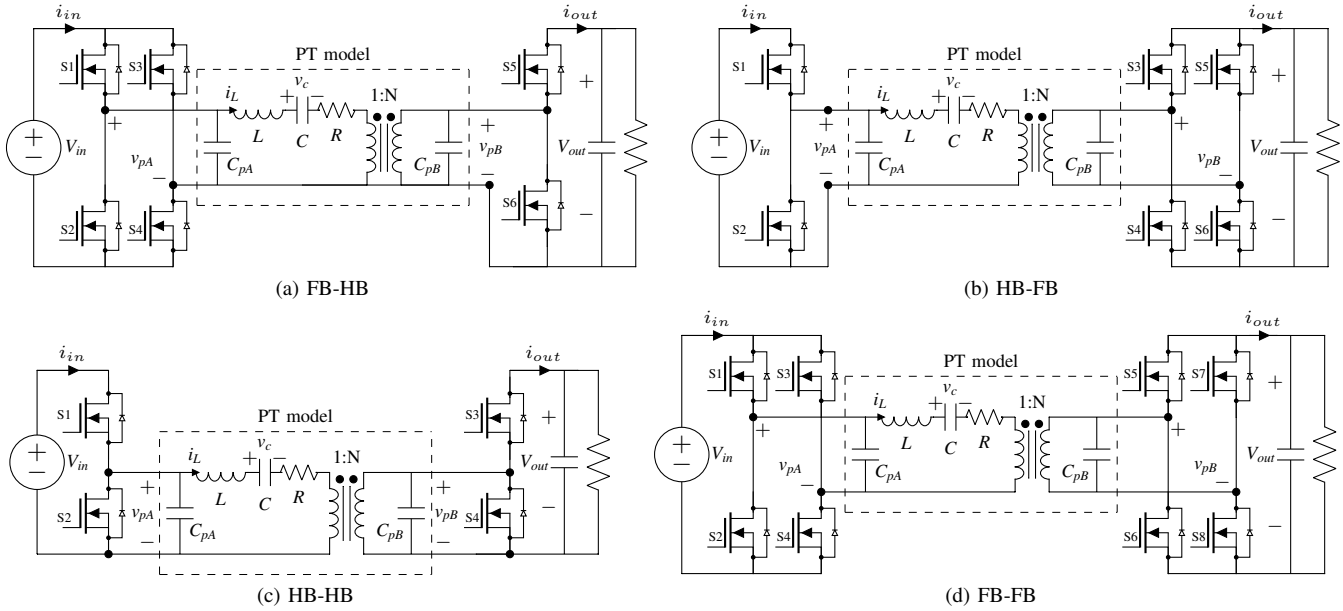


Fig. 2. Topologies for realizing the isolated switching sequences listed in Table III.

C. Practical Considerations

These 16 potential switching sequences can be filtered based on practical considerations such as wide operating ranges capable of the high-efficiency behaviors listed in Section II-A. First, the periodic steady state operating range of a switching sequence is confined by its ability to balance energy and charge within the PT across a switching cycle. This requires the following energy balance equation to hold, using the V_{in}, -V_{in} \| V_{out}, -V_{out}, *Zero+* sequence as an example:

$$V_{in}(|q_{Vin}| + |q_{-Vin}|) = \frac{V_{out}}{N}(|q_{Vout}| + |q_{-Vout}|) \qquad (1)$$

in which we equate the energy sourced from V_{in} to the energy delivered to the load in a single cycle (assuming an ideal PT), and where q_n refers to the direction-specific quantity of charge transferred by i_L (as defined in Fig. 1) during stage n.

Neglecting open stages for now, charge balance on C requires positive- and negative-i_L stages to have equal-magnitude charge transfer. For the same example, this requires:

$$|q_{Vin}| = |q_{-Vin}| = |q_{Vout}| + |q_{Zero+}| = |q_{-Vout}| \qquad (2)$$

The solution to (1) and (2) is the idealized[2] range of voltage gain supported by this switching sequence. In this case, $|q_{Vout}|$ can range from 0 to $|q_{Vin}|$ and still satisfy (2), allowing (1) to become:

$$N < \frac{V_{out}}{V_{in}} < 2N \qquad (3)$$

This is the ideal operating range for which this switching sequence provides the desired high-efficiency behaviors. 4x6- and 6x4-stage switching sequences are capable of maintaining such behaviors across wide voltage gain ranges, but 4x4-stage sequences support only specific voltage gains if any. Thus, 4x4-stage sequences are less practical for most power conversion applications and are therefore eliminated from this scope. On the other hand, 6x6-stage sequences exhibit excess charge circulation (resulting in lower efficiencies) and unnecessary control complexity compared to the 4x6- and 6x4-stage sequences, so we likewise remove them.

The final eight switching sequences are displayed with their ideal voltage gain ranges and other constraints in Table III; this is the proposed set of sequences for isolated dc-dc converters.

D. Topologies

Each switching sequence in Table III can be realized with either a half-bridge or a full-bridge at each PT port as shown

[2]This voltage conversion range is ideal in that (a) it neglects loss in the PT, and (b) it neglects open stage charge transfer differences between the ports.

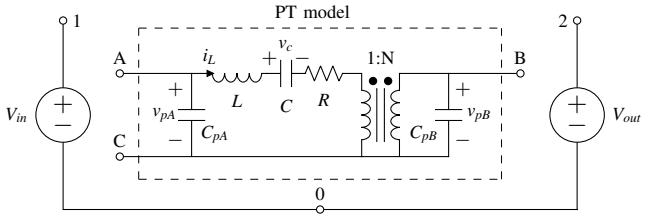


Fig. 3. Non-isolated source-load system assumed for switching sequence enumeration, with the PT represented by the reduced Mason circuit model [30]. Other terminal capacitances are neglected.

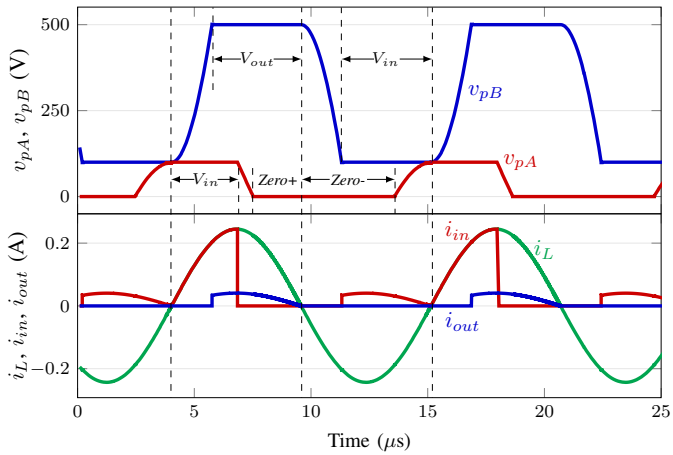


Fig. 4. Example waveforms for switching sequence V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} with each stage labeled in black. v_{pA} and v_{pB} refer to the switch nodes between S1, S2 and S3, S4, respectively, as labeled in Figs. 5 and 10. V_{in} = 100 V, V_{out} = 500 V, and P_{out} = 5 W, assuming the on-board PT parameters of Table V.

in the four isolated topologies of Fig. 2. This sub-sequence enumeration process did not discriminate between the two terminals of a single port, so topologies containing half-bridges can be similarly implemented with the opposite terminal fixed. Although these resulting topologies are common, we emphasize that the proposed switching sequences inform operation of these topologies for the desired high-efficiency behaviors. Also, if the rectifier in any of these topologies operates with a 4-stage sub-sequence, it may be implemented passively to simplify control.

III. Non-isolated Converter Implementations

We next expand the set of proposed converter implementations to non-isolated PTs, which allow for a wider variety of switching sequences that more efficiently utilize the PT for applications not requiring isolation. A non-isolated PT is modeled as shown in Fig. 3; both ports are referenced to node C, creating a 2-port, 3-terminal device. To enumerate non-isolated converter implementations, we assume the common-negative dc-dc source-load system shown in Fig. 3.

The general strategy described in Section II for identifying isolated converter implementations may be adopted for enumerating and downselecting non-isolated converter implementations, though non-isolated PTs do exhibit some key differences. Unlike with isolated PTs, the common node C of a non-isolated PT introduces dependence between the two ports that warrants consideration of both ports together when deriving converter implementations. Also, because the set of potential stages, switching sequences, and topologies is larger without the isolation requirement, additional steps may be taken to downselect these based on practical needs.

The strategy employed in this work to enumerate and downselect non-isolated step-up converter implementations is detailed in Appendix A. This process yields twelve switching sequences of interest, which are displayed in Table IV along with their ideal operating ranges and other constraints. Notably, 6x6 stage sequences are permitted in this set as long as both sub-sequences depend on the same transition of PT terminal C for regulation. Also, these implementations assume $C_{pA} >> C_{pB}$ (typical for a step-up PT), so PT terminals A and C are prohibited from connecting to the $+V_{out}$ node to avoid the impractically-long open stages that would be required to resonate their voltages up to $+V_{out}$ for ZVS.

The non-isolated switching sequences of Table IV can be realized with the topologies displayed in Fig. 5, each requiring four unidirectional-blocking switches. Predictably, this set of non-isolated topologies is larger than that for isolated PTs, allowing additional opportunities for applications not requiring isolation. Further, these topologies could be extended to have full-bridges at their input ports or may be synthesized to provide the capabilities of multiple topologies; this is further discussed in Appendix A-C. Similar to the isolated topologies, the rectifier switches of these topologies may be implemented passively if the output port uses a 4-stage sub-sequence.

IV. Operating Principle

With PT-based dc-dc converter implementations established, we now illustrate their general operation with an example. Fig. 4 displays waveforms for the non-isolated V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} switching sequence; this sequence has one of the highest efficiency capabilities as described in Section VII and can be realized with the topology of Fig. 5(b). This 6x4-stage sequence has three input-port connected/zero stages and two output-port connected stages as labeled on the waveforms, with open stages between each for ZVS. These waveforms also illustrate how the sub-sequences of each port align according to i_L, providing all-positive instantaneous power transfer as shown by i_{in} and i_{out} with unidirectional i_L for each stage (minimizing charge circulation). Although other proposed switching sequences are comprised of different stages and sub-sequences, these principles remain the same.

It should be noted that the waveforms of Fig. 4 require precise switch timing. To simulate a desired switching sequence and PT, we can analyze the PT's states across a resonant cycle, constrain them for periodic steady state operation, and calculate exact switching times. This process is detailed in Appendices B and C, and closed-loop control is discussed in Appendix D.

V. Charge Transfer Analysis

PT-based converter switching sequences can be intuitively analyzed using PT charge transfer patterns. Fig. 6 illustrates how an assumed-sinusoidal i_L cycle can be segmented by input port stages (top plot) or output port stages (bottom plot)

TABLE IV
PROPOSED NON-ISOLATED SWITCHING SEQUENCES, TOPOLOGIES, AND CONSTRAINTS

Switching Sequence (Input | Output)	Topology (Fig. 5)	Ideal V_{out}/V_{in} Range	Charge Transfer Utilization Factors (K)	Voltage Ranges (V_{ppA}, V_{ppB})
V_{in}, *Zero+*, *Zero-* | V_{out}, *Zero-*	(a)	$0 < \frac{V_{out}}{V_{in}} < N$	$0 < K_A < \frac{1}{2}$, $K_{Bin} = 0$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in}	(b)	$1 < \frac{V_{out}}{V_{in}} < N{+}1$	$0 < K_A < \frac{1}{2}$, $K_{Bin} = \frac{1}{2}$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}-V_{in}
Zero+, -V_{in}, *Zero-* | V_{out}-V_{in}, *Zero-*	(d)	$1 < \frac{V_{out}}{V_{in}} < N{+}1$	$0 < K_A < \frac{1}{2}$, $K_{Bin} = \frac{1}{2}$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}-V_{in}
Zero+, -V_{in}, *Zero-* | V_{out}, -V_{in}, *Zero-*	(e)	$0 < \frac{V_{out}}{V_{in}} < N{-}1$	$0 < K_A < \frac{1}{2}$, $\frac{-1}{2} < K_{Bin} < 0$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}+V_{in}
Zero+, -V_{in}, *Zero-* | V_{out}, *Zero-*, V_{in}	(f)	$1 < \frac{V_{out}}{V_{in}} < N$	$0 < K_A < \frac{1}{2}$, $0 < K_{Bin} < \frac{1}{2}$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero+*, *Zero-* | V_{out}, V_{out}-V_{in}, *Zero-*	(g)	$1 < \frac{V_{out}}{V_{in}} < N$	$0 < K_A < \frac{1}{2}$, $0 < K_{Bin} < \frac{1}{2}$, $K_{Bout} = \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero-* | *Zero+*, V_{out}, *Zero-*	(a)	$N < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $K_{Bin} = 0$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}
V_{in}, *Zero-* | V_{in}, V_{out}, V_{in}	(b)	$N{+}1 < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $0 < K_{Bin} < \frac{1}{2}$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}-V_{in}
Zero+, -V_{in}, | -V_{in}, V_{out}-V_{in}, -V_{in}	(c)	$N < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $K_{Bin} = 0$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}
Zero+, -V_{in}, | *Zero+*, V_{out}-V_{in}, *Zero-*	(d)	$N{+}1 < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $0 < K_{Bin} < \frac{1}{2}$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}-V_{in}
Zero+, -V_{in}, | *Zero+*, V_{out}, -V_{in}	(e)	$N{-}1 < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $K_{Bin} = \frac{-1}{2}$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}+V_{in}
V_{in}, *Zero-* | V_{in}, V_{out}, *Zero-*	(g)	$N < \frac{V_{out}}{V_{in}} < \infty$	$K_A = \frac{1}{2}$, $\frac{-1}{2} < K_{Bin} < 0$, $0 < K_{Bout} < \frac{1}{2}$	V_{in}, V_{out}

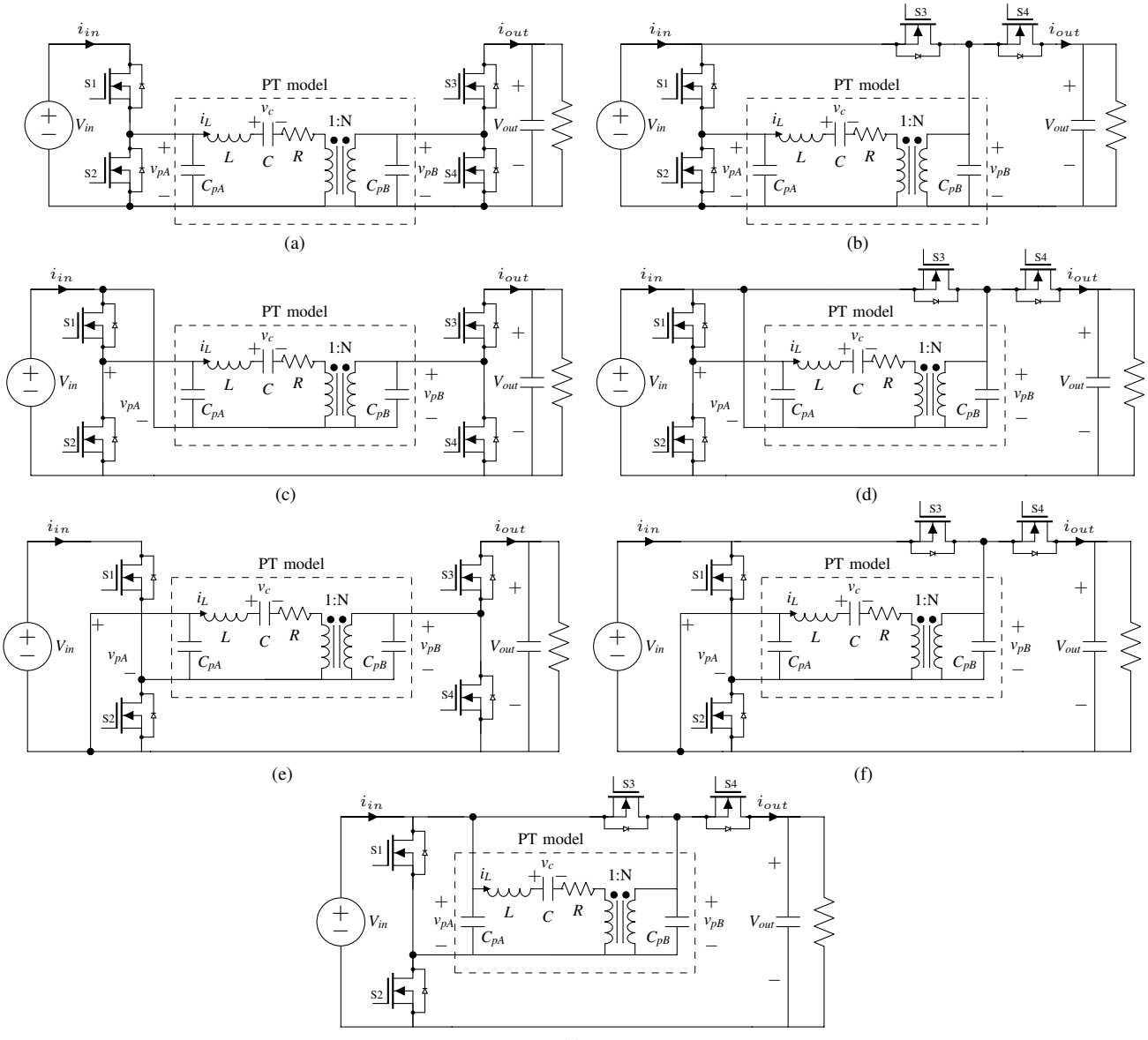


Fig. 5. Topologies for realizing the non-isolated switching sequences listed in Table IV.

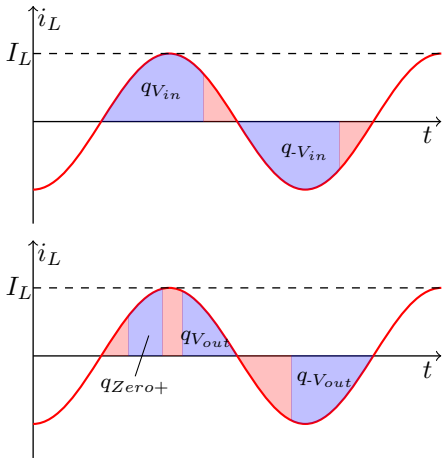


Fig. 6. Sinusoidal approximation of i_L based on the charge transfer q_n required of each stage, from the perspective of the input (top) and output (bottom) ports of an isolated PT. Connected/zero stages shaded purple; open stages shaded red. Example sequence: V_{in}, -V_{in} | V_{out}, -V_{out}, *Zero+*.

for a given switching sequence. The shaded regions under the i_L curve (i.e., the sectional integrals of i_L) equal the charge transferred during each stage, so charge transfer estimates can lend useful information about the PT's resonant cycle and vice versa. Here we introduce PT charge transfer concepts that serve as foundations for analyses in Sections VI and VII.

A. Charge Transfer Utilization Factor (K)

The switching sequences in Tables III and IV vary widely in how effectively they utilize the PT's resonant cycle to transfer energy. We quantify the productivity of a single port's sub-sequence with a "charge transfer utilization factor", K. As defined in [9], K is the proportion of a sub-sequence's connected and zero stage charge transfer that sources energy from the source or delivers energy to the load. K_A refers to the input port sub-sequence sourcing energy from V_{in}, and K_B refers to the output port sub-sequence delivering energy to V_{out} for isolated PTs. For non-isolated PTs, K_{Bin} and K_{Bout} respectively refer to the output port sourcing energy from V_{in} and delivering energy to V_{out}.

Using the output port in Fig. 6 as an example isolated PT sub-sequence,

$$K_B = \frac{Q_{conn(Vout)}}{Q_{conn} + Q_{zero}} = \frac{|q_{V_{out}}| + |q_{-V_{out}}|}{|q_{V_{out}}| + |q_{-V_{out}}| + |q_{Zero+}|} \tag{4}$$

The applicable range for K is bounded by charge balance on capacitance C, which requires the total charge transferred by positive- and negative-i_L to be equal. For an individual port, positive and negative open stage charge transfer is balanced for C_{pA} or C_{pB}, so positive and negative connected/zero stage charge transfer must also be balanced for C. For the above example:

$$|q_{Vout}| + |q_{Zero+}| = |q_{-Vout}| \tag{5}$$

Thus, for this example switching sequence, $|q_{Vout}|$ can range from 0 to $|q_{-Vout}|$, which confines K_B to the range $\frac{1}{2} < K_B < 1$. A similar derivation for K_A yields $K_A = 1$.

When deriving K_{Bin} and K_{Bout} for non-isolated PT sub-sequences, only connected stages involving V_{in} and V_{out}, respectively, are considered in the numerator of (4). K_{Bin} may be positive or negative depending on whether the output port contributes to or counters energy sourced from V_{in}.

The K values for all switching sequences are displayed in Tables III and IV; 4-stage sub-sequences have fixed K values, while 6-stage sub-sequences support ranges of K.

B. Total Charge Transfer

From the perspective of either port, the magnitude of charge transferred by i_L during one resonant cycle can be partitioned into connected/zero stage charge transfer ($Q_{conn} + Q_{zero}$) and open stage charge transfer (Q_{open}) [9]. A sub-sequence's connected/zero stage charge transfer is the following function of charge sourced/delivered and K, using the input port of the isolated sequence in Fig. 6 as an example:

$$Q_{conn} + Q_{zero} = \frac{Q_{in}}{K_A} = \frac{E_{in}}{K_A V_{in}} = \frac{P_{in}}{f K_A V_{in}} \tag{6}$$

in which f may be assumed within the PT's inductive region[3].

A sub-sequence's open stages collectively charge and discharge C_{pA} or C_{pB} across its full peak-to-peak voltage range V_{ppA} or V_{ppB}, respectively, and these ranges are displayed for each switching sequence in Tables III and IV. This results in the following open stage charge transfer for the isolated sequence's input port:

$$Q_{open} = 2C_{pA}V_{ppA} \tag{7}$$

Thus, the total magnitude of charge that must be transferred by i_L during each cycle (Q_{total}) is:

$$Q_{total} = Q_{conn} + Q_{zero} + Q_{open} = \frac{P_{in}}{f K_A V_{in}} + 2C_{pA}V_{ppA} \tag{8}$$

If we were to instead compute Q_{total} from the perspective of the output port for this example,

$$Q_{total} = N\left(\frac{P_{out}}{f K_B V_{out}} + 2C_{pB}V_{ppB}\right) \tag{9}$$

For non-isolated sequences, $K_B = K_{Bout}$ may be substituted into (9) for calculating Q_{total} from the output port's perspective. K_{Bin} impacts the connected/zero stage charge transfer required of the input port's sub-sequence, which must be considered when deriving Q_{total} from the input port's perspective. For that case,

$$Q_{total} = \frac{\frac{P_{in}}{f V_{in}} + 2K_A C_{pA} V_{ppA} + 2K_{Bin} C_{pB} V_{ppB}}{K_A + \frac{K_{Bin}}{N}} \tag{10}$$

Q_{total} provides means to easily assess the PT's total charge transfer, which we use to derive the PT's amplitude of resonance in Section V-C and ZVS region in Section VI.

[3]The inductive region for a PT is narrow with respect to frequency, so the exact f assumed in this calculation has little effect on the result as long as it falls within the PT's inductive region.

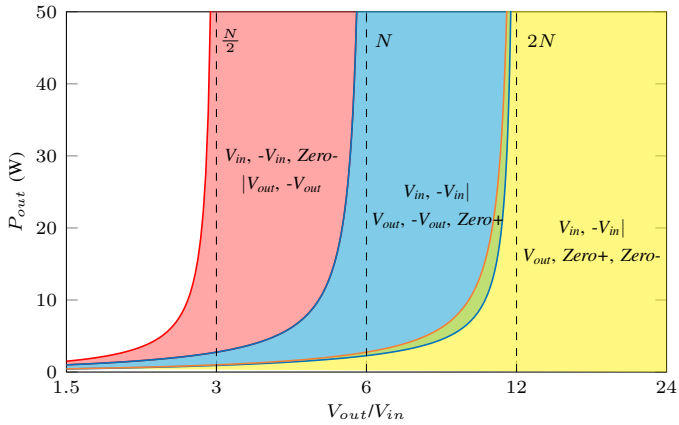


Fig. 7. ZVS region defined by (13) for three isolated switching sequences, assuming the manufacturer-provided PT parameters in Table V and V_{in} = 100 V. Ideal boundaries are marked with dotted lines.

C. Amplitude of PT Resonance

The total charge transferred by i_L in one resonance cycle can be utilized to estimate the amplitude of i_L (I_L), which quantifies the PT's amplitude of resonance [9]. If we assume i_L to be sinusoidal as illustrated in Fig. 6, I_L can be calculated by equating Q_{total} to the integral of $|i_L|$ over one cycle:

$$Q_{total} = 2\int_0^{\frac{1}{2f}} i_L dt = 2\int_0^{\frac{1}{2f}} I_L \sin(2\pi f t)dt = \frac{2I_L}{\pi f} \tag{11}$$

$$\Rightarrow I_L = \frac{\pi}{2} f Q_{total} = \pi\Big(\frac{P_{in}}{2K_A V_{in}} + fC_{pA}V_{ppA}\Big) \tag{12}$$

using the input port of an isolated PT as an example, though I_L may also be computed with Q_{total} of (9) or (10). I_L may be calculated from the perspective of either PT port, but doing so using a 4-stage-sequence port allows simpler computation with constant K value(s). For six-stage sequences, K varies within a defined range as shown in Section V-A but can be computed based on the operating point as detailed in [9]. This is also required for non-isolated switching sequences for which both K_{Bin} and K_{Bout} are unfixed[4].

I_L provides important insight into the PT's energy storage and loss, and we employ it to analytically estimate efficiency in Section VII.

VI. Zero-Voltage-Switching Region

Ensuring a switching sequence is capable of ZVS is the first step in evaluating its suitability for a given operating point and PT. In addition to switch capacitances, the PT terminal capacitances C_{pA} and C_{pB} must resonate to exactly their next-stage voltages for ZVS during open stages. Here we determine the operating region for which a given switching sequence is capable of ZVS considering this open stage charge transfer. This analysis assumes C_{pA} and C_{pB} dominate their respective switch node capacitances, though neighboring switch capacitances may be added to C_{pA} and C_{pB} if significant.

[4]For PTs with $N >> 1$, $K_{Bin} \approx 1 - \frac{NV_{in}}{2V_{out}}$ for the V_{in}, *Zero-* | V_{in}, V_{out}, V_{in} sequence, $K_{Bin} \approx \frac{NV_{in}}{2V_{out}}$ for the *Zero+*, -V_{in}, | *Zero+*, V_{out}- V_{in}, *Zero-* sequence, and $K_{Bin} \approx -\frac{1}{2} + \frac{NV_{in}}{2V_{out}}$ for the V_{in}, *Zero-* | V_{in}, V_{out}, *Zero-* sequence (based on the strategy for deriving K in [9]).

TABLE V
Example PT Parameter Values

Parameter	Manufacturer-Provided [33]	On-board Measurement
C_{pA}	960 pF	1.6 nF (with switches)
C_{pB}	8 pF	83 pF (with diodes)
L	59 mH	44 mH
C	60 pF	72 pF
R	24 Ω	27 Ω
N	6	6 (assumed)

We can examine a given switching sequence's ZVS region by first calculating the total charge transferred by i_L (detailed in Section V-B) from the perspective of each port. This calculation considers the charge transfer necessary for all stages of the switching sequence, including open stages for ZVS, assuming the aforementioned constraints (e.g., i_L polarities) are preserved. For the isolated case,

$$Q_{total} = \frac{P_{in}}{fK_A V_{in}} + 2V_{ppA}C_{pA} = N\Big(\frac{P_{out}}{fK_B V_{out}} + 2V_{ppB}C_{pB}\Big) \tag{13}$$

and for the non-isolated case,

$$\begin{aligned} Q_{total} &= \frac{\frac{P_{in}}{fV_{in}} + 2K_A C_{pA}V_{ppA} + 2K_{Bin}C_{pB}V_{ppB}}{K_A + \frac{K_{Bin}}{N}} \\ &= N\Big(\frac{P_{out}}{fK_{Bout}V_{out}} + 2V_{ppB}C_{pB}\Big) \end{aligned} \tag{14}$$

The two sides of these Q_{total} equations are equal by definition and reveal likely-significant differences in the charge transfer requirements for each PT port. For a given operating point, the switching sequence compensates these differences by varying K_A and/or K_B (K_A, K_{Bin}, and/or K_{Bout} for the non-isolated case), which are fixed for 4-stage sequences and confined to specific ranges for 6-stage sequences. Thus, these ranges for K dictate the operating region for which (13) and (14) are true, which defines the switching sequence's ZVS region.

Equipped with PT parameters and a given switching sequence's V_{ppA}, V_{ppB}, and K boundaries, we can solve (13) or (14) for the range of operating points capable of ZVS. Neglecting R in the PT (i.e., $P_{in} = P_{out}$), Fig. 7 maps the ZVS regions of three neighboring isolated switching sequences on power and voltage gain axes; this is a useful representation for visualizing the operating regions served by different switching sequences. These sequences allow for a continuous range of ZVS, with boundaries between FB and HB sequences overlapping. As power increases, connected/zero stages dominate the PT's charge transfer, and the boundaries for these ZVS regions approach their ideal V_{out}/V_{in} range asymptotes (calculated in Section II-C). Known nonidealities such as loss and parasitic capacitance can be implemented in (13) through P_{in} or P_{out} and C_{pA} or C_{pB}, respectively, but neither disrupt the continuity of ZVS across sequence combinations.

Closed-loop control for ZVS and other high-efficiency behaviors is discussed in Appendix D.

VII. Efficiency Estimation

Within topological and ZVS constraints, a switching sequence may be selected for a given PT and operating region based on achievable efficiency. Calculating the PT's exact

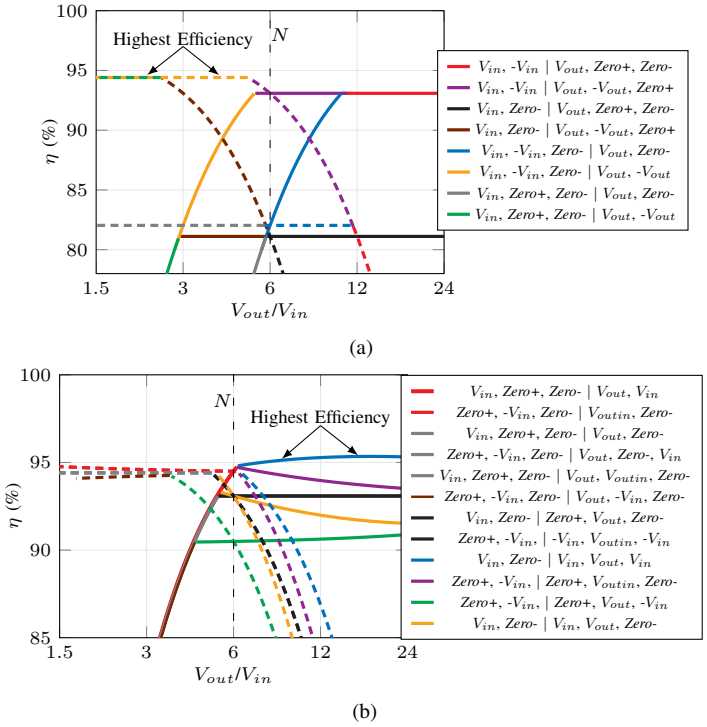


Fig. 8. Estimated efficiency vs. $\frac{V_{out}}{V_{in}}$ for varying only V_{in} (dashed lines, V_{out} = 400 V) or only V_{out} (solid lines, V_{in} = 66.7 V) for (a) isolated sequences in Table III with P_{out} = 8 W, and (b) non-isolated sequences in Table IV with P_{out} = 2 W. Efficiency estimates based on (15), assuming the manufacturer-provided PT parameters in Table V and the ZVS regions of (13) and (14). Sequences marked by the same color within a plot have indistinguishable efficiency characteristics, though only black and gray correspond between (a) and (b). In legend, V_{outin} = V_{out}-V_{in}.

efficiency for a given switching sequence is not directly accessible without an exact periodic steady state solution (Appendix C-D), which requires heavy computation. Thus, this section explores tools for analytically estimating PT efficiency.

A. Efficiency Model

The dominant loss mechanism for a piezoelectric component vibrating in the proximity of its resonant frequency tends to be mechanical loss [34]. Thus, we focus on the PT's mechanical efficiency for estimating the performance of a PT-based converter implementation. Mechanical efficiency can be estimated using the amplitude of resonance in (12) as follows [9]:

$$\eta = \frac{P_{out}}{P_{out} + fE_{loss}} \approx \frac{P_{out}}{P_{out} + \frac{1}{2}I_L^2 R} \tag{15}$$

Using this estimation technique, Fig. 8 compares the efficiencies of all switching sequences in Tables III and IV across their respective ZVS regions (as derived in Section VI) using the manufacturer-provided PT parameters in Table V. Beginning at $\frac{V_{out}}{V_{in}} = N$, Fig. 8 illustrates how efficiency changes with voltage conversion ratio when varying only V_{in} (dashed lines) or only V_{out} (solid lines) for each sequence. The efficiency trends are not symmetrical due to offsets in their ZVS boundaries, but they do demonstrate considerably wide gain ranges with high efficiency.

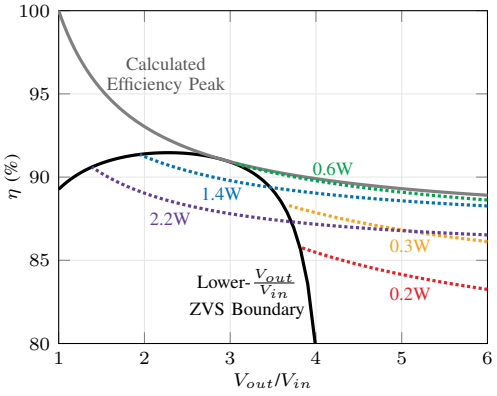


Fig. 9. Achievable efficiency vs. $\frac{V_{out}}{V_{in}}$ for sequence V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} considering the ZVS boundary of (14), assuming the on-board PT parameters in Table V and V_{out} = 360 V. Example power levels marked by color.

Fig. 8 also reveals significant differences in obtainable efficiency between the sequences themselves. For a given operating point and PT, (15) shows that I_L should be minimized for high efficiency. However, sequence characteristics that minimize I_L are in direct conflict (ie. a full-bridge sequence enables higher K than a half-bridge sequence but requires twice the open stage charge transfer), creating a tradeoff that must be evaluated by the designer. Full-bridge sequences achieve highest efficiencies for the power level of Fig. 8(a), though half-bridge sequences are capable of these efficiencies at a lower power level as shown in Fig. 8(b) (sequences plotted in black and gray are directly comparable between the plots since they can be equally realized with or without isolation). Further, Fig. 8(b) illustrates how some non-isolated sequences are capable of higher efficiencies than isolation-compatible sequences if permitted by the application. For both plots, the specific implementation that achieves highest efficiency varies based on operating point and PT properties, underscoring the utility of this estimation technique.

B. Peak Efficiency

Evaluating the peak achievable efficiency for a given switching sequence and PT is also useful when selecting and designing an implementation. To estimate peak efficiency, we can directly maximize η with respect to operating point parameters. For a switching sequence with a fixed K_B or K_{Bout} (i.e., a 4-stage sub-sequence), efficiency is maximized with respect to P_{out} when

$$P_{out} = 2fC_{pB}V_{ppB}V_{out}K_B \tag{16}$$

which provides peak efficiency of

$$\eta_{peak} = \frac{1}{1 + \frac{2\pi^2 fN^2 RC_{pB}V_{ppB}}{K_B V_{out}}} \tag{17}$$

for which $K_B = K_{Bout}$ may be substituted for non-isolated sequences. For switching sequences with fixed K_A, this maximum efficiency and corresponding power condition can be similarly derived to be functions of C_{pA}, V_{in}, V_{ppA}, and K_A (and other relevant parameters related to K_{Bin}, if applicable).

PT-based converters can be designed to achieve maximum efficiency for a nominal operating point by satisfying (16). For example, to increase the maximum-efficiency power level [5] for a given voltage specification, the designer may choose a PT with a higher $f * C_{pB}$ product or a switching sequence with a higher $V_{ppB} * K_B$ product.

It should be noted that the peak efficiency operating point in (17) is only achievable if it falls within the switching sequence's ZVS region. Fig. 9 displays the peak efficiency and ZVS-boundary efficiency for the V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} switching sequence with the on-board measured PT parameters in Table V. For $\frac{V_{out}}{V_{in}} > 3$, the peak efficiency operating point falls within the ZVS region and can be achieved along with several other high-efficiency operating points surrounding the peak. For $\frac{V_{out}}{V_{in}} < 3$, the ZVS boundary prevents peak efficiency from being reached, confining the achievable efficiency with ZVS to a lower value.

VIII. Experimental Validation

At this time, non-isolated PTs tend to have wider commercial availability than isolated PTs due to their prevalence in CCFL backlight drivers. Therefore, we illustrate an example converter implementation and validate the analyses herein with the non-isolated V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} switching sequence. This is one of the highest-performing sequences in the $\frac{V_{out}}{V_{in}} < N$ range according to Fig. 8(b), and because it regulates with its input port (i.e., K_{Bout} is fixed), it can be implemented with a circuit topology having only two active switches such as Fig. 10.

A. Prototype

We implement the topology of Fig. 10 on a two-layer 1-oz copper board as shown in Fig. 11, with the parts listed in Table VI. The STEMiNC PT was selected from commercially available PTs based on performance capability using the efficiency estimation method of Section VII. Since C_{pA} and C_{pB} are relatively small for this PT, both the active switches and Schottky diodes were selected for minimal output capacitance to minimize their contributions to the switch node capacitances. Once mounted on the board with all components, the PT's effective parameters were characterized using an impedance analyzer (with no external voltage bias, and 1 Vpp excitation) to have the on-board values provided in Table V.

We operate this prototype with open-loop control of all gate signals, which we manually tune for the desired switching sequence and its high-efficiency behaviors. Since this work focuses on steady-state operation rather than start-up or dynamic behavior, the open-loop switching times are applied as-is at start-up and suffice for establishing the desired steady-state operation. The effect of an oscilloscope probe on the PT's output port capacitance is non-negligible, so this probe is removed for the experimental results of Fig. 14. Further, because the PT's properties have high dependence on temperature, the results of Fig. 14 are acquired shortly after powering up the converter and not necessarily at thermal equilibrium.

[5]Mechanical loss becomes more dominant in the PT at higher power, so the efficiency model is expected to remain valid to the extent that the PT's model parameters remain valid (as further discussed in Appendix E).

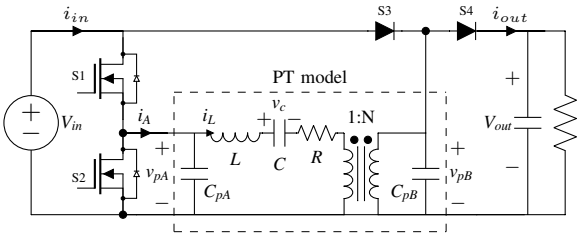


Fig. 10. Example implementation of the topology in Fig. 5(b), with S3 and S4 implemented as diodes.

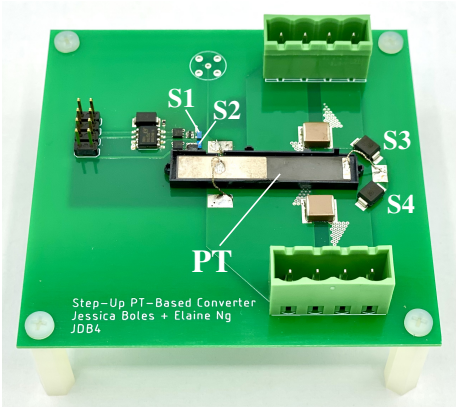


Fig. 11. Prototype circuit board for the topology of Fig. 10.

TABLE VI
Prototype Parts List

Component	Part
PT	STEMiNC SMSTF50P2S6
Active Switch	EPC 2012C GaN FET
Schottky Diode	Genesic Semiconductor GB01SLT06-214
Gate Driver	Texas Instruments UCC27611

B. Waveforms

This prototype's experimental waveforms are displayed in Fig. 12. These waveforms illustrate key elements of the desired waveforms in Fig. 4, including the switching sequence's high-efficiency behaviors. The resonant transitions of v_{pA} and v_{pB} between connected stages indicate ZVS, and the positioning of these stages with reference to the inverter's output current i_A demonstrates all-positive instantaneous power transfer and unidirectional current within each stage to minimize charge circulation. It is also shown that i_A drops to near-zero during open stages, indicating that most of i_L is being used to charge/discharge C_{pA} and therefore validating that C_{pA} is dominant over switch capacitances as assumed for ZVS analysis in Section VI.

Fig. 13 illustrates how the switching sequence adapts for different voltage gains with constant V_{in} and P_{out}. Between these operating points, the input port's *Zero+* stage drastically changes in length, ultimately disappearing in Fig. 13(a). This translates to a change in K_A, which can serve as a control handle for regulating V_{out} as discussed in Appendix D.

C. Gain

Fig. 14(a) plots experimental $\frac{V_{out}}{V_{in}}$ as a function of frequency for different power levels, and each curve represents a constant load resistance. The proposed sequences require operation in

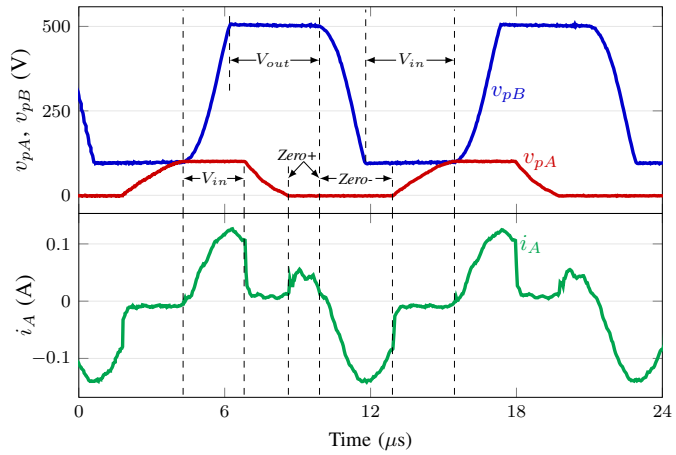


Fig. 12. Experimental waveforms for switching sequence V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} operating at V_{in} = 100 V, V_{out} = 500 V, and P_{out} = 1.5 W. Stages are labeled in black, and v_{pA} and v_{pB}, and i_A are defined in Fig. 10.

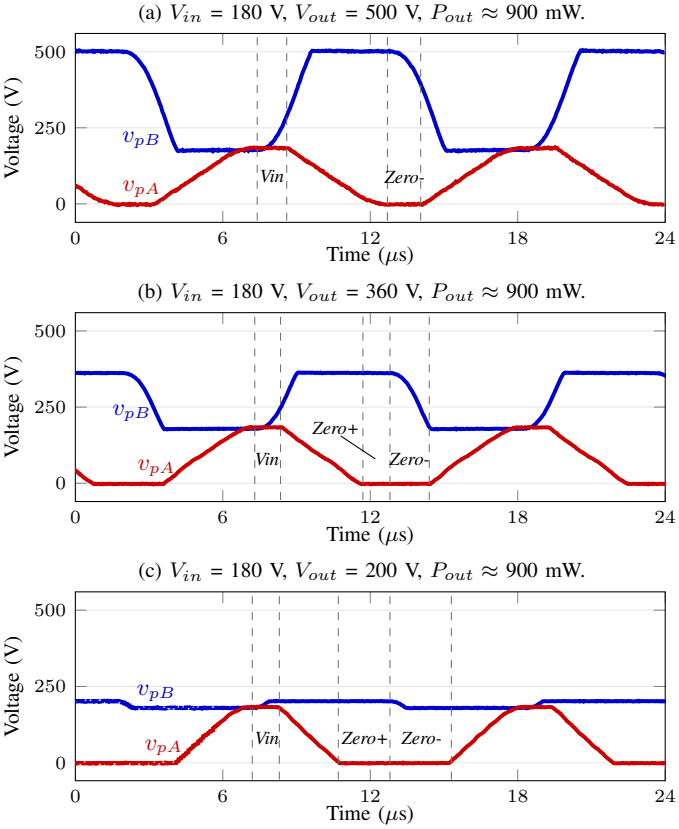


Fig. 13. Experimental waveforms for switching sequence V_{in}, *Zero+*, *Zero-* | V_{out}, V_{in} operating at 900 mW and V_{in} = 180 V for (a) $\frac{V_{out}}{V_{in}}$=2.78, (b) $\frac{V_{out}}{V_{in}}$=2, and (c) $\frac{V_{out}}{V_{in}}$=1.11 with the prototype described in Section VIII-A. Stages of the input port sub-sequence are labeled.

the PT's inductive region, which is slightly above its resonant frequency (≈89 kHz for this PT). Fig. 14(a) maps how these switching sequences adapt for different V_{out} and/or power, analogous to selecting K_A or constraining the final degree of freedom in the periodic steady state solution of Appendix C-B. For the same $\frac{V_{out}}{V_{in}}$, higher power and/or voltage is achieved with frequencies at the low end of the inductive region

TABLE VII
ESTIMATED POWER STAGE LOSS BREAKDOWN

PT	Switch $R_{ds,on}$	Diode V_{fwd}	Total	η
60 mW	77 μW	4 mW	64 mW	90.3 %

Operating point: V_{in} = 120 V, V_{out} = 360 V, P_{out} = 0.6 W, I_L = 67 mA

(closer to the resonant frequency), and lower voltage/power is obtained at higher frequencies (but not exceeding the anti-resonant frequency). Closed-loop control for such is discussed in Appendix D.

D. ZVS and Efficiency

To evaluate the prototype's performance, we conduct data sweeps over various $\frac{V_{out}}{V_{in}}$ and power levels. Table VII shows the estimated power-stage loss breakdown for an example operating point, revealing the PT to be the dominant source of loss. Fig. 14(b) plots power-stage efficiency vs. $\frac{V_{out}}{V_{in}}$ according to output power, keeping V_{out} constant and varying V_{in}. The relatively flat efficiency slope for a given power level echoes the estimated trend for PT efficiency in Figs. 8(b) and 9. For constant V_{out}, this sequence is capable of wide $\frac{V_{out}}{V_{in}}$ ranges with little efficiency penalty.

In 14(b), each power sweep was conducted for the full $2 < \frac{V_{out}}{V_{in}} < 6$ range to the extent that ZVS could be achieved. For $P_{out} < 0.8$ W, the ZVS boundary was encountered before the sweep could be completed at low $\frac{V_{out}}{V_{in}}$. Thus, we overlay this switching sequence's modeled ZVS boundary from Fig. 9 (given the on-board PT model characteristics provided in Table V), which appropriately traces the observed ZVS boundary. Further, the experimental efficiency peaks with respect to power for $\frac{V_{out}}{V_{in}}$ greater than the ZVS boundary, as also modeled in Fig. 9.

Fig. 14(c) similarly displays efficiency vs. $\frac{V_{out}}{V_{in}}$ according to power level for constant V_{in} and varying V_{out}. In this case, efficiency drastically drops as $\frac{V_{out}}{V_{in}}$ decreases, a trend that is also reflected in Fig. 8(b) for this sequence. Although this may be unattractive for some applications, Fig. 8 suggests the opposite trend to be true for other sequences serving the $\frac{V_{out}}{V_{in}} > N$ region (i.e., these sequences would be capable of high-efficiency voltage regulation with constant V_{in}).

Overall, the efficiency trends of this prototype validate the estimated trends of Section VII, constrained by the ZVS boundary derived in Section VI. The peak experimental efficiencies track the modeled values, though with steeper decline with respect to power than expected. In addition to non-PT losses in the circuit, this discrepancy can be attributed to the charge transfer analysis of Section V neglecting R; the calculated value for I_L does not consider the additional charge transfer necessary to make up for loss in the PT and therefore degrades in validity with higher loss. This discrepancy may also be due to differences between the PT's small-signal and large-signal characteristics with respect to amplitude of resonance as discussed in Appendix E.

The efficiencies obtained for this prototype exceed the whole-converter efficiencies reported for most magnetic-less PT-based dc-dc converters in the literature, attesting to the high performance capabilities of the proposed switching sequences.

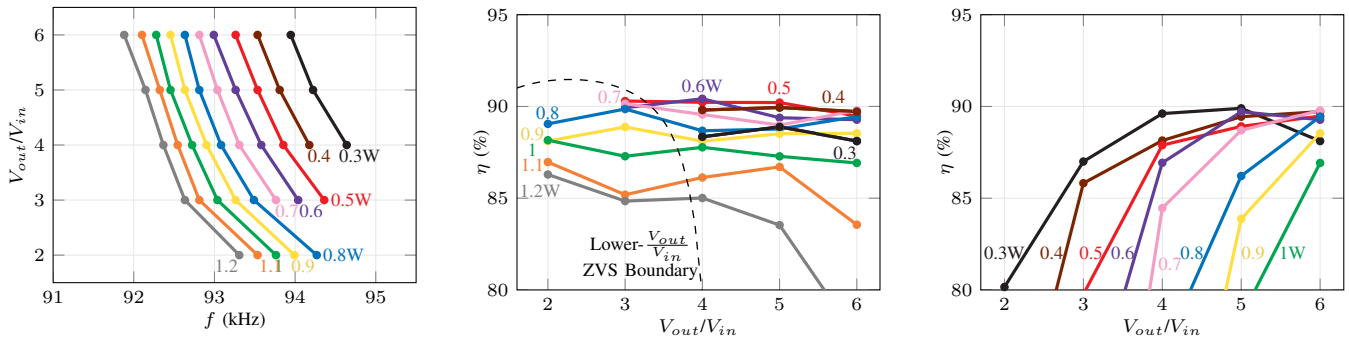


Fig. 14. (a) Experimental $\frac{V_{out}}{V_{in}}$ vs. frequency for constant V_{out} = 360V and various power levels (marked). Curves represent constant load resistances. (b) Experimental power-stage efficiency vs. $\frac{V_{out}}{V_{in}}$ for constant V_{out} = 360V and various power levels (marked). ZVS boundary calculated using (14). (c) Experimental power-stage efficiency vs. $\frac{V_{out}}{V_{in}}$ for constant V_{in} = 100V and various power levels (marked). Efficiencies do not consider auxiliary power.

The power levels corresponding to these efficiencies is limited by the off-the-shelf PT; this dependence on PT parameters, along with strategies for increasing power capability, is discussed in Section VII-B. Further gains in efficiency and power handling capability may be achieved through optimization of the PT itself.

IX. Conclusion

In this work, we have systematically enumerated isolated and non-isolated dc-dc converter implementations that rely solely on a PT for energy storage. This process yields eight isolated switching sequences and twelve non-isolated switching sequences that facilitate high-efficiency behaviors across wide operating ranges. Such high-efficiency behaviors include ZVS, all-positive instantaneous power transfer, and minimum charge circulation. These switching sequences can be realized with practical topologies, many of which may be implemented with only two active switches.

Charge transfer analysis can be employed to quantify PT cycle utilization, derive ZVS boundaries, and estimate PT efficiency; these steps are useful for selecting the most appropriate converter implementation and/or PT for a given application. ZVS boundaries are continuous across switching sequences but skew at low power due to differences in PT port capacitances. Efficiency estimation through the amplitude of resonance model enables simple comparison of performance between sequences, which vary in relative efficiency capability depending on the desired operating point and boundaries for ZVS. Non-isolated switching sequences are found to be capable of higher efficiencies than isolated sequences for the same PT. Once a converter implementation has been selected, we can solve for periodic steady state switching times that may be used for ideal simulation of a desired converter topology and switching sequence.

This analysis is validated in an experimental prototype based on a commercially-available PT. The proposed switching sequences enable higher whole-converter efficiencies than reported for most magnetic-less PT-based converters through strategic utilization of the PT. The proposed ZVS boundary and efficiency models provide close approximation of the trends observed experimentally, attesting to their utility when selecting an implementation. Assuming further optimization of the PT, PT-based converters are auspicious for high-voltage, low-power applications, especially those requiring significant conversion ratios and/or isolation.

Appendix A
Non-isolated Switching Sequences and Topologies

Non-isolated PT-based converter switching sequences can be enumerated using the process detailed in Section II with modifications to accommodate the PT's common terminal. For this process, we assume the non-isolated source-load system and non-isolated PT model shown in Fig. 3.

A. Terminal Configurations

We begin by identifying connections to the source/load system for each of the three PT terminals and arranging these into potential *terminal configurations*. A terminal configuration is a specific combination of how the PT's three terminals are connected, which inherently specifies stages between the two ports. We focus on only connected/zero stages at both ports for these configurations, assuming open stages occur between each for either or both ports as necessary. We refer to each configuration by the PT's terminal labels (A, B, and C), each followed by the terminal's source/load connection (0, 1, and 2), as defined in Fig. 3[6]. Permuting the three possible source/load connections for each of the three PT terminals reveals 27 potential terminal configurations for non-isolated PTs.

We then filter these configurations assuming a step-up PT, and therefore $V_{out} > V_{in}$. Accordingly, we first reduce to configurations for which terminals A and C do not connect to node 2 ($+V_{out}$), since C_{pA} is often significantly greater than C_{pB} for step-up PTs (i.e., it would take an impractical length of time to resonate the node voltages of A or C to $+V_{out}$ for ZVS)[7]. Similar to isolated PTs, we also constrain the polarity of i_L for (1) all-positive instantaneous power transfer, again assuming i_L to be unidirectional within a single configuration, and (2) charging/discharging C_{pA} or C_{pB} for ZVS during

[6]For example, the configuration "A1B2C0" has terminal A connected to $+V_{in}$, terminal B connected to $+V_{out}$, and terminal C connected to *Gnd*.

[7]It should be noted that this constraint is specific to step-up configurations. For step-down configurations, terminals A and C should not connect to V_{in}.

TABLE VIII
POTENTIAL NON-ISOLATED CONFIGURATIONS BY i_L POLARITY

Polarity	Terminal Configurations	Terminal Transitions
$i_L > 0$	A0B2C0, A1B0C0, A1B0C1, A1B1C0, A1B2C0, A1B2C1	A1 → A0, B0 → B2, C0 → C1, B1 → B2
$i_L < 0$	A0B0C1, A0B1C0, A0B1C1	A0 → A1, B2 → B0, C1 → C0, B2 → B1
Either	A0B0C0, A1B1C1	N/A

transitions between configurations. Thus, the eleven remaining configurations and eight possible terminal transitions between them are shown with their i_L constraints in Table VIII.

B. Switching Sequences

To enumerate switching sequences, we permute the potential configurations listed in Table VIII. Similarly to isolated PTs, we assume open stages occur between the connected stages of each port to enable ZVS. Further, since supporting wide voltage gain ranges was found to require six or more stages for both isolated PTs in Section II-C and PRs in [9], we likewise focus on six-stage sequences for non-isolated PTs. Enumerating permutations of three configurations in Table VIII reveals 330 distinct six-stage sequences, which we then downselect for sequences with:

1) A maximum of five total terminal connections to the source/load system (the minimum number of terminal connections that yields viable switching sequences).
2) At least one connection to node 1 ($+V_{in}$) and one connection to node 2 ($+V_{out}$).
3) No two terminals always tied together.
4) No repetition of the same terminal configuration.
5) At least one configuration each for positive and negative i_L (for charge balance on C across the cycle).
6) One sequential span each of positive and negative i_L, considering both connected and open stages for each port (for completion in one PT resonant cycle) [9].
7) Sequential zero stages for a given port realized at the same node in the source-load system (to avoid excess charge circulation).

Once enumerated, these switching sequences can be conceptualized by the sub-sequences of each PT port, and the ideal voltage conversion ranges for these sequences can be calculated using the same energy and charge balance strategy presented in Section II-C.

We further downselect to switching sequences that would be simplest to maintain with closed-loop control, requiring as few control loops as possible. Thus, we filter to sequences for which only one PT terminal transitions between two connected stages in a single half-cycle (i.e., between two connected stages of the same i_L polarity). Only one such transition is needed for voltage regulation as described in Appendix D, so sequences with additional transitions of this nature require unnecessary control complexity and are therefore eliminated. This results in 4x6 stage switching sequences if the transitioning terminal is A or B, but it creates a 6x6 stage sequence if C serves as the transitioning terminal; we consider 6x6 stage sequences only in the context of this transition for non-isolated PTs.

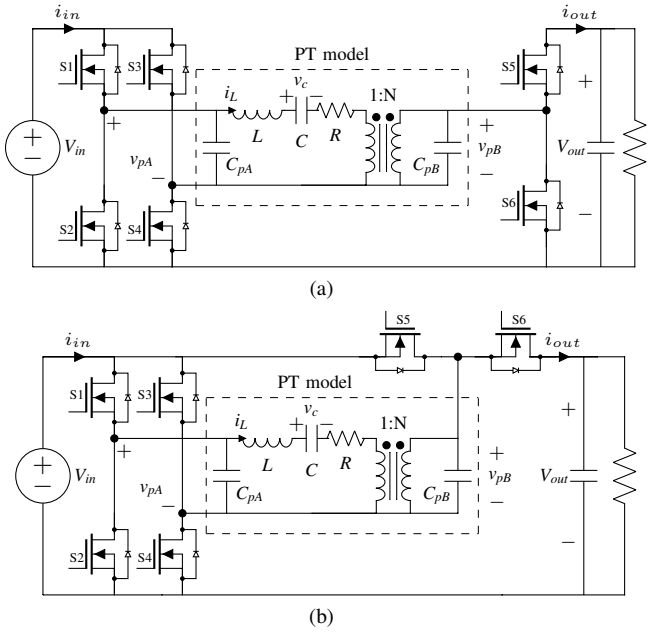


Fig. 15. Synthesized topologies for realizing multiple non-isolated switching sequences listed in Table IV, along with additional sequences that require a full-bridge inverter.

This filtering process yields twelve switching sequences of interest for non-isolated PT-based converter implementations. These sequences are displayed in Table IV in terms of each port's sub-sequences, along with their ideal voltage conversion ranges and other constraints.

C. Expanded Non-isolated Topologies

The non-isolated switching sequences of Table IV can be realized with the topologies displayed in Fig. 5, each requiring four unidirectional-blocking switches. To realize multiple sequences, the topologies of Fig. 5 may be synthesized with additional switches. Fig. 15 displays two example topologies that are each capable of realizing multiple switching sequences in Table IV. Further, each of these topologies support their own additional sets of switching sequences that require a full-bridge inverter.

The topologies of Fig. 5 may be similarly expanded to allow three terminal connections for node B, though this requires adding a bidirectional-blocking switch.

APPENDIX B
RESONANT CYCLE MAPPING

During the enumeration process, the switching sequences at each PT port were assumed to operate independently, so the timing of stage transitions at each port relative to the other is not specified. Mapping the switching sub-sequences of each port to the PT's resonant cycle is imperative for analyzing the PT's resonance and solving for periodic steady state operation. We refer to the span of resonance between each transition point (at either port) as a *segment*, and segments vary based on switching sequence, operating point, and PT parameters.

A. Charge Transfer by Stage

To map a switching sequence to the PT's resonant cycle, we first solve for the charge transferred by i_L during each of its stages. The connected/zero stage charge transfer for each port is established by the energy transferred to/from the source-load system and charge balance on C as described in Section V-A. For the sub-sequence V_{out}, -V_{out}, *Zero+*, this results in:

$$|q_{V_{out}}| + |q_{-V_{out}}| = \frac{E_{out}}{V_{out}} = \frac{P_{out}}{fV_{out}} \tag{18}$$

$$|q_{V_{out}}| + |q_{Zero+}| = |q_{-V_{out}}| \tag{19}$$

These equations suffice for calculating connected/zero stage charge transfer in a 4-stage sequence, but one additional constraint is needed for a 6-stage sequence. This is provided by the sequence's energy balance equation (1), which relates the connected/zero stage charge transfer of each port. Thus, the charge transfer during each of the five connected/zero stages in a 4x6- or 6x4-stage sequence can be solved using this simple system of equations.

The charge transfer of each open stage can be calculated using the change in voltage (ΔV_{pA} or ΔV_{pB}) on C_{pA} or C_{pB} required for ZVS as follows, using the output port for example:

$$|q_{\Delta V_{pB}}| = C_{pB}\Delta V_{pB}. \tag{20}$$

B. Stage Transition Ordering

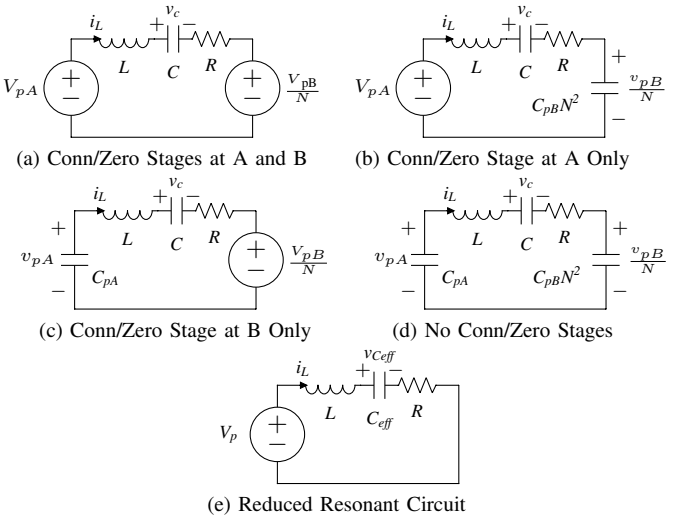
The charge transferred by i_L during each stage governs the stages' time durations, which we now utilize to map the order of all stage transitions between the two ports. First, both the input and output port sequences have stage transitions that must be synchronized to the PT's i_L zero crossings to satisfy the i_L polarity constraints in Tables II and VIII. These transitions align the two switching sequences temporally.

Once the i_L zero crossing transitions have been defined, the durations of each stage neighboring the zero crossings can be compared port-to-port based on the charge that must be transferred by i_L during each individual stage as calculated in Appendix B-A. The transitions for stages requiring less charge transfer occur temporally closer to the i_L zero crossing, and stages requiring more charge transfer begin or end further in time from the zero crossing. This process can be extended to other stage transitions by adding their stages' charge transfer onto a port's existing sum and then comparing between ports.

Using this strategy, we can map the order of all stage transitions at either port throughout the switching sequence, which divide the PT's resonant cycle into segments. This is useful for analyzing the PT's resonance and constraining for periodic steady state as detailed in Appendix C.

APPENDIX C
PERIODIC STEADY STATE SOLUTION

Once a switching sequence has been selected, we can analyze the PT's states across its resonant cycle and constrain them for periodic steady state operation, which produces useful information including switching times. This first requires determining the order in which stage transitions occur, which is detailed in Appendix B. The analysis of this section stems from principles of state plane analysis illustrated for PRs in [9] and for isolated step-down PTs in [1].



(a) Conn/Zero Stages at A and B
(b) Conn/Zero Stage at A Only
(c) Conn/Zero Stage at B Only
(d) No Conn/Zero Stages
(e) Reduced Resonant Circuit

Fig. 16. Equivalent circuits for PT resonance based on port connections.

TABLE IX
PARAMETERS FOR REDUCED RESONANT CIRCUIT (FIG. 16(E))

Connected/Zero Stage Ports	V_p	C_{eff}	$v_{C_{eff}}$
A and B	V_{pA}-$\frac{V_{pB}}{N}$	C	v_c
A Only	V_{pA}	$\frac{CC_{pB}N^2}{C+C_{pB}N^2}$	$v_c + \frac{v_{pB}}{N}$
B Only	-$\frac{V_{pB}}{N}$	$\frac{CC_{pA}}{C+C_{pA}}$	$v_c - v_{pA}$
none	0	$\frac{CC_{pA}C_{pB}N^2}{C+C_{pA}+C_{pB}N^2}$	$v_c - v_{pA} + \frac{v_{pB}}{N}$

A. Equivalent Resonant Circuits

Each segment of the PT converter's cycle can be analyzed using an equivalent resonant circuit. There are four potential equivalent resonant circuits corresponding to connected/zero stages or open stages at each port; these are shown in Figs. 16(a)-(d) with voltage sources representing connected/zero stage voltages and terminal capacitances (C_{pA} or C_{pB}) present during open stages. The PT resonates in a single resonant circuit for the duration of each segment, switching to a new resonant circuit at each segment transition.

To simplify analysis, all four resonant circuits can be reduced to the equivalent circuit of Fig. 16(e) with an aggregate offset voltage V_p and an effective capacitance C_{eff} using the parameters listed in Table IX. This reduced resonant circuit serves as a tool for standardizing stage behaviors when solving for periodic steady state.

B. Ideal Periodic Steady State Solution

The periodic steady state solution (PSSS) of the PT's state trajectories quantifies exactly how a switching sequence must operate to realize its intended efficiency advantages. An ideal PSSS (assuming $R = 0$) can be obtained analytically with light computation and provides a close estimate of the exact PSSS to the extent that $R \to 0$.

To solve for an ideal PSSS, we apply Conservation of Energy (CoE) and Conservation of Charge (CoC) equations to the PT's state variables during each segment, assuming the final states equal the first states and that ZVS occurs at each stage transition. These equations rely on only the states at each

stage transition point and can be crafted segment-by-segment in the order determined in Appendix B. Using the reduced resonant circuit of Fig. 16(e), every segment has the following CoE constraint:

$$C_{eff}(v_{C_{eff}1} - V_p)^2 + Li_{L1}^2 = C_{eff}(v_{C_{eff}2} - V_p)^2 + Li_{L2}^2 \quad (21)$$

in which states marked with "1" correspond to the beginning of the segment and states marked with "2" correspond to the end of the segment.

Segments with open stages have additional CoC constraint(s) depending on which additional capacitances (C_{pA} and/or C_{pB}) participate in resonance. For open stages at the input, the following CoC equation applies:

$$C(v_{c2} - v_{c1}) = -C_{pA}(v_{pA2} - v_{pA1}) \quad (22)$$

Open stages at the output likewise require:

$$C(v_{c2} - v_{c1}) = NC_{pB}(v_{pB2} - v_{pB1}) \quad (23)$$

Thus, each segment adds $1+n$ equations to the system, where n equals the number of port capacitances resonating.

From here, the i_L polarity constraints listed in Tables II and VIII can be added by setting i_L equal to zero at the appropriate segment transition points; this constrains two i_L transition states for each port. For a 4x6- or 6x4-stage sequence, this leaves one remaining degree of freedom (assuming V_{in} and V_{out} have already been defined) that dictates the power delivered to the load. Using these constraints, one can solve this system of equations for the ideal PSSS of all transition point states. For a given PT, sequence combination, and operating point, this solution describes the single set of state trajectories that provides all of the advantageous behaviors discussed herein, amounting to maximum efficiency.

C. Ideal Switching Times

The time duration of each segment across a switching cycle can be extracted from the PT's ideal transition point states in the PSSS. One approach for this involves multiplying a segment's resonant period times the proportion of this resonant period that it completes. This requires calculating the "angle" between the segment's start and end points, both referenced from the circuit's center of resonance. In the reduced resonant circuit of Fig. 16(e), L and C_{eff} resonate around a center point of $i_L = 0$ and $v_{C_{eff}} = V_p$. We define an impedance-normalized vector U_x for each transition x to be:

$$U_x = \left(v_{C_{eff}x} - V_p,\ \ i_{Lx}\sqrt{\frac{L}{C_{eff}}},\ \ 0 \right) \quad (24)$$

in which V_p and C_{eff} are specific to the segment of interest, even for the same transition point. The angle between two neighboring transition point vectors can be calculated using the four-quadrant inverse tangent function. Its proportion of the period (out of 2π) can then be multiplied by the segment's resonant period to calculate the segment's time duration:

$$t_{1-2} = \sqrt{LC_{eff}}\,\mathrm{atan2}\left(\frac{||U_1 \times U_2||}{U_1 \cdot U_2} \right) \quad (25)$$

We should note that frequency is *not* an independent control variable; it is collectively determined by these switching times.

D. Exact Periodic Steady State Solution

Calculating an exact PSSS considering loss due to R requires time-domain integration of i_L^2, which is not easily implemented using only the PT states at each stage transition. If needed, an exact PSSS can be obtained by symbolically solving the PT's system of time-domain differential equations that govern its states during each segment. This produces a system of complex exponentials, which can then be solved numerically for the exact PSSS using the ideal PSSS as an initial guess to aid convergence.

Similar to the ideal PSSS, the system of exact differential equations can be assembled segment-by-segment as in Appendix B. This system has the same transition point state variables as the ideal system, plus the segments' time durations as variables. After applying all equations and constraints for a 4x6- or 6x4-stage sequence combination, one degree of freedom remains for modulating power. The exact PSSS is useful for calculating switching times for loss-inclusive simulations.

Appendix D
Closed-Loop Control

Although this work focuses on converter topologies and steady-state switching sequences, these implementations realistically require closed-loop control for regulating V_{out} and maintaining the switching sequences' high-efficiency behaviors. As discussed in Appendix C, such high-efficiency behaviors require precise timing of each stage, leaving one degree of freedom for regulating V_{out} in 4x6- and 6x4-stage sequences. Implementing closed-loop control for this timing is challenging in that it requires the modulation of frequency, duty cycle, dead time, and phase shift between ports.

To discuss the intricacies of this system, we assume all switches are equipped with sensed turn-on schemes when ZVS occurs. This leaves only the "on" durations for each switch as control variables. First, the degree of freedom for voltage regulation lies in the 6-stage sequence, specifically the transition between the two connected/zero stages of same i_L polarity. These stages are confined to sharing the same half-cycle, and adjusting their distribution within the half-cycle alters the unfixed K and therefore the energy balance within the PT. Thus, the switch on-time governing the end of the first connected/zero stage (and therefore the transition to the second connected/zero stage) may be used as the primary control handle for regulating V_{out}. This is described with more detail in [35], in which we refer to the half-bridge responsible for this transition as the "regulating" half-bridge.

All other switch on-times may be controlled for ZVS and all-positive instantaneous power transfer (i.e., ensuring no reverse conduction) using well-understood methods for resonant converters. This includes both 4-stage sequences (if implemented with active switches) and the single-stage half-cycle of a 6-stage sequence. As such, these control loops maintain the switching sequence's high-efficiency behaviors. Because the PSSS of a switching sequence is fully constrained by these behaviors (except for the degree of freedom used for regulation), maximum efficiency is achieved as long as the

switching sequence itself is maintained. It should be noted that frequency is not an independent control variable; the switching period is collectively determined by the 6-stage sequence's switch on-times and adaptive resonant transitions for ZVS. A method for estimating this frequency can be found in [36].

A detailed control implementation for these switching sequences is beyond the scope of this work but has been explored for six-stage-sequence PR-based converters in [35], [37].

APPENDIX E
PT MODEL VALIDITY

In this work, we assume the PT's model parameters to be constant. Realistically, however, these model parameters are expected to vary with temperature, age, and other environmental factors. It is likewise anticipated that large-signal PT model parameters may deviate from their small-signal characterized values, which is not yet well-understood in the literature. While previous PT-based converter implementations have required precise resonant frequency tracking, the proposed switching sequences in this work operate in the PT's inductive region and are therefore less sensitive to resonant frequency variation. However, the dependence of the PT's model parameters on environmental factors still necessitates use of closed-loop control to maintain the switching sequence's high-efficiency behaviors as discussed in Appendix D.

REFERENCES

[1] J. D. Boles, E. Ng, J. H. Lang, and D. J. Perreault, "High-efficiency operating modes for isolated piezoelectric-transformer-based dc-dc converters," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics*, Aalborg, Denmark, Nov. 2020, pp. 1–8.

[2] E. Ng, J. D. Boles, J. H. Lang, and D. J. Perreault, "Non-isolated dc-dc converter implementations based on piezoelectric transformers," in *Proc. IEEE Energy Conversion Congress and Exposition*, Vancouver, Canada, Oct. 2021, pp. 1–8.

[3] C. R. Sullivan, B. A. Reese, A. L. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *Proc. IEEE Intl. Symposium on 3D Power Electronics Integration and Manufacturing*, Raleigh, NC, USA, Jun. 2016, pp. 1–23.

[4] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, USA, Feb. 2009, pp. 1–14.

[5] P. A. Kyaw, A. L. Stein, and C. R. Sullivan, "Fundamental examination of multiple potential passive component technologies for future power electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 708–10 722, 2018.

[6] A. M. Flynn and S. R. Sanders, "Fundamental limits on energy transfer and circuit considerations for piezoelectric transformers," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 8–14, 2002.

[7] J. D. Boles, J. E. Bonavia, P. L. Acosta, Y. K. Ramadass, J. H. Lang, and D. J. Perreault, "Evaluating piezoelectric materials and vibration modes for power conversion," *IEEE Transactions on Power Electronics*, 2022.

[8] A. Vazquez Carazo, "Piezoelectric transformers: An historical review," in *Actuators*, vol. 5, no. 2. MDPI, 2016.

[9] J. D. Boles, J. J. Piel, and D. J. Perreault, "Enumeration and analysis of dc-dc converter implementations based on piezoelectric resonators," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 129–145, 2021.

[10] S. Moon and J.-H. Park, "High power dc–dc conversion applications of disk-type radial mode Pb (Zr, Ti) O3 ceramic transducer," *Japanese Journal of Applied Physics*, vol. 50, no. 9S2, p. 09ND20, 2011.

[11] B. Pollet, G. Despesse, and F. Costa, "A new non-isolated low power inductorless piezoelectric dc-dc converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 002–11 013, 2019.

[12] W. D. Braun, E. A. Stolt, L. Gu, J. Segovia-Fernandez, S. Chakraborty, R. Lu, and J. M. Rivas-Davila, "Optimized resonators for piezoelectric power conversion," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 212–224, 2021.

[13] M. Touhami, G. Despesse, and F. Costa, "A new topology of dc-dc converter based on piezoelectric resonator," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics*. IEEE, 2020, pp. 1–7.

[14] S. Bronstein and S. Ben-Yaakov, "Design considerations for achieving ZVS in a half bridge inverter that drives a piezoelectric transformer with no series inductor," in *Proc. IEEE Power Electronics Specialists Conference*, vol. 2, Cairns, Australia, Jun. 2002, pp. 585–590.

[15] M. Rodgaard, T. Andersen, and M. A. Andersen, "Empiric analysis of zero voltage switching in piezoelectric transformer based resonant converters," in *Proc. IET International Conference on Power Electronics, Machines and Drives*, Bristol, UK, Mar. 2012, pp. 1–6.

[16] E. L. Horsley, A. V. Carazo, N. Nguyen-Quang, M. P. Foster, and D. A. Stone, "Analysis of inductorless zero-voltage-switching piezoelectric transformer-based converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2471–2483, 2012.

[17] M. P. Foster, J. N. Davidson, E. L. Horsley, and D. A. Stone, "Critical design criterion for achieving zero voltage switching in inductorless half-bridge-driven piezoelectric-transformer-based power supplies," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5057–5066, 2015.

[18] R. L. Lin, F. C. Lee, E. M. Baker, and D. Y. Chen, "Inductor-less piezoelectric transformer electronic ballast for linear fluorescent lamp," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, Mar. 2001, pp. 664–669.

[19] J. M. Alonso, C. Ordiz, and M. A. Dalla Costa, "A novel control method for piezoelectric-transformer based power supplies assuring zero-voltage-switching operation," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1085–1089, 2008.

[20] S.-Y. Chen and C.-L. Chen, "ZVS considerations for a phase-lock control dc/dc converter with piezoelectric transformer," in *Proc. Annual Conference of the IEEE Industrial Electronics Society*, Paris, France, Nov. 2006, pp. 2244–2248.

[21] M. Ekhtiari, Z. Zhang, and M. A. Andersen, "Analysis of bidirectional piezoelectric-based converters for zero-voltage switching operation," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 866–877, 2017.

[22] M. Ekhtiari, T. Andersen, M. A. Andersen, and Z. Zhang, "Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 783–793, 2017.

[23] M. S. Rødgaard, "Bi-directional piezoelectric transformer based converter for high-voltage capacitive applications," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Charlotte, NC, USA, Mar. 2015, pp. 1993–1998.

[24] M. S. Rødgaard, M. Weirich, and M. A. Andersen, "Forward conduction mode controlled piezoelectric transformer-based PFC LED drive," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4841–4849, 2012.

[25] M. Sanz, P. Alou, A. Soto, R. Prieto, J. Cobos, and J. Uceda, "Magnetic-less converter based on piezoelectric transformers for step-down dc/dc and low power application," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, Miami Beach, FL, USA, Feb. 2003, pp. 615–621.

[26] D. Vasic, Y.-P. Liu, F. Costa, and D. Schwander, "Piezoelectric transformer-based dc/dc converter with improved burst-mode control," in *2013 IEEE Energy Conversion Congress and Exposition*. IEEE, 2013, pp. 140–146.

[27] B. Ju, W. Shao, L. Zhang, H. Wang, and Z. Feng, "Piezoelectric ceramic acting as inductor for capacitive compensation in piezoelectric transformer," *IET Power Electronics*, vol. 8, no. 10, pp. 2009–2015, 2015.

[28] M. Ekhtiari, Z. Zhang, and M. A. Andersen, "State-of-the-art piezoelectric transformer-based switch mode power supplies," in *40th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2014, pp. 5072–5078.

[29] Z. Yang, J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, "Resonant current estimation and phase-locked loop feedback design for piezoelectric transformer-based power supplies," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 466–10 476, 2020.

[30] W. P. Mason, *Electromechanical Transducers and Wave Filters*. D. Van Nostrand Co., 1948.

[31] J. Forrester, J. N. Davidson, M. P. Foster, and D. A. Stone, "Influence of spurious modes on the efficiency of piezoelectric transformers: A

sensitivity analysis," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 617–629, 2020.

[32] L. Wang and R. P. Burgos, "Comprehensive analysis of models and operational characteristics of piezoelectric transformers," in *Proc. IEEE Applied Power Electronics Conference and Exposition*, New Orleans, LA, USA, Mar. 2020, pp. 1422–1429.

[33] "Equivalent circuit parameters for piezo transformers". Steiner & Martins, Inc. [Online]. Available: http://www.steminc.com/piezo/EquivCircuitPT.asp

[34] K. Uchino and S. Hirose, "Loss mechanisms in piezoelectrics: how to measure different losses separately," *IEEE Transactions on Ultrasonics, ferroelectrics, and frequency control*, vol. 48, no. 1, pp. 307–321, 2001.

[35] J. J. Piel, J. D. Boles, and D. J. Perreault, "Feedback control for a piezoelectric-resonator-based DC-DC power converter," in *IEEE Workshop on Control and Modeling for Power Electronics*, Cartagena de Indias, Columbia, Nov. 2021, pp. 1–8.

[36] L. de Araujo Pereira, A. Morel, M. Touhami, T. Lamorelle, G. Despesse, and G. Pillonnet, "Operating frequency prediction of piezoelectric dc-dc converters," *IEEE Transactions on Power Electronics*, Early Access.

[37] M. Touhami, G. Despesse, F. Costa, and B. Pollet, "Implementation of control strategy for step-down DC-DC converter based on piezoelectric resonator," in *2020 22nd European Conference on Power Electronics and Applications*, Lyon, France, Sep. 2020, pp. 1–9.