Single-Phase Universal-Input PFC Converter Operating at High Frequency

Juan A. Santiago-González, David M. Otten (co-equal first authors), Seungbum Lim, Khurram K. Afridi and David J. Perreault, *Fellow, IEEE*

Dept. of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA, USA
otten@mit.edu and djperrea@mit.edu

Abstract- **Single-phase ac to dc converters for computers and related applications have requirements that are difficult to meet while achieving both high power density and high efficiency: wide input voltage range, large voltage step down, galvanic isolation, harmonic current limits and hold-up requirements. This work explores a circuit architecture and topology that is structured to facilitate operation at multi-MHz frequencies in order to address this challenge. We present a 250 W, 24 V output, universal input PFC converter prototype that leverages the proposed approach to achieve a power density of 34.9 W/in^3 while meeting the 80 PLUS Platinum efficiency standard, EN61000-3-2 line harmonic requirements and half-cycle holdup. The converter operates at variable switching frequencies in the range of 1-4 MHz; the measured efficiency at 230 Vac RMS, 60 Hz input is 95.33% at full load and 84.57% at 8% load.**

Keywords—**Power Factor Correction, single phase PFC, universal input, high frequency**

I. INTRODUCTION

While the transmission and distribution of electric power over the grid is done using ac waveforms, many of today's loads are electronic devices that require dc voltages, such as laptops, personal computers, mobile phones, and LED lights. Ac to dc converters are used to transform power from the grid to power useful for an electronic load. These converters, present in nearly all modern grid-connected electronic devices, tend to be a bottleneck in the miniaturization of electronics. Owing to the desire for miniaturization and the large amount of energy processed through such converters, decreasing their volume while maintaining or improving performance is a problem of present practical importance.

An important approach towards miniaturizing power converters is increasing the switching frequency of the converter [1]. Despite the benefits of higher switching frequencies, there are a number of challenges that inhibit their use, such as excessive frequency-dependent losses and increased complexity of sensing and control [1]. In addition, there are many other factors that limit miniaturization of grid-interface power converters for single-phase systems. A chief one is the need for twice-line-frequency energy buffering and holdup in the face of power interruptions. The energy storage needed to ride through line voltage crossings, meet line harmonic requirements and provide holdup during line dropout

is a function of output power and the line frequency, and does not depend on switching frequency [2-10]. The wide operating range (in input voltage and power) required of ac-dc converters operating under "universal input voltage" requirements (e.g., 85 Vac-264 Vac) likewise makes it difficult to miniaturize converters for this application, as does the need to meet ac line current waveform requirements (e.g. EN-61000-3-2 [11]) for high power quality, meet industry standards on efficiency (e.g. 80 PLUS [12]), provide good thermal management for inevitable losses, provide galvanic isolation [13,14], and meet strict EMI constraints [15,16]. Simultaneously meeting all these requirements while achieving high power density is a challenge [7,17,18].

Achieving miniaturization demands designs that can address these challenges while mitigating high-frequency losses and which can best utilize available semiconductor devices, passive components and controls. This paper explores a new architecture and design approach to increase the performance of universal-input grid interface ac/dc converters. Specifically, it focuses on design techniques for high power factor, high efficiency and high energy density single-phase isolated ac/dc power converters in the range of hundreds of watts, such as suitable for computer power supplies and similar applications.

Section II presents background on ac/dc converters. Section III gives an architectural overview of the design and details the design of each subsystem. Section IV shows experimental results. Section V compares this converter to other designs. Finally, Section VI concludes the paper.

II. TYPICAL AC/DC CONVERTERS

Ac/dc converters broadly address two challenges: (1) drawing energy from the ac line with acceptable waveform quality while providing sufficient energy buffering to handle line zero crossings and holdup requirements, and (2) providing isolation, voltage transformation, and regulation of the dc output. There are two main types of circuit architectures used to solve this problem: single-stage designs, e.g. [19-21], which accomplish both functions with one power stage, and two-stage designs [22-25] which split these functions up among multiple stages. (There are also design variants that are somewhere in between single stage and two full cascaded stages, such that one of the stages does not process all the power (e.g., [22]), but for

purposes here we treat such designs as two stage designs.) Single-stage converters typically have fewer components and the design and control schemes are simpler [17,18]. Power is only processed once, but the energy processing limits of single-stage designs tend to hurt their achievable performance (e.g., in terms of waveform quality, volume, etc.). On the other hand, the two-stage approach provides more flexibility and control handles that enables system-wide tradeoffs which can result in high-performance converters. In this type of converter, power is processed twice, so it is imperative that the tradeoffs are well understood and the components and topology carefully selected so that the circuit offers an overall increase in performance. Broadly speaking, single-stage designs are most often found in low-power systems where component count tends to drive cost and performance requirements are somewhat relaxed, while two (or more) stage designs are dominant in high-power and high-performance systems.

In this paper a two-stage power factor correction (PFC) circuit architecture is explored that is suitable for high-frequency (multi-MHz) operation while providing high efficiency and power density. Fig. 1 shows a simplified view of the general architecture of the converter. The front end is the PFC stage that manages drawing energy from the line with high waveform quality and providing energy buffering for twice-line-frequency ripple and holdup. The 2nd stage is an isolation and regulation stage that provides voltage step down, galvanic isolation, and regulated control of the output. The energy buffering capacitors are placed between the two stages.

A. PFC Stage

The PFC stage is the "front end" of the ac/dc converter, providing the interface to the ac grid. Its main purpose is to extract current from the line at high power factor, making the ac/dc converter look close to a resistive load. While near unity power factor is often desirable, international standards for computer power supplies such as EN61000-3-2 [11] and 80 PLUS [12] allow for some harmonic content. The "relaxed" constraint enables the use of distorted (non-sinusoidal) current drawn from the line, which in turns gives the designer a variety of options in topology and control scheme selection. [17,18, 22,26]. In particular, the ability to draw some degree of harmonic currents allows reduction in the required energy storage for twice line frequency buffering [4-6, 27-31], permits a broader range of topologies to be used (e.g., ones that may not be able to draw current over the full line cycle), and provides greater flexibility in control.

In typical commercial ac/dc converters the PFC stage consists of a line-frequency rectifier followed by a boost-type converter [17,18,31] or a "bridgeless" design in which the boost converter is integrated with the rectifier [7,19]. The boost converter has several useful characteristics in this context: it has one magnetic component, it has a common-referenced switch, and, most importantly, it can operate to draw current from the line over the full line cycle. In short, it is a very popular topology because of its low component count, simple control scheme and high power factor. One drawback of the boost-type PFC is the high output voltage, which must be higher than the peak input voltage (i.e. higher than 373 V in an universal
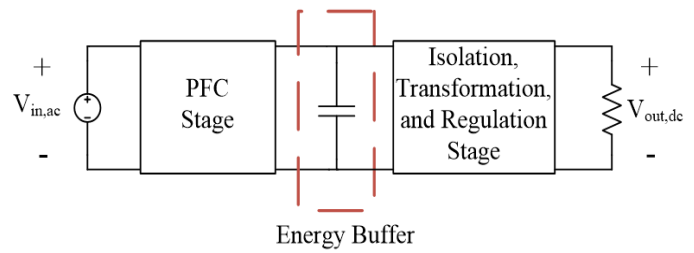

Fig. 1 Typical architecture for a two-stage, single-phase ac/dc converter.

input design), far higher than the ultimate output voltage of the system. As the boost converter cannot achieve zero-voltage switching over much of its operating range, it is somewhat limited in achievable switching frequency and miniaturization, especially given its high-voltage operation and wide operating range. Moreover, operating at this high output voltage also increases the step-down ratio of the second stage, which hurts the achievable size and efficiency of the second stage. On the other hand, buck-type PFC converters [17,18,23] offer the opposite trade-offs: lower device stress and lower second stage step-down ratio but also lower achievable line waveform quality and power factor, as such a PFC stage can only operate over the parts of the line cycle where the instantaneous line voltage is higher than the output voltage of the PFC stage. Other types of converters (e.g., flyback or buck-boost stages) can split this difference, providing intermediate characteristics [22,31], though some such designs can impose quite high stresses [24,32].

B. Energy Buffering Capacitors

Energy buffering for twice-line frequency power pulsations and holdup is usually accomplished with electrolytic capacitors, owing to favorable tradeoffs in size, cost and efficiency. Nevertheless, such capacitors can take up to 30 to 40 % of a high-power-density ac/dc converter's total volume. Their size is determined by three constraints: the energy that needs to be stored and delivered every half line cycle while meeting line harmonic requirements, the energy needed for hold-up time requirements (i.e. to provide energy to the output during a specified-duration dropout of the ac input voltage) and the temperature rise due to the current flowing through it. In single-phase ac/dc converters the input power drawn from the line is necessarily pulsating while constant power is delivered to the load. The amount of energy needed, the allowed ripple on the capacitor voltage and the average capacitor voltage all affect the sizing of the capacitors.

The capacitor energy requirement can be summarized as follows: for a given converter design the capacitor energy requirement will be dominated by either line energy buffering or hold-up time.

C. Isolation and Regulation Stage

The second stage in Fig. 1 takes the energy from the first stage (including the energy buffer) and delivers it to the output. Typically this is done with a step-down isolated dc/dc converter. The converter provides regulation of the output voltage and incorporates a transformer that provides isolation
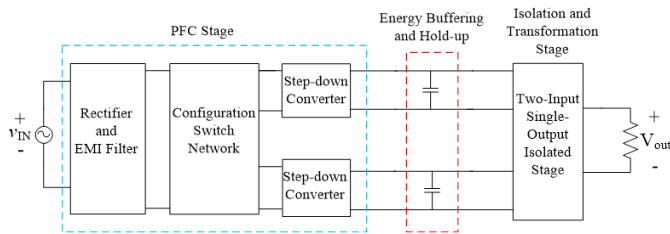
Fig. 2 Proposed single phase ac/dc converter architecture. The converter consists of a rectifier bridge, a configuration switch network, two step-down converters, energy buffering capacitors and a two-input, single-output isolation and transformation stage.
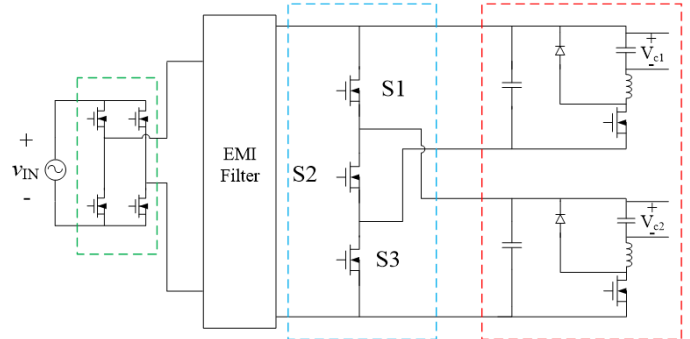

Fig. 3 Details of the PFC stage: active line rectifier (green), configuration switch network (blue) and step-down converters (red). If the input voltage is high, S2 turns on and the inputs to the step-down converters connect in series. If the input voltage is low, S1 and S3 turn on and the inputs to the step-down converters are connected in parallel. The output of each step-down converters is connected to an energy buffering capacitor.

[13,14]. (Capacitive isolation is possible [33,34], but not generally favorable for volume or efficiency, and the transformer also helps to provide necessary voltage transformation.) The converter should also be able to handle a range of input voltages corresponding to that provided from the PFC stage during a hold-up time transient event.

III. SYSTEM ARCHITECTURE

In this section we present an overview of the proposed system architecture illustrated in Fig. 2, and describe how it addresses some of the constraints and tradeoffs in the previous section. We focus on its individual elements: (1) The dual element PFC stage and its reconfiguration to address the wide input line voltage range; (2) the energy buffer capacitor bank which provides energy storage for twice-line-frequency energy buffering and output holdup; and (3) the two-input, single-output isolation and regulation stage. The following sections then provide design details about these individual stages.

A. Proposed PFC Stage

As described previously and shown in Fig. 2, the PFC stage consists of 2 step-down converters and a configuration switch network; the detailed structure including the active rectifier, configuration network and buck converters is shown in Fig. 3. The configuration network connects the step-down converters in series if the ac input voltage is high (i.e. 170 to 264 Vac RMS) and in parallel if it is low (i.e. 85 to 130 Vac RMS). This reconfigurability reduces both the maximum input voltage and required input voltage range of the two buck converters over the universal ac input range. As will be seen, this enables us to design a very high-frequency miniaturized converter block for the PFC function (1-4 MHz switching frequency range) that is nonetheless extremely efficient (~98%). Moreover, the nominal output voltage of each of the two converters was chosen to be 72 V (average), which allows the buck-type converter to operate over a sufficient part of the line cycle to meet EN61000-3-2 line harmonic requirements. This use of a buck PFC with reconfiguration also reduces the voltage conversion requirement of the subsequent stage (thereby improving its achievable size and efficiency).

1. Step-down Converter Operation

The step-down converters are resonant-transition inverted buck converters, or "RTI" buck converters, as illustrated in Fig.
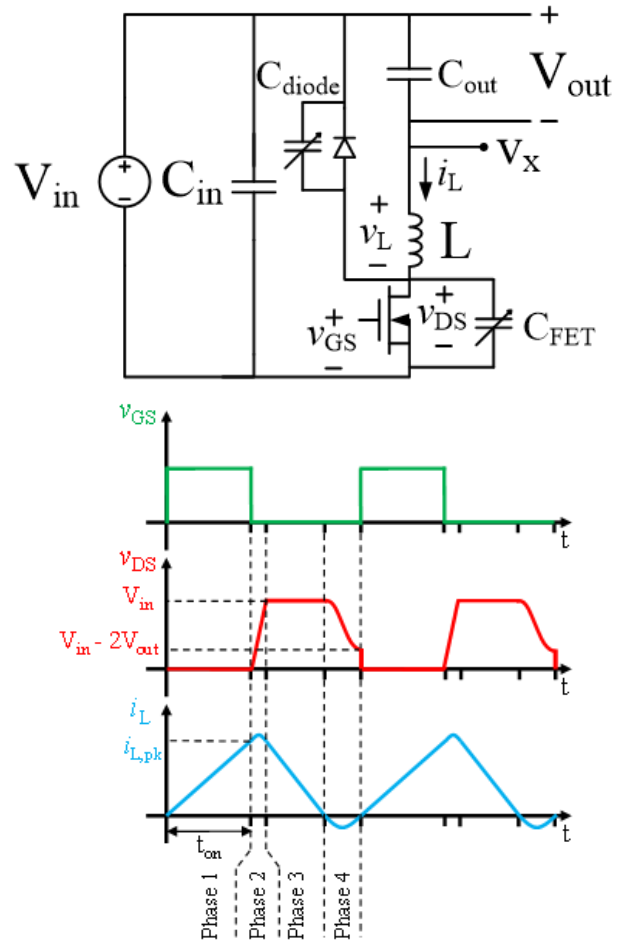

Fig. 4 Resonant transition inverted buck converter and its ideal waveforms. This topology is excellent for miniaturization as it operates in high-ripple mode which enables the use of a small inductor. Also, ZVS or near ZVS is maintained over a roughly ~3:1 step down ratio which minimizes losses as switching frequency increases and the power switch is ground referenced which facilitates operation at high frequency.

4 [22,35]. This converter has several features that make it suitable for realizing high density and high efficiency: it operates in discontinuous conduction mode (allowing for small

inductor value and size) and maintains zero voltage switching (ZVS) up to a 2:1 step down voltage ratio, with low-loss "near ZVS" operation at up to a 3:1 step-down conversion ratio. Additionally, the single active switch in the inverted buck topology is ground referenced, which simplifies driving it at HF, and by virtue of it being a step-down converter the switch voltage stress is smaller than the more traditional boost type converter. This enables the use of highly efficient and small footprint GaN FETs. Moreover, input current can be (indirectly) controlled through transistor on time, without the need for current sensing [22,35,36].

The first-stage PFC converters use transistor on-time control as a proxy for current control. A result of this is that the switching frequency varies with operating point. The prototype developed here operates between 1 and 4 MHz, an order of magnitude higher than typical PFC stages, with substantial benefits for required passive component volume and EMI filter size [22,37].

2. Component Selection of RTI Buck

The RTI buck converter is the building block of the PFC stage. During PFC operation each buck converter will process a peak power of about 300 W with an average of about 125 W with performance across the range of 30 to 300 W being of highest interest. Appendix A contains details of the component selection process. Table 1 summarizes the resulting power stage design of the RTI buck converter.

3. Input Current Shaping

During development, it was noted that the RTI buck converter operates with higher efficiency at lower input voltages. If the input current follows the line voltage, the PFC converter will draw high current at the peak of line voltage, which means it draws the highest amount of power when it is the least efficient. However by changing the current reference the converter can draw higher power when the line voltage is smaller, thus reducing the amount of power processed at peak voltage (which in turn increases converter average efficiency over a line cycle). This input current shaping adds distortion to the line current and is limited by EN61000-3-2 regulations. As will be discussed in the experimental results section, there is room to improve efficiency by shaping of the input current waveform over the line cycle while remaining within the EN61000-3-2 limits. This type of nonsinusoidal current shaping strategy has been utilized to advantage in previous grid-interface converters for both efficiency and waveform considerations [22] as well as for capacitor size reduction [4-6,22].

4. Active Rectifier Bridge and Configuration Switch

As shown in Fig. 3 (green outline), an active line-frequency rectifier bridge is used at the input of the supply to increase efficiency. STB32NM50N FETs with a typical on-resistance of 0.1 ohms are used to provide low conduction losses and withstand peak input voltages of 500 volts. The gates are driven by Vishay VOM1271 photovoltaic MOSFET drivers with integrated fast turn-off. They are able to turn off the rectifier

TABLE I
FINALIZED PART LIST FOR RTI BUCK CONVERTER

Part	Name
Transistor MOSFET	3x EPC2025
Diode	MBRB40250TG
Inductor	E-22-3F45, L=5µH 5 turns of 46/450 litz wire, 7.5 mils airgap in each core leg, 62 mil spacer between airgap and winding
Input Capacitors	3x 1µF, 250V 1825 package 2x 0.1µF, 250 V 0805 package
Output Capacitors	6x 1µF, 250V 1812 package 1x 0.1uF, 250V 0805 package

FETs in under 20 µs though it takes 1 - 2 ms to turn them on. Because the rectifiers operate at line frequency, this is not a problem. The input voltage is continuously monitored by the processor and compared with the buck converter output voltage. If the input is more than 15 volts higher than the output voltage, the appropriate FETs are turned on. If the voltage difference is less than 8 volts, they are turned off. (These boundary values of operation were chosen experimentally. They provide enough margin and stability for the control loops. The buck converter cannot operate when the input voltage is below the output.) When the supply is first powered up and no gate drive signals are supplied, the body diodes of the FETs perform as a conventional full bridge rectifier.

The configuration switch network shown in Fig. 3 (blue outline) is used to connect the two buck converters in series or parallel. Infineon BSC600N25NS3 FETs with an on-resistance of 60 mohms and a Vds of 250 volts are used for this function. S1 and S2 are also driven by Vishay VOM1271 photovoltaic MOSFET drivers but S3 does not require an isolated drive. When no gate drive signals are present, the two buck converters are connected in series by the body diode of S2. This default condition at power up allows time for the control processor to measure the input line voltage and determine if series or parallel operation is required. The appropriate configuration switches are normally turned on when the supply is first started and not changed during operation.

B. Selecting Energy Buffering Capacitors

The energy buffering capacitors are chosen by selecting the minimum volume capacitance that meets the intersection of the following constraints: i) the twice-line-frequency energy buffering requirement, ii) the hold-up time energy requirement, and iii) the capacitor RMS current limit. Each of these constraints is explained in more detail as follows:

One limit on capacitor voltage ripple is the high-efficiency input voltage range of the second stage converter. We define the capacitor voltage ripple ratio R_C as:

$$R_C = \frac{V_{max}}{V_{nom}} - 1 \qquad (1)$$

where V_{nom} is the nominal voltage or average voltage that the energy is stored at and V_{max} is the maximum value of the voltage ripple (usually the rated 'working' voltage of the capacitor, or the maximum input voltage of the second stage). From here one can determine the minimum capacitance C_{ripple} needed to maintain the capacitor voltage ripple below an allowed amount, and relate it to the amount of energy needed to be buffered every half cycle:

$$C_{ripple} = \frac{E_{buff}}{2R_C V_{nom}^2} \qquad (2)$$

where E_{buff} is the twice line cycle energy buffered.

A second constraint on capacitor size is holdup. The converter needs to be able to deliver full dc power P_{dc} to the load during a transient event when the ac input power is cut-off for a duration $t_{hold-up}$. The amount of capacitance $C_{hold-up}$ needed to provide constant dc power to the load during time $t_{hold-up}$ is [38]:

$$C_{hold-up} = \frac{2P_{dc} t_{hold-up}}{(V_{nom}(1 - R_C))^2 - V_{min}^2} \qquad (3)$$

where V_{min} is the minimum allowed voltage of the second stage converter.

A final constraint on capacitor sizing is adequate RMS current capability, especially for electrolytic capacitors. It is typical practice from manufacturers to specify the capacitor's rated RMS current for various frequencies.

Now we apply these constraints to the design to size our energy buffering capacitors. The energy buffering capacitors are split equally between the two PFC stage outputs. Each of the two submodules process half the rated power (125 W each) and buffer half the energy at its output; the second stage combines power from the two PFC stages and energy buffer to supply the single output. The second stage converter used in this design has an input voltage range (for each input) of 35-75 V. Identifying all the values needed, this translates to V_{max} of 75 V, V_{nom} (or average) of 72 V and V_{min} (or minimum allowed during a hold-up event) of 35 V. The value of the ripple ratio R_C is 4.16%, and the twice-line-frequency energy that we need to buffer E_{buff} is 0.478 J per capacitor bank. The hold-up time $t_{hold-up}$ is 20 ms (full 50 Hz line cycle). This leads to a value of C_{ripple} of 1.106 mF and $C_{hold-up}$ of 1.357 mF. The value of capacitor RMS current rating, per capacitor bank, is 1.68 A at 100 Hz. Based on these constraints, the capacitor bank sizing is determined by holdup requirements. The energy buffering capacitor bank chosen as the best candidate comprises two of EKYB800ELL681MK40S capacitors (each rated for 80 V, capacitance of 0.68 mF and RMS current capacity of 1.47 A) in parallel at each PFC output.

C. Isolation Stage

The proposed design requires a second (isolation, transformation and regulation) stage having two inputs - one for each of the two PFC converter outputs. The proposed isolation stage converter is shown in Fig. 5. This converter operates similarly to a dual active bridge (DAB) [21,22,39], but enables
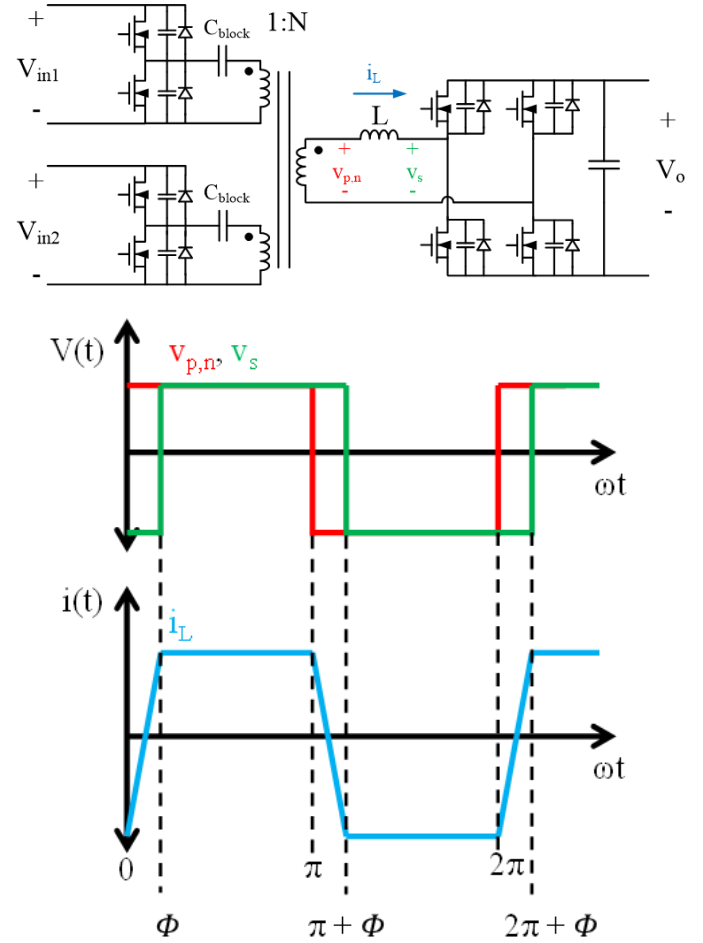

Fig. 5 Second (isolation) stage converter and ideal waveforms. This converter operates similar to a dual active bridge (DAB) converter. It also provides galvanic isolation, power combining and output regulation. The half bridge inverters on the primary side operate in phase with each other, while the rectifier full bridge at the secondary is phase shifted with respect to the inverters. The phase shift is used as a control handle for output regulation.

power to be drawn from (and transferred between) two inputs while providing a single output. The relative phase shift between the inverters and the rectifier is used to control the output power delivered under normal operating conditions at high power levels. The output power of the converter is described by the following equation:

$$P_O = \frac{N V_{in} V_O}{2\omega L} \Phi \left(1 - \frac{abs(\Phi)}{\pi} \right) \qquad (4)$$

where N is the 1:N turns ratio of the transformer, V_{in} and V_o are the input and output voltages, ω is the switching frequency in radians, L is the equivalent inductance referred to the secondary (including transformer leakage and any additional inductance) and Φ is the phase shift (in radians) between the inverters and the rectifier. The trapezoidal current shown in Fig. 5 provides the minimum RMS current for a given output power. If the voltage relationship $N V_{in} / 2 = V_O$ is not satisfied the current will not be flat topped and the RMS current will be higher. This converter is designed to be very efficient at a nominal input value of voltage and for small deviations around it (to account

TABLE II
FINALIZED PART LIST FOR THE ISOLATED CONVERTER

Part	Name
Inverter FET	EPC2016C
Rectifier FET	EPC2024
Transformer	E-22-DMR51, L_{leak}= 80 nH, L_{mag}=8.2 μH Primaries: 3 turns of 48/1000 litz wire each, Secondary: 2 turns of 48/1000 litz wire, Winding configuration: PSSP (2 secondaries connected in parallel) Each one is half core Fair-Rite 3061990871
Inductor (one per primary)	5 turns of 1000/48 litz wire L= 280 nH

for the twice line frequency ripple on the energy buffering capacitors). However, the converter can operate at reduced efficiency over a wide range of inputs for a transient event such as the hold-up time. For example, by decreasing frequency monotonically the output power can be regulated during a hold-up time event.

Another important characteristic of this converter is its zero-voltage switching (ZVS) capability. During the switch dead time part of the cycle, the incoming FET's voltage will ring down so that it turns on at a lower voltage. With sufficient switch current, the switch voltage will ring down all the way to zero. The minimum switch current needed for ZVS is given by [38]:

$$I_{SW,min} = \frac{2\sqrt{V_{in}V_O/N}}{Z_O} \tag{5}$$

where Z_O is the characteristic impedance of the transformer equivalent inductance and the switch capacitance. As a consequence, ZVS is lost at light loads. Dead time control [40] is used here to increase light-load efficiency of the second stage. The next sub-section details how this control technique is implemented.

A summary of the components used in the isolation stage is shown in Table 2. The design parameters were a nominal input voltage V_{in} of 72 V, output voltage V_O of 24 V, output power of 250 W and a switching frequency at nominal of 575 kHz. Appendix B details the selection criteria for these components.

D. Dead Time Control

In typical DAB converters, regulation is achieved by controlling the phase-shift between the primary and secondary bridges. One disadvantage of this approach is the increase in transistor switching loss at light loads [40,41]. Based on the authors' conference paper [39], we propose a control algorithm that increases light-load efficiency in DAB converters, and utilize it here to improve the system. The new control technique consists of using phase-shift as a control handle when operating above a certain output power, and then transitioning to switch dead time as a control handle when operating at lighter loads. With this new control algorithm, light load efficiency can be increased significantly [40].

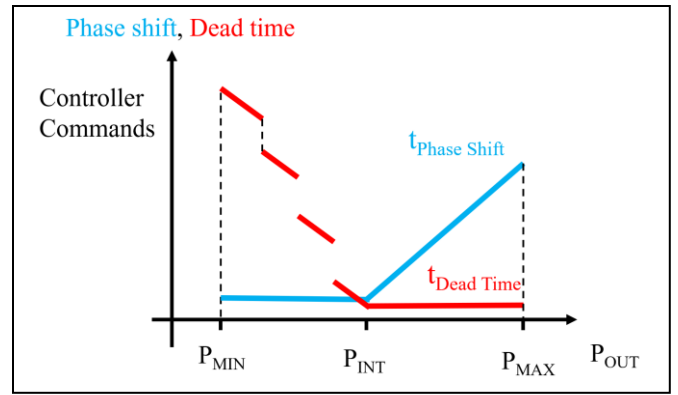Fig. 6 shows the controller commands as a function of output

Fig. 6 Isolation stage control algorithm. For operation between rated, maximum power (P_{MAX}) and an intermediate value (P_{INT}), dead time ($t_{Dead\ Time}$) is held constant and phase shift time ($t_{Phase\ Shift}$) is modulated as a control signal. Between P_{INT} and the minimum power (P_{MIN}), phase shift time is held constant and dead time is used as a control signal. The reasons for the discontinuity in the dead time command signal are discussed in detail in [40].
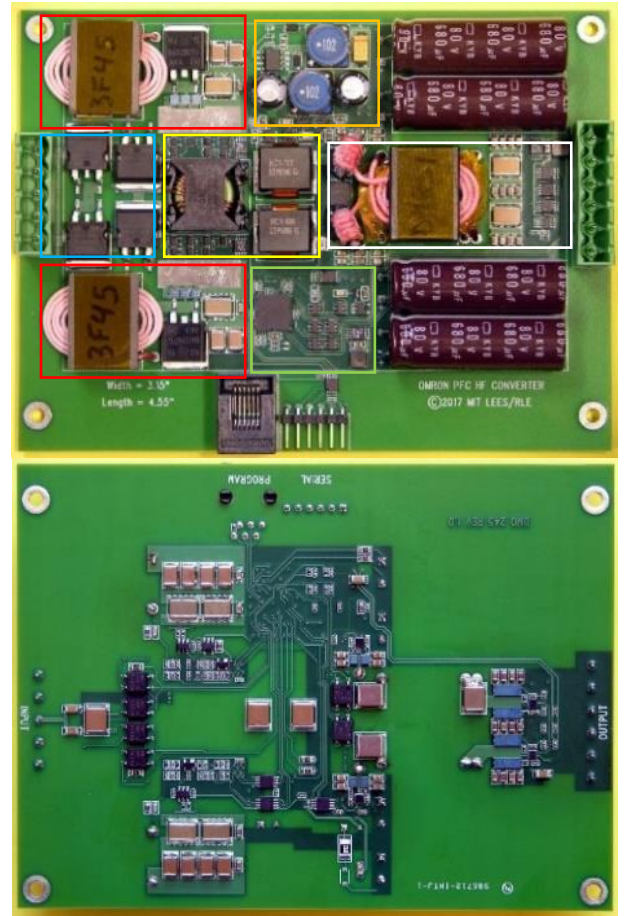

Fig. 7 Top and bottom sides of the full system PCB. While not routed, there is space provided for cutouts for the capacitors and magnetics which bring the total board height to 0.5 inches. The height is limited by the diameter of the electrolytic capacitors. Blue square: line rectifier, yellow: EMI filter, red: RTI-buck converters, white: isolation stage, green: control circuitry, and orange: auxiliary power supply.

power. Phase shift time, $t_{Phase\ Shift}$, is used to modulate output power between the rated or maximum output power and an intermediate value. During this range of operating points, dead

TABLE III
BOX VOLUME BREAKDOWN OF THE FULL SYSTEM

Item	Area (in^2)	Volume* (in^3)	Fraction (%)
EMI Filter	1.216	0.608	8%
Line Rectifier	1.215	0.608	8%
Mode Switch	0.278	0.139	2%
Buck Converters	3.58	1.79	25%
Energy Buffer	3.45	1.725	24%
Control	1.036	0.518	7%
Isolation Stage	2.706	1.353	19%
Control Supply	0.852	0.426	6%
Total	14.33	7.166	100%
Density	34.89	W/in^3	

*The total height is 0.5 inches.

Fig. 8 Line voltage (red), line current (yellow), output voltage (blue) and output current (purple) for the following operating point: 230 Vac input, 24 Vdc output voltage at an output power of 251 W. The power factor is 0.948 and efficiency 95.2%. The converter does not draw peak current when the voltage is maximum. THD$_i$=24%

time ($t_{Dead\ Time}$) is held constant. For power levels between the intermediate value and the minimum converter power, phase shift time is held constant and dead time is used to provide regulation. The discontinuities or "jumps" in dead time commands are due to non-linearities in the output power vs dead time transfer function. For details in the control algorithm and the output power vs dead time transfer function, the reader is referred to [40].

In the next section, experimental results on the full converter performance are shown.

IV. EXPERIMENTAL RESULTS

A photograph of the full converter is shown in Fig. 7. Various subsystem blocks can be seen, including the line rectifier, EMI filter (on the dc side of the rectifier), PFC converter, isolation stage, auxiliary power supply and control circuitry. This prototype converter provides a "box volume" power density of 34.9 W/in^3, which is achieved through the proposed
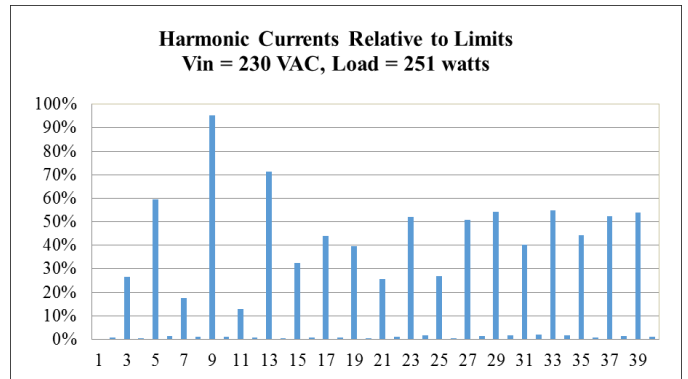

Fig. 9 Harmonic currents relative to the limits stated by EN61000-3-2 from the current waveform in Fig. 8. The 9th harmonic is the closest to its limit.
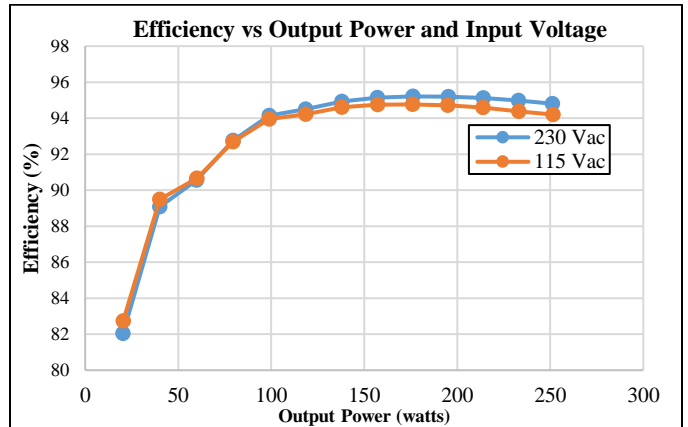

Fig. 10 System efficiency vs output power for high line (230 Vac) and low line (115 Vac) voltages.
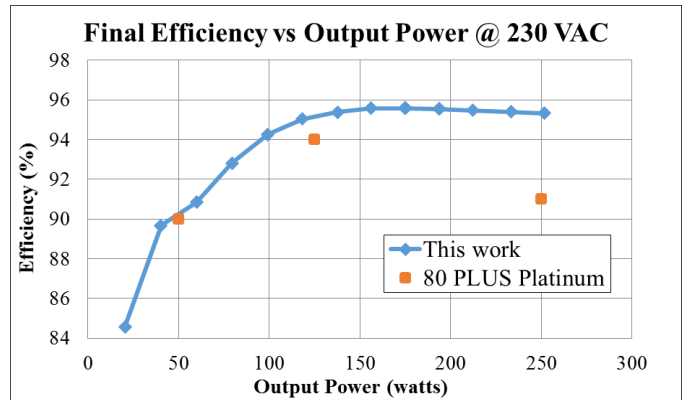

Fig. 11 Full system efficiency at 230 Vac RMS, 60 Hz input. Efficiency at full power and 230 Vac is 95.33%. The output voltage is 24 V. The orange points are the efficiency requirement for 80 PLUS Platinum. The proposed converter meets the 80 PLUS Platinum requirements.

architecture and multi-MHz operation. A breakdown of the volume is shown in Table 3. The RTI buck converter, the energy buffering capacitors and the isolation stage dominate the volume of the system.

Fig. 8 shows the system input and output waveforms for rated power at 230 Vac input, while Fig. 9 shows the line current harmonic current content normalized to EN-6100-3-2 limits. The total harmonic distortion (THD) of the ac current is 24%.
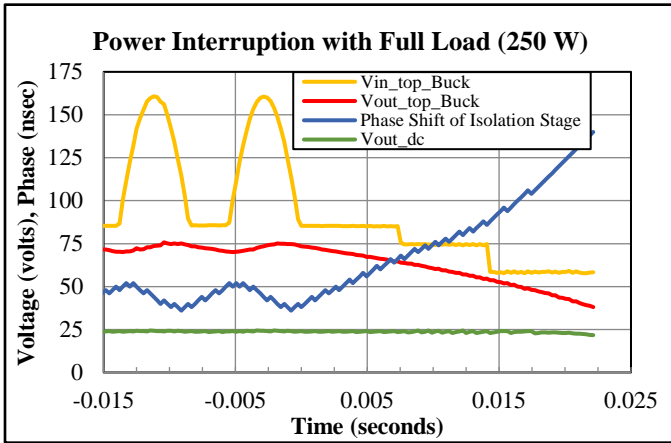
Fig. 12 Power interruption experimental waveforms. The waveforms are constructed from data sensed by the microcontroller. The bottom Buck waveforms are not shown since they are identical to the top. The isolation stage delivers full power to the load during the 20 ms hold-up time, a full 50 Hz line cycle. The phase shift of the isolation stage increases to compensate for the energy buffering capacitor voltage droop.
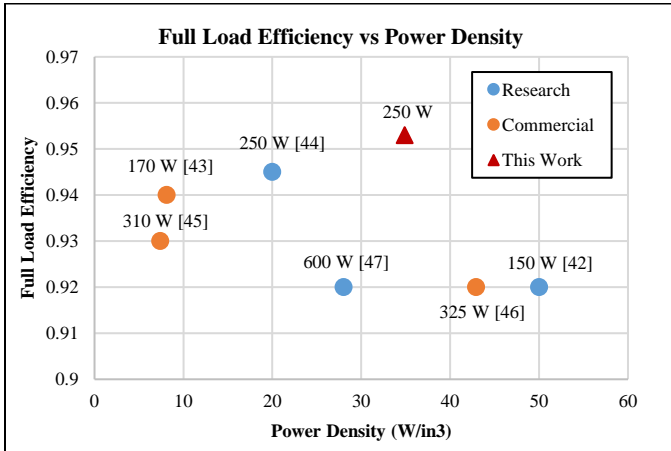

Fig. 13 Full load efficiency vs power density for different converters. All the converters featured here have universal input, energy buffering capacitors and roughly similar output voltage and power ratings under natural convection cooling conditions.

Figure 10 shows the full system efficiency for high line (230Vac) and low line (115 Vac) input voltages. Most of the extra loss at low line comes from the input bridge rectifier which processes twice the current of the 230 Vac case. Figure 11 shows the full system ac-to-dc efficiency data and compares it to the 80 PLUS Platinum [12] efficiency standard for computer power supplies. The efficiency at full power (250 W) and 230 Vac input is 95.33%. The peak efficiency is 95.58% at 175 W. This efficiency includes control circuitry losses.

Figure 12 shows waveforms of the converter during a power interruption. The isolation stage delivers full power during the hold-up time of 20 ms by discharging the energy buffering capacitors. As discussed in Section III-B, energy buffering capacitor size is determined by the hold-up time requirement. If this constraint is relaxed, even higher power density could be achieved as the energy buffer capacitor takes up 24% of

TABLE IV
DATA FROM VARIOUS CONVERTERS, INCLUDING BOTH
RESEARCH DESIGNS AND COMMERCIAL DESIGNS

	[42]	[43]	[44]	[45]	[46]	[47]	This work
Output Power (W)	150	170	250	310	325	600	250
Density (W/in^3)	50	8.1	20*	7.38	42.9	28	34.9
Efficiency	0.92	0.94	0.945	0.93	0.92	0.92	0.953
Output Voltage (V)	12	24	48	28	24	24	24
Universal Input	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Power Factor	0.96	0.96	0.99	0.99	0.99	0.97*	0.948

*Estimated

converter volume.

The converter has a total of 17 FETs, which increases costs and complexity. However, the trade-off is the high efficiency operation at steady state and the very similar performance between 230 Vac and 115 Vac. The control strategy of the converter is discussed in Appendix C.

V. COMPARISON TO OTHER CONVERTERS

Figure 13 shows a full load efficiency vs power density plot for various converters in the literature and available commercially [42-47]; full details of each plotted point are indicated in Table 4, along with the values achieved in this paper. The converters selected have similar specifications to the design discussed here for the purpose of performing a fair comparison. Specifically, they all operate over universal input voltage, have energy buffering capacitors and have roughly similar output voltage and power ratings under natural convection cooling conditions.

The comparison demonstrates the high performance enabled by the proposed approach. We consider full-load efficiency as an important metric because this is the condition that often determines achievable size reduction owing to thermal constraints. Of the commercial converters [43,45,46] shown, only the 170 W converter from Murata [43] is rated as 80 PLUS Titanium (the highest tier awarded by 80 PLUS, and one tier higher than the design demonstrated here). This plot suggests a clear trade-off between achievable size and efficiency in ac/dc converters. This is to be expected. For example, one can increase power density by shrinking magnetics size in a design, but such a reduction typically worsens loss (owing to increased core and conductor loss).

The proposed conversion approach yields an exceptionally high combination of size and efficiency (considering both full
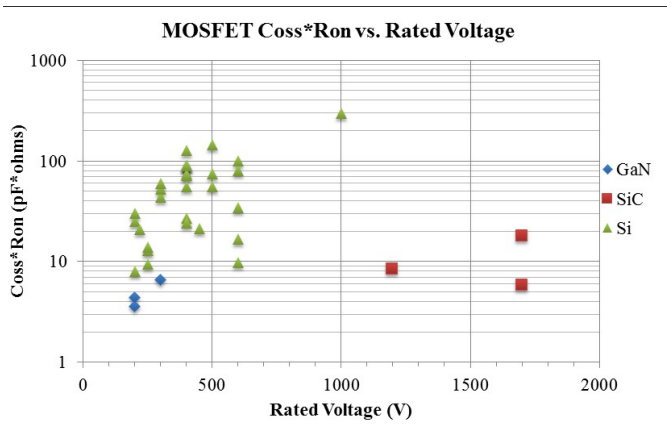
Fig. 14 Plot of MOSFET's soft switching figure of merit as a function of voltage. GaN transistors showed the best (minimum) figure of merit.

load and "80 PLUS" efficiency metrics). This high performance, which extends the Pareto front in the important metrics of efficiency and power density, is accomplished while meeting the numerous challenges in PFC conversion detailed in section I (wide input range, isolation, holdup, etc.). If we were to remove some of these constraints, such as universal input or hold-up time, the proposed approach would be able to achieve still higher power density at constant efficiency, or achieve higher efficiency at constant power density. It may be concluded that the proposed approach is effective for high-density PFC power supplies for computer applications.

VI. CONCLUSIONS

In this work a universal input single phase power supply is introduced that enables high power density and efficiency under high-frequency (1-4 MHz) operation. The architectural and topology decisions are presented, and a prototype converter is designed, built and tested. The design constraints and trade-offs are discussed. The proposed converter utilizes reconfiguration to reduce the operating range requirements of the first (PFC) stage, and facilitates achieving Multi-MHz operation and small size of the stage. It also reduces the conversion ratio requirements on the second stage. Active rectification and line current shaping are also used to achieve high efficiency and power density, as is careful selection of circuit topologies to realize the proposed architecture. Overall, a combination of high efficiency (>95% from universal input to 24 V dc output) and high power density (34.9 W/in^3) is achieved, while meeting key requirements of such grid-interfaced converters.

APPENDIX A

In this appendix the selection criteria for the RTI buck converter components is discussed in detail. The selection of the MOSFET was based on the soft-switching figure of merit $C_{OSS}*R_{ON}$ (output capacitance of the FET times on-resistance from Drain to Source) [48], which is plotted in Fig. 14 against rated voltage. The 300 V GaN FET EPC2025 was picked as the appropriate FET, and a prototype test board was prepared to

check if there is an advantage in paralleling these devices. Utilizing 3 FETs in parallel minimizes the loss over the complete operating range. Two FETs provided higher loss at high power while 4 FETs increased the low power loss significantly.

The diode was selected in a similar fashion. A handful of Si Schottky diodes were tested on the test board and the efficiency of the converter was measured. Ultimately the MBRB40250TG was selected for the final design.

The inductance value is designed to be as small as possible to minimize inductor size while being able to deliver power across a 10:1 power range, in continuous operation (i.e., without bursting). Taking into consideration minimum power (30 W), maximum input voltage (186 V), the inductance needed is approximately 5 µH. The inductor design considerations are core and winding losses, volume and temperature rise. The inductor was hand-wound using commercially available E shaped magnetic cores and litz wire. A Matlab script was written to sweep through various combinations of core materials, core geometries and winding configurations to find the best designs. The winding losses are calculated using Dowell's Equation (accounting for skin effect and proximity effect) [49] and the core losses are calculated based on fittings of datasheet core loss data and core loss data measured by Hanson, et al [36]. These designs were narrowed down to a handful and they were tested on the tester board. The inductor chosen for the final design uses an E-22-3F45 core, uses 5 turns of 46/450 litz wire, has 7.5 mils of airgap in each leg of the core, and a 62 mil spacer between airgap and winding. A summary of the components of the RTI buck converter is shown in Table 1.

APPENDIX B

In this appendix the selection process for the isolation/transformation stage is discussed. The MOSFETs were selected in a similar manner to the ones from the PFC block: pick a handful of devices based on their datasheets and test them on a test board. The FETs used in the inverters are EPC2016C and in the rectifier EPC2024.

The transformer is designed in a similar manner as above: using a Matlab script and testing a few designs using a test board. The Matlab script (available in [37]) uses information about core material, core geometry, switching frequency, litz wire winding (diameter and number of strands) and turns ratio to estimate copper [50] and core losses. The transformer used in the final circuit uses two E22 core halves of DMR51 core material. Each primary (P) has 3 turns and the secondary (S) has 2 turns. There are two secondary coils, each of two turns, connected in parallel. The transformer is wound PSSP (top to bottom) using 1000/48 litz wire.

The transformer leakage inductance is used to satisfy the operating conditions of the circuit. From equation (4) one can see that there exists an upper bound on inductance value (for a fixed frequency, turns ratio and input/output voltages) that satisfies the output power requirement. To deliver 250 W with a 575 KHz switching frequency, a nominal input voltage of 72 V and an output voltage of 24 V the leakage inductance referred

to the secondary is approximately 300 nH. On this circuit additional leakage inductance is needed on top of what the transformer provided. Two rod core inductors were placed on each primary of the transformer. The inductors used were each part 3061990871 (61 material) from Fair-Rite using 5 turns of 1000/48 litz wire (each providing an inductance of about 280 nH).

APPENDIX C

In this appendix the control strategy of the converter is discussed, including the PFC stage and the isolation stage.

The PFC stage uses a proportional and integral (PI) controller to maintain the output voltage at a nominal value of 72 V. The startup sequence consists of a series of gate pulses that trickle charge the energy buffering capacitors to avoid excessive stress on the FETs. The PI controller takes over once the capacitors reach their nominal voltage. The startup sequence takes about 1 second.

The isolation stage controls the phase shift between the input and output bridges to maintain a constant output voltage, following the relationship in equation (4). During the startup sequence, the output bridge operates using the body diodes of the FETs until the output reaches 5 V. This voltage is the minimum necessary to turn on the control circuitry and gate drivers on the secondary side of the transformer. This way the isolation barrier is kept intact. During light load operation, the phase shift is kept at a minimum and the output is controlled via dead-time control, as discussed in Section III-D.

REFERENCES

[1] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Lietermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009.* Feb 2009, pp. 1-14.

[2] M. Chen, K.K. Afridi, and D.J. Perreault, "Stacked Switched Capacitor Energy Buffer Architecture," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5183-5195, Nov. 2013.

[3] Y. Jang, M.M. Jovanovic, D.L. Dillman, "Hold-Up Time Extension Circuit With Integrated Magnetics," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 394-400, March 2006.

[4] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of Eliminating Electrolytic Capacitor in AC/DC Power Supplies for LED Lightings," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1399-1408, May 2009.

[5] B. Wang, X. Ruan, K. Yao, and M. Xu, "A Method of Reducing the Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 592-601, Mar. 2010.

[6] A.J. Hanson, A. Martin, D.J. Perreault, "Energy and Size Reduction of Grid-Interfaced Energy Buffers through Line Waveform Control," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11442-11453, Nov. 2019.

[7] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381-1390, May 2008.

[8] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778–4794, July 2016.

[9] K. K. Afridi, M. Chen, and D. J. Perreault, "Enhanced bipolar stacked switched capacitor energy buffers," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1141–1149, March 2014.

[10] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4905–4924, June 2017.

[11] EN 61000-3-2:2014. European Standard. Comité Européen de Normalisation Electrotechnique (CENELEC), p. 21, August 2014.

[12] 80 PLUS. Ecos Consulting and EPRI. https://plugloadsolutions.com/80PlusPowerSupplies.aspx

[13] IEC, "Information technology equipment - safety. part 1: General requirements," IEC 60950-1, 2005.

[14] IEC, "Protection against lightning - part 3: Physical damage to structures and life hazard," IEC 62305-3, 2010.

[15] FCC 15.107 Electronic Code of Federal Regulations www.ecfr.gov

[16] 'Electromagnetic compatibility (EMC) – part 4–6: Testing and measurement techniques – immunity to conducted disturbances, induced by radio-frequency fields, IEC 61000 Edition 3.0, 2008-10'

[17] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single Phase Power Factor Correction: A Survey," *IEEE Transaction on Power Electronics,* vol. 18, no. 3, pp. 749-755, May 2003.

[18] G. Moschopoulos and P. Jain, "Single-Phase Single-Stage Power–Factor-Corrected Converter Topologies," *IEEE Transactions on Industrial Electronics*, vol 52, no. 1, pp. 23-35, Feb 2005.

[19] M. Scherbaum, M. Reddig, R. Kennel, and M. Schlenk, "An Isolated, bridgeless, quasi-resonant ZVS-switching, buck-boost single-stage AC-DC converter with power factor correction (PFC)," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 74–81, March 2017.

[20] M. Narimani, and G. Moschopoulos, "A New Interleaved Three-Phase Single-Stage PFC AC–DC Converter With Flying Capacitor," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3695-3702, July 2015.

[21] D. L. O' Sullivan, M. G. Egan, M. J. Willers, "A Family of Single-Stage Resonant AC/DC converters With PFC," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 398-408, Feb. 2009.

[22] S. Lim, D. M. Otten, and D. J. Perreault, "New AC-DC Power Factor Correction Architecture Suitable for High-Frequency Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2937–2949, April 2016.

[23] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A Family of Single-Phase Hybrid Step-Down PFC Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5271-5281, July 2017.

[24] B. Mahdavikhah, and A. Prodic, "Low-Volume PFC Rectifier Based on Nonsymmetric Multilevel Boost Converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1356-1372, March 2015.

[25] D. Shahzad, M. Farooq, S. Pervaiz, K.K. Afridi "A High-Power-Density High-Efficiency Soft-Switched Single-Phase Universal Input to 28-V Isolated AC-DC Converter Module Designed for Paralleled Operation," *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 8262-8280, July 2022.

[26] X. Ruan, B. Wang, K. Yao, and S. Wang, "Optimum injected current harmonics to minimize peak-to-average ratio of led current for electrolytic capacitor-less ac-dc drivers," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1820–1825, July 2011.

[27] G. M. Soares, P. S. Almeida, J. M. Alonso, and H. A. C. Braga, "Capacitance minimization in offline led drivers using an active-ripple compensation technique," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3022–3033, April 2017.

[28] M. Nassary, M. Orabi, E. M. Ahmed, E. S. Hasaneen, and M. Gaafar, "Modified harmonic injection technique for electrolytic capacitor-less led driver," in 2017 Nineteenth International Middle East Power Systems Conference (MEPCON), Dec 2017, pp. 1459–1464.

[29] Q. Hu and R. Zane, "Minimizing required energy storage in off-line led drivers based on series-input converter modules," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 2887–2895, Oct 2011.

[30] S. Lim, D. M. Otten, and D. J. Perreault, "New ac-dc power factor correction architecture suitable for high-frequency operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2937–2949, April 2016.

[31] A. Hanson, D.J. Perreault, "A High-Frequency Power Factor Correction Stage With Low Output Voltage," *IEEE Transactions on Power Electronics*, vol. 8, no. 3, pp. 2143–2155, Sept 2020.

[32] J.W. Yang, H.L. Do, "Efficient Single-Switch Boost-Dual-Input Flyback PFC Converter With Reduced Switching Loss," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7460-7468, Dec 2015.

[33] D. Shmilovitz, S. Ozeri, M. Ehsani, "A Resonant LED Driver with Capacitive Power Transfer," *Applied Power Electronics Conference and Exposition (APEC), 2014*, Mar. 2014.

[34] W. Inam, "Adaptable power conversion for grid and microgrid applications," PhD Thesis. Chapter 6. 2016.

[35] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 805-816, Feb. 2015.

[36] S. Lim, S. Bandyopadhyay, and D.J. Perreault, "High-Frequency Isolated ac-dc Converter with Stacked Architecture," *Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1789-1796, Mar. 2017.

[37] A.J. Hanson, J.A. Belk, S. Lim, C.R. Sullivan, and D.J. Perreault, "Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7909-7925, November 2016.

[38] J.A. Santiago-González, "Miniaturization of Ac-Dc Power Converters for Grid Interface", PhD. Thesis, Massachusetts Institute of Technology, Cambridge, MA, USA, 2018.

[39] A. Burgio, D. Menniti, M. Motta, A. Pinnarelli, N. Sorrentino, and P. Vizza, "A Two-input Dual Active Bridge Converter for a Smart User Network Using Integrated Power Modules," *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Nov. 2015.

[40] J.A. Santiago-González, D.M. Otten, and D.J. Perreault, "Light Load Efficiency Improvements in Dual Active Bridge Converters via Dead time Control," *IEEE Control and Modeling of Power Electronics (COMPEL)*, June 2018.

[41] H. Chen, "Advanced electrified automotive powertrain with composite DC-DC converter", PhD Thesis, University of Colorado Boulder, Chapter 4, 2016.

[42] M. Chen, S. Chakraborty, and D.J. Perreault, "Multitrack Power Factor Correction Architecture," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2454-2466, March 2019.

[43] Murata Power Solutions MVAC250-12F datasheet, https://power.murata.com/data/acdcsupplies/mvac250.pdf

[44] L. Gu, W. Liang, M. Praglin, S. Chakraborty and J. M. Rivas Davila, "A Wide-Input-Range High-Efficiency Stepdown Power Factor Correction Converter Using Variable Frequency Multiplier Technique," *IEEE Transactions on Power Electronics*, vol. 33, no.11, pp. 9399-9411, Nov. 2018.

[45] TI PMP9640 PFC Demo Board. Texas Instruments. Available at: http://www.ti.com/tool/PMP9640.

[46] SynQor datasheets: PFICU24HTx14 PFC module, ACLFUNVETx230 AC line filter. Buffer capacitor datasheet: Rubycon 450QXW150MEFC18X40, uses 2 in parallel.

[47] S. Pervaiz, A. Kumar and K. K. Afridi, "GaN-Based High-Power-Density Electrolytic-Free Universal Input LED Driver," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp.3890-3901, July/Aug 2018.

[48] J. R. Warren, III, K.A. Rosowski, and D.J. Perreault, "Transistor Selection and Design of a VHF DC-DC Power Converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 27-37, January 2008.

[49] P.L. Dowell, "Effects of eddy currents in transformer windings," Proc. IEE, vol. 113, no. 8, Aug. 1966, pp. 1387-1394.

[50] C.R. Sullivan, "Optimal Choice for Number of Strands in a Litz-Wire Transformer Winding," *IEEE Transactions on Power Electronics*, vol. 14, no.2, pp. 283-291, March 1999.

Juan A. Santiago-González received his B.S. degree in electrical engineering from the University of Puerto Rico, Mayagüez Campus, Mayagüez, PR, in 2011, and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2013 and 2018, respectively.

He is currently with De-Ice Technologies, in Somerville, MA. His research interests include power electronics, resonant converters, power supplies and radio-frequency power amplifiers.


David M. Otten received the B.S. and S.M. degrees from the Massachusetts Institute of Technology (MIT), Cambridge in 1973 and 1974 respectively.

In 1974 he joined the MIT Electric Power Systems Engineering Laboratory (EPSEL) as a staff engineer. Since 1984 he has been a Principal Research Engineer in the renamed Laboratory for Electromagnetic and Electronic System (LEES) at MIT. His research interests include instrumentation, power electronics, and the micromouse robot contest.
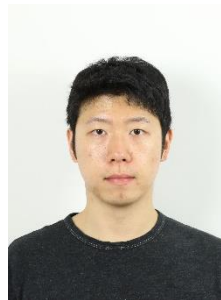
Seungbum Lim received the BS degree in electrical Engineering from Seoul National University, Seoul, Korea, and S.M. and Ph.D degree in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA. His research interests include power electronics, resonant converters, soft-switching techniques, and RF power amplifiers.
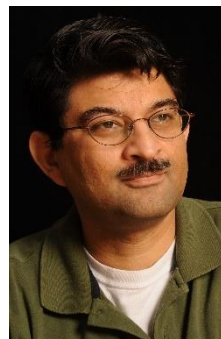

Khurram K. Afridi (S'93-M'98-SM'16) received the B.S. degree in electrical engineering from the California Institute of Technology (Caltech) in 1989 and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT) in 1992 and 1998, respectively.

During summers and between degrees he worked for JPL, Lutron, Philips, and Schlumberger. In 1997, he joined the founding team of Techlogix as Chief Technology Officer and became Chief Operating Officer in 2000. From 2004 to 2008 he also led the development of LUMS School of Science and Engineering

(SSE) as Project Director, and was appointed Associate Professor and the Werner-von-Siemens Chair for Power Electronics in 2008. From 2009 to 2014 he was a Visiting Associate Professor in the Department of Electrical Engineering and Computer Science at MIT, and from 2014 to 2018 he was an Assistant Professor in the Department of Electrical, Computer and Energy Engineering at the University of Colorado (CU) Boulder. Since 2018 he is an Associate Professor in the School of Electrical and Computer Engineering at Cornell University.

His research interests are in power electronics and energy systems incorporating power electronic controls. He is an associate editor of the IEEE Journal of Emerging and Selected Topics in Power Electronics and a Distinguished Lecturer of the IEEE Vehicular Technology Society. Dr. Afridi is a recipient of Caltech's Carnation Merit Award, CU Boulder's Goh Faculty Fellowship, Cornell's Engineering Research Excellence Award, the BMW Scientific Award, and the NSF CAREER Award. He is co-author of six IEEE prize papers.
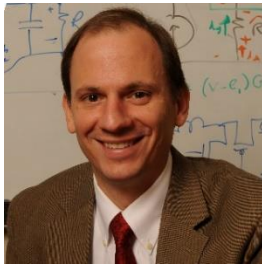
David J. Perreault (S'91, M'97, SM '06, F'13) received the B.S. degree from Boston University, Boston, MA, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA.

In 1997 he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate, and became a Research Scientist in the laboratory in 1999. In 2001, he joined the MIT Department of Electrical Engineering and Computer Science, where he is presently the Ford Professor of Engineering and the William R. and Betsy P. Leitch Professor in Residence at MIT.

His research interests include design, manufacturing, and control techniques for power electronic systems and components, and in their use in a wide range of applications. He also consults in industry, and co-founded Eta Devices, inc. (acquired by Nokia in 2016) and Eta Wireless, inc. (acquired by Murata in 2021). Dr. Perreault is a member of the National Academy of Engineering. He received the Richard M. Bass Outstanding Young Power Electronics Engineer Award, the R. David Middlebrook Achievement Award, the ONR Young Investigator Award, and the SAE Ralph R. Teetor Educational Award. He is co-author of fifteen IEEE prize papers, and of the second edition of the textbook "Principles of Power Electronics" (Cambridge University Press, 2023).