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Diode evaluation and series diode balancing for high-voltage high-frequency power converters

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***Abstract*—Miniaturization of high voltage power converters is severely limited by the availability of fast-switching, low-loss high-voltage diodes. This paper explores techniques for using discrete low-voltage diodes in series as one high voltage diode in high-frequency applications (e.g., hundreds of kHz and above). We identify that when series connecting diodes, the parasitic capacitance from the physical diode interconnections to common can result in voltage and temperature imbalance among the diodes, along with increased loss. We quantify the imbalance and propose two related compensation techniques. To validate the approaches, a full-bridge rectifier is tested with each branch consisting of four 3.3 kV SiC diodes in series. Experimental results showcase the imbalance and demonstrate the effectiveness of the compensation techniques. Additionally, we characterize the performance of a range of diodes for use in high-frequency, high-voltage converters. The proposed technique and evaluation results will be valuable for the design of lightweight and miniaturized high voltage power converters.**

***Index Terms*—High voltage diodes, series diode balancing, high-frequency converter, high-voltage converter**

I. Introduction

Applications such as electro-aerodynamic propulsion, small-scale electrostatic precipitators, portable X-ray machines, and others have stimulated the need for lightweight and miniaturized high voltage power converters operating at output voltages of tens of kV [2]–[10]. This motivates increasing switching frequencies from a few hundred kHz and below to the high hundreds of kHz and MHz range. One of the bottlenecks to achieving high frequency at high output voltage while preserving high efficiency is the lack of low-loss high-voltage diodes capable of operation at high frequency [5], [11]. Si Schottky diodes are appealing in high frequency applications but they are mostly rated below $250\,\mathrm{V}$ [12]; commercially available Silicon Carbide (SiC) diodes exhibit low loss and can block up to $3.3\,\mathrm{kV}$; however, above $5\,\mathrm{kV}$, the only presently affordable and available diodes are Si high-voltage diodes [12]. These diodes have rarely been used in the high hundreds of kHz and MHz range, and have not been characterized for operation at such frequencies.

To better explore the range of diodes that might be useful in such applications, we have tested a range of diodes (from $400\,\mathrm{V}$ to $15\,\mathrm{kV}$) in a full-bridge rectifier topology at $600\,\mathrm{kHz}$ and $1\,\mathrm{MHz}$. Most of the tested Si high voltage diodes are not suitable for operation at or above $600\,\mathrm{kHz}$ at even a fraction of their rated outputs without heat sinks. Nonetheless, low voltage fast recovery diodes ($400\,\mathrm{V}$ to $600\,\mathrm{V}$) and SiC Schottky diodes ($650\,\mathrm{V}$ to $3.3\,\mathrm{kV}$) are promising candidates for building high-voltage, high-frequency systems. The evaluation methods and results will be explained in details in Section II.

One can use such high-frequency, low-loss low-voltage diodes in various ways to achieve a high-voltage output. One can (1): have multiple transformer windings or multiple resonant tanks that are separately rectified and stacked in series (e.g., [4], [8], [13]); (2): Use the diodes in voltage multiplying rectifier topologies (e.g., [5], [9], [14]–[16]); and/or (3): Series connect discrete low-voltage diodes to construct an approximate equivalent to a high-voltage diode (e.g., [17]).

Each method has limitations: the losses of a voltage multiplier increase drastically with the number of stages [15], [18]. The complexity (and often-times the loss) of a transformer increases with more secondaries as does its nonideality of operation, especially when high insulation levels are needed between outputs. Series connection of devices leads to questions about how the individual devices actually act, and the impact on their voltage sharing during the off-state and their losses owing to switching and conduction.

This paper explores design considerations in the use of series-connected low-voltage diodes as a single high voltage diode for high-frequency applications. We observe that there are serious off-state voltage and temperature imbalance issues that can arise when series-connecting such diodes. We present a theoretical model showing that significant voltage imbalance and loss differences can be caused by parasitic capacitances of the diode interconnection points to common.

The paper also describes two related compensation techniques to mitigate voltage imbalance and loss owing to these interconnect capacitances. The proposed techniques function by adding external low-loss capacitors to restore voltage balance and reduce diode losses. We present analytical solutions as well as theoretical limitations of these techniques. We present experimental results using four $3.3\,\mathrm{kV}$ diodes to form a high-voltage diode, showcasing the voltage/temperature imbalance issue as well as demonstrating the effectiveness of the compensation techniques. The compensation capacitors can be further integrated into the PCB design, thus can enable the design of ultra-lightweight high voltage rectifiers.

Section II explains the diode evaluation tests and the results. Section III presents the theoretical model for series-connected discrete diodes and the voltage imbalance issue. Section IV explains the compensation techniques and their limitations. Section V presents the experimental results, both showcasing

The paper is an extension of a conference paper, Y. He and D. J. Perreault, Series diode balancing and diode evaluation for high-voltage high-frequency power converters, in Applied Power Electronics Conference and Exposition (APEC), March 2019 [1]. Here we extend the work to include diode evaluations at higher frequencies and more accurate test results.

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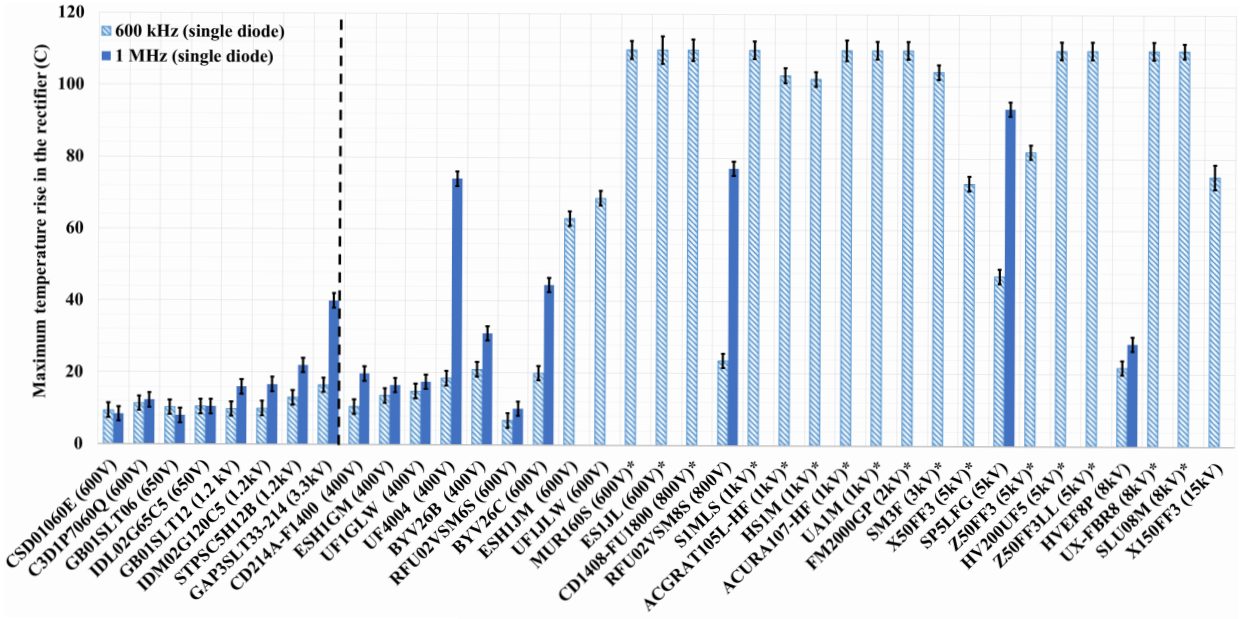
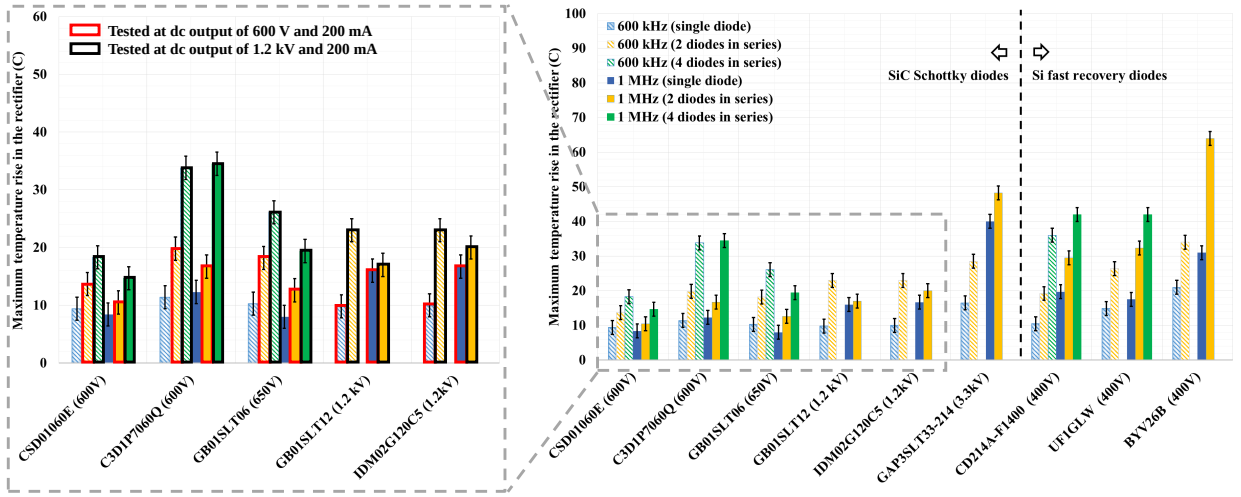


(a)



(b)

Figure 1: Maximum temperature rise in the rectifier when diodes are tested in a full-bridge rectifier topology at 600 kHz and 1 MHz. All tests start at room temperature 25 °C to 28 °C and the temperature of the hottest spot in the rectifier is recorded to calculate the "maximum temperature rise". The specifications of diodes, the details of all test conditions, experimental setup and error estimations are explained in Appendix A and Table II. **(a)** Maximum temperature rise of single diode tests. In these tests, each leg of the full-bridge rectifier consists of a single diode. The rectified dc voltage is 45 % to 50 % of the nominal diode rated voltage and the rectified dc current is approximately 10 % to 20 % of the nominal diode rated current (which means that the average diode current is 5 % to 10 % of its nominal rated dc current). When testing the same diode at two different frequencies, the rectified dc voltage and the dc current are kept the same. Diodes listed without an asterisk were tested for 10 min such that they reached thermal equilibrium and the maximum temperature rise on the rectifier was recorded; diodes listed with an asterisk did not reach thermal equilibrium before the temperature became too high, these tests were cut off earlier when the maximum temperature rise in the rectifier reached roughly 100 °C. **(b)** Maximum temperature rise of multi-diode tests. In these tests, each leg of the rectifier consists of multiple diodes connected in series. The rectified dc voltage is 45 % to 50 % of the rated voltage of the leg and the rectified dc current is approximately 10 % to 20 % of the diode rated current. Each test lasted 10 min and the maximum temperature rise in the rectifier was recorded. As with single-diode tests, when testing the same combination across frequencies, the rectified dc voltage and current are kept the same.

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the imbalance issue as well as the effectiveness of one version of the proposed compensation techniques for improving system performance. Section VI concludes the paper.

II. Evaluation of High Voltage Diodes

To identify suitable diodes operating at high voltage and high frequency, we tested 37 off-the-shelf diodes in a full-bridge rectifier topology from three perspectives:

- Compare across diodes when a single diode is used within a fixed range of voltage and current de-rating factors. We refer to these tests as "single diode tests".
- Compare across selected diodes when multiple diodes are connected in series as a single higher-voltage diode to meet a given blocking voltage requirement. We refer to these tests as "multi-diode tests".
- Repeat and compare the above tests at 600 kHz and 1 MHz while holding other test conditions constant.

We use "maximum temperature rise in the rectifier" as a metric to evaluate the diodes in all tests for two reasons: (1) the temperature rise correlates well with power losses and can be measured in a non-intrusive way; and (2) the maximum temperature rise data can be used to decide whether cooling devices (e.g., heat sinks) are needed, which is an important factor in realizing miniaturized and lightweight designs.

The diodes under test include Si fast recovery diodes (both low voltage and high voltage) and SiC Schottky diodes. The nominal blocking voltages of these diodes range from $400\,\mathrm{V}$ to $15\,\mathrm{kV}$, and the nominal average forward currents range from $30\,\mathrm{mA}$ to $5\,\mathrm{A}$. Experimental details for conducting these tests are described in Appendix A.

A. Single diode tests

Figure 1a shows the maximum temperature rise results of the single diode tests (Table II in Appendix A shows full specifications of the diodes under test and the test conditions). The results reveal that at $600\,\mathrm{kHz}$, SiC Schottky diodes ($650\,\mathrm{V}$ to $3.3\,\mathrm{kV}$) and several low voltage Si fast recovery diodes ($400\,\mathrm{V}$ to $800\,\mathrm{V}$) show significantly lower maximum temperature rises compared to most high voltage Si fast recovery diodes ($3\,\mathrm{kV}$ to $15\,\mathrm{kV}$). One exception is an $8\,\mathrm{kV}$ diode (HVEF8P), which is tested at $\sim 4\,\mathrm{kV}$ output voltage and $\sim 5\,\mathrm{mA}$ average output current. It shows promise when used at high frequency for high-voltage low-current applications.

For diodes with a maximum temperature rise lower than $\sim 80\,^{\circ}\mathrm{C}$, we further characterize the diode losses themselves. This is accomplished using dc signals to develop measured relations between diode dissipation and maximum temperature rise. The details are explained in Appendix A and it is concluded that the maximum temperature rise and the total diode losses are closely correlated as expected.

Three aspects that could contribute to the higher losses and higher maximum temperature rises shown in most high-voltage Si fast recovery diodes are: (1) the conventional ways to boost the blocking voltage (e.g. multi-junction, single deep-diffused junction, or glass passivated) raise the forward voltage of the diode, proportionally increasing the conduction losses; (2) as the off-state voltage increases, the switching losses tend to increase rapidly; (3) higher blocking voltage introduces larger leakage current [19], resulting in more severe heating thus even worse tolerance of losses [20].

Figure 1a also suggests that increasing the switching frequency from $600\,\mathrm{kHz}$ to $1\,\mathrm{MHz}$ in general increases the maximum temperature rise, however, the magnitude of the increment varies case by case and shows no obvious trends. Among those that show promises in the $600\,\mathrm{kHz}$ tests, the $3.3\,\mathrm{kV}$ SiC diode (GAP3SLT33) and several Si fast recovery diodes (UF4004, BVY26C, and RFU02VSM8S) show significantly higher maximum temperature rise at $1\,\mathrm{MHz}$, suggesting that the total losses of these diode in the frequency range of interest are dominated by switching losses. As listed in Table II, these diodes have a non-zero "reverse recovery time" or "switching time", which helps explain the increased switching losses at high frequency even in the case of SiC schottky diodes.

B. Multi-diode tests

Figure 1b presents the maximum temperature rise results of the multi-diode tests (Table II in Appendix A shows full specifications of the diodes under test and the test conditions). The results suggest that for both Si fast recovery diodes and SiC Schottky diodes, connections of more diodes in series lead to higher maximum temperature rises of the diodes, even though their nominal carrying and blocking requirements stay the same. This presents a challenge when using series connections of low-voltage diodes to realize "high-voltage equivalent" diodes in high voltage applications. For example, looking across tests with $1.2\,\mathrm{kV}$ and $200\,\mathrm{mA}$ dc rectifier output, 4 GB01SLT06 diodes in series presents higher maximum temperature rise than 2 GB01SLT12 diodes in series, even though in the single diode tests GB01SLT06 performs better than GB01SLT12.

As will be explained in the next section and demonstrated in the experimental results in Fig. 8, the maximum temperature rises in the multi-diode tests are usually at the diodes closer to the ac node. In Section III, we explore the causes of the increased "maximum temperature rise" when multiple diodes are connected in series. Owing to both the increased losses and poor voltage sharing, additional efforts may often be required if high-performing low-voltage diodes are to be series connected and utilized for high-voltage rectification at high frequency. We introduce compensation means for addressing this challenges in Section IV.

III. Challenges when series connecting diodes

Series connection of diodes to attain higher effective blocking voltages is well known, and issue of voltage imbalance due to the variation among diodes has been observed [21]. The common solution is to parallel balancing resistors with the diodes to ensure that each diode reaches the same dc state [21]. This static "resistive" balancing approach may be most effective for low switching-frequency conditions (i.e., where off-state times are long as compared to the RC time constants involved). Here we identify that the net effective parasitic capacitance to common at the connection nodes between the diodes also contributes to voltage imbalance and to increased loss. The effect of these capacitances becomes increasingly important as operating frequency rises, and becomes a major consideration in achieving high performance at the high operating frequencies considered here.

A. Parasitic capacitance causing voltage imbalance

Figure 2 shows a circuit diagram of a full-bridge rectifier. Each branch consists of M series-connected diodes $D_1, D_2, ..., D_M$. Each node has its parasitic capacitances to the ac node and to a common node (referring to a node with fixed dc voltage with respect to ground, in this case either the ground or the high voltage dc output). For a high-frequency, high-voltage application, one usually minimizes the area of the ac node to prevent the ac noise from coupling to other nodes, and/or implements grounded shielding around the circuits. In practice, these techniques usually yield a significantly larger capacitance from the diode interconnections to common than

that to the ac node. Therefore we simplify the parasitic capacitance at each node as a net capacitance to common, shown as $C_{p1}, C_{p2}, ..., C_{pM}$ in Fig. 2. These capacitances sink or source charge from each node.

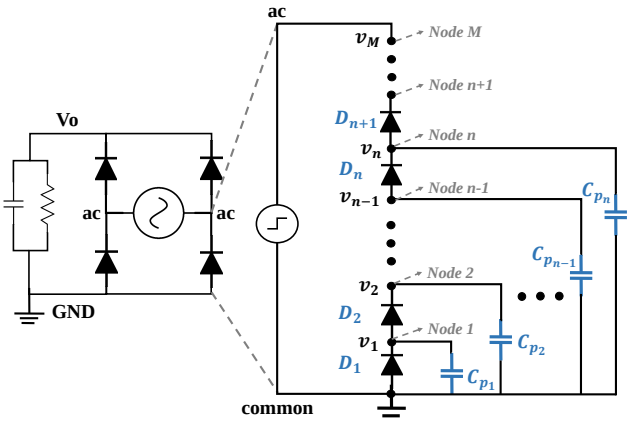


Figure 2: Circuit model of multiple diodes connected in series as a single diode, showing a net parasitic capacitance from each node to common.

At high frequencies, the voltage distribution among diodes is mostly determined by the capacitances[1]. As a first order analysis, we assume each diode has the same capacitance C_D across it (this includes the diode junction capacitance and the parasitic capacitance between the two nodes to which the diode is connected). We likewise assume the net parasitic capacitance from each diode connection node to common has the same value C_P. For simplicity, we ignore the non-ideality of both C_D and C_P (i.e., the voltage dependencies, etc). Thus we simplify Fig. 2 to Fig. 3a.

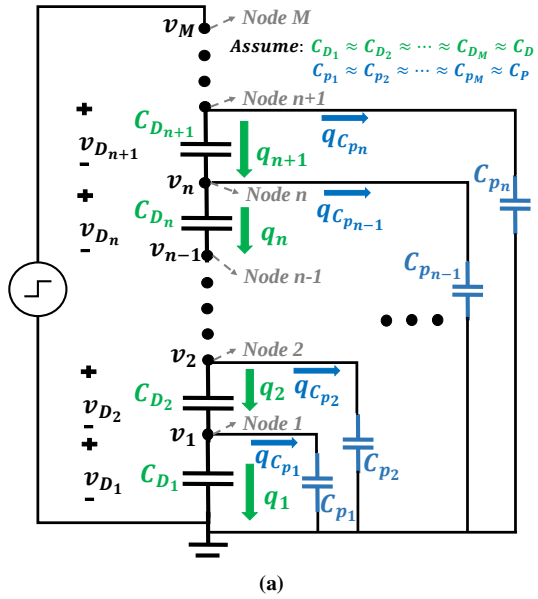
In the following analysis, we consider an incremental increase in the source voltage applied between the ac node and common; this increment will inject an incremental amount of charge into the diode chain.

To charge the voltage v_{D_1} at Node 1 from zero to v_1, the charge going through the parasitic capacitance of D_1 (C_{D_1}) is $q_1 = v_1 C_D$, and the charge going through C_{p_1} is $q_{Cp1} = v_1 C_P$. Since both charges come from D_2, the charge going through the parasitic capacitance of D_2 (C_{D_2}) is $q_2 = q_1 + q_{Cp1} = v_1 C_D + v_1 C_P$. If we want $V_{D1} \approx v_{D2}$, we must make sure $q_2 \approx q_1$, thus $q_1 \gg q_{Cp1}$ (equivalently $C_D \gg C_p$).

To generalize, at Node N, $q_n = v_{Dn} C_D$ and $q_{Cpn} = v_n C_P$. If we want $v_{Dn+1} \approx v_{Dn} ... \approx v_{D1}$, or equivalently $v_n \approx n v_{D1}$, we must make sure $q_n \gg q_{Cpn}$, equivalently $C_D \gg nC_p$. To provide approximate voltage balancing among the diodes, we require $C_D \gg nC_p$.

Considering using n diodes in series, each at some fixed percentage of its rated voltage, to construct an equivalent diode

[1]In practice, there are also stray inductances in series with the diodes owing to the diode packaging and circuit layout. However, these inductances tend not to have a significant effect on diode voltage sharing. This is not surprising given that series packaging inductances tend to affect each device in a similar manner. Moreover, as this work focuses on applications operating at relatively high voltage and low current, the capacitances may be expected to have a much more substantial effect compared with inductances. Indeed, simulations revealed negligible impact of parasitic inductances, even for inductance levels much higher than found for typical devices and layouts. In the following analysis, we thus ignore the effect of the stray inductance.



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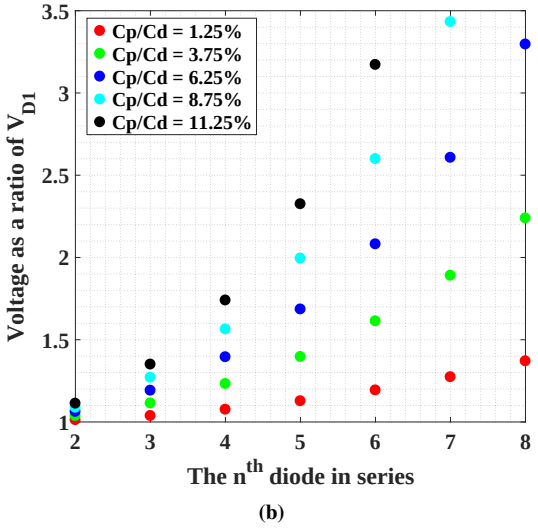


(b)

Figure 3: Simplified ac circuit model for multiple diodes connected in series and the voltage ratio due to the presence of net parasitic capacitances from each node to common. **(a)** Simplified ac circuit model of Fig. 2 at high frequencies. **(b)** Voltages across the nth diode as a ratio of that across the 1st diode as calculated with equation (1).

of n times the individual diode rating. As any of the following three parameters changes: n increases, C_D decreases, or C_P increases, the constraint $C_D \gg nC_p$ becomes more difficult to meet. In practice, this constraint often cannot be met, resulting in voltage imbalances among the diodes. Intuitively, the diode closest to the ac node needs to carry all the charge going down the diode chain and that going through all the parasitic capacitances. If all diodes are identical (and thus have identical capacitances), then this diode passes more charge through its capacitance C_D than diodes below it, and thus needs to block higher voltage. (As shown in Fig. 3a, $v_{D_i} = C_D \times q_i$, because $q_1 > q_2 > ... > q_M$, we have $v_{D_1} > v_{D_2} > ... > v_{D_M}$).

As shown in Appendix B, a closed form expression for the diode voltages in Fig. 3a in terms of the bottom diode voltage v_{D1} can be found as:

$$\frac{v_{Dn}}{v_{D1}} = \frac{1}{\sqrt{a(a+4)}} \left\{ \left(\frac{a+2+\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a+\sqrt{a(a+4)}}{2} \right) - \left(\frac{a+2-\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a-\sqrt{a(a+4)}}{2} \right) \right\} \quad (1)$$

where $a = C_P/C_D$. We plot these voltages for different values of C_P/C_D in Fig. 3b. It can be seen that the diode closes to the common potential blocks the lowest voltage, and as the number of series diodes increases, the off-state voltage imbalance increases; in addition, when C_P/C_D gets bigger, the voltage imbalance gets worse.

The voltage imbalance suggests the switching loss among diodes is also imbalanced: the diodes closer to the ac node must carry higher capacitive switching currents and are charged/discharged to larger off-state voltages and thus exhibit higher loss. In stating this, we recognize that the currents carried through diode capacitances (and associated device voltage swings) induce significant loss in the diodes. These losses may be due to joule heating and/or may represent other loss phenomena, as observed with capacitance losses in other device types [22]–[24]. Based on this, if each diode has similar thermal path to ambient, then diodes closer to the ac node would show higher maximum temperature rise as well as higher off-state voltage than diodes closer to a dc potential. The experimental results "before compensation" in Fig. 8 and Fig. 9a in Section V demonstrate this predicted voltage and temperature imbalance.

IV. Compensation Techniques for Achieving Voltage Balance

With the series diode connection, the charge going through each diode is different due to the presence of parasitic capacitance to the external environment at each connection node, Moreover, additional losses are introduced owing to the lossy nature of the device capacitances carrying the currents associated with these external parasitics. We can redistribute the charge flows through the diodes and mitigate some of the associated voltage imbalances and losses by adding low-loss external capacitors. Two related compensation techniques are proposed in this section.

A. Independent compensation

Figure 4a illustrates the first compensation technique, which we refer to as "independent" compensation. Taking Node 1 as an example, C_{p_1} draws charge from the node having voltage v_1. Instead of providing this charge $q_{C_{p_1}}$ from D_2, we can inject the charge directly to Node 1 through an additional capacitor C_{c_1} connected between Node 1 and the ac node. In this way, we guarantee $q_1 = q_2$ thus $v_{D1} = v_{D2}$. The amount of charge needs to be injected as the diode voltage charges from zero to its final off-state value v_1 is $q_{Cp1} = v_1 C_P$. Since, after compensation, C_{c_1} blocks $(M-1)v_1$, where M is the number of series-connected diodes (assuming after adding the compensation, all diode voltages balance), the required capacitance of C_{c_1} is $\frac{1}{M-1}C_P$. Similarly for Node n, we can inject the charge directly from the ac node to the nth parasitic capacitance through C_{c_n}.

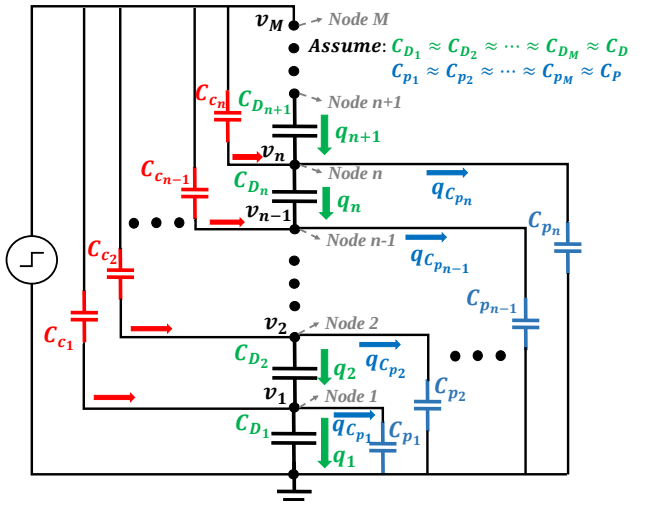


Figure 4: Circuit diagram of two related compensation techniques **(a)** Independent compensation: adding compensation capacitors to each node. **(b)** Coupled compensation: adding compensation capacitors across each diode.

These additional compensation capacitors solely provide charge to the corresponding parasitic capacitance, and can be independently adjusted. Their values are calculated as below.

$$C_{c_1} = \frac{1}{M-1}C_P, ..., C_{c_n} = \frac{n}{M-n}C_P, ..., C_{c_M} = (M-1)C_P \quad (2)$$

The lower and the upper bound of the compensation capacitances are $\frac{1}{M-1}C_P$ and $(M-1)C_P$ respectively. As M increases, the lower bound decreases approximately inversely with the number of series-connected diodes and is eventually limited by the smallest physical capacitance that one can accurately implement; the upper bound increases approximately linearly with the number of series-connected diodes and is limited by the increased losses and the load regulation effect associated with the total capacitance between the ac node and common [25]. A benefit of this technique is that each

compensation capacitance may be selected/adjusted based on the voltage distribution impact at a single node. At the same time, each of the compensation capacitances blocks different voltage making their implementation more cumbersome.

B. Coupled compensation

An alternative compensation approach is to add a low-loss capacitor across each diode to carry the charge for the parasitic capacitances. A benefit of this implementation, which we refer to as "coupled" compensation, is that each compensation capacitor blocks the same voltage; a disadvantage is that the charges going through them (and the capacitor values) are coupled. All the charges are carried by the top compensation capacitor, and they trickle down the chain to each parasitic capacitance. Consequently, the value of each compensation capacitor is a function of the parasitic capacitances of all of the nodes down the chain.

The capacitance of each compensation capacitor is calculated and listed in (3). C'_n provides the sum of charges for $Q_{C_{p_1}}$, $Q_{C_{p_2}}$,..., $Q_{C_{p_{n-1}}}$. Since $Q_{C_{p_i}} = iV_1C_P$, the sum of the charges is $V_1[C_P + 2C_P + ... + (n-1)C_P] = \frac{n(n-1)}{2}V_1C_P$. Thus $C'_n = \frac{n(n-1)}{2}C_P$.

$$C'_2 = C_P, ..., C'_n = \frac{1}{2}n(n-1)C_P, ..., C'_M = \frac{1}{2}M(M-1)C_P \quad (3)$$

With coupled compensation, the largest required capacitance increases quadratically with the number of diodes in series.

C. Comparison

Figure 5 shows the compensation capacitances needed for each node or each diode in the two compensation implementations. One limiting factor in practical realizations is that a given compensation capacitance should be neither too small nor too large for practical implementation, as illustrated qualitatively with the two grey areas.

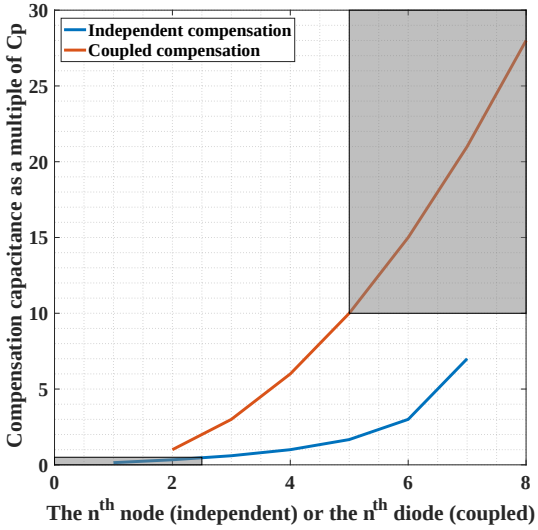


Figure 5: Compensation capacitance required at each node normalized to parasitic capacitance C_P. The compensation capacitance required at any node should not be too small, as limited by the physically realizable capacitance, nor too big, as limited by the physical capacitor size and parasitics. These limits are conceptually illustrated by the two grey areas.

The total capacitive energy storage is identical in either implementation:

$$E_{independent} = \sum_1^M \frac{1}{2}C_{c_n}V^2_{C_{cn}} = \frac{C_PV_1^2}{2}\sum_1^M n(M-n)$$

$$E_{coupled} = \sum_1^M \frac{1}{2}C'_nV^2_{C'_n} = \frac{C_PV_1^2}{2}\sum_1^M \frac{n(n-1)}{2}$$

$$E_{independent} = E_{coupled} = \frac{C_PV_1^2}{2}\frac{M^3-M}{6}$$

However, the facility with which such injection can be implemented with available components or PCB structures (in terms of capacitance values and voltages) will determine the best method to select in a given application. The independent method requires smaller capacitances but higher voltage rating of each compensation capacitor (one could use low-voltage capacitors in series, but it adds complexity in the physical layout of these capacitors). In the coupled method, each compensation capacitor is rated at the same voltage, but higher capacitances are required for larger number of stages. Often, the coupled compensation is easier to implement with discrete components or by PCB design.

In practical applications, the parasitic capacitances $C_{p_i}(i = 1, 2, ..., M)$ may not be equal as assumed above. However, the concept remains valid and the compensation capacitances can be calculated for the general case as well. See Appendix C for the detailed derivation of the compensation capacitances in the general case.

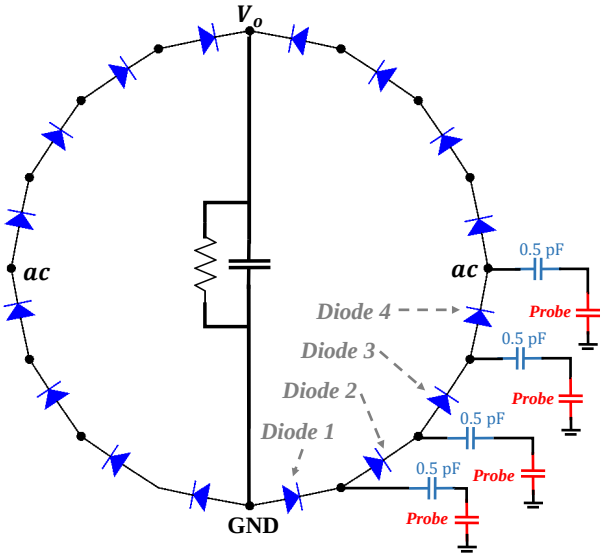
V. Experimental Results

A. Setup and measurement techniques

The experimental setup is shown in Fig. 6. Four 3.3 kV GeneSiC diodes (GAP3SLT33-214) are connected in series for each leg of a full-bridge rectifier. The rectifier is driven from a custom-built inverter and high-voltage transformer with an approximately trapezoidal voltage waveform at 600 kHz. The rectifier outputs 3.6 kV and 20 mA (P_o =72 W) into a resistive/capacitive load. The details of the driving circuit and the load are described in Appendix A. We measure the voltages at four nodes on one leg of the rectifier using four Teledyne LeCroy PPE4KV probes, as shown in Fig. 6. For sensing, we add a 0.5 pF NP0 capacitor at each node as a divider capacitor to reduce the effect of the probe capacitance on the voltage distribution. We also add a capacitor divider and a probe adapter at all other nodes to minimize the differential effects of the probes at the four measurement nodes. By subtracting the voltage readings from four probes, we obtain four voltages that are proportional to the ac component of voltages across Diodes 1 to 4. In terms of voltage balancing, we only care about the ratio of these voltages instead of their absolute values. The 0.5 pF NP0 capacitor, denoted as C_{NP0}, and the probe capacitance, denoted as C_{Probe} form a capacitor voltage divider. We note the probe reading as V_{Probe} and the corresponding node voltage as V_{node}, then $V_{node}/V_{probe} = C_{Probe}/C_{NP0}$. The probe capacitance is estimated to be 10.5 pF, the sum of 6 pF from the PPE4kV probe and 4.5 pF from the probe-to-board adapter. Therefore

the diode off-state voltages are approximately 21 (10.5/0.5) times the peak-to-peak values of the measured voltages.

The circular design of the PCB in Fig. 6 is selected to provide a compact, symmetric layout (tight connections among diodes and compensation capacitors yet with spaces to mount the four probes). The effectiveness of the proposed compensation technique, which will be demonstrated in Part C, is not limited to the circular layout.



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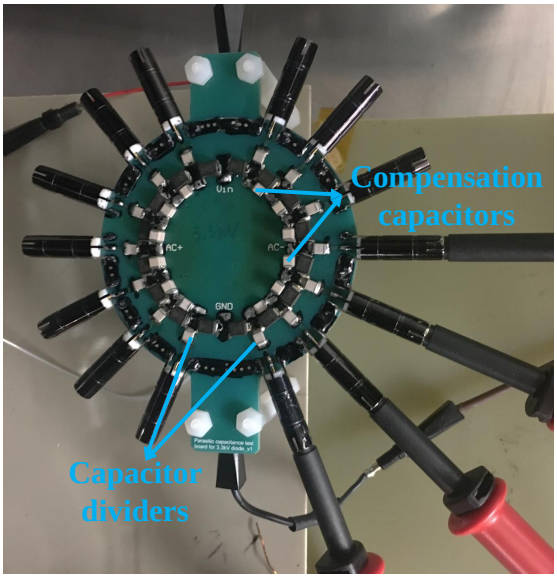


(b)

Figure 6: The full-bridge rectifier circuit for testing the compensation techniques. **(a)** measurement diagram showing divider capacitors and probes. **(b)** a photograph of the experimental test board.

B. Implementation the compensation capacitance

Several CAD and FEA tools [26] are used to simulate the parasitic capacitances of the PCB layout in Fig. 6. The process gives us a capacitance matrix consisting of a parasitic capacitance between every two nodes. We simplify the matrix down to only the capacitances between each node and common

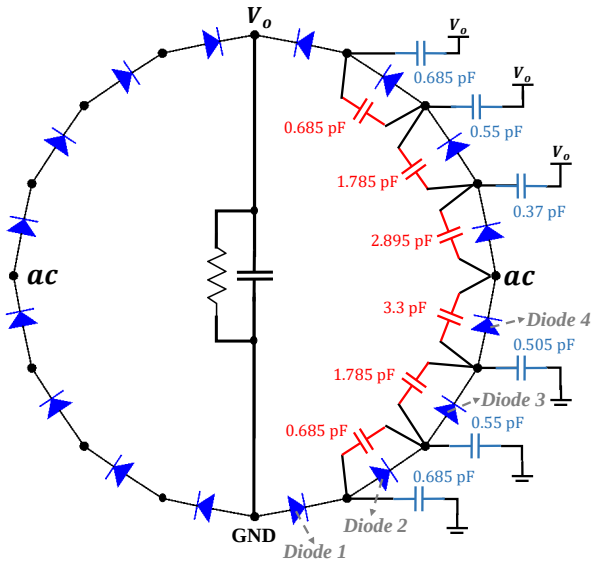


Figure 7: The estimated parasitic capacitance of each node to common (in blue) and the required compensation capacitance across each diode (in red). The capacitances are symmetric across the V_o-GND axis. We implement these using the available capacitors with the closest available capacitance values.

(GND or V_o), as shown in blue in Fig. 7. See Appendix C for detailed simulation and the simplification process.

We choose to implement the coupled compensation because of the availability of discrete capacitors at the required voltage rating. Following the concept in Section IV, we can calculate the required compensation capacitances, shown in red in Fig. 7. See Appendix C for the detailed calculation process. In the experiments, we used Vishay Vitramon Quad HIFREQ series capacitors to obtain the closest discrete capacitances available: 0.5 pF (VJ1111D0R5VXRAJ), 1.5 pF (VJ1111D0R5VXRAJ and VJ1111D1R0BXRAJ) and 3 pF (VJ1111D1R0BXRAJ and VJ1111D2R0BXRAJ) respectively. These are C0G capacitors. They have low loss at high frequencies and small voltage dependencies. Generally, capacitors with small voltage dependencies and stable capacitance values are desirable; as such required capacitances are small, NP0/C0G capacitor types are one good choice for this function.

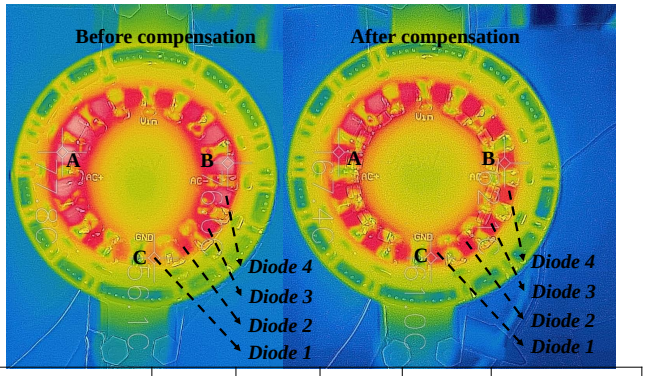
C. Experimental results

Figure 8 shows the temperature profiles of before and after compensation at three different locations in the rectifier (denoted as Nodes A, B and C). Nodes A and B mark two diodes closer to the ac node and Node C marks one diode closer to common. Figure 9 presents the divided-down and ac-coupled voltage waveforms across Diodes 1 to 4 before and after compensation. Each waveform is proportional to the actual off-state voltage of an individual diode.

Before compensation, Node A shows the maximum temperature rise in the rectifier (Node B is very similar), Node C remains ~20 °C cooler than Nodes A and B. Correspondingly, in Fig. 9a the amplitudes of the diode off-stage voltages decrease in the order of Diode 4 to 1 and the worst-case discrepancy (i.e., the ratio of the maximum diode voltage over the minimum diode voltage) is 2.91. This imbalance in temperature and voltage is especially undesired when the

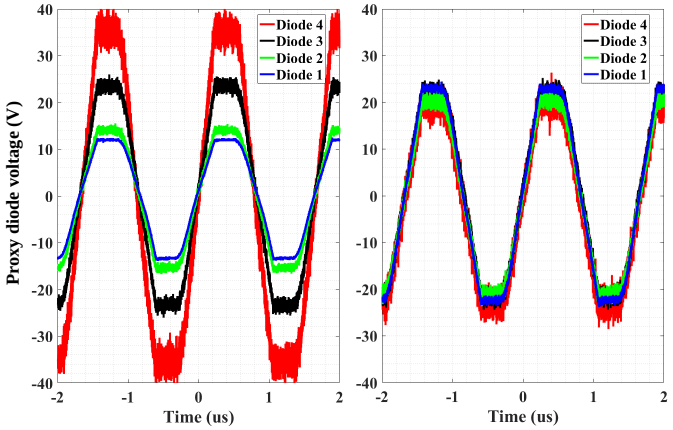
diodes closer to ac nodes reach a certain temperature (∼80 °C to 90 °C at the package): thermal runaway [27] of the hotter diodes provides positive feedback that can greatly further worsen the discrepancy and overall performance.

After compensastion, by contrast, temperature at Node A and Node B reduces by ∼10 °C and that at Node C increases - the diode temperature become more balanced. The temperature discrepancy between the hottest and the coldest diodes drops from 20 °C to 7 °C. Moreover, the average temperature of Nodes A, B and C drops from 70 °C to 64 °C, indicating decreased overall losses. Correspondingly in Fig. 9b, the amplitudes of the off-stage voltages across Diodes 1 to 4 become more balanced and the worst-case discrepancy (ratio of highest to lowest off-state voltage) drops to 1.15.



Conditions	Node A (C)	Node B (C)	Node C (C)	Average (C)	Maximum delta (C)
Before compensation	77.8	76	56.1	~70	77.8 – 56.1 ~ 20
After compensation	67.4	62.1	61	~64	67.4 – 61 ~ 7

Figure 8: Temperature profile before/after compensation. In both cases, the rectifier operates at 600 kHz and outputs 3.6 kV at 20 mA (72 W).



(a) Before compensation **(b) After compensation**

Figure 9: Proxy (divided down and ac coupled) diode voltages before/after compensation. In both cases, the rectifier operates at 600 kHz and outputs 3.6 kV 20 mA (72 W). The voltage ratio is 1 : 1.16 : 1.94 : 2.91 before compensation, and 1 : 0.89 : 0.97 : 0.87 after compensation. The worst-case voltage discrepancy as a percentage is $2.91/1 = 291\%$ and $1/0.87 = 115\%$.

The above comparison coincides with the analysis in Section III that the voltage imbalance is the main factor driving loss and temperature imbalances and resulting in increased maximum and average temperature rises in the rectifier when multiple diodes are connected in series. It also demonstrates the effectiveness of the compensation technique for substantially mitigating the voltage and temperature imbalance. See Appendix C for an accuracy analysis of the proposed methods.

It is also notable that for continuous high-frequency switching of the rectifier diodes as explored here, there is no need for any additional means for balancing diode off-state voltages, because the diode voltages reset each switching cycle and the capacitances are the determining factor in diode voltage distribution. This is clearly illustrated in the results of Fig. 9. In other applications where the diodes may remain statically off over long durations (and may have different leakage currents), some additional static balancing (e.g., via resistors) may be desirable, though such resistor balancing alone cannot be expected to be effective for high-frequency switching.

VI. Conclusion

The paper explores compensation techniques for using discrete low-voltage diodes in series as one high voltage diode. Additionally, the performance of a range of diodes are characterized for use in high-voltage converters. We identify that when series connecting diodes for high-frequency operation, the parasitic capacitance of the physical connections to common can result in severe voltage and temperature imbalances, and corresponding increases in loss. We propose two related compensation techniques to mitigate this issue. We demonstrate the voltage imbalance issue and validate the compensation approach through experimental results. Both the proposed techniques and the diode evaluation results will be useful for miniaturization of high voltage converters.

Appendix A
Temperature Rise Experiments

A. Setup and measurements

The specifications of all diodes under tests are listed in Table. II. We categorized them into 3 groups based on sizes and used 3 PCBs to conduct the tests, as shown in Fig. 11: RFU02VSM6S, RFU02VSM8S, ESH1GM and ESH1JM were in one group; diodes blocking 5 kV to 15 kV were grouped together; all other diodes were grouped together. Within each group, the thermal path of the PCB is approximately the same.

We drive all of the diode rectifiers with a custom-built inverter and transformer [5]; a simplified schematic for this system is shown in Fig. 12. The specifications of the inverter, the transformer and the load are listed in Table I. C_s, L_s are external capacitors and inductors. C_p represents the parasitic capacitance of the transformer and the diodes reflected to the primary side. The resonant tank was tuned such that the current in L_s was near sinusodial at the frequency of interest, resulting in a trapezoidal voltage at the rectifier input. The load of the rectifier is a custom-built variable resistor load. Output capacitors were connected across the load to ensure the output voltage ripple to be within at least 5 %.

The rectified dc voltage was measured using a Tektronix 6015A probe. The load current was measured on the ground side using a Agilent 34410A digital multimeter in series with the resistor load. The temperature was measured by a FLIR

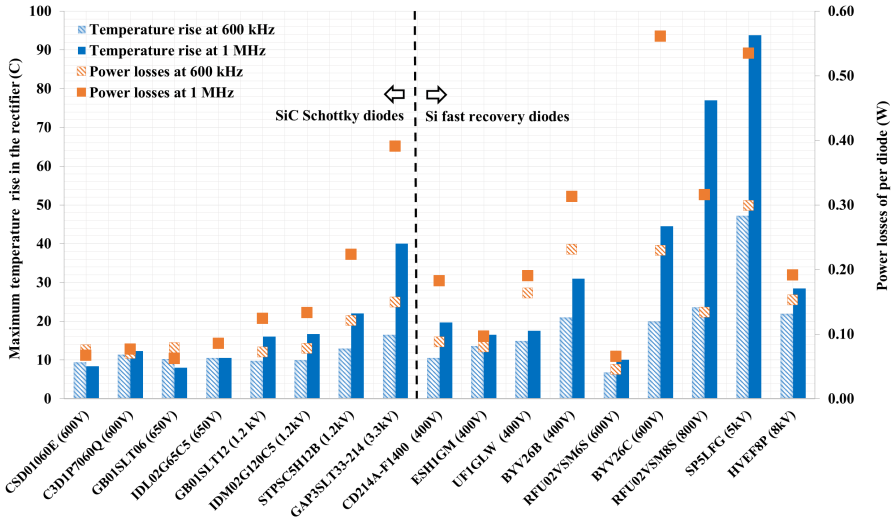


Figure 10: The losses of selected diodes in the single diode tests

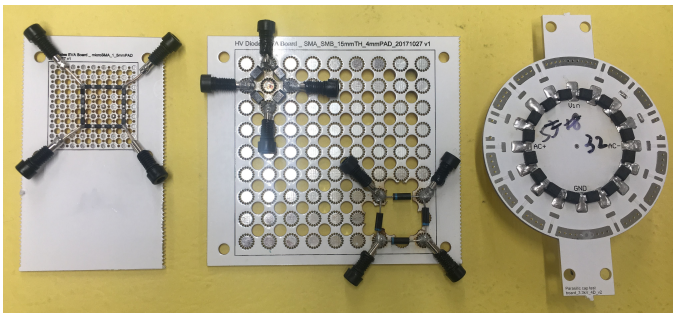


Figure 11: Three PCBs for the diode tests. The left board is used for diode RFU02VSM6S, RFU02VSM8S, ESH1GM and ESH1JM; the middle board is used for diodes blocking 5 kV to 15 kV; the right board is for the rest.

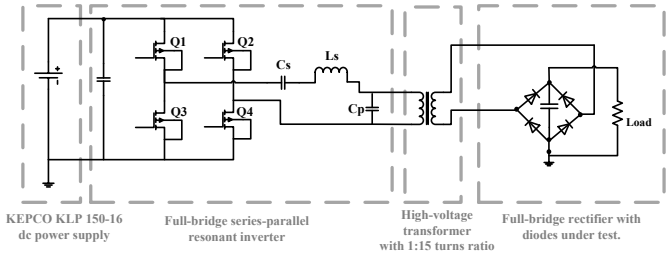


Figure 12: A simplified schematic of the custom-built inverter and transformer to drive the diodes under test. The specifications of the inverter, the transformer and the load are listed in Table I.

Table I: Specifications of the custom-built inverter, transformer and load. The values marked with asterisk are for a specific operating point (the switching frequency is 1 MHz, the input voltage to the inverter is 40 V, the output voltage of the rectifier is 1.5 kV and the average output current is 30 mA). For each test in Table II, C_s, L_s, load resistor and output capacitor are tuned such that the resonant tank will provide the appropriate gain and frequency, the load will draw appropriate power and the output capacitor will ensure the output ripple voltage stays within 5 % of the output voltage.

Section	Component		Part Number or Value
Inverter	MOSFETs		GS66504B
	Series capacitor C_s		9.9 nF*, TDK C3216C0G Series
	Parallel capacitor C_p		∼5 nF, parasitic capacitance of the transformer and diodes reflected to the primary side
	Inductor	Core size	RM14
		Material	TDK N49
		Windings	MWS AWG 14 (150/36)
		Value	13.4 uH*
Transformer		Core size	ETD49
		Material	Ferroxcube 3F35
		Primary	MWS AWG 14 (150/36)
		Secondary	Teledyne Reynolds 18 kV FEP wire
		Bobbin	ABS 3D print
		Turns	10:150 turns
Load	Resistor		Series and parallel 100 Ω to 100 000 Ω resistors, Ohmite B20 series (20 W) or Vishay Dale RS series (10 W)
	Output capacitor for V_o <=2 kV		One or more 15 nF 3 kV X7R capacitors, AVX 2225HC153KAT1A
	Output capacitor for V_o >2 kV		One of more 1 nF 12 kV ZM capacitor, Murata DHR4E4B102K2BB

E6 hand-held thermal camera placed at a fixed distance away from the PCB board.

All the test conditions are listed in Table. II. The error of the temperature measurement is calculated as the maximum between ±2 °C and ±2% of the temperature reading.

B. Loss characterization

For diodes with a maximum temperature rise lower than 80 °C in the 600 kHz and 1 MHz tests (short for ac tests), we conduct a separate dc test: drive the same full-bridge rectifier with a dc source at various voltages and currents. We record the maximum temperature rise in each test after the rectifier reaches thermal equilibrium. A mapping between maximum temperature rise and power loss can be generated based on these tests. Then we back calculate the diode losses in ac tests by interpolating this temperature-loss map. In Fig. 10, we show the maximum temperature rise of selected single diodes (same data as in Fig. 1a), and the loss corresponding to the maximum temperature rise.

APPENDIX B
CLOSED-FORM ANALYTICAL SOLUTION OF THE DIODE VOLTAGES

We start with the charge equation at each node in Fig. 3a.

$$q_{n+1} = q_n + C_P v_n, ..., q_2 = q_1 + C_P v_1, q_1 = C_D v_1$$

Then we substitute q_i in the function of q_{i+1}'s function,

Table II: Specifications of diodes under tests and conditions of tests in Fig. 1a and Fig. 1b. Even though the resonant tank was re-tuned for tests across frequencies, the conditions of tests were kept approximately the same. All data is updated in September 2019.
∗ These tests did not reach thermal equilibrium and were cut off after the temperature became too high (cut off time varies between 30 to 90 seconds).
◇ Through-hole diodes. In all the tests in Section II, the leads of these diodes were cut to $<3\,\mathrm{mm}$ and soldered on one of the PCBs shown in Fig. 11.
• Most high voltage diodes ($>= 5kV$) have unconventional packages. Here "diode body length (mm)" × "diode body width (mm)" is listed.
§ The names of following manufacturers are abbreviated: Taiwan is Taiwan Semiconductor, Dean is Dean Technology, VMI is Voltage Multiplier Inc.
†† For most Si diodes under tests, datasheets do not provide the temperature information of the "Forward Current".
† These reverse recovery times are defined as "Switching Time" in the corresponding datasheets.

Manufacturer PN	Manufacturer§	Type	Nominal voltage (V)	Forward current†† (mA)	Reverse recovery (ns)	Capacitance @1 V (pF)	Package	Number of diodes in series	Average output voltage (V)	Average output current (mA)
CSD01060E	Wolfspeed	SiC Schottky	600	1000 (T_c ∼158 °C)	∼0	80(@0 V)	TO-252-2	1	298	197.3
								2	598	200.3
								4	1200	187
C3D1P7060Q	Infineon		600	1700 (T_c ∼150 °C)	∼0	82.5(@0 V)	PowerQFN 3.3 × 3.3	1	301	198
								2	597	198.7
								4	1200	187
GB01SLT06	GeneSiC		650	1000 (T_c ∼150 °C)	20†	76	DO-214AA	1	298	197.5
								2	599	199.1
								4	1190	186.3
IDL02G65C5	Infineon		650	2000 (T_c ∼ 150 °C)	∼0	70	ThinPak 8 × 8	1	300	199.5
GB01SLT12	GeneSiC		1200	1000 (T_c ∼160 °C)	10†	71	DO-214	1	599	198.4
								2	1190	190.9
IDM02G120C5	Infineon		1200	2000 (T_c ∼170 °C)	∼0	182	TO-252-2	1	598	197.5
								2	1200	186.7
STPSC5H12B	ST		1200	5000 (T_c ∼ 150 °C)	∼0	450	DPAK	1	597	197.8
GAP3SLT33	GeneSiC		3300	300 (T_c ∼125 °C)	10†	38	DO-214	1	1490	29.7
								2	3000	29.8
CD214A-F1400	Bourns Inc.	Si	400	1000	25	17	DO-214AC	1	199	197.5
								2	401	198.4
								4	801	190
ESH1GM	Taiwan		400	1000	25	3(@4 V)	Micro SMA	1	201	201
UF1GLW	Taiwan		400	1000	20	25(@4 V)	SOD-123W	1	205	202.7
								2	400	202.2
								4	800	189
UF4004	ViSHAY		400	1000	50	17	DO-41 ◇	1	200	198
BYV26B	ViSHAY		400	1000	30	25	SOD-57◇	1	203	199.8
								2	400	202.5
RFU02VSM6S	ROHM		600	200	35	3	TUMD2SM	1	301	39.9
BYV26C	ViSHAY		600	1000	30	25	SOD-57 ◇	1	298	196
ESH1JM	Taiwan		600	1000	25	3(@4 V)	Micro SMA	1	301	200
UF1JLW	Taiwan		600	1000	25	15(@4 V)	SOD-123W	1	299	201
MUR160S	Taiwan		600	1000	50	50	DO-214AA	1*	298*	207*
ES1JL	Taiwan		600	1000	35	9.6	Sub SMA	1*	299*	197*
CD1408-FU1800	Bourns Inc		800	1000	35	16	1408	1*	300*	150*
RFU02VSM8S	ROHM		800	200	35	3	TUMD2SM	1	407	40
S1MLS	Taiwan		1000	1200	-	10	SOD-123HE	1*	500*	13*
ACGRAT105L-HF	Comchip		1000	1000	-	12	2010	1*	500*	5.6*
HS1M	Taiwan		1000	1000	75	18	DO-214AC	1*	400*	160*
ACURA107-HF	Comchip		1000	1000	75	18	DO-214AC	1*	400*	190*
UA1M	SMC Diode		1000	1000	75	-	DO-214AC	1*	400*	40*
FM2000GP	MCC		2000	500	500	30(@4 V)	DO-214AC	1*	800*	70*
SM3F	Dean		3000	350	65	6(@4 V)	SMA J-Lead	1*	1500*	80*
X50FF3	VMI		5000	75	30	3	6.6 × 4.3 ◇•	1*	2500*	17*
SP5LFG	Dean		5000	140	50	7.2(@0 V)	8.6 × 2.8 SMT•	1	2500	30
Z50FF3	VMI		5000	180	30	16	8.9 × 5.5 ◇•	1*	2500*	36*
HV200UF5	Dean		5000	200	50	12(@0 V)	9 × 5 ◇•	1*	2500*	42*
Z50FF3LL	VMI		5000	400	50	18	10 × 5.5 SMT•	1*	2500*	60*
HVEF8P	Dean		8000	30	20	0.33(@0 V)	6.6 × 2.5 ◇•	1	3990	5.35
UX-FBR8	Dean		8000	420	40	7.5(@0 V)	9 × 5 ◇•	1*	4000*	40*
SLU08M	Dean		8000	400	40	7.5(@0 V)	14 × 3.8 SMT•	1*	4000*	50*
X150FF3	VMI		15000	25	30	1.2	9.1 × 4.3 ◇•	1*	5000*	3.5*

$$\begin{aligned} q_{n+1} &= q_n + C_P v_n \\ &= q_{n-1} + C_P v_{n-1} + C_P v_n = ... \\ &= q_1 + C_P(v_n + v_{n-1} + ... + v_1) \end{aligned}$$

Combine with

$$q_{n+1} = C_D(v_{n+1} - v_n)$$

We can solve for v_{n+1}

$$v_{n+1} = v_n + v_1 + \frac{C_P}{C_D}\sum_1^n v_i$$

Rearrange the equation, v_{n+1} is a function of v_n and v_{n-1},

$$v_{n+1} = v_n + (-v_{n-1} + v_{n-1}) + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i + \frac{C_P}{C_D}v_n$$
$$= v_n - v_{n-1} + (v_{n-1} + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i) + \frac{C_P}{C_D}v_n$$
$$= v_n - v_{n-1} + v_n + \frac{C_P}{C_D}v_n = (\frac{C_P}{C_D} + 2)v_n - v_{n-1}$$

We can find the closed-form solution of this series by solving the equation

$$x^2 = (\frac{C_P}{C_D} + 2)x - 1$$

Denote $a = \frac{C_P}{C_D}$, the roots to $x^2 - (a+2)x + 1 = 0$ are

$$x_1 = \frac{a + 2 + \sqrt{a(a+4)}}{2}, x_2 = \frac{a + 2 - \sqrt{a(a+4)}}{2}$$

Thus v_n is in the format

$$v_n = c_1 x_1^n + c_2 x_2^n$$

Where c_1 and c_2 are constants. The voltage drop across the nth diode is then

$$v_{Dn} = v_n - v_{n-1} = c_1 x_1^{n-1}(x_1 - 1) + c_2 x_2^{n-1}(x_2 - 1)$$

We can solve for c_1 and c_2 by using the initial condition $v_{D1} = v_1$ and get the closed-form analytical solution in (1).

APPENDIX C
SIMULATE THE CAPACITANCE MATRIX OF A PCB LAYOUT AND CALCULATE THE COMPENSATION CAPACITANCES

A. Simulate and simplify the capacitance matrix of a PCB

First, we export the PCB layout of the rectifier from Altium Designer to a .STEP file; then we import the .STEP file to FreeCAD, use a plug-in script provided by Fast Field Solver to process this geometry and save it as a net list file; lastly, we import the netlist file in the Fast Field Solver to solve for the capacitance between each two nodes in the geometry, as shown in Fig. 13.

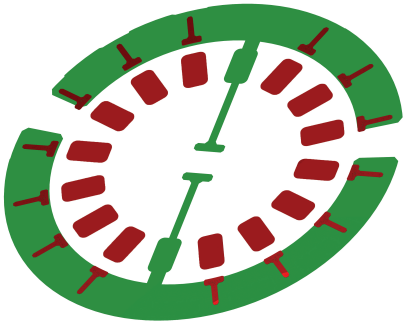


Figure 13: The copper layout of the full-bridge rectifier. In the Fast Field Solver [26], one can define a group of conductors (traces, pads, via, etc) as one node. In this geometry, ground node and V_o node are in green; rest of the nodes are in red. The square-shape pads are nodes connecting two diodes and the T-shape pads are nodes connecting to the probe adapters.

The simulated capacitance matrix is shown in Fig. 14. We ignore the capacitance to ground from pads far away from the ground node (same for the V_o node). We further ignore the capacitances in green since they are very small, then combine the capacitances at each node, we get the simplified parasitic capacitances as shown in blue in Fig. 15.

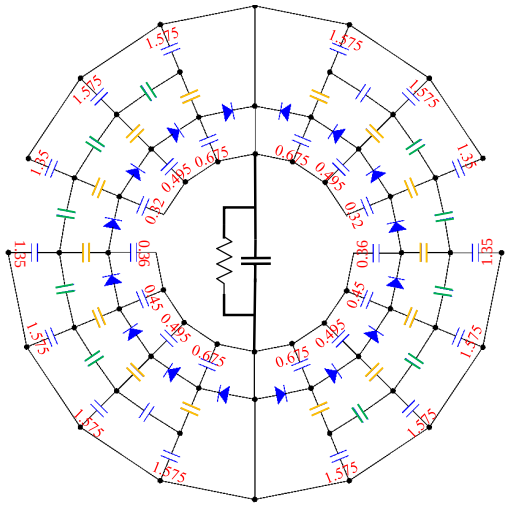


Figure 14: The simulated capacitance matrix of the PCB layout in Fig. 13. All capacitances to common (GND or V_o) are in red and in pF. The capacitors in green are between two probe pads and are 0.002 pF; the capacitors in yellow are between each diode pad and probe pad and are 0.045 pF

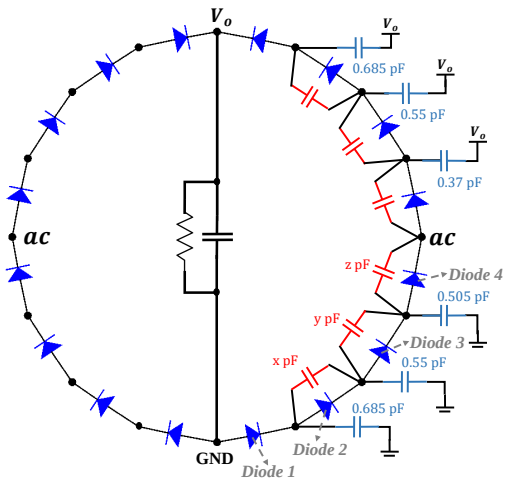


Figure 15: The estimated parasitic capacitance of each node to common (in blue); the capacitances are symmetric across the V_o-GND axis. The required compensation capacitors are marked in red.

B. Calculate the compensation capacitances in the general case where parasitic capacitances are not equal

Figure 16 shows a similar diagram to that of Fig. 4b. The only difference is that the parasitic capacitances from each node to common C_{p_n} have different values.

We split C_{p_i} into i capacitors in series, with the value of each as iC_{p_i} (for example, capacitor C_{p_2} is split into two capacitors each of value $2C_{p_2}$ connected in series and C_{p_n} is split into n capacitors each of value nC_{p_2} connected in series). We assume after compensation, $v_{D_1} = v_{D_2} = ... = v_{D_M}$, therefore the nodes on each dot-dash line in Fig. 16 are at the same voltage potential, thus are virtually connected.

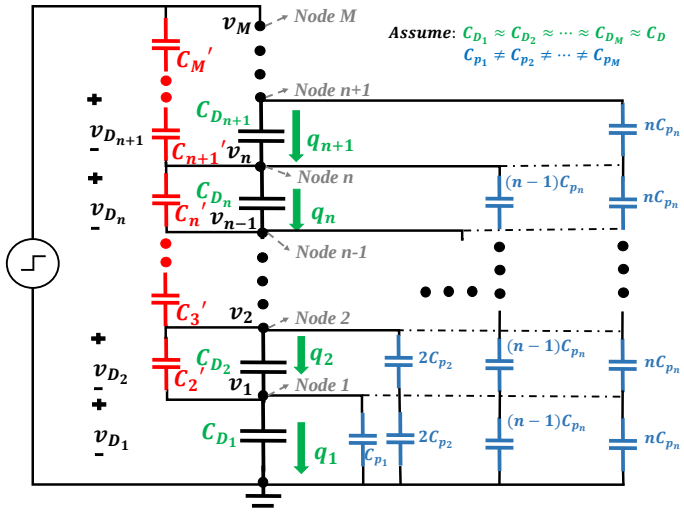


Figure 16: Schematic for calculation of compensation capacitances for the decoupled method in the general case where parasitic capacitances from each node to common are not equal.

To ensure $v_{D_2} = v_{D_1}$, we need

$$C_2' = C_{p_1}$$

To ensure $v_{D_3} = v_{D_2}$, we need

$$C_3' = C_{p_1} + 2C_{p_2}$$

Following the trend, to ensure $v_{D_n} = v_{D_{n-1}}$, we have

$$C_n' = C_{p_1} + 2C_{p_2} + ... + (n-1)C_{p_{n-1}}$$

The compensation capacitances for the independent compensation method in the general case can be calculated in a similar fashion.

As an example, the capacitances x, y, z in Fig. 15 are calculated as follows:

$$x = 0.685pF$$
$$y = 0.685 + 2 \times 0.55 = 1.785pF$$
$$z = 0.685 + 2 \times 0.55 + 3 \times 0.505 = 3.3pF$$

As mentioned in Section V, capacitances x, y and z are implemented with discrete capacitors with values of 0.5 pF, 1.5 pF and 3 pF respectively.

The accuracy when using the proposed compensation methods in practical applications can be affected by: 1) the accuracy of the simplified diode model in Section III and IV (it does not include non-ideality of diodes, such as voltage dependency of C_D, the leakage current and its temperature dependency, etc; 2) the accuracy of the simulated capacitance matrix of the PCB (include the tolerance of the FEA simulation process, the accuracy of the assumed dielectric constant of the PCB core, manufacture tolerances of the PCB board, etc); 3) the implementation of the compensation capacitances (availability of discrete capacitors, tolerance, voltage dependency of capacitors, etc). Note that as regards diode and compensation capacitor nonlinearity, it is typically possible to establish equivalent capacitance values for devices and capacitors (e.g., as done in [28]) that enable the methods developed here to be applied even when such nonlinearities are significant.

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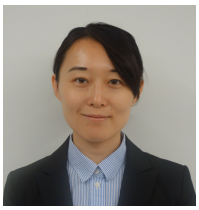

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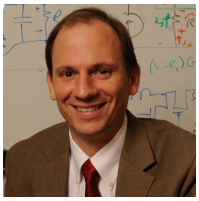

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