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Tunable Matching Networks based on Phase-Switched Impedance Modulation[1]

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***Abstract*—The ability to provide accurate, rapid and dynamically-controlled impedance matching offers significant advantages to a wide range of present and emerging radio-frequency (RF) power applications. This work develops a new type of tunable matching network (TMN) that enables a combination of much faster and more accurate impedance matching than is available with conventional techniques, and is suitable for use at high power levels. This implementation is based on a narrow-band technique, termed here *phase-switched impedance modulation* (PSIM), which entails the switching of passive elements at the RF operating frequency, effectively modulating their impedances. The proposed approach provides absorption of device parasitics and zero-voltage switching (ZVS) of the active devices, and we introduce control techniques that enable ZVS operation to be maintained across operating conditions. A prototype PSIM-based TMN is developed that provides a 50 Ohm match over a load impedance range suitable for inductively-coupled plasma processes. The prototype TMN operates at frequencies centered around 13.56 MHz at input RF power levels of up to 200 W. Keywords—tunable matching network, antenna tuning unit, impedance matching, switched capacitor, impedance modulation, phase-switching.**

I. Introduction

Dynamic component tuning and impedance matching have application to a diverse range of radio-frequency (RF) power applications, including software-defined radios [1], frequency-agile and adaptive RF transmitters and receivers [2], [3], new types of highly-efficient RF power amplifiers [4], plasma drivers [17], generators [5], [6], wireless power transfer [7, 19, 20], power converters [14] and many other industrial processes. Electronically-controlled tunable impedance matching networks (TMNs) in particular can be valuable in many RF applications. Such TMNs (e.g., [15]) – also known as "Antenna Tuning Units", or ATUs – typically match a variable load impedance to a desired input impedance (e.g., 50 Ohms) at an RF operating frequency, though other functions are possible.

For high-frequency (HF) and very-high-frequency (VHF) applications (e.g., 3-300 MHz), a TMN is typically implemented as an ideally-lossless, lumped-element reactive network, where some of its reactive elements are realized as variable (tunable) components. That is, the impedance of the tunable components at a particular frequency, or over a range of frequencies, can be controlled externally to dynamically match the load impedance to a desired input impedance. Based on the technology employed for realizing the variable reactance elements, conventional TMNs can be classified as either analog (continuously adjustable) or digital (adjustable among a set of discrete values). (Here we characterize the tuning mechanism itself, neglecting the fine-scale discretization that may be imposed by the control system.) The former group of TMNs relies on variable reactance elements whose impedance can be tuned in an (ideally) continuous manner. For instance, conventional high-power RF plasma drives often employ TMNs based on mechanically adjusting physical passive components, such as by using stepper-motor-adjusted variable-vacuum capacitors [18]. While widespread, this technique is extraordinarily slow. Faster response can be obtained by appropriately adjusting bias conditions of electronic components such as varactors [8] or MEMS-varactors [9]. Nevertheless, power handling with such components is somewhat limited by the relatively high bias voltages required when operating at high power levels [10].

In digital TMNs, on the other hand, tunability is achieved by implementing the variable reactive elements as digitally-switched arrays, thus allowing adjustment of the impedance of the variable reactances in discrete steps. The realization of digital TMNs is typically based on CMOS switches [13], MEMS switches [11], PIN diodes [12] or discrete power transistors. MEMS switches are characterized with very low on-state resistance and can operate at rf frequencies up to tens of GHz with negligible power consumption. The reliability of MEMS switch-based TMNs, however, is still an issue due to the large control voltages required by MEMS switches. On the other hand, PIN diode and CMOS switch-based TMN realizations offer the capability to handle very high power levels at the expense of some power loss in the switches due to their on-state resistance. Such TMN realizations are particularly favorable for on-die integration and find wide applicability in software-defined radio (SDR) IC modules and other on-chip TMNs. The main drawback of digital TMNs, however, is their limited tuning resolution, and hence, the accuracy with which impedance matching can be achieved with an acceptable number of switched components. In some high power applications where accurate impedance matching is required over a very wide

[1] This paper is an extension to the authors' conference paper entitled "Tunable impedance matching networks based on phase-switched impedance modulation", *IEEE Energy Conversion Congress and Exposition*, 2017. It offers in-depth discussion of the operation and design of PSIM-based TMN networks, presents additional implementation details and provides extensive prototype performance results.

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impedance range, such as RF plasma drivers, for example, the use of digital TMNs may be impractical due to the large number of digital switches needed to achieve the required fine tuning resolution. For instance, conventional high-power RF plasma drivers often still employ TMNs based on stepper-motor-adjusted continuously-variable capacitors as a result of the requirements for accurate impedance matching and operation over very wide impedance ranges.

The limitations of existing techniques motivates improvement of the capabilities of TMNs to provide more accurate and faster impedance matching (higher tuning bandwidth) over wider impedance ranges while simultaneously allowing operation at high power levels with minimum insertion loss. This is the goal of the new approach developed here, which expands upon the authors' conference paper [21]. Section II introduces the concept of phase-switched impedance modulation. Sections III, IV and V describe implementation and control techniques for a PSIM-based tunable matching network and present the design of a prototype system operating at frequencies centered at 13.56 MHz. Section VI examines the performance of the prototype PSIM-based matching system, and Section VII concludes the paper.

II. PHASE-SWITCHED IMPEDANCE MODULATION

A. The Concept

Phase-switched TMNs are a class of tunable matching network which achieve tunability by incorporating one or more phase-switched variable reactances. A phase-switched variable reactances modulates the effective impedance of a switched reactive element (capacitor, inductor, or some combination of both) by switching the connection of the element at the RF frequency. In essence, it is a narrow-band technique for controlling the effective impedance seen looking into the terminals of a reactive element at the frequency at which this element is switched (e.g., with a shunt or a series switch) by appropriately adjusting the phase and/or duty-cycle of the switch. The use of switched reactive elements was exploited in [14] in the different context of controlling resonant dc-dc converters by modulating their effective tank network resonant frequency, in [16] to tune the resonant frequency of a wireless power transfer receiver to a fixed transmitter frequency, and in [20] to tune the tank network resonant frequency of a wireless power transmitter. However, it has not previously been applied to the notion of tunable matching networks for dynamic impedance matching.

To illustrate the notion of a phase-switched variable reactance, consider the parallel combination of a capacitor C_0 and an ideal switch being driven with a purely sinusoidal current source (see Fig. 1).

The switch state is controlled by the signal q; the switch is on or off when q is high or low respectively. If q is zero all the time, i.e. the switch is permanently turned off, then the effective capacitance C_{EFF} seen looking into the network is equivalent to the physical capacitance C_0. On the other hand, if the switch is always on, then the capacitor C_0 is effectively shorted, and the network behaves as an infinite capacitor in the sense that the voltage across it remains zero irrespective of its terminal current (at the drive frequency). Thus it makes sense to conclude that one ought to be able to control the effective capacitance C_{EFF} of the switched capacitor anywhere from C_0 to infinity by controlling the conduction angle of the switch from 0 to 2π with proper phase.

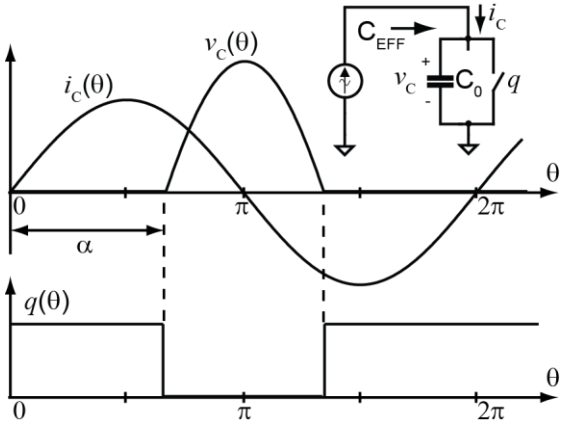

Fig. 1: Schematic illustrating the implementation of a phase-switched variable capacitance and its current and voltage waveforms. The effective capacitance C_{EFF} at the switching frequency can be modulated by controlling the conduction angle of the switch which is related to α.

Suppose that the switch is turned off every cycle of the current waveform α radians after the current transitions from negative to positive, and it is turned back on after the capacitor voltage rings down to zero. The source current i_C, capacitor voltage v_C and switch control signal q for this scenario are shown in Fig. 1 as a function of the cycle angle θ. Thus, the switch is turned off α radians after the current through it becomes positive, and is turned back on when the net charge delivered into the capacitor returns to zero. Note that turning the switch on after the capacitor voltage rings down to zero ensures zero-voltage-switching (ZVS) turn on of the switch. Likewise, the switch turns off under ZVS owing to the capacitor C_0 in parallel with the switch, and C_0 naturally absorbs the parasitic switch capacitance. Each of these traits is valuable for efficient operation at high frequencies.

As can be inferred from Fig. 1, by adjusting α, i.e. setting how far into the cycle the switch turns off, one can control the conduction angle of the switch and the peak capacitor voltage. It is clear from Fig. 1 that for a purely sinusoidal current source the conduction angle of the switch is given by 2α. Performing a Fourier analysis on the capacitor voltage (under sinusoidal current drive) reveals that its fundamental component lags the current by 90° for any switch conduction angle, suggesting that the switched capacitor network does indeed behave effectively as a variable capacitor at the switching frequency. Consequently, by analyzing the relationship between the switch conduction angle and the magnitude of the fundamental component of $v_C(\theta)$, it can be shown that the effective capacitance of the switched capacitor as a function of α is given by (1) [14].

$$C_{EFF} = \frac{\pi}{\pi - \alpha + \sin(\alpha)\cos(\alpha)} C_0 \qquad (1)$$

Indeed (1) is consistent with the intuitive expectation for infinite effective capacitance when the switch is always on ($\alpha = \pi$) and predicts the equivalence between C_{EFF} and C_0 when

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the switch is permanently off ($\alpha = 0$). Fig. 2 plots the normalized effective capacitance C_{EFF}/C_0 of the switched-capacitor network of Fig. 1 at the switching frequency. (Here we refer to C_{EFF}/C_0 as the *effective modulation factor*.) As can be seen, C_{EFF} does indeed increase rapidly with α and approaches infinity with α approaching π (corresponding to a switch conduction angle of 2π).

The precision with which effective capacitance can be adjusted depends upon the resolution with which the switch conduction angle can be controlled. Although theoretically one can conclude that the effective capacitance can be modulated continuously over an infinite range, from a practical perspective, the range over which C_{EFF} can be modulated depends on the amount of harmonic distortion one is able to tolerate in the network.

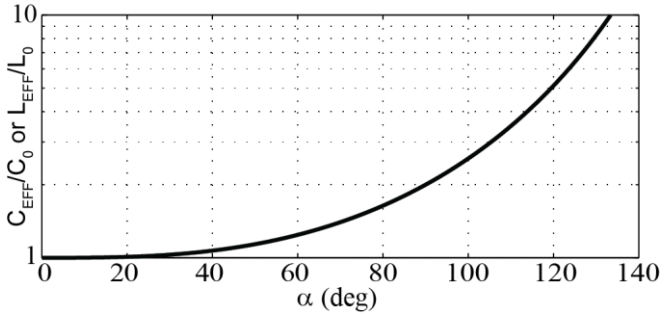

Fig. 2: Normalized effective capacitance C_{EFF} of the switched capacitor network at the switching frequency versus α for a purely sinusoidal current excitation.

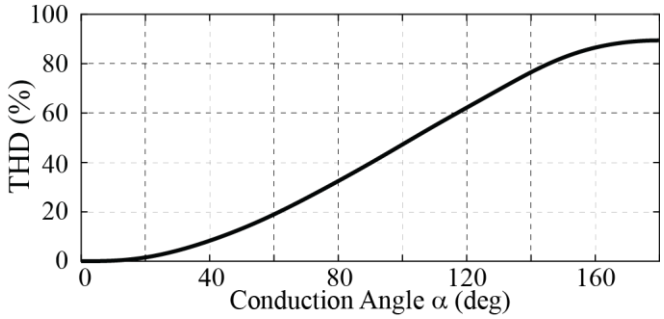

Fig. 3: Total harmonic distortion of the voltage waveform v_C for the ideal PSIM element of Fig. 1 versus the switch conduction angle α.

As α increases towards π, the conduction angle (given by 2α for a purely-sinusoidal current excitation) of the switch increases, and hence the ringing of the capacitor voltage v_C (see Fig. 1) is limited to a shorter period. As Fig. 3 depicts, this results in significant harmonic content of the capacitor voltage for large C_{EFF}/C_0 ratios. The total harmonic distortion *THD* plotted in Fig. 3 is defined here as the ratio of the rms of all harmonics of v_C to the total rms of the waveform[2]. Note that as Fig. 3 suggests, the *THD* of v_C saturates at approximately 90% as the conduction angle increases. Indeed, this can be shown to be the case and can be understood by considering Fig. 1: taking the limit of α as it approaches 180°, the peak of v_C, the magnitude of its fundamental and all of its harmonics tend to zero at a comparable rate. This is also illustrated in Fig. 4 showing the magnitude of the first five harmonics of v_C relative to that of the fundamental as α increases to 180°.

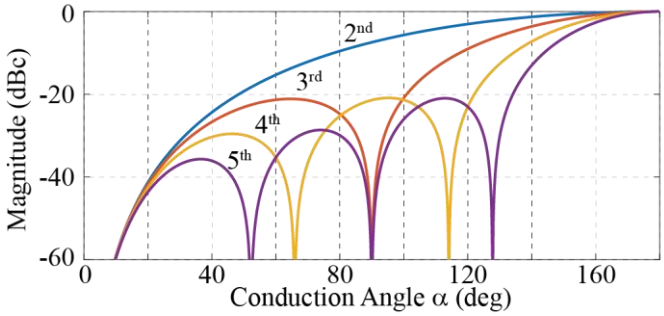

Fig. 4: Magnitude of the harmonic components relative to that of the fundamental of the voltage waveform v_C for the ideal PSIM element of Fig. 1 versus the switch conduction angle α.

The amount of harmonic distortion one can tolerate is highly dependent on the limit of harmonic content that is allowed into the source and/or load. It is, however, important to distinguish between the harmonic distortion of the capacitor voltage of the switched network of Fig. 1 and the harmonic content that is actually injected into the source/load of the RF system. The switched network of Fig. 1 serves as a fundamental building block in the design of PSIM TMNs for RF systems. TMN designs often naturally provide a degree of harmonic filtering; if necessary, additional filtering can be incorporated into these systems to further reduce injected harmonic content into the source and/or load.

It is important to note that the derivation of (1) and the PSIM analysis presented in this section assume a purely sinusoidal current excitation of the switched capacitor network of Fig. 1. In reality, this may not be the case; harmonic content in i_C can cause the relationship between C_{EFF}, C_0 and α to differ from the one expressed by (1). Nevertheless, if this relationship remains monotonic with α, an external feedback controller can be employed to appropriately adjust α based on some overall system performance metric (e.g. impedance measurements as we demonstrate in section VI). In the TMN design presented here, we aim to maintain the harmonic content of i_C to be less than -10 dBc. (For the system implementation described in section III, this roughly corresponds to a 0° - 110° range for α, or 4x in effective capacitance modulation.)

B. Practical Implications

One possible realization of the PSIM element of Fig. 1 comprising an N-channel device in parallel with some external capacitance C_0 is shown in Fig. 5A. Such an implementation is particularly suitable for RF applications as it allows one to absorb the parasitic capacitance of the device into C_0 while maintaining zero-voltage switching (ZVS) of the device and thus minimizing voltage-current overlap losses.

Furthermore, the unipolar voltage-blocking characteristic of device due to the intrinsic body-diode (or the ability of the

[2] In this work, total harmonic distortion (*THD*) of a voltage waveform is defined as $THD = \sqrt{\sum_{n=2}^{\infty} V_n^2} / \sqrt{\sum_{n=1}^{\infty} V_n^2}$, where V_n is the magnitude of the n[th] harmonic of the waveform. According to this definition, the maximum possible *THD* that can be attained is 100 % and corresponds the case when the entire energy of the waveform is contained in its harmonics, i.e. $V_1 = 0$.

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device to turn-on in reverse in the case of GaN devices) somewhat simplifies the control and synchronization of the device by providing a certain *safety margin* in achieving ZVS.

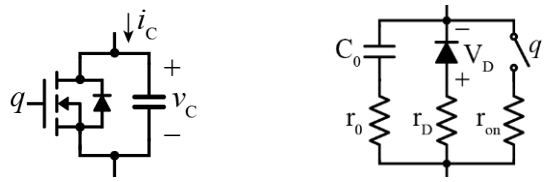

Fig. 5: Implementation of a PSIM element with an N-channel FET (A), and equivalent circuit model (B), where r_0 is the ESR of the total base capacitance C_0, r_{on} is the on-resistance of the FET, and r_D and V_D are the on-resistance and forward voltage drop of the body diode, respectively.

To better understand this, consider Fig. 6 illustrating the three possible operating modes of the PSIM element from Fig. 5A depending on the synchronization of the device gate-drive signal q with respect to the PSIM current i_C. Here we assume sinusoidal current excitation, i.e. $i_C = I_0 \sin(\omega t)$, and we denote the intervals of forward and reverse device conduction during which the device is commanded on (q is high) with w_F and w_R respectively. In the case of Fig. 6A, the device is commanded on for equal intervals of forward and reverse conduction ($w_F = w_R$) thus achieving *ideal* ZVS operation without engaging the body-diode. This operating mode is also depicted in Fig. 1 and is the basis for the derivation of the PSIM effective capacitance relation (1).

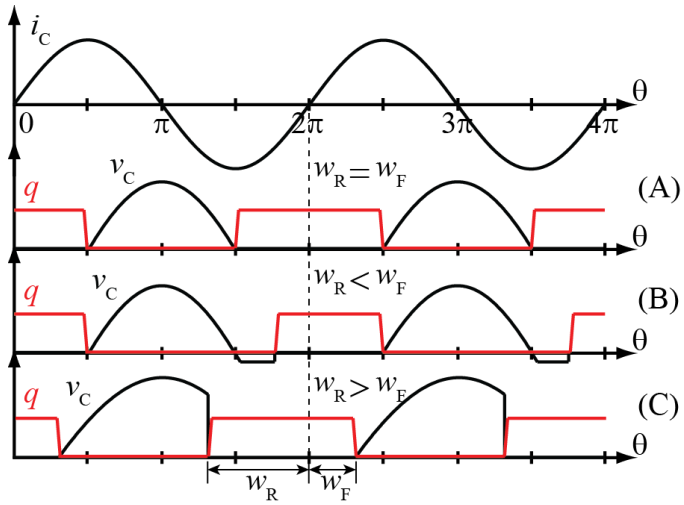

Fig. 6: Switching waveforms for the PSIM element of Fig. 5 under a sinusoidal current excitation i_C for (A) ideal zero-voltage switching, (B) partial body-diode conduction (or reverse device turn-on), and (C) operation with loss of zero-voltage switching, i.e. hard-switching. w_R and w_F denote the width of the forward and reverse conduction intervals, respectively, during which the device is commanded on, i.e. q is high.

Even though ideal ZVS is the most efficient and often desired PSIM operating mode, as we later show in Section III.B, this mode may be challenging to achieve under all conditions as it requires very accurate synchronization between q and i_C. An alternative practically-viable operating mode for the PSIM is shown in Fig. 6B in which $w_F > w_R$; we refer to this mode as *quasi*-ZVS in the sense that the capacitor voltage v_C rings down to near zero volts, although in this case, the intrinsic body-diode engages for a portion of the reverse conduction period of the switch. It is the power losses due to the conduction of the body-diode that renders *quasi*-ZVS as a more lossy alternative to ideal ZVS. Note that (1) can also be used in the case of Fig. 6B as a reasonable approximation to the effective PSIM capacitance, provided that the peak of v_C is much larger than the forward voltage drop of the body-diode, which is often the case in practical applications. For both Fig. 6A and Fig. 6B the forward conduction angle α in (1) is equivalent to w_F.

Finally, Fig. 6C illustrates the case of $w_R > w_F$ resulting in hard switching of the device and large switching losses; hence this operating mode is typically avoided. It is interesting to note from Fig. 6 that all three cases achieve the same total device conduction angle, although in each case, the total pulse width $w_R + w_F$ and phase of q are different. In fact, there are infinite many combinations of pulse width and phase of q that will achieve a given switch conduction angle and the desired effective capacitance. Nevertheless, to minimize losses in the PSIM element, it is best to operate as close to ideal ZVS as possible while avoiding hard switching of the device.

There are many other practical design considerations to be addressed in realizing a PSIM capacitor. Among these are the power loss in the PSIM switch (e.g., owing to conduction loss in the device), the peak off-state of the device voltage vs. operating condition, the average voltage appearing across the device during operation, and the impact of device capacitance nonlinearity. We discuss each of these considerations in the Appendix, with detail provided in [24].

C. Alternative PSIM Implementations

For the discussion above we have assumed that the switched capacitor network of Fig. 2 is half-wave switched, i.e. the switch is operated in such a way so that the capacitor voltage waveform is unipolar (see Fig. 1). This may often be preferable in RF systems based on the PSIM element implementation of Fig. 5A since typical power transistors can only block a unipolar voltage. However, it is interesting to note that other switching schemes such as full-wave switching [14] are also possible. In the case of full-wave switching, the switch is turned off twice every cycle, with the off periods being centered around the instants when the current $i_C(\theta)$ is zero. For a purely sinusoidal excitation of the network, this results in a bipolar capacitor voltage waveform with zero dc average. Full-wave switched networks inherently result in reduced harmonic content of the capacitor voltage compared to half-wave switched networks for the same α. On the other hand, implementing full-wave switching may be practically harder to realize and less beneficial for high frequency RF applications, since in that case the switch has to operate at twice the operating frequency and bidirectional blocking switches are required.

PSIM implementation based on the switched capacitor network of Fig. 1 is particularly well suited for RF applications as the parasitic switch device capacitance can be absorbed into the shunt capacitor C_0. Nevertheless, there exist other possibilities for implementing phase-switched impedance modulation. For instance, by analogy to the switched capacitor network, it is also possible to construct a switched inductor network (comprising a series combination of a switch and an inductor) that allows continuous control of its effective

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inductance (at the switching frequency). Such a switched inductor network corresponds to the topological dual of the switched capacitor network of Fig. 1 with the current through the inductor being analogous to the voltage across the switched capacitor (see Fig. 1) – a result that follows from the properties of topological duality. Of course, in the case of the switched inductor network, care must be taken to turn the switch off only when the current through the inductor drops to zero; this necessitates accurate switch control which may be hard to achieve in RF applications. Moreover, one does not realize zero-voltage switching in this case, but zero current switching.

The switched capacitor and inductor networks serve as fundamental building blocks for implementing phase-switched impedance modulation. These two basic networks are only able to provide strictly capacitive or inductive variable reactances (but not both). Nevertheless, some applications could benefit substantially from variable reactances whose value can be controlled over a range spanning both capacitive and inductive reactances, and/or by modulating the effective reactance over a more limited range. For instance, in the design of tunable impedance matching networks, it is sometimes required for the tunable reactive elements to be able to achieve both capacitive and inductive values. In such cases, one can further augment the two basic capacitor and inductor switched networks with additional reactive components to allow impedance modulation over a range that includes both capacitive and inductive impedances. Several such networks are described in [24] and [25], although many other network variants are also possible. In this work, however, we focus on the switched-capacitor implementation of Fig. 1; in-depth exploration of the advantages and disadvantages of alternative PSIM element implementations is the subject of future work.

III. TUNABLE IMPEDANCE MATCHING NETWORK DESIGN

To demonstrate the effectiveness of phase-switched impedance modulation for implementing tunable impedance matching, we have developed a TMN design based on an impedance step-up L-section matching network with electronically-variable effective impedances. Such a network configuration is suitable for plasma drive applications where the driving-point impedance of an RF plasma-excitation coil must often be stepped-up and matched to the output impedance of a power amplifier PA (e.g., see [17] for a plasma matching system at similar power levels). A power amplifier is thus connected at the IN terminal, and the plasma load is connected at the OUT terminal, with the TMN serving to match the variable plasma load impedance to the 50 Ω load desired for the PA. As Fig. 7 shows, this network comprises input and output series resonant tanks along with a single phase-switched capacitor element. The ground-referenced phase-switched capacitor for this design has the advantages described above for high frequency operation, including zero-voltage switching, absorption of device parasitics and simple transistor drive.

It's important to recognize that in order for any TMN to be able to match load impedances that vary independently both in resistance and reactance (i.e. provide an impedance match over a two-dimensional region in the Smith chart), the TMN must comprise at least two reactances that can be tuned quasi-independently. In the case of the TMN of Fig. 7, one of the variable reactances is the shunt capacitance realized with the phase-switched capacitor C_0. While we could implement the second variable reactance using another phase-switched capacitor, here we utilize a different technique. The second variable reactance is implemented using the series-resonant output tank formed by C_2 and L_2: its reactance X is controlled by adjusting the operating frequency over a narrow band about the nominal operating frequency. For instance, when operating at the resonant frequency f_0 of the L_2C_2 tank, the reactance X is effectively zero. Increasing the operating frequency f above f_0 results in an increasing inductive reactance X (X>0), while decreasing f below f_0 causes X to increase capacitively (X<0).

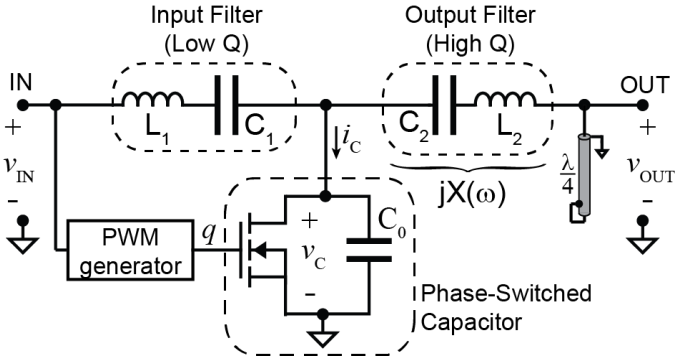

Fig. 7: Network topology of an L-TMN with dynamic-frequency tuning comprising a phase-switched capacitor C_0 and frequency-controlled reactance X. The input filter reactance does not vary considerably with frequency modulation.

Thus the TMN design demonstrated here utilizes frequency modulation as a second control handle for load impedance transformation. Here we refer to this technique as dynamic frequency tuning (DFT). The impedance jX of the output tank is determined by the characteristic impedance of the tank Z_0 and the deviation of the operating frequency f from the tank's resonant frequency f_0 and is given by (2), where $2\pi f_0 = 1/\sqrt{L_2C_2}$ and $Z_0 = \sqrt{L_2/C_2}$.

$$X = Z_0 \frac{f^2 - f_0^2}{f_0 f} \tag{2}$$

As (2) suggests, the range over which the output reactance X is adjustable can be expanded by either choosing L_2 and C_2 to obtain higher tank characteristic impedance, or by allowing for larger amounts of frequency modulation (or both). It can be shown that to achieve a reactance range of $[X_{min}; X_{max}]$ for an operating frequency range of $[f_{min}; f_{max}]$, one must select the resonant frequency and characteristic impedance of the tank according to (3) and (4) which can then be easily solved to obtain L_2 and C_2.

$$f_0 = \sqrt{\frac{(X_{max}f_{min} - X_{min}f_{max})f_{max}f_{min}}{X_{max}f_{max} - X_{min}f_{min}}} \tag{3}$$

$$Z_0 = \frac{f_0(X_{max}f_{max} - X_{min}f_{min})}{f_{max}^2 - f_{min}^2} \tag{4}$$

The amount of frequency modulation allowed is highly dependent on the particular application and may be constrained by radio-frequency emission regulations for the particular

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frequency band of operation. For instance, in the current system design f_{min} and f_{max} are selected to be 12.20 MHz and 14.92 MHz, respectively which corresponds to a ± 5 % variation centered around a 13.56 MHz nominal frequency. This choice of frequency operating range is consistent with the one adopted by many plasma systems in the semiconductor fabrication industry. On the other hand, the choice of Z_0 (or X_{min} and X_{max}) depends on the matching network topology and the load impedance range that one desires to be able to match. As we demonstrate below, to achieve a load impedance matching range similar to the one exhibited by some industrial-grade TMN systems for plasma applications, we select Z_0 = 250 Ω. (This corresponds to X_{min} = -19.7 Ω and X_{max} = 30.4 Ω.) In addition to serving as a frequency-variable tunable reactance, the L_2/C_2 tank also provides filtering, limiting the injection of high-frequency harmonic currents into the output.

Similarly, the input filter comprising L_1 and C_1 is designed to limit the injection of high-frequency harmonic content by the TMN back into the PA. Furthermore, note from Fig. 7 that the current i_C flowing through the phase-switched capacitor is the difference of the input and output filter currents; reducing their harmonic content in turn leads to a PSIM excitation current i_C that is closer to the ideal sinusoid of Fig. 1. Thus, on one hand it is desirable to choose a large input filter characteristic impedance to reduce harmonics, while on the other hand, this also leads to larger variations of its reactance with frequency modulation. (As we demonstrate in the next section, the latter effect may not desirable as it could complicate the synchronization and control of the PSIM switch.) In this design, we select L_1 and C_1 so that the filter is series-resonant at the nominal operating frequency of 13.56 MHz with a characteristic impedance of 100 Ω (smaller than that of the output tank). Based on spice simulation of the design, this corresponds to less than −10 dBc harmonic content in the input filter and phase-switched capacitor currents, and approximately less than ±10 Ω variation in the reactance of the input filter (for up to ±5% frequency modulation).

Note that C_1 and C_2 in the system of Fig. 7 also serve as dc blocking capacitors to provide dc isolation between the drain of the switch and the PA and load respectively. This is an important requirement for this TMN implementation since modulating the conduction angle of the switch imposes a variable dc bias at the transistor drain which could interfere with the internal biasing of the PA and, in some applications, the load characteristics. The shorted quarter-wavelength stub in parallel with the output of the TMN in Fig. 7 serves to provide additional filtering of even harmonic components. It reduces harmonic content injected in the load by presenting a shunt impedance at the TMN's output that is high at odd harmonics and low at even harmonics of the operating frequency. For the design presented here, the impedance of the stub (at the fundamental frequency) is much larger than the load impedance over the entire load and frequency operating range of the TMN. Hence, besides the additional filtering it provides, the quarter-wavelength stub does not impact the control of the TMN, i.e. the choice of frequency and switch conduction angle for matching a load to the PA. Of course, depending on the particular application, one may adopt different output filter designs. For instances, in applications with less stringent output harmonic content requirements, operating the TMN with the L_2/C_2 tank alone may be sufficient. The TMN design presented here is tailored towards driving plasma loads, and for the particular application it is desirable to keep the harmonic content injected in the output to less than -20 dBc.

The L-TMN prototype described here is designed to operate at a nominal frequency of 13.56 MHz in the ISM band with up to ±10% frequency modulation (L_1 = 1.17 μH, C_1, = 117pF, L_2 = 2.97 μH, C_2 = 47.5 pF, C_0 = 270 pF, 50 Ω quarter-wavelength line impedance). The yellow-shaded and the dotted red-line regions in the Smith chart of Fig. 8 illustrate the range of load impedances that this TMN design can successfully match to a 50 Ω source impedance for 5% and 10% frequency modulation respectively. (The frequency modulation percentage is defined here as the ratio of the peak frequency deviation to the nominal operating frequency.) As can be seen from Fig. 8, the range of reactive loads that the TMN can match to 50 Ω increases with the amount of frequency modulation. Such dynamic-frequency tuning techniques are commonly employed in plasma-related applications. Hence, for every particular value of load impedance within the tunable range, there is a unique combination of operating frequency and switch conduction angle α that is required to provide an impedance match between the load and the PA.

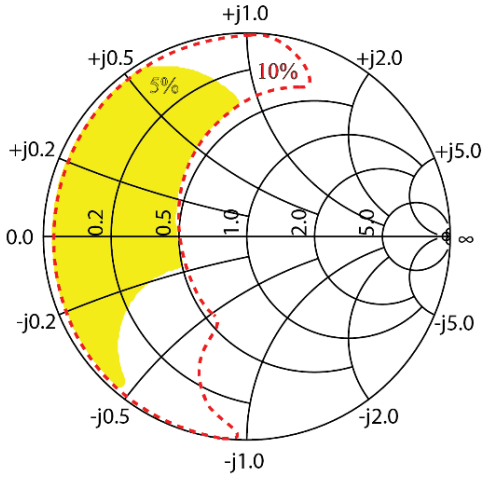

Fig. 8: Typical load impedance range that can be matched to a 50 Ω source with 5 % (yellow) and 10 % (red) frequency modulation for the TMN design of Fig. 7 with L_1 = 1.17 μH, C_1, = 117pF, L_2 = 2.97 μH, C_2 = 47.5 pF, C_0 = 270 pF.

The load impedance ranges shown in Fig. 8 correspond to modulating the effective capacitance of the RF-switched capacitor by up to 4X the value of the base capacitance C_0. (This amount of capacitance modulation roughly corresponds to varying α in Fig. 1 from 0° to 110°.) Further capacitance modulation expands the TMN matching range (at the expense of injecting higher harmonic content into the load and the PA) to include load impedances with lower resistive components. On the other hand, decreasing the base capacitance C_0 (while allowing the same amount of capacitance modulation) results in shifting the TMN matching range towards load impedances with higher resistive components. Note that with the network topology shown in Fig 1, one can conveniently use C_0 to absorb the drain-to-source capacitance of the switch (and in high-frequency implementations, C_0 may comprise only switch capacitance). A TMN with the load impedance matching range

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shown in Fig. 8 is particularly suitable for inductively-coupled plasma (ICP) applications where TMNs are employed to match the drive-point impedance of an RF excitation coil to the output impedance of an RF power amplifier (typically 50 Ω).

Table I lists the switch conduction angle, operating frequency, peak voltage across the switching device and power loss distribution for matching various capacitive and inductive loads to 50 Ω based on a simulation of the TMN design of Fig. 7 with L_1 = 1.17 μH, C_1 = 117pF, L_2 = 2.97 μH, C_2 = 47.5 pF, at approximately 150 W of input power. The quality factors for inductors L_1 and L_2 are assumed to be 900 and 800 respectively, consistent with the actual quality factors achieved in the implementation of the TMN design. The switching device used in the simulation is a 650V GaN transistor (GS66504B, GaN Systems) with its spice model provided by the manufacturer. Note that the base capacitance C_0 (see Fig. 7) in the simulation comprises the drain-to-source capacitance of the switch and 100 pF of external capacitance.

TABLE I. SWITCH CONDUCTION ANGLE, OPERATING FREQUENCY AND POWER LOSS DISTRIBUTION FOR A SIMULATED TMN DESIGN EXAMPLE MATCHING VARIOUS LOAD IMPEDANCES TO A 50 Ω SOURCE IMPEDANCE AT APPROXIMATELY 150 W OF INPUT POWER.

Test Case	Load (Ω)	Conduction Angle (°)	Frequency (MHz)	Drain Voltage ($V_{DS,PK}$)	P_{L1} (W)	P_{L2} (W)	P_{FET} (W)	Power Efficiency (%)
A	19.1 + j32.3	121.5	13.21	262	0.36	2.52	0.73	97.6
B	20.3 + j1.62	141.7	14.04	263	0.36	2.36	1.00	97.5
C	17.9 – j13.6	165.6	14.50	285	0.37	2.63	1.92	96.7
D	9.91 + j24.7	190.8	13.31	300	0.37	4.54	4.01	94.6
E	9.61 – j1.10	198.0	14.00	302	0.37	4.71	3.86	94.0
F	10.0 – j16.3	197.5	14.45	306	0.34	9.46	9.37	94.0
G	5.40 + j31.6	217.7	13.02	336	0.37	7.80	6.45	89.9
H	3.97 + j0.98	226.2	13.79	348	0.36	10.2	9.82	86.0
K	5.33 – j11.8	218.2	14.18	326	0.38	7.98	7.58	89.2

When selecting the transistor, it is preferable to realize most of the PSIM base capacitance using the drain-to-source capacitance of the device. This allows one to use the largest possible device, thus minimizing device on-resistance and conduction losses. Furthermore, the device must be rated to withstand the peak voltage imposed by the PSIM network. Based on the detailed evaluation in the Appendix, for typical modulation ranges, one can estimate the peak voltage on the device to be approximately 2.5x the magnitude of its fundamental component. In this work, the TMN is designed to provide a 50 Ω impedance matching and operate at up to 200 W of input power which corresponds to an input RF voltage magnitude of 140 V. This is roughly the magnitude of the fundamental component of the voltage across the transistor since the input L_1-C_1 tank in Fig. 7 is series-resonant at the operating frequency. Hence, at 200 W of input power, one would expect the peak voltage across the device to be approximately 350 V. In this design, we chose to use the GS66504B transistor since its drain-to-source capacitance is comparable to the required PSIM base capacitance C_0 while offering a sufficient voltage margin for up to 200 W of TMN input power.

One can see from Table I that the simulated TMN design is able to match both capacitive and inductive loads to 50 Ω with most of the power losses in the TMN being distributed evenly between the output inductor and the switching device. It is interesting to note that although L_1 and L_2 have comparable quality factor, the power P_{L2} dissipated in L_2 is much larger than P_{L1}. This is because both the rms current through L_2 and its inductance are larger than those of L_1.

To ensure an impedance match between the load and the source impedance, the conduction angle and operating frequency must be selected appropriately. Note that the conduction angle listed in Table I is the total conduction angle of the switch and it includes both forward and reverse conduction of the device. (The total switch conduction angle and α in Fig. 1 are related, however, they are not equivalent. The total switch conduction angle includes both forward and reverse device conduction, while α corresponds only to forward conduction.) One can see from Table I that loads with smaller resistive components require larger conduction angles of the switch. On the other hand, the required operating frequency roughly decreases for an increasing inductive load reactance and increases for an increasing capacitive load reactance.

For the TMN of Fig. 7 it can be shown that the effective input impedance Z_{IN} seen looking into the IN port (at the operating frequency) is given by (5), where X_1 and X_2 are the net reactances of the input and output filters, respectively, B_{psim} is the effective susceptance of the shunt PSIM element, and Z_L is the load impedance. However, when analyzing the operation of matching networks, it is often more convenient and insightful to do so by referring to a Smith chart.

$$Z_{IN} = \left((Z_L + jX_2)^{-1} + jB_{psim}\right)^{-1} + jX_1 \qquad (5)$$

To illustrate the operation and control of the TMN design of Fig. 7 in more detail, consider the Smith chart of Fig. 9 with some inductive and capacitive loads Z_1 and Z_2 respectively that one wishes to match to 50 Ω (the center of the Smith chart). The dashed circle corresponds to a conductance of 0.2 S, i.e. the equivalent load of a 50 Ω resistance in parallel with some reactance.

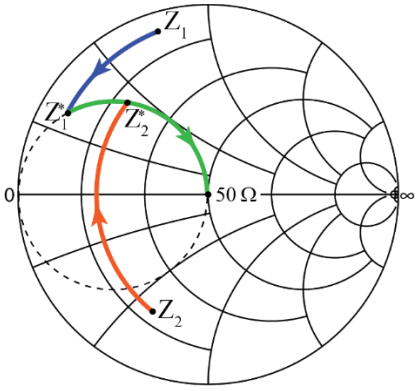

Fig. 9: Impedance matching of an inductive load Z_1 and capacitive load Z_2 using the TMN of Fig. 7 by first performing frequency control and then phase-switched capacitance modulation.

For the L-section matching network design of Fig. 7, frequency modulation causes the TMN's input impedance to move along a circle of constant resistance in the Smith chart (e.g., red and blue curves in Fig. 9). On the other hand, phase-switched impedance modulation of the shunt capacitor results in the TMN's input impedance traversing a circle of constant conductance in the Smith chart (green curve in Fig. 9). (Here we

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ignore the small effect of the input filter on the TMN's input impedance with frequency modulation.) Thus, in the context of the TMN design presented here, one can visualize the mechanism of impedance matching as a two-step process consisting of frequency control followed by phase-switched impedance modulation. For example, in the case of matching load Z_1 in Fig. 9, one can first begin by decreasing the operating frequency below the resonant frequency f_0 of the output tank so as capacitively offset the load and thus bring the TMN's input impedance to the point Z_1^* on the 0.2 S dashed conductance circle (blue line). At this point, one can proceed by increasing the conduction angle of the switch, forcing the TMN's input impedance to traverse along the dashed conductance circle until it reaches 50 Ω (green line). This essentially corresponds to adjusting the effective shunt capacitance to resonate out the susceptive component of Z_1^*. On the other hand, when matching a capacitive load such as Z_2, one may begin by first increasing the frequency above f_0 to inductively offset the load to point Z_2^* on the 0.2 S conductance circle (orange line) and then appropriately increase switch conduction angle until the TMN's input impedance reaches 50 Ω (green line). As Fig. 9 suggests, loads with larger resistive components require less shunt capacitance, and hence, a smaller switch conduction angle. In terms of frequency control, inductive loads require smaller operating frequency than capacitive loads. Note that one can reactively offset the entire TMN matching range shown in Fig. 8 by simply changing the resonant frequency of the output tank.

Although in the above matching example frequency control is performed prior to switched-capacitance modulation, in practice, one ought not to do it in this fashion. In fact, a controller optimized for fast dynamic response and agile impedance matching may require simultaneous adjustment of frequency and switch conduction angle.

IV. Gate-Drive Control and Synchronization

The ability to synthesize the appropriate gate waveform for driving the switch is of crucial importance to the TMN operation. As Fig. 1 suggests, the gate drive signal q should be synchronized to the current i_C flowing through the switched-capacitor network over the entire TMN frequency modulation range. Furthermore, one must be able to accurately control the conduction angle of the switch. In essence, this requires one to generate a gate waveform with a variable duty cycle synchronized to the switched capacitor current i_C. The resolution with which one can vary the duty cycle determines the resolution with which the effective capacitance can be modulated and hence sets the limit on the overall TMN impedance matching resolution. Synchronizing the gate drive signal directly to the switched-capacitor current waveform, however, can be problematic as this requires one to measure the current i_C; measurement of RF current waveforms is often a challenge. Instead, for the TMN design presented here, we offer an alternative approach based on synchronizing the gate drive signal q with the TMN's input voltage v_{IN}.

To illustrate this approach, consider the TMN design presented in Fig. 7 with L_1 = 1.17 μH, C_1, = 117pF, L_2 = 2.97 μH, C_2 = 47.5 pF, C_0 = 270 pF. Since the TMN's input filter is series-resonant at the 13.56 MHz nominal operating frequency, the fundamental frequency components of v_{IN} and the drain voltage v_D are in phase at this frequency. Furthermore, since the phase-switched capacitor network behaves effectively as a capacitor, the fundamental frequency component of the switched capacitor current i_C leads that of v_D by 90º. Of course, this is exactly true only at the nominal operating frequency – the frequency at which the TMN's input filter is series-resonant. However, in the prototype design considered here, the characteristic impedance of the input filter is selected to be relatively low compared to 50 Ω, and as a result, the filter remains nearly-resonant over the entire frequency modulation range. It can be shown that for this TMN design, the phase shift between the fundamental components of v_{IN} and i_C is approximately 90º ± 5º over a ±5% frequency modulation range and the corresponding load impedance range shown in Fig. 8. (Of course, the actual deviation of the phase shift from 90° depends on the operating frequency, the resonant frequency of the input filter L_1C_1 and its characteristic impedance. This phase shift is 90° only when operating at the resonant frequency of the input filter. The ±5° variation claimed here is based on a spice simulation of the presented TMN design.) Hence, by synchronizing the gate drive signal directly to the TMN's input voltage (and by appropriately phase-shifting it), one is able to effectively synchronize the switching of the capacitor to the current i_C. This is the underlying principle of the proposed gate-drive synchronization approach.

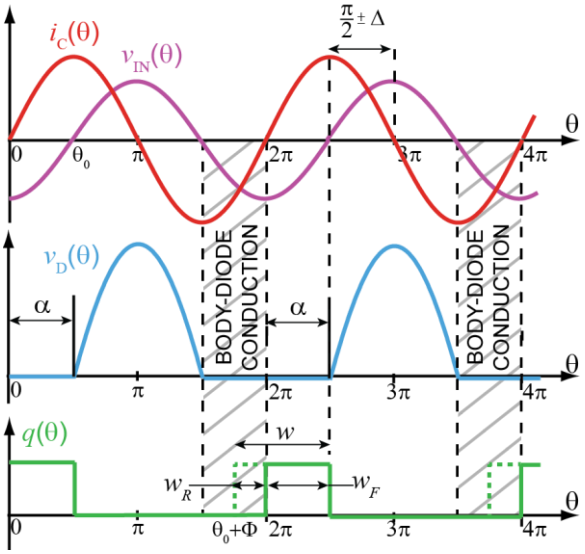

Fig. 10: Current and voltage waveforms for the TMN of Fig. 7. The switch gate waveform q is phase-locked with respect to the TMN input voltage v_{IN}, which is lagging the current through the switched-capacitor network i_C by approximately 90°. The phase shift Φ between v_{IN} and q is defined with respect to the negative-to-positive transition of v_{IN} and the rising edge of q. By controlling the switch conduction angle one can adjust the effective capacitance of the switched capacitor.

As Fig. 10 illustrates in more detail, the gate-drive signal q having variable pulse width w is phase-locked to the TMN's input voltage v_{IN}, i.e. a phase shift Φ is maintained between the rising edge of q and the negative-to-positive v_{IN} transition. As we discuss shortly, the gate drive signal generation circuit is capable of independently controlling both Φ and w over the entire frequency modulation range. Since i_C leads v_{IN} by approximately 90º, one can choose w and Φ appropriately so that the switch is turned on for a duration α ($0 \le \alpha \le \pi$) after the

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negative-to-positive transition in i_C. Note that if the switch is not turned on immediately after the drain voltage v_D rings back down to zero, the switch goes into reverse conduction mode and the body diode clamps the drain voltage near zero (since at this instant the current i_C is negative). Assuming the switched capacitor current i_C in Fig. 10 is purely sinusoidal, it can be shown that the duration of the reverse conduction mode is also α. To ensure zero-voltage switching (ZVS), the switch must be turned on either exactly at the positive-to-negative transition of v_D, or while the body-diode is conducting. Of course, in the latter case, the phase shift Φ between q and v_{IN} must be appropriately selected with the pulse width w chosen greater than α. This allows one to use the body-diode conduction mode effectively as a ZVS *safety margin* by alleviating the requirement for precise switch turn-on; ZVS operation is guaranteed, provided that the switch is turned on anytime during the body-diode conduction interval.

Here we introduce a PLL-based approach for generating a variable duty cycle gate waveform that allows one to control its angular pulse width w and phase Φ (relative to an input voltage) independently from frequency, i.e. frequency modulation affects neither w or Φ. This greatly simplifies the overall system control. (The ability to dynamically control Φ is not necessary for the operation of the TMN design presented here; it is incorporated in the design of this phase-locked PWM generator and gate driver only for additional versatility.) The phase-locked PWM circuit comprises a cascade of two PLL modules (see Fig. 11). Each PLL module is designed to generate an output signal at its OUT terminal such that the signal fed back to its IN terminal is frequency-locked to the reference signal at its REF terminal and is phase-shifted from it by a certain amount. This phase shift is digitally controlled by a microcontroller and can be adjusted from -180° to 180° with a 10-bit resolution. The resolution is a result of the particular implementation of the PLL and can be easily increased.

Consider Fig. 11 and assume for a moment that the time delay element in the feedback path of PLL1 is zero. This causes PLL1's output signal A to be frequency-locked to the RF input and phase-shifted from it by Φ. For the particular implementation of PLL1, a phase shift of Φ between the reference and the output signals implies that the rising edge of the output signal pulse lags the negative-to-positive transition in the reference signal by Φ. In turn, the output of PLL1 serves as the input of PLL2, whose output signal B is phase-shifted by w from signal A. Signals A and B are combined through gate drive logic to produce the signal q with variable angular pulse width w and phase shift Φ between its rising edge and the negative-to-positive transition of the RF signal. Note that by selecting the time delay τ in the feedback path of PLL1 to match the delay of the gate driver, one can eliminate the dependence on frequency of the phase shift between q and the RF signal. (In reality, it is difficult to know the exact delay of the gate-driver. Hence, as we demonstrate in the next section, the delay element is implemented as an adjustable RC low-pass filter that can be manually tuned until its delay matches that of the gate driver.) In the TMN design presented here, the RF reference signal fed to PLL1 is obtained directly from the TMN's input voltage v_{IN} (see Fig. 7) through capacitive voltage division.

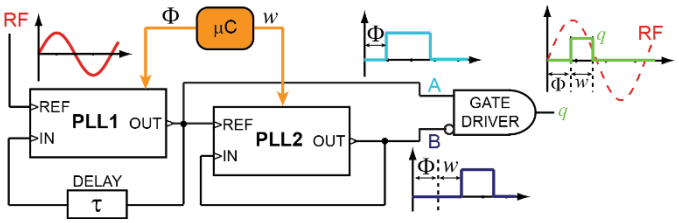

Fig. 11: Block diagram of the phase-locked PWM generator and gate driver circuit employed for generating a variable duty-cycle waveform with pulse width w and phase shift Φ. The time delay element τ in the feedback path of PLL1 is selected to match the gate driver delay and thus eliminate the dependence of Φ on frequency modulation.

The gate-waveform generation module of Fig. 11 is capable of generating a variable duty-cycle gate drive which can be adjusted from 0 % to 100 % with 0.1 % resolution while synchronizing it to the switched-capacitor current waveform over the entire frequency modulation range. As mentioned, this resolution in duty-cycle control is a result of the particular implementation and can be easily increased if necessary.

It is important to clarify that although the PWM circuit is capable of generating a signal q with arbitrary pulse width w and phase shift Φ that are unaffected by frequency modulation, this is not the case for the forward conduction angle α. That is, a constant pulse-width and phase of q does not imply a constant α as the TMN's operating frequency is modulated. This is because the gate drive signal q is phase-locked with respect to v_{IN}, and hence, any small variation in the phase shift between the fundamental components of i_C and v_{IN} translates directly into modulation of forward conduction angle α of the switch. Similarly, this also affects the duration of the reverse conduction interval. For instance, if the phase shift between v_C and i_C changes by Δ from the nominal 90° (e.g., due to modulation of the operating frequency), the switch will stay in forward conduction mode for a duration of α + Δ assuming phase Φ and pulse width w of the gate drive signal q are kept constant.

Control of the switch forward conduction α and the TMN's operating frequency is the responsibility of an external feedback loop. For example, such a feedback loop could be based on monitoring the quality of impedance matching between the power amplifier and the TMN by measuring the reflected power or the impedance at the TMN's input port, much as in conventional TMN designs. (The design of a feedback control loop that can fully utilize the available bandwidth offered by the PSIM TMN is the subject of future work. In Section IV, however, we demonstrate the closed-loop operation of the PSIM TMN with a lower bandwidth controller that was originally intended for the control of TMNs based on mechanically-tuned capacitors.)

As we described in Section II.B, to minimize losses in the switching device, it is desired to operate it in the ideal ZVS mode as shown in Fig. 6A, corresponding to $w_F = w_R$. Of course, to achieve this, one must simultaneously control both the phase Φ and pulse width w of q as one modulates α. For the sake of simplicity, here we employ an alternative, simpler control strategy in which Φ is kept constant, and control of α is achieved through pulse-width-modulation of q alone. This corresponds to operating the device in *quasi*-ZVS mode as shown in Fig. 6B,

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i.e. the body-diode of the device is allowed to engage for a portion of the reverse conduction period.

Of course, to guarantee zero voltage switching over the entire TMN operation range, Φ must be chosen appropriately to allow for variation in the phase shift between v_{IN} and i_C as frequency is modulated. (The phase shift Φ between v_{IN} and q is defined with respect to the negative-to-positive transition of v_{IN} and the rising edge of q – see Fig. 10.) To do so, one can begin by first estimating the expected variation Δ in the 90º nominal phase shift between i_C and v_{IN} for a given TMN frequency operating range. (A nominal phase shift of 90° corresponds to operation at the resonant frequency of the input L_1C_1 tank.) One possible selection of Φ that ensures *quasi*-ZVS operation over most of the range of α is $\Phi = 3\pi/2 - \Delta$. At the nominal operating frequency, this corresponds to $w_R = \Delta$ in Fig. 10; however, as one modulates frequency, the phase shift between i_C and v_{IN} changes by a small amount and causes w_R to vary from 0 to 2Δ. Thus, the device is always turned-on during conduction of the body-diode. Furthermore, recall from Fig. 6B that in *quasi*-ZVS mode, w_R must be less than w_F. Since the maximum expected value of w_R is 2Δ, one must also maintain a minimum w_F of 2Δ, resulting in a minimum total pulse width $w = 4\Delta$.

For example, in the TMN design presented here the maximum variation Δ in the phase shift between i_C and v_{IN} is approximately 5º. Thus, we can choose Φ = 265º and a minimum allowed gate signal pulse width of 20º. Note from Fig. 2 that operating the phase-switched capacitor network with α less than 20º does not contribute significant additional dynamic range in effective capacitance. Of course, one can also chose Φ to be less than 265° thus reducing the time during which the body-diode is engaged. This, however, requires one also to increase the minimum limit on the pulse width of q, which can eventually lead to reducing the dynamic range of the PSIM capacitance.

V. System Implementation

One can think of the TMN system proposed here as comprising a power stage and a gate-waveform generation module. The power stage consists of the RF phase-switched capacitor and the input and output filters as shown in Fig. 7, and it is responsible for providing the load-to-source impedance match. A 650 V GaN FET (GS66504B, GaN Systems) is used for a switch due to its fast turn-on and turn-off times and relatively low output device capacitance (40 pF at 300 V drain-to-source voltage). For 200 W of TMN input power, this device offers approximately 300 V of drain-to-source voltage margin, and it comes in a leadless, easy-to-work-with, low-inductance package with excellent thermal characteristics. Although in the simulated TMN design an additional 100 pF of external capacitance is added in parallel with the device, in the actual TMN implementation of Fig. 12 no additional shunt capacitance is required to achieve the same load impedance matching range as the simulated design. The device capacitance forms the entire phase-switched capacitor C_0. This discrepancy is mainly attributed to underestimation of the device capacitance by the employed simulation model.

Both inductors are coreless solenoids with a 3" inside diameter and are wound with 0.25" copper tube (see Fig. 12). The input filter inductor L_1 comprises 3.75 turns with approximately 0.55" turn-to-turn spacing plus interconnect. Its inductance is measured to be approximately 1.2 μH with a quality factor greater than 900 at 13.56 MHz. The output filter inductor is wound with 8 turns with approximately 0.51" turn-to-turn spacing plus interconnect and has a measured inductance of 3.2 μH and a quality factor of approximately 800 at 13.56 MHz. Machined delrin spacers are fitted between the turns of the inductors for a more rigid construction. The resonant frequencies of the input and output filters are tuned to be 13.56 MHz and 13.40 MHz respectively by adjusting the values of the input and output filter capacitors C_1 and C_2. C_1 has a total capacitance of approximately 115 pF and is formed by the parallel combination of 1.5 kV NP0 ceramic capacitors (HIFREQ series, Vishay), while C_2 consists of a series-parallel combination of 2.5 kV NP0 ceramic capacitors (HiQ series, AVX) with a total capacitance of approximately 44 pF .

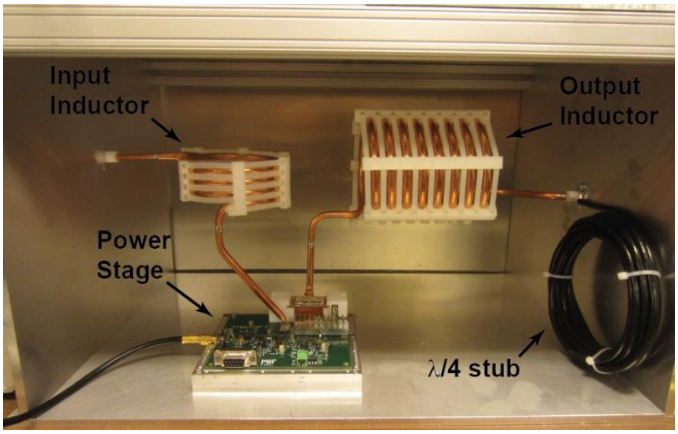

Fig. 12: Overall TMN system implementation showing the input and output filter inductors, the power stage and the quarter-wavelength stub.

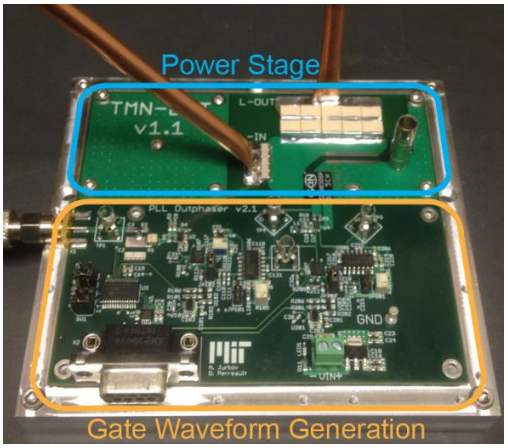

Fig. 13: Closer view of the power stage along with the gate waveform generation module. Control of the switch conduction angle is achieved through a UART serial interface.

The quarter-wavelength stub at the TMN's output is made of approximately 3.65 m of 50 Ω coax cable (RG58) coiled and shorted at one end. The TMN implementation presented here is rated up to 200 W of RF input power (with operation up to ~400 W expected to be possible with improved device heatsinking). The power stage electronics and the gate-waveform generation

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module are integrated onto a single 4-layer FR4 PCB (see Fig. 13).

A schematic of the PLL blocks used in the gate waveform generation module is shown in Fig. 14. The design is based on a PLL chip (ADF4001, Analog Devices Inc.) and a 5-20 MHz VCO (SN54LS624, Texas Instruments). The ADF4001 conveniently integrates a digital phase-frequency detector, charge pump and programmable frequency dividers for the REF and IN input signals. For this application, both dividers are programmed with unity gain (no division). The frequency of the REF and IN signals is determined by the dynamic frequency tuning control and varies by ±5% around 13.56 MHz.

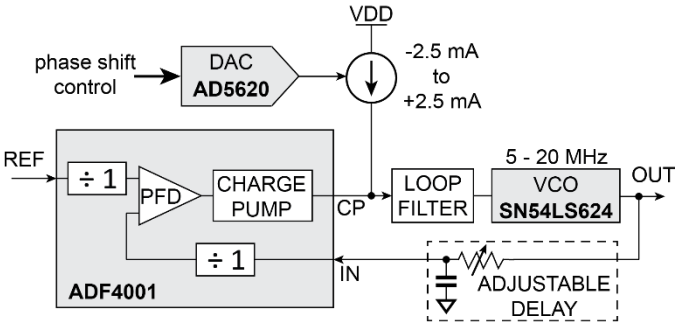

Fig. 14: Implementation of the PLL blocks of Fig. 11 based on the ADF4001 PLL chip (Analog Devices Inc.). Phase shift between the REF and OUT signals can be adjusted by controlling the current injected into the charge pump output node.

The dc average of the charge pump output current into the CP node is proportional to the phase shift between the REF and IN signals. When the REF and IN signals are in phase, the charge pump output current is on average zero. On the other hand, when the phase shift between REF and IN approaches 360°, the average output current of the charge pump approaches a pre-programmed full-scale current (5 mA for the PLL design presented here). An adjustable phase shift between REF and IN can be introduced by injecting a current into the CP node. In this design, this is achieved by an external voltage-controlled dc current source controlled by a 12-bit DAC (AD5620, Analog Devices Inc.). The DAC communicates to a local microcontroller (PIC18F26K22, Microchip Inc.) via a serial SPI interface. The injected current into the CP node can be adjusted over a ± 2.5 mA range and is roughly sufficient to achieve up to ±180° of phase shift between REF and IN. Note that it is the resolution with which one can adjust this injected current that ultimately determines the resolution with which the PSIM switch conduction angle can be modulated and hence, its effective capacitance resolution. The voltage-controlled current source in Fig. 14 is implemented with a pair of temperature-compensated NPN and PNP transistor-based current mirrors (BCV61 and BCV62, Infineon Technologies) that are biased against each other. Detailed schematics and bill-of-materials are provided in [24], Appendix D.

The loop filter essentially converts the current injected into the CP node to a voltage that drives the VCO. For this design, the loop filter is realized with a lead compensator while the location of its pole and zero are selected to achieve a 1 MHz loop bandwidth and 45° phase margin. The lock time of the PLL is measured to be less than 3 µs.

The delay in the feedback path of the PLL1 block in Fig. 11 is realized with a simple low-pass RC filter. It is empirically adjusted to provide approximately 20 ns of delay to compensate the time delay in the gate driver. One way to achieve this is to perform a frequency sweep (over the TMN operating frequency range) of the reference input signal RF to the PWM generator in in Fig. 11 while simultaneously measuring RF and the output pulse q on an oscilloscope. The delay of the RC filter is then adjusted until a constant phase shift is observed between q and RF as frequency is swept.

The gate driver used in this design (UCC27511, Texas Instruments Inc.) provides both inverting and non-inverting inputs and conveniently implements the logic AND operation of the two PLL outputs A and B in Fig. 11. As an example, Fig. 15 illustrates the generation of approximately 50 % duty-cycle gate-drive waveform q at 13.56 MHz with its rising edge aligned in phase with the positive-to-negative transition of the RF input signal (see Fig. 11). (Additional waveforms along with more detailed exploration of the performance of the PWM generator are provided in [24], Chapter 4.)

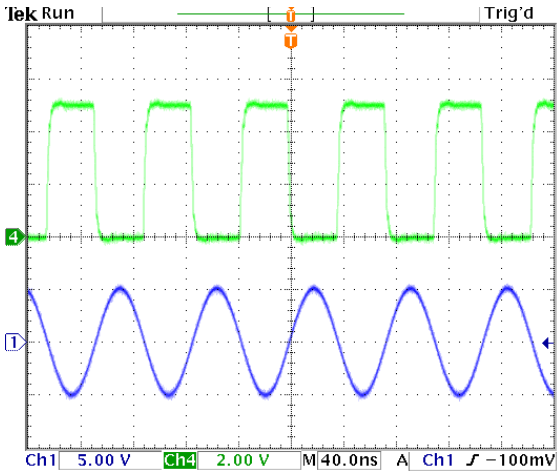

Fig. 15: Example generation of a 50 % duty-cycle gate-drive waveform q (ch 4, green) at 13.56 MHz based on the design of Fig. 11. In this case, the rising edge of the PWM waveform is aligned in phase with the positive-to-negative transition of the reference RF signal (ch 1, blue).

VI. EXPERIMENTAL PERFORMANCE

A. *Measurement Setup*

To evaluate the performance of the matching system presented here, the TMN is powered from a 150 W RF power amplifier (150A100B, Amplifier Research) having a 50 Ω output impedance as shown in Fig. 16. It is sinusoidally excited by a function generator (DG2041A, Rigol) whose frequency can be externally adjusted. The power amplifier is connected to the TMN through an I-V probe (Model#: 000-1106-117, MKS Instruments) which directly measures the input impedance looking into the TMN. This I-V probe is also capable of directly measuring the input power to the TMN at the fundamental operating frequency. The impedance measurements derived from this probe are used directly by the TMN controller to indicate when impedance matching is achieved and provide feedback information for adjusting the switch conduction angle and operating frequency. (Consequently, the accuracy and bandwidth with which impedance can be measured has a direct

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impact on the overall system performance. The I-V probes employed in this work provide a 100 kHz sampling rate and are specified to have an accuracy of ±1 % in impedance magnitude and ±0.4° in impedance phase.)

The TMN controller shown in Fig. 16 is designed and fabricated by MKS Instruments Inc., and it is originally intended for controlling TMN systems based on variable vacuum capacitors. To evaluate the steady-state performance of the system (see section VI-B), the controller is operated in open-loop, i.e. external commands are manually provided to the controller to adjust f and α until proper impedance matching is achieved. On the other hand, when evaluating the transient performance (see sections VI-C and -D), we allow the controller to operate in feedback mode thus automatically adjusting f and α based on input impedance measurements. The actual control algorithm employed is proprietary to MKS Instruments Inc.

In this work, the criteria for achieving impedance matching is to limit reflected power to less than 1%, corresponding to a VSWR of less than 1.22. An identical I-V probe is connected at the output of the TMN to measure its output power. The TMN's output port is terminated with a resistive/reactive load impedance located within the 10 % frequency-modulation matching range shown in Fig. 8.

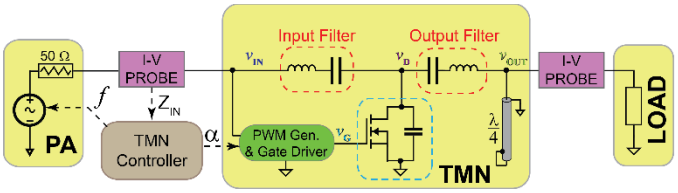

Fig. 16: Experimental setup for measuring the performance of the TMN. The switch conduction angle α and the operating frequency f are adjusted until the load is matched to 50 Ω. The TMN's input impedance and input / output powers are measured directly by IV probes.

To test the TMN, we utilize a home-built adjustable RF load. To facilitate ease of adjustment of the load over the targeted impedance range, the load is implemented with a variable length transmission line (50 Ω RG214 coax cable) terminated with the parallel combination of a 50 Ω RF power resistor (CTN-250-2, Meca Electronics Inc.) and a variable vacuum capacitor (CVMN-1000A, Comet). By adjusting the length of the line from 0 to 3 m and varying the capacitance over a 50 pF – 1000 pF range, one can generate all the inductive loads and most of the capacitive loads in Fig. 8 corresponding to the 5 % frequency modulation load range.

B. Steady-State PSIM-TMN Performance

To demonstrate the steady-state performance of the TMN, the switch conduction angle and the operating frequency are adjusted until the I-V probe measures 50 Ω input impedance, i.e. the load is matched to the power amplifier. Table II shows example of load impedances (along with the required switch conduction angle and operating frequency) at which the TMN matches the load to 50 Ω at 150 W power output from the PA with less than 1 % of reflected power at the input port of the TMN. Note that the conduction angle in Table II reflects the total switch conduction angle, i.e. it is the combination of forward and reverse device conduction. As can be seen, the TMN is able to match a wide range of capacitive and inductive loads as suggested by Fig. 8. Consistent with the expected operation of the L-section-based TMN design, matching of loads with small resistive components requires larger switch conduction angles. As the resistive component of the load increases, the required conduction angle decreases. In terms of frequency control, the larger the inductive component of the load, the smaller the frequency required to provide impedance matching, while loads with larger capacitive components demand higher operating frequency, as expected.

Comparing the conduction angle listed in Tables I and II one can see that the simulated design does require larger shunt capacitance than the actual TMN implementation for every load impedance, especially in test cases A and B. Note further, that the simulation results in Table I are based on the GS66504B device with an additional external capacitance of 100 pF, while in the actual TMN implementation, no additional capacitance was added in parallel with the same device. Although there is a small parasitic capacitance between the drain pad and ground of the TMN's power stage pcb (less than 10 pF), it is not enough to account for such discrepancy in conduction angle. The necessity for larger switch conduction angle for a given load impedance in the simulated TMN design is attributed to underestimation of the device capacitance and its voltage dependence by the employed simulation model of the device. The small difference in the required operating frequency between the TMN implementation (Table II) and the simulated design (Table I) for a given load impedance is due to fact that the resonant frequency of the output tanks of the simulated and implemented TMN designs are not identical.

The power efficiency measurements in Table II reflect the efficiency of the TMN at the fundamental operating frequency and exclude any power loss owing to the gate driver and the gate waveform generation circuit. As mentioned, TMN's input and output power are measured directly with a pair of I-V probes connected at the input and output of the TMN. The lower power efficiency measurements in Table II compared to the simulated efficiency in Table I are attributed to additional device losses. Note further that the difference between the measured and simulated power efficiency increases as the resistive component of the load impedance decreases. Load impedances with lower resistive components result in a significant increase of drain current. Hence, the additional device losses measured in Table II can be either due to a larger device channel on-resistance, i.e. dynamic on-resistance, or losses in the device capacitance [23]. Neither of these effects are accounted for in the spice model of the device. Nonetheless, the efficiency of the prototype TMN is adequate for the type of system considered, and achievable efficiency can significantly improve as available switch device performance improves. Note that in this measurement setup we use a linear class-A power amplifier. This class of amplifiers are characterized with a maximum theoretical efficiency of 50 %, but exhibit even lower efficiencies in reality. In general, however, one can utilize a switched-mode DC-AC resonant inverter as the source of the rf power, provided that it is capable of operating over the frequency bandwidth required by DFT.

An example oscilloscope snapshot of the TMN voltage waveforms at the input port v_{IN}, output port v_{OUT}, switch drain v_D, and the gate-drive v_G for a 5.00 + j15.6 Ω inductive load (test

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case G, Table II) at 150 W of input power (into the TMN) is shown in Fig. 17.

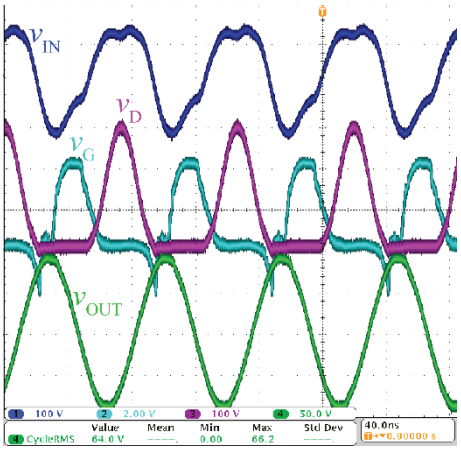

Fig. 17: TMN input port voltage v_{IN}, output port voltage v_{OUT}, gate-drive voltage v_G and switch drain-to-source voltage v_D for test case G (Table I) at 150 W of RF input power into the TMN.

It can be clearly seen that the switch exhibits zero-voltage turn on which is a highly desired feature for reducing switching losses. Note that for the test case illustrated in Fig. 17, the drain voltage rings down to zero and stays near 0 V (due to reverse switch conduction) even before the switch is commanded to turn on. (There are no body-diodes in the GaN FETs utilized; instead, they turn on in reverse, providing an "effective" body diode.) In addition, Fig. 17 shows a nearly-pure sinusoidal TMN output voltage (the voltage across the load) suggesting a relatively small harmonic content injected into the load (measured to be less than -20 dBc). Similar output harmonic content is found for the rest of the test cases in Table II. On the other hand, one can easily notice that the input TMN voltage has significant harmonic content for the test case in Fig. 17. A small portion of it is due to relatively weak input filtering of the drain voltage. However, most of the harmonic content observed in TMN input voltage is attributed to near-saturation of the power amplifier used to drive the TMN; it is notable that the phase lock gate drive generation system performs extremely well even in the face of this distortion from the power amplifier.

The noticeable rise and fall time of the gate-drive signal are a result of the driving capability of the gate driver and the gate-to-source capacitance of the transistor (approximately 130 pF). Note that in this case, the relatively slow device turn-on does not significantly impact losses in the device since the turn-on occurs while the device is in reverse conduction.

Similar voltage waveforms are measured for the rest of the test cases in Table I, suggesting that the PSIM-based TMN implementation proposed here is effective at accurately matching a wide range of load impedances. It is important to note that harmonic content in the output depends on both the TMN's output filter and the frequency profile of the load impedance. For instance, an inductive load generated with the variable-length transmission line implementation discussed above has a very different frequency characteristic from that of an equivalent inductive load formed by the series combination of a resistor and an inductor. Hence, the design of the TMN's output filter must be carefully tailored to the particular load characteristic and the amount of harmonic content injected in the load that one is willing to tolerate.

TABLE II. SWITCH CONDUCTION ANGLE AND TMN OPERATION FREQUENCY REQUIRED TO MATCH VARIOUS LOAD IMPEDANCES TO A 50 Ω SOURCE IMPEDANCE AT 150W OF INPUT POWER.

Test Casc	Load (Ω)	Conduction Angle (°)	Frequency (MHz)	Output Harmonic Content (dBc)	Power Efficiency (%)
A	19.1 + j32.3	0	13.18	-25	91.8
B	20.3 + j1.62	0	13.99	< -40	95.5
C	17.9 – j13.6	144.8	14.37	-39	93.8
D	9.91 + j24.7	182.8	13.36	-40	90.3
E	9.61 – j1.10	195.1	13.97	-20	90.3
F	10.0 – j16.3	194.6	14.38	< -40	88.0
G	5.40 + j31.6	210.6	13.06	-40	79.5
H	3.97 + j0.98	218.8	13.81	-20	75.7
K	5.33 – j11.8	206.2	14.18	< -40	79.7

C. *Transient PSIM-TMN Performance*

To demonstrate the transient behavior of the TMN, the system of Fig. 16 is equipped with a controller identical to the ones used by MKS Instruments to control some of their own TMNs based on mechanically tunable vacuum capacitors. The controller samples the TMN input impedance seen by the PA via the input I-V probe at a sampling rate of 100 kHz and correspondingly adjusts the desired PA operating frequency and TMN shunt capacitance. The detailed implementation of the controller and its control law is proprietary to MKS Instruments.

As we mentioned previously, the experimental setup in Fig. 16 uses a 150 W linear class A amplifier (150A100B, Amplifier Research) with a 50 Ω output impedance. The drive signal for the PA is generated directly by the controller at the desired operating frequency and amplitude level to achieve a commanded PA output power level. The desired TMN shunt capacitance is communicated to the TMN over a serial interface in the form of a digital capacitor code in the 0 – 1000 range. In the case of TMNs based on mechanically tunable capacitors, this digital code typically maps linearly to the actual capacitance value. However, in the case of the PSIM-based implementation, the digital capacitance code is instead mapped linearly to the commanded switch conduction angle α (see Fig. 10); code value of 0 corresponds to a permanently-off switch (α = 0), while a code value of 1000 is roughly equivalent to a permanently-on switch (α ≈ 180°). Hence, there is a non-linear, but monotonic relationship between the digital capacitor codes issued by the controller and the actual effective capacitance realized by the PSIM TMN. We find that this nonlinearity is not problematic for the control loop used here and results in stable system behavior for all transient experiments performed in this work.

For example, Fig. 18 shows the transient response of the PSIM-based TMN when powering into a fixed 2 + j20 Ω inductive load. Initially, the power amplifier is off, and the PSIM controller is initialized with a frequency of 14.20 MHz and a capacitor code of 100, corresponding nearly to a permanently-off switch. (Digital capacitor codes less than 200 corresponding roughly to α ≤ 36° have negligible effect on the effective PSIM capacitance – see Fig. 2.) At the 10 ms mark, the PA is commanded to an output power of 50 W.

As Fig. 18 shows, the TMN undergoes approximately a 15 ms transient with the forward power settling to the commanded

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power level of 50 W. Note that the TMN is able to provide a good impedance match to 50 Ω with minimal reflected power within a tuning time that is already at least on order of magnitude faster than typical response times of conventional TMNs based on mechanically-tuned capacitors.

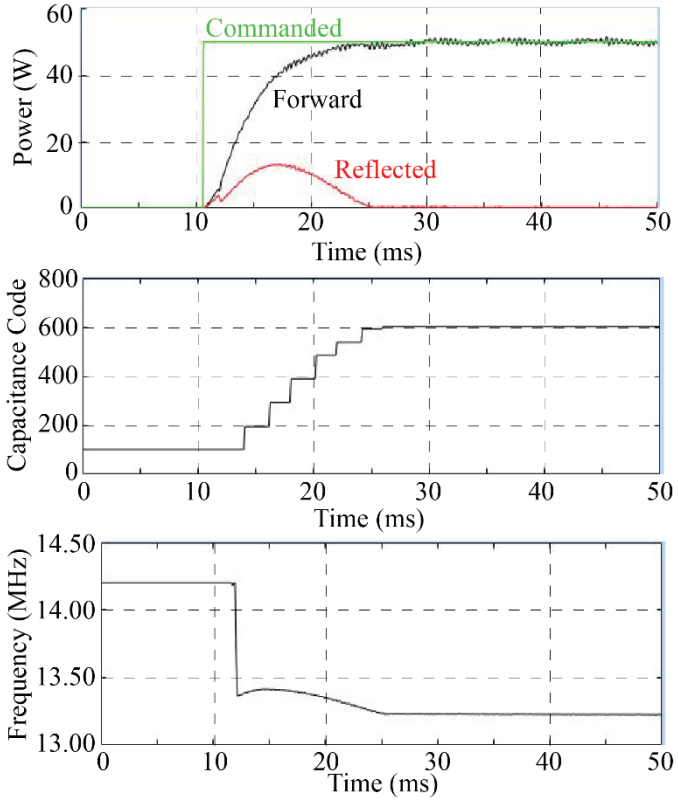

Fig. 18: Forward and reflected power versus time at the input port of the PSIM TMN for a 0 W to 50 W step in commanded PA output power (top) and the corresponding capacitance (middle) and frequency (bottom) controls necessary to achieve impedance matching between the 50 Ω PA output impedance and a 2 + j20 Ω load.

As previously mentioned, the controller used in this setup was originally designed for the control of mechanically-tuned capacitors which are typically driven by stepper or servo motors. To minimize the jitter in the motors and the wear and tear of all moving parts, the controller is typically designed to wait a certain time period after every capacitor command before issuing the next one. This explains the stepwise nature of the control signal in Fig. 18 with approximately 2.5 ms of wait period between successive capacitor commands. To further reduce capacitance control effort, the controller used in this work attempts to tune the capacitance only if the reflected power exceeds approximately 5% of the forward power. Of course, the PSIM-based TMN implementation presented here alleviates the mechanical limitations associated with controlling stepper motor-driven variable capacitors.

With an appropriately designed controller, one ought to be able to achieve still much faster response times and more accurate impedance matching than demonstrated here. An important step towards the design of such a custom controller is the development of a full dynamic model of the PSIM-TMN system. Furthermore, to fully utilize the inherent high bandwidth capability of PSIM-based systems, one must also be able to measure impedances rapidly and accurately at radio frequencies. The exploration of these and other topics towards further improving the dynamic performance of PSIM-based TMNs is the subject of future work.

D. PSIM-TMN Performance with Inductively-Coupled Plasma Loads

The generation and control of inductively-coupled plasma (ICP) is of importance to the semiconductor manufacturing industry among others. To be able to perform the sophisticated semiconductor wafer processing demanded by industry, plasma has to be generated and maintained over a wide range of process parameters such as gas composition, pressure, flow rate, excitation power, etc. A typical ICP chamber, as shown in Fig. 19, consists of a plasma excitation cavity through which a known gas flows at a precisely controlled rate and pressure. The plasma is generated by RF electric and magnetic fields produced by exciting a coil wrapped around this cavity at a particular frequency and power level. A secondary cavity located below the main one houses the chuck – a special platform which holds the wafer to be processed. The chuck is itself typically driven with a separate RF "bias" source producing electric fields that serve to increase the directivity of plasma ions bombarding the wafer [22].

The generation of plasma in such systems is particularly challenging since the driving-point impedances for both the coil and the chuck vary widely with process parameters and the state of the plasma. Since most conventional RF power amplifiers are designed to operate into a fixed or a very narrow range of load impedances, TMNs are used to match the widely varying impedances presented by the excitation coil and chuck to their respective PAs. Due to the requirements for accurate impedance matching over a wide load range and operation at high power levels, such systems usually rely on mechanically tunable TMNs and suffer from extraordinarily slow tuning speeds [18]. Here we demonstrate the ability of the PSIM TMN to match dynamically varying plasma loads to a 50 Ω source impedance with at least two orders of magnitude reduction in tuning time compared to most mechanically-tuned TMNs.

Fig. 19 shows the experimental setup of an 800 W ICP test chamber at an MKS Instruments testing facility. A high-power PA driving the main plasma excitation coil is used to generate and sustain the plasma with a number of gases at various pressures and flow rates and at power levels ranging from 100W – 800 W. A second power amplifier operating at tens of W is used to drive the wafer chuck with an rf bias. Based on the power levels of the TMN prototype developed here, we demonstrate the PSIM TMN for matching the widely-varying wafer chuck driving-point impedance to the 50 Ω output impedance of a linear class A amplifier (A500, ENI) for the rf bias, while a conventional TMN based on mechanically-tunable vacuum capacitors is used to match the excitation coil impedance to a high-power PA. An identical controller to the one described in the previous section adjusts the PSIM switch conduction angle and frequency of the wafer chuck rf bias drive based on an I-V probe (Model#: 000-1106-117, MKS Instruments) measurement of the load impedance seen by the PA. Modulation of the wafer chuck drive frequency is constrained within a ±5% band around 13.56 MHz.

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It is observed that rf bias and plasma excitation power have considerably larger impacts on the chuck driving-point impedance compared to the effect of gas composition, flow rate and pressure. Nevertheless, the PSIM-based TMN is capable of providing fast and accurate impedance matching over a wide range of process parameters including changes in excitation and bias power.

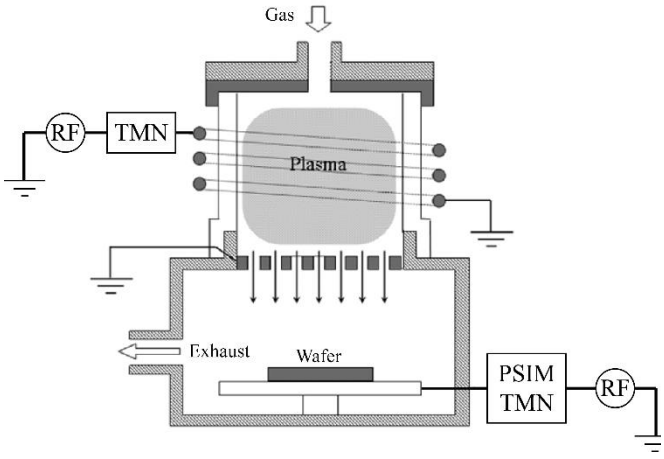

Fig. 19: Experimental setup for testing the performance of the PSIM-TMN with plasma loads. The PSIM-TMN matches the wafer chuck to a low power PA. A conventional TMN based on mechanically-tunable capacitors is used to match a high-power PA to the plasma excitation coil.

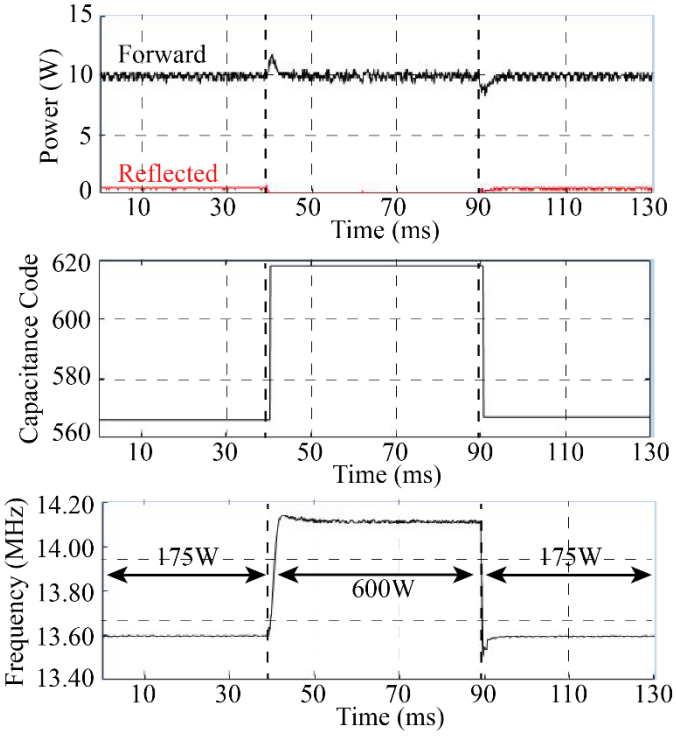

Fig. 20: Forward and reflected power versus time at the input of the PSIM TMN (top) and the corresponding shunt capacitance (middle) and frequency (bottom) controls for a 175 W - 600 W pulse on the plasma excitation coil.

For example, Fig. 20 shows the forward and reflected power at the input of the PSIM TMN for a 10 W commanded bias power during a 175 W – 600 W pulse in the plasma excitation power. It can be seen that the tuning transient lasts approximately 5 ms for both the falling and rising edges of the 600 W pulse with less than 5% of reflected power. Even faster tuning times of less than 3 ms are demonstrated in Fig. 21 for a 10 W – 40 W step in the chuck bias power with a constant plasma excitation of 600 W. (For the results shown in Fig. 20 and 18, the plasma is generated in an argon gas at 20 mT pressure and 125 sccm flow rate.) Note that for the experiments discussed in this section, the internal controller gains were adjusted to allow for faster tuning and higher utilization of the available bandwidth of the PSIM TMN. This is the reason why the tuning transients in Fig 17 and Fig. 21 are considerably faster than the one demonstrated in Fig. 18.

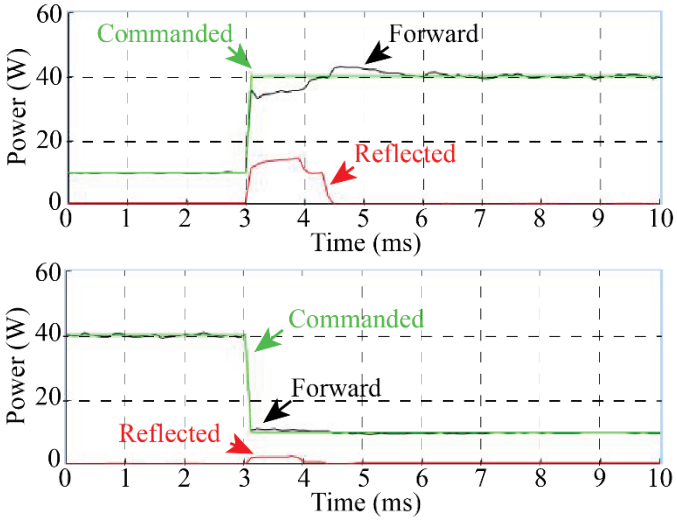

Fig. 21: Forward and reflected power versus time at the input of the PSIM TMN for a 10W – 40 W step in the chuck rf bias power with 600 W in the plasma excitation coil.

It appears from Fig. 20 that the capacitance code issued by the controller settles in a single control step. Note however that the controller will only attempt to adjust the PSIM capacitance if the reflected power measured by the I-V probe exceeds 5% of the forward power. As mentioned previously, this dead-band in capacitance control is implemented to eliminate jitter in the servo motors when the controller is used as originally intended with TMNs based on mechanically-tuned capacitors. Although in Fig. 20 a capacitance code of 566 and 619 corresponding respectively to 175 W and 600 W of plasma excitation power may not result in a perfect impedance match between the bias PA and the chuck, the measured reflected power falls within the controller dead-band. As a result, the controller issues no further adjustment to the PSIM capacitance.

It is important to note that the sampling rate of the I-V probe and the data rate of the serial communication link between the controller and the PSIM match considerably limits the tuning speed with which impedance matching can be performed in our prototype setup. The PSIM technique inherently allows much faster capacitance modulation; its response speed is mainly determined by how fast one can control the conduction angle of the switch. If one is able to synthesize the required gate-drive signals for the PSIM transistor with high enough bandwidth, one can theoretically modulated the effective PSIM capacitance on a rf cycle-per-cycle basis. By using PSIM along with a higher bandwidth controller with no dead-band and faster impedance sampling, one ought to be able to achieve even faster and more accurate impedance matching with tuning time in the range of a

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few µs – this is nearly six orders of magnitude reduction in the tuning time compared to most conventional vacuum capacitor-based TMNs!

VII. CONCLUSION

This work proposes a tunable matching network based on *phase-switched impedance modulation* (PSIM), a technique for implementing variable impedances based on switching of passive elements at the RF operating frequency. PSIM is a narrow-band technique in that it allows effective modulation of the effective impedance only at the switching frequency. We introduce a PSIM impedance and matching network implementation that enables zero-voltage-switching of the active device with simple timing. Moreover, we introduce a PLL-based modulation control system that provides the necessary sensing and drive of the PSIM circuit. To demonstrate the effectiveness of the proposed approach we present a PSIM-based TMN design capable of matching a wide load impedance range associated with inductively-coupled plasma processes to a 50 Ω power amplifier. The TMN's performance is demonstrated in a narrow frequency band centered around 13.56 MHz at an input RF power of up to 150 W. The matching network presented here provides accurate impedance matching (to < 1% reflected power) while injecting less than -20 dBc of harmonic content in the load and maintaining zero-voltage-switching over the entire load range. We also demonstrate the use of this system (with a conventional closed-loop controller) on both known loads and driving a plasma chamber. It is shown that such a PSIM-based TMN opens the door to a combination of much faster and more accurate impedance matching than is available with conventional techniques.

VIII. APPENDIX

One can calculate the power losses in a PSIM element by first computing an equivalent series resistance R_{ESR} (in series with the effective PSIM capacitance) as given by (6). It can be shown (see Appendix B, [24]) that the equivalent series resistance for the case of Fig. 6A ($w_F = w_R$) and Fig. 6B (with $w_R = 0$) is given by (7) and (8) respectively, where k is the effective capacitance modulation factor defined by C_{EFF}/C_0.

$$P_D = \frac{1}{2} I_0^2 R_{ESR} \tag{6}$$

$$R_{ESR} = \frac{r_0}{k} + r_{on}\left(1 - \frac{1}{k}\right) \tag{7}$$

$$R_{ESR} = \frac{r_0}{k} + \left(\frac{r_{on}}{2} + \frac{r_D}{2}\right)\left(1 - \frac{1}{k}\right) + \frac{V_D}{\pi I_0}(1 - \cos(\alpha)) \tag{8}$$

Here we model the PSIM element as shown in Fig. 5B, where r_D and r_{on} are the on-resistance of the diode and the switch respectively, V_D is the diode forward voltage drop, and r_0 is the effective ESR of the total base capacitance C_0. For typical power devices, r_D is comparable or larger than r_{on}, and so, as (7) and (8) suggest, operating a PSIM element under *quasi*-ZVS, i.e. allowing the body-diode to engage, is lossier compared to operation with ideal ZVS for any given capacitance modulation factor k. Furthermore, as can be seen from (7) and (8), losses increase with larger capacitance modulation – this is another reason why one should avoid operation of the PSIM at large values of k. In the current prototype, we limit capacitance modulation up to approximately a factor of 4x. Implementation details of the switch driving and synchronization scheme employed are further presented in Section III.B.

Another important practical aspect of PSIM to consider is the voltage stress imposed on the device. It can be shown (see Appendix B, [24]) that in the case of Fig. 6A and Fig. 6B the peak voltage V_{PK} across the device (normalized to $|V_1|$, the magnitude of the fundamental component of v_C) is given by (9), where α is the forward conduction angle of the switch.

$$\frac{V_{PK}}{|V_1|} = \frac{\pi(1 + \cos(\alpha))}{\pi - \alpha + \sin(\alpha)\cos(\alpha)} \tag{9}$$

This relationship is plotted in Fig. 22 versus α. As can be seen, the peak of the voltage across the device is approximately twice the magnitude of its fundamental component for less than 3x modulation of the PSIM effective capacitance. In fact, this ratio is slightly below 2 for up to 90° of switch forward conduction angle, corresponding to 2x modulation of the PSIM capacitance. However, modulating the PSIM effective capacitance by more than a factor of 3x cause the peak-to-fundamental magnitude ratio to rapidly increase.

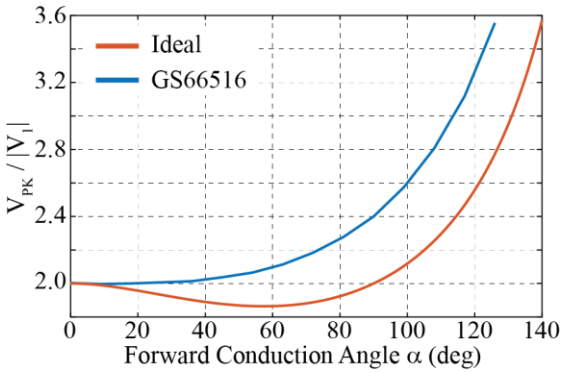

Fig. 22: Ratio of the peak capacitor voltage V_{PK} to the magnitude of the fundamental component V_1 of the capacitor voltage waveform v_C for the PSIM element of Fig. 5A versus switch forward conduction angle α. The ratio is plotted for an ideal, linear base capacitance (red) and an actual 650V GaN FET (GS66516T, GaN Systems) with no additionally added external capacitance in parallel with the transistor (blue).

Note that for the TMN system of Fig. 7, the magnitude of the fundamental component V_1 of the voltage across the PSIM element is roughly determined by the input power level and impedance of the TMN seen into the IN port. This is because the input filter is nearly resonant over most of the operating frequency range, and hence the magnitude of the fundamental component $V_{IN,1}$ of the input voltage is roughly equal to V_1.

In practice, the device capacitance can be combined in parallel with an additionally-added external capacitance, or can be used on its own to form the PSIM base capacitance C_0. In general, however, due to the non-linear characteristic of the device capacitance, C_0 tends to decrease with increasing device voltage, altering the shape of the ideal PSIM voltage waveform illustrated in Fig. 6A. More specifically, larger C_0 at low voltages causes slower slew rates of v_C near the base of the voltage pulse, while smaller C_0 at higher voltages results in faster v_C slew rate near the peak of the pulse. Consequently, this somewhat alters the ratio between the peak of the voltage V_{PK}

and the magnitude of its fundamental component V_1. For example, Fig. 22 plots this ratio versus the switch forward conduction angle for a 650 V GaN FET device (GS66516, GaN Systems) without any additional external capacitance in parallel with it. The plot is based on a spice simulation of the manufacturer-provided device model. In this case, the device is excited with a purely-sinusoidal current i_C just as in Fig. 6A, where the current magnitude is appropriately adjusted to maintain the peak of the device voltage v_C at approximately 600 V as the conduction angle of the switch is varied.

Note from Fig. 22 that even though the peak-to-fundamental ratio $V_{PK}/|V_1|$ for the GS66516 device is higher than that for the ideal case with the linear base capacitance, the two are still relatively close to each other. For example in the case of the GS66516 device, the peak voltage stress on the device remains less than 2.5x the magnitude of its fundamental component for up to 3x modulation of the PSIM effective capacitance. Furthermore, the peak-to-fundamental ratio plot for the GS66516 device in Fig. 22 corresponds to realizing the entire PSIM base capacitance only with intrinsic output device capacitance; by adding some external, linear capacitance in parallel with the device, one can increase the PSIM base capacitance C_0 while effectively *swamping* some of the non-linearity in the device capacitance and thus resulting in a peak-to-fundamental ratio that is closer to the ideal one. As a practical rule-of-thumb, one can assume that the peak voltage stress on the PSIM switching device is roughly 2-2.5x the magnitude of its fundamental voltage component for small PSIM effective capacitance modulation factors of up to 3x.

When designing PSIM elements, it is also important to consider the current stress imposed on the switch. It can be shown (see Appendix B, [24]) that for the PSIM implementation of Fig. 5, the rms current $I_{sw,rms}$ flowing through the switch when it is on (through r_{on}) depends on the effective capacitance modulation factor k according to (10), where C_0 is the PSIM base capacitance, and ω is the operating frequency (in rad/s).

$$I_{SW,rms} = 0.5V_1\omega C_0\sqrt{2k(k-1)} \qquad (10)$$

As (10) suggests, the rms current increases roughly linearly with the capacitance modulation factor. Of course, when k=1, the switch is permanently off, and no current flows through r_{on}.

Sometimes it is also of interest to know the DC component of the PSIM device voltage. It is straightforward to show that for the ideal ZVS case of Fig. 6A, the DC component V_{DC} of v_C is given by (11), where α is the forward conduction angle, and ω is the angular frequency of i_C.

$$V_{DC} = \frac{I_0}{\omega C_0}\left[\frac{(\pi-\alpha)\cos(\alpha)+\sin(\alpha)}{\pi}\right] \qquad (11)$$

As expected, it can be seen from (11) that V_{DC} is largest when α=0, i.e. when the device is always off, since in this case the peak voltage across the device is largest for a given magnitude of the current i_C.

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