A Modeling Approach for the VIRT and Other Coupled Electronic and Magnetic Systems

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Abstract-Recently, a new class of magnetic component has emerged in which the electronics that connect to these components are fundamental to defining the conductive loops that comprise them. In these "Coupled Electronic and Magnetic Systems" (CEMSs), a clear partition cannot be made between the electrical and magnetic domains and this prevents the application of established modeling techniques for deriving their circuit representation. One such CEMS is the Variable Inverter/Rectifier Transformer (VIRT), which enables a transformer with fractional effective turns and a variable effective turns ratio. Previous investigations into the VIRT have invoked simplifying assumptions to synthesize a circuit representation, omitting the full-details of operation such as the possibility and implications of ac currents induced on conductors that encircle the VIRT. Other fractionalturn transformers have simply assumed a circuit representation without undertaking modeling. In this work, a modeling approach is proposed which enables the circuit representation of a CEMS to be extracted directly from first principles. Two case studies are explored and the derived models are shown to match well with experiment. The proposed approach is suitable both for assessing the finer details of the VIRT, and other fractional-turn transformers, and as a framework for deriving and understanding new CEMS implementations.

Index Terms—Magnetics Modeling, Variable Inverter Rectifier Transformer, VIRT, Coupled Electronic and Magnetic System, CEMS

I. INTRODUCTION

Converter miniaturization is fundamental to the evolution of many applications, enabling such advancements as increasing the computational and storage density of the servers that realize the internet, supporting the meteoric capability of CPUs and GPUs, transitioning to fully electric transportation systems, and reducing the minimum size of portable electronic devices. Transformers represent a critical bottleneck toward miniaturization in these applications.

Proposals for improved transformer designs have typically been either at the "component" level or at the "system" level. In the former case, the transformer is improved "between its terminals" - it maintains the same operation but does so with higher performance (e.g., lower loss and volume). Examples include employing winding interleaving, leveraging new high-performance magnetic materials [1], winding construction techniques to mitigate the effect of gap fringing fields [2], and improving termination losses [3]. Conversely, system-level techniques improve the transformer "outside its terminals" - the system presents more favourable operating conditions which allows a higher performance transformer to

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Fig. 1: Half-turn VIRT model. (a) Circuit definition. (b) Core definition. N_p primary turns are wound in series around the center post as shown in green. The axis on which the cross-section in (a) is taken is also shown.

be designed. Examples include topology selection, such as the use of an LLC dc transformer (DCX) to achieve large voltage step-down [4], the multi-track framework [5], [6], in which a merged switched-capacitor and magnetic architecture enables the magnetic components to be kept in their high performance ranges, and the matrix transformer concept, in which a single transformer is decomposed into multiple seriesprimary, parallel-secondary ones [7]. While component-level and system-level techniques for improving transformers are distinct, they share a common feature in that there is a clear partition between the transformer itself and the system it connects to. That is, the transformer itself is always identifiable as a stand-alone component and conventional means for modeling its behaviour can be employed [8].

Recently, a new class of component has emerged in which this clear partition cannot be made. One example, named a Variable Inverter/Rectifier Transformer (VIRT), is shown in Fig. 1. The VIRT realizes a transformer with fractional effective turns and variable effective turns ratios (i.e. for N_p turns wound on the primary, $N_p : 1/2$, $N_p : 2/3$, $N_p : 1$, and $N_p : 2$ conversion is achievable) by physically distributing rectifiers¹ around a magnetic core, and is especially valuable for miniaturizing high step-down, high output current transformers [9]–[16]. In the VIRT, electronics complete the conductive loops around the magnetic core – the magnetic component itself is therefore inherently coupled to the electronic system it connects to. We refer to this kind of system, in which electronics are fundamental to defining the current loops in a magnetic component, as a "coupled electronic and magnetic system" (CEMS).

To derive a circuit representation of the VIRT CEMS in Fig. 1, one must be able to identify the conductive paths around the core, but these are defined by the changing switch states. Furthermore, the connecting electrical circuit cannot be clearly resolved into separate loops. For example, conductors exist around the core in order to parallel the dc buses of the rectifiers. One clear set of "terminals" between the transformer and the connecting electronics cannot be identified. Thus, a different modeling framework is required in order to synthesize circuit representations of the VIRT, and of CEMSs in general.

In the original description of the VIRT in [9], [10], a simplified modeling approach was proposed which relies on the following assumptions:

- The core, gaps, and connecting electronics are symmetrically distributed about the center of the transformer core.
- 2) Identical distributed rectifier structures are used (i.e. a half-bridge terminates each half-turn).
- 3) Negligible flux exits the core (e.g. owing to shorted conductive paths around the core).
- 4) Conductors encircling the core have negligible loss.

These assumptions have been sufficient for devising effective models that have matched well with experiment, and have also enabled the design of high performing prototypes [9]-[14], [16]. One key limitation is that they do not allow quantification of, or insight into, the possible flow of currents on the dc bus connections outside of the core. Additionally, the requirement of system symmetry may not be ideal for packaging of a given VIRT implementation, but asymmetric constructions cannot be investigated under these assumptions. Should designers be interested in these details or in exploring other CEMS implementations, it is essential to have a modeling approach which allows the core construction, choice of electronics, and physical asymmetry to be arbitrarily specified. Furthermore, the complete description offered by a general modeling framework provides important insight and clarity to designers seeking to improve their understanding of how a particular CEMS operates.

It should be noted that the approach in [9], [10] has been the only proposal for modeling these kinds of systems from first principles. Other fractional-turn transformer implementations which rely on physically distributed electronics have simply stated a schematic representation for the given magnetic structure [17]–[19]. A clear modeling basis is critical to allow these implementations to be completely described, including the possible influence of wrapping conductors, and also provides a framework for extensions of these concepts. Another recent work describes a different concept for a "fractional turn" in which it is proposed that a transformer can be wound with a secondary having a winding length that is less than one full turn [20]. In that work, the circuit schematic of the transformer is again not modeled from first principles. Critically, if such modeling is performed it becomes apparent that the operation of the transformer must be defined in terms of complete loops, and this highlights that one cannot truly have conduction in less than one turn. Modeling approaches for these kinds of structures are essential for ensuring their accurate description and loss prediction, and for providing a consistent basis from which designers can understand these systems.

In this paper, a modeling approach is proposed which allows a designer to specify an arbitrary electronic configuration around a magnetic core and systematically produce a full switching model of this CEMS. To the authors' knowledge, this is the first such proposal in the literature. In Section II, an overview of the VIRT CEMS is provided for clarity, and in Section III the general CEMS modeling procedure is described. Then, two experimental case studies are evaluated, serving both to illustrate the method and also to demonstrate the utility and performance of the proposed approach. The method is found to produce models which match well with experiment.

II. OVERVIEW OF THE VIRT

For clarity, an overview of the VIRT is provided here. There are four half-bridge pairs in Fig. 1: Q_1 and Q_2 , Q_3 and Q_4 , Q_5 and Q_6 , and Q_7 and Q_8 which operate in a complementary manner (e.g. if Q_1 is on, Q_2 is off). When Q_1 , Q_4 , Q_6 and Q_7 are switched in-phase, the VIRT is operating in fullbridge/full-bridge (FB/FB) mode - one can view the system as comprising an upper FB rectifier and a lower FB rectifier which are connected by conductors through the transformer window. Each of these rectifiers has a local dc bus defined by the load resistance R_T or R_B and a decoupling/output capacitance C_T or C_B . Four wires (or traces on a printed circuit board (PCB)), modeled by resistors R_{GL} , R_{VoL} , R_{VoR} , and R_{GR} in Fig. 1, connect the local dc bus of each fullbridge rectifier so that they are tied to a single output port, and these can be assumed to be short-circuits for understanding the key working principle. Under the modeling assumptions described in the introduction, the result of FB/FB operation is that the output voltage is inserted twice into the single loop around the center-post of the transformer [10]. If there are N_p primary turns, the step-down ratio between the primary of the transformer and the output is N_p : 1/2 – twice the physical turns ratio of the transformer. The current in this loop is also half as large for the same output power, greatly reducing copper loss [16]. The VIRT can also be operated in

¹The distinction of whether these switches behave as rectifiers or inverters depends on the direction of power flow and is inherently unimportant. Here they are described as rectifiers for convenience, as many common topologies, such as the LLC resonant converter, feature transformers which connect directly to rectifiers on their secondaries.

half-bridge/half-bridge (HB/HB) mode by holding Q_4 and Q_6 on while switching Q_1 and Q_7 in-phase. The output voltage is now inserted only once into the single loop, changing the effective ratio of the VIRT to N_p : 1. While this key operating principle has been validated by experiment, the simplified assumptions of previous models do not enable insight into the finer details of this system, such as the impact of the bus connections, and they are not clearly extendable to other CEMS implementations.

III. GENERAL MODELING PROCEDURE

It is assumed that the designer begins with a 2D representation of the CEMS by taking a cross-section of the system on the plane that the electronics are on. This results in a circuit which envelops cross-sections of magnetic material. Furthermore, the designer must also have a description of the complete magnetic core structure. The depiction of the VIRT in Fig. 1 is one such example of this representation.

The key insight in the modeling approach is that the 2D representation described above can be directly interpreted as both a conventional electrical circuit schematic and as the physical topology of the system. This allows the well-established formalism of circuit analysis to be applied with a simple augmentation to account for the physical constraints imposed by the system.

The modeling procedure is described below, and it shifts between the electrical (circuit) perspective of the 2D representation and the magnetic (physical) perspective as described in Table I.

- 1) **Enforce switch states** to yield linear time-invariant circuit stages (as in conventional switching circuit analysis).
- 2) Count the number of nodes, n, and branches, b, in the circuit in a conventional way, as if the core sections were not there. For clarity, this work uses the definitions in [21]. Specifically, a node is "a point at which two or more elements have a common connection" and a branch is "a single path, containing one simple element, which connects one node to any other node."
- 3) Count the number of loops, p, that encircle core sections but are part of a single node in the circuit. This additional step accounts for the fact that the circuit physically couples to a magnetic core, and therefore, by Faraday's law, KVL around a closed loop is not necessarily zero (owing to linked flux). There are inductive elements associated with these loops which are not "visible" in the circuit diagram but which must be counted.
- 4) Identify KVL loops in the circuit. There are b-n+p+1 independent loops. This many loops must be identified and numbered, and each component must be part of at least one loop. For convenience they should be selected such that they have clearest mapping to the magnetic circuit model (e.g. by having loop currents around single core leg sections).
- Create a magnetic circuit model using the KVL loop currents. The currents associated with each identified KVL loop can be directly mapped into the magnetic circuit domain.

- Transform the magnetic circuit model into an electric circuit. This proceeds in a straightforward manner [8], [22].
- 7) Use KVL relations to insert electronic components into the electric circuit. At this stage, the nature of the electric circuit model is clear, but the connecting components have not yet been interfaced. Care must be taken in doing this as a single component may be part of many KVL loops. Each component must insert the same voltage drop in every loop that it connects to, and must carry the sum of the currents in these loops. This insertion of voltage and summation of current characteristic is identical to the behaviour of an ideal transformer. Thus each component is interfaced through an ideal transformer to the circuit model. The same behaviour can be modeled with pairs of dependent sources [22].

In the remainder of the paper, this modeling procedure is applied to two case studies in order to further clarify the steps involved and to demonstrate the efficacy of the approach².

IV. CASE STUDY 1: RESISTIVE NETWORK

The first case study provides a pedagogically valuable example of how to use the modeling approach. The relatively simple configuration in Figs. 2a and 2b is considered in which a resistive network is distributed around a magnetic core having N_p primary turns around the center post. This is not a CEMS as it does not involve electronic components, but the ambiguous nature of the secondary winding (i.e. that clear individual windings cannot be identified) is an example where the proposed approach can be useful.

This circuit has two nodes (n=2) as indicated in Fig. 2c, two branches (b=2), and two single-node loops enveloping core sections (p=2). Thus in total there are three independent KVL loops. A natural choice for these loops is the three paths around each of the core legs indicated in Fig. 2d. The direction of these loops is unimportant as long as they are carefully tracked, but are selected as shown in Fig. 2d with knowledge that flux in the outer legs flows in the opposite direction as flux in the center post.

The currents associated with the three loops can be mapped into the magnetic circuit model shown in Fig. 3a. This model includes reluctances \mathscr{R}_L , \mathscr{R}_M , and \mathscr{R}_R corresponding to the left, middle, and right gaps, respectively, and reluctance \mathscr{R}_e associated with the out-of-core "external" path (ref. Fig. 2b). \mathscr{R}_{lk} is also added, corresponding to the path for leakage fields between the primary and the resistive network.

The magnetic circuit model is transformed into an equivalent electric circuit model by taking its dual, mutating permeances into inductances, and then adding ideal transformers [8], [22]. Note that the model inductances relate to the core reluctances as $L_M = 1/\mathscr{R}_M$, $L_L = 1/\mathscr{R}_L$, $L_R = 1/\mathscr{R}_R$, $L_{lk} = N_p^2/\mathscr{R}_{lk}$ and $L_e = 1/\mathscr{R}_e$.

²It is also worth highlighting that the proposed modeling framework is valid for the 'base case' in which the electronics are connected to the magnetic component in a conventional way, without being fundamental to defining its conductive loops. Thus, it can be used generally for modeling magnetic components connected to electronics.

TABLE I: The modeling steps, which shift between an electrical (circuit) perspective and a magnetic (physical) one.

Electrical (Circuit) Domain	Magnetic (Physical) Domain
1. Enforce switch states	
2. Count circuit nodes (n) and branches (b)	
	3. Count the single-node loops encircling core sections (<i>p</i>)
4. Identify $b - n + p + 1$ KVL loops	
	5. Use the loop currents to create a magnetic circuit model
6. Transform the magnetic circuit model of Step 5 into an	
electric circuit model	
7. Replace loop current sources in the model of Step 6 with	
the circuit components comprising each loop	



Fig. 2: Resistive network used in Case Study 1. (a) Circuit definition. (b) Core definition with axis of cross-section in (a) shown. N_p primary turns are wound in series around the center post as shown in green. (c) Circuit with the two nodes highlighted. (d) Selected loops.



Fig. 3: Models for Case Study 1. (a) Magnetic circuit. (b) Electric circuit with current source inputs. (c) Final circuit model.

TABLE II: Planar transformer construction for Case Study 1.

Stackup	SSPPSS	Primary trace width	0.428 mm
Number of turns	115511	Copper weight	2 oz/ft^2
Secondary width (in window)	3.16 mm	Board thickness	1.6 mm
Layer- to-layer spacing	0.24mm	Material	FR-4

In this simple case, each resistor is part of only one loop, and the current sources associated with each KVL loop can be directly replaced with each of these resistors as shown in Fig. 3c. This is the same model that would be obtained if R_L , $R_T + R_B$ and R_R were connected via separate windings around the left, center, and right posts, respectively, demonstrating an equivalence which may not have been clear on initial inspection of the circuit.

A. Case Study 1: Experimental Evaluation

The experimental prototype shown in Fig. 4 is built having $N_p = 10$ primary turns and resistor values of $R_T = R_B =$ 1.2 Ω , $R_L = 0.5\Omega$, and $R_R = 8.2\Omega$. A back-to-back EQ20 core with a 20 mil gap across all three legs and a set of planar windings described in Table II are used. The transformer is wound with all four secondary layers in parallel and the two primary layers in series. The associated inductances in the model of Fig. 3c, as determined from the gaps, are $L_M = 0.146 \mu$ H, and $L_L = L_R = 0.073 \mu$ H. The resistances of the planar windings and the 2 mil copper foil used to make the required connections are assumed to be negligible compared to the relatively large connecting resistors. The leakage inductance is measured to be 0.9μ H. The external reluctance is estimated to be 3.66×10^7 A/Wb using a 3D ANSYS Maxwell Finite Element Analysis (FEA) simulation as described in Section IV-B.

The model of Fig. 3c is simulated in PLECS and is com-



Fig. 4: Experimental prototype used in Case Study 1.

TABLE	III: C	Compar	ison betwe	en sim	nulatio	on and e	expei	rime	ent
in Case	Study	1. The	amplitude	es and	time	delays	to V	T_T a	are
shown.									

	$\mathbf{V}_T = \mathbf{V}_B$	\mathbf{V}_L	\mathbf{V}_R
100kHz			
Sim.	0.07V	0.058V, 0ns	0.058V, 0ns
Exp.	0.075V	0.06V, 0ns	0.07V, 0ns
1MHz			
Sim.	0.294V	0.218V, 75ns	0.295V, -32ns
Exp.	0.29V	0.19V, 110ns	0.36V, -34ns

pared to measurements³ at 100kHz and 1MHz. The results are shown in Table III and Fig. 5. Qualitatively, note that at low frequencies, the low impedance of the inductances dominate the parallel R-L branches of the model, and the voltages on the four resistors are similar. At high frequencies, the resistors dominate these branches and significant asymmetry is seen. Quantitatively, however, the 1MHz results show some error in the phase and amplitude of the predicted waveforms, and these are explored in the next section.

B. Case Study 1: Model Sensitivity

While the model produces results which match closely with experiment, it is insightful to understand what kind of physically reasonable changes in the estimated parameters improve this matching. The errors in the 1MHz results are in the estimates of V_L and V_R , which are related to the impedances of the branch containing L_e , L_L in parallel with R_L , and L_R in parallel with R_R .

 R_L and R_R have a tolerance of 5%. Shifting either or both of these resistances to their extremes has a negligible effect on the model, thus the error cannot be attributed to the tolerance of these resistors. This leaves the estimates in L_e , L_R , and



Fig. 5: Comparison between experimental (solid blue lines) and simulated results (dashed black lines) for Case Study 1. (a) 100kHz. (b) 1MHz. (c) 1MHz after parameter estimate updates discussed in Section IV-B.

 L_L as possible sources of error. Fig. 6 plots the error between the model and experiment associated with varying the external reluctance estimate between 0.5-1.5 times, and the estimate of the gap length between 14 and 25 mils. Because the inductor is uniformly gapped on all three legs, variation of this gap length is equivalent to varying the inductors L_R and L_L in the model. Namely, $L_R = L_L = \frac{\mu_0 A_{c,e}}{2g}$, where $A_{c,e}$ is the effective crosssectional area of the gap (assumed equal to that of the EQ20 core, 59mm²), g is the gap length, and μ_0 is the permeability of free space. Fig. 6 shows that a significant reduction in the modeling error is obtained if the external reluctance estimate and the length of the gap are both smaller than originally estimated. For example, Fig. 5c shows the improved matching

³A function generator excites the primary with a sinusoidal voltage at the studied frequency and the voltage on each resistor is measured using a Tektronix P6251 differential probe connected to a Tektronix MSO4104 oscilloscope.



Fig. 6: Error between the model and experiment in Case Study 1 with variations in the estimated gap length (used to estimate L_L and L_R) and external reluctance.

of the model at 1MHz if g = 14 mils and R_e is 2.64×10^7 A/Wb (0.7 times the original estimate).

It is unlikely that the gap length itself is less than 20 mils, as the plastic material used to define the gap is stiff. It is instead suspected that this relatively long gap enables sufficient fringing paths so as to increase the effective cross-sectional area. A verification of this is that the measured magnetizing inductance of 10.4μ H is higher than what is predicted strictly from the gap reluctances (7.3 μ H), and is similar to the result of assuming q = 14 mils (or equivalently, assuming a 1.4 times larger cross-sectional area for the gaps). Thus, the model is improved by more precisely estimating the reluctance of the gaps to include fringing effects. While this is not unique to the proposed modeling approach, the result of overestimating the gap reluctances is more significant here owing to the finer details that the model is able to capture (e.g., if the main output variables were V_T and V_B , they remain very well predicted even with the original parameter estimates).

Error in the external reluctance estimate is expected owing both to the fact that this reluctance is inherently affected by the environment of the experiment, which is not considered in the estimate, and because of the nature of the estimate itself. This estimate is obtained from a 3D ANSYS Maxwell simulation in which one turn is wound around the center-post of an ungapped EQ20/EQ20 core, and is excited by a 1A current at 1MHz. The external reluctance is estimated by modeling the system using the circuit in Fig. 3a with i_1 , i_2 , and i_3 set to zero such that $\mathscr{R}_e = \frac{1 - \phi_M \mathscr{R}_M}{\phi_E}$, where \mathscr{R}_M is estimated from the core geometry, and the mid-post flux, ϕ_M , and external flux, ϕ_e , are extracted from the simulation. A relatively small energy error tolerance of 0.003% is specified in the solver to improve the estimate of the fringing flux. However, the requirement to estimate this small external flux is a likely source of error. A means to more precisely estimate the external reluctance, including the details of the real-world environment around the transformer, will improve the accuracy of the model.

Overall, the results of the model using the originally es-



Fig. 7: Half-turn VIRT model used in Case Study 2. The circuit and core definition are shown in Fig. 1. (a) Stage 1. (b) Stage 2. (c) Stage 1 with nodes highlighted. (d) Loops used to synthesize magnetic circuit model.

timated parameters match well with experiment, and errors are reasonably attributed to difficulties in precisely estimating the gap reluctances including fringing flux and the external reluctance. Using simplified estimates for these parameters remains useful, and the analysis in this section provides guidance on how to relate observed errors to the model parameter estimates.

V. CASE STUDY 2: HALF-TURN VIRT

In the second case study, the modeling procedure is applied to a half-turn VIRT as defined in Figs. 1a and 1b. Between the bottom and top rectifiers, finite resistance bus connections are used, modeled by R_{VoL} , R_{VoR} , R_{GL} , and R_{GR} for the leftside V_o connection, right-side V_o connection, left-side ground connection, and right-side ground connection, respectively. Decoupling capacitors C_T and C_B provide a local decoupling path for each rectifier. If the half-bridge operating modes of the VIRT are employed, blocking capacitors are required as shown. It is assumed that these blocking capacitors are large enough that they do not interfere with the ac operation of the VIRT, and thus they can be treated as short-circuits during modeling.

There are two switching states of interest, defined by the switching action of the rectifiers⁴. These states are drawn in Figs. 7a and 7b. Each state has two nodes (n=2) (as indicated in Fig. 7c), six branches⁵ (b=6), and no single-node loops (p=0). Thus there are five independent KVL loops. A natural choice for these five loops is to define: two loops around the left post, one encompassing R_{GL} and the other R_{VoL} ; two loops around the right post, one encompassing R_{GR} and the other R_{VoR} ; and one loop around the center post encompassing R_T , C_T , and R_B , C_B . In the second switching state, the same

⁴Note that additional switching stages can be defined, if desired, including a "dead time" stage, or asymmetric switching operation of the rectifiers.

⁵The parallel resistor-capacitor network loading each rectifier is counted as one component.



 $\begin{array}{c|c} & \mathcal{R}_{L} & \mathcal{R}_{M} \\ & \mathcal{R}_{L} & \mathcal{R}_{M} \\ & \mathcal{R}_{R} \\$

Fig. 9: Models for the CEMS in Case Study 2. (a) Magnetic circuit. (b) Electric circuit with current source inputs.

(b)

operational insight into the VIRT. Then, the full switching model is presented.

odel. A. Case Study 2: Fundamental Harmonic Approximation Model

As is often the case in modeling, a more intuitive representation can be achieved by applying simplifying constraints (i.e. by accepting less precision in the model). One motivation of employing the modeling approach described in this paper is to assess potential circulating currents in the VIRT. In particular, it is valuable to understand what factors influence current flow on the bus connectors, especially since it is desirable for there to be negligible power loss in these elements associated with induced ac currents. While the full switching model described in Section V-B provides a means to assess this with detail in simulation, two simplifying assumptions can be employed to analytically describe this circulating current.

First, it is assumed that all voltages and currents in the system can be modeled as sinsuoids. This fundamental harmonic approximation (FHA) is appropriate when the VIRT is used in an LLC converter operating near its resonant frequency [23], for example. Because sinusoids are half-wave symmetric, application of the FHA requires only one of the two switching stages to be analyzed. Assuming that the on-resistance of the switches is negligibly small, this reduces the number of connections that must be made to the circuit of Fig. 9b from 14 to 6. Furthermore, only the two load connections are part of multiple KVL loops, and thus only two ideal transformers need to be added. The FHA allows the top and bottom load connections to be modeled by an equivalent resistance $R_{T,e}$ and $R_{B,e}$, respectively. The resulting circuit is shown in Fig. 10a and is assembled systematically. Namely:

Fig. 8: Definition of the five loops used in the VIRT model. (a)-(e) show loops 1-5, respectively.

five loops can be identified. This means that the magnetic circuit derived from the first state is the same as in the second state, confirming that the magnetic coupling is invariant under switching as expected from the original modeling of the VIRT in [10]. These five loops can be drawn around the core as shown in Fig. 7d and their precise definition is shown in Fig. 8.

From the identified loops, the magnetic circuit model in Fig. 9a can be derived and transformed into the circuit model in Fig. 9b. This model again includes reluctances \mathscr{R}_L , \mathscr{R}_M , and \mathscr{R}_R corresponding to the left, middle, and right gaps, respectively, reluctance \mathscr{R}_e associated with the out-of-core "external" path, and \mathscr{R}_{lk} corresponding to the path for leakage fields between the primary and secondary. The model inductances relate to the core reluctances as $L_M = 1/\mathscr{R}_M$, $L_L = 1/\mathscr{R}_L$, $L_R = 1/\mathscr{R}_R$, $L_{lk} = N_p^2/\mathscr{R}_{lk}$ and $L_e = 1/\mathscr{R}_e$.

The remaining step is to connect the 8 switches, 2 load connections, and 4 bus resistors to this model. It will be shown that the full switching model of the VIRT can be constructed in a systematic way using this circuit and the definition of the loops associated with each current in Fig. 8. However, the 14 component connections yield a circuit which, although being general and straightforward to input into a simulation, is visually complicated and tedious to study analytically. Thus, a simplified model is first described which provides useful



Fig. 10: Model of the half-turn VIRT under the fundamental harmonic approximation (a) Circuit. (b) Simplified circuit assuming $R_{VoL} = R_{GL} = R_{VoR} = R_{GR} = 2R_o$

- 1) Current source $\{i_1, i_2, i_3, i_4\}$ is replaced with $\{R_{VoL}, R_{GL}, R_{VoR}, R_{GR}\}$ connected in series with the primary winding of an ideal 1:1 transformer. The secondary of this transformer connects across $\{R_{B,e}, R_{B,e}, R_{T,e}, R_{T,e}\}$. Set notation is used for conciseness⁶.
- 2) Current source i_5 is replaced with the primary windings of two ideal 1:1 transformers connected in series. The secondary of one of the transformers connects to $R_{T,e}$. The secondary of the other transformer connects to $R_{B,e}$.

This circuit can be further simplified by assuming that $R_{VoL} = R_{GL} = R_{VoR} = R_{GR} = 2R_o$, representing the case where the bottom rectifier connects to the top rectifier using identical conductors on both sides of the core. Additionally, assume that $L_L = L_R = L_M/2$, representing that the outer core legs have equal reluctances which are twice as large as the center-post reluctance, and that $R_T = R_B = R_L$ (i.e. that the rectifiers are loaded equally). These are assumptions of symmetry that have been employed in all implementations of the VIRT thus far [9]–[16], and they yield the circuit model in Fig. 10b. Because the rectifiers are connected to a dc output, the load resistance of the top and bottom rectifiers can be mapped to an equivalent resistance of $R_{T,e} = R_{B,e} = \frac{8}{\pi^2}R_L$ [24].

The current through each bus connector in this simplified

circuit is

$$i_o = -\frac{V_m}{2R_o} \frac{1}{\left(1 + \frac{L_M}{L_e}\right) + j\frac{\omega L_M}{2R_o}} \tag{1}$$

which has magnitude

$$|i_{o}| = \frac{V_{m}}{\sqrt{4R_{o}^{2}\left(1 + \frac{L_{M}}{L_{e}}\right)^{2} + \omega^{2}L_{M}^{2}}}$$
(2)

A number of useful insights are obtained from this analysis:

- 1) If the external flux path is assumed to be arbitrarily large such that no flux exits the core, then $L_e \rightarrow 0$ and there is no current induced on the dc bus connections, as was the expectation from the original simplified modeling of the VIRT [10]. Note that applying $i_o = 0$ and $L_e = 0$ to the schematic of Fig. 10b results in the same model as derived in that original study as well.
- 2) The ratio of L_M to L_e is a key determiner of the induced current. In particular, the gap reluctances should be much smaller than the external reluctance in order to minimize this current. This is typically the case as simple gap reluctance estimates break down for very large gap lengths⁷.
- A large bus connector resistance reduces the magnitude of induced current.

B. Case Study 2: Full Switching Model

The full switching model yields a more complicated but complete representation of the system. This model can be constructed in a systematic way from the circuit in Fig. 9b and the definition of the loops associated with each current in Fig. 8 using the following procedure:

- 1) Draw the rectifiers on the schematic of Fig. 9b
- For each loop definition in Fig. 8, replace the current source associated with that loop with the physical rectifier connections. These connections must be made through ideal transformers.

For clarity, the replacement of the current sources $i_1 - i_5$ in Fig. 9b with their physical connections is described below:

- 1) Current source $\{i_1, i_2, i_3, i_4\}$ is replaced with $\{R_{VoL}, R_{GL}, R_{VoR}, R_{GR}\}$ connected in series with the primary windings of two ideal 1:1 transformers. The secondary of one of the transformers connects across switch $\{Q_1, Q_2, Q_3, Q_4\}$. The secondary of the other transformer connects across switch $\{Q_5, Q_6, Q_7, Q_8\}$. The transformer polarities are selected to match the physical connections. Set notation is used for conciseness⁸.
- 2) Current source i_5 is replaced with the primary windings of two ideal 1:1 transformers connected in series. The secondary of one of the transformers connects between

⁶For example, current source i_1 is replaced with R_{VoL} connected in series with the primary winding of an ideal 1:1 transformer. The secondary of this transformer connects across $R_{B,e}$.

⁷In the limit, removal of the endplate yields the largest possible gap and the reluctance of the "gaps" become similar to the external reluctances of the core.

⁸For example, current source i_1 is replaced with R_{VoL} connected in series with the primary windings of two ideal 1:1 transformers. The secondary of one of the transformers connects across switch Q_1 such that it inserts its source-drain voltage. The secondary of the other transformer connects across switch Q_5 such that it inserts its drain-source voltage.



Fig. 11: Full switching model of the half-turn VIRT in Fig. 1. The transformer couplings are indicated by matching coloured/dashed lines. All unlabeled transformers have a turns ratio of 1:1.

the source of Q_1 and the source of Q_3 . The secondary of the other transformer connects between the source of Q_5 and the source of Q_7 .

The resulting switching model is shown in Fig. 11. It is highly coupled, making it more difficult to study analytically than the simplified FHA model in Fig. 10b. However, it is easily input into simulation software. Furthermore, note that if the external reluctance is assumed to be arbitrarily large, the dc bus connections are assumed to be ideal short-circuits, and the outer gap reluctances are equal ($L_L = L_R$) then the transformers connected to each of the switches can be removed and the original VIRT model (derived under these assumptions) is produced [10].

C. Case Study 2: Experimental Evaluation

The experimental evaluation interfaces the VIRT with a stacked-bridge LLC converter having the configuration in Table IV. The detailed design and operation of this converter is described in [14]. This VIRT is designed to operate in FB/FB or HB/HB mode to interface a 380V dc bus to a 5V or 9V output, respectively. The system schematic is shown in Fig. 12. The experimental prototype is shown in Fig. 13.

In FB/FB mode the resonant tank is excited at 1.07MHz and $R_T = 1\Omega$ while in HB/HB mode, the frequency is 1.26MHz and $R_T = 1.72\Omega$. In both cases, R_B is disconnected reflecting the situation where all dc power is extracted at only one port (thus, dc currents are expected to flow on the dc bus connections around the core). Note that the stacked-bridge inverter operates in voltage quartering mode as described in [10], [25]. The inverter switches are estimated to have a C_{oss} of 150pF and the rectifiers a C_{oss} of 1400pF. These capacitors can be directly added to the switching model by placing them in parallel across their respective switches.

The dc connections between the two rectifiers are established by using four Litz wire bundles. This allows both a clearer estimate of the impedance of these connections, and



Fig. 12: Stacked-bridge LLC inverter which drives the VIRT in Fig. 11 in the experimental evaluation of Case Study 2.

allows them to be probed⁹ to measure any circulating currents. Each bundle comprises six 480/48 litz wires which are 4.4 inches long. The resulting impedance of each of the four dc bus connections is shown in Table IV. Note that the left-side resistances are larger because the Litz bundles are connected to pads on the PCB which themselves connect to the rectifiers through traces on the PCB. On the other hand, on the right side, there is a direct connection of the Litz bundles to the rectifiers. These different physical connections also account for the different inductance measurements. The inductance of these wires can be directly added to the simulation by placing inductors in series with the bus resistances. The external reluctance estimate for the back-to-back EQ20 core is 3.66×10^7 A/Wb as discussed in Section IV-B. A switch on-resistance of $3.3 \text{m}\Omega$ is assumed and modeled by a resistor in series with each switch.

1) FB/FB Mode: First, FB/FB mode is considered with a 380V input and 5V output at 25W. Fig. 14 compares the experimental measurements of v_{inv} , i_{Lr} , the currents in the dc bus connections, and the drain-source voltages of Q2, Q4, Q6, and Q8, to results obtained from a PLECS simulation of the schematic in Fig 12. The simulation matches well with experiment. The dc bus currents are reasonably well predicted, having an error of 25-50% in estimated peak-topeak magnitude and a 2-25% error in their estimated mean values. These errors may be attributable to a sensitivity in the estimate of the external leakage reluctance and the relatively small bus connection impedances, and the fact that significant (un-modeled) dead time exists between the two rectifier switching states when in this below-resonance operating point. The sensitivity of the model is discussed in Section V-D.

Importantly, the estimated and measured results highlight that the induced ac current does not yield a significant increase in the rms current carried by each dc bus connection (which must carry approximately 2.5A of dc current, net, to the output). Additionally, the triangular currents in the bus connections have a fundamental component at the switching frequency of approximately 0.43Apk, much lower than the (approximately) 4.7Apk carried in the half-turns. Thus, the case study demonstrates that minimal ac current is induced into the wrapping dc bus connections in this example typical VIRT design, and also that these currents, and the overall operation of the converter, can be well predicted by the switching model.

⁹TCP202 current probes were used.

Component	Value
Inverter	
GaN FETs	350V EPC2050
VIRT Rectifiers	
MOSFETs	30V TPN2R703NL
Blocking capacitors,	3x 4.7uF/25V/0805 per rectifier,
C_{block}	C2012X7R1E475K125AB
Decoupling capacitors,	2x 4.7uF/25V/0805 per half-bridge,
C_d	C2012X7R1E475K125AB
Output capacitors, C_o	12x 10uF/25V/1210,
	C3216X7R1E106K160AB
LLC	
Resonant capacitor	4.87 nF
Resonant inductor	4.1 μ H derived from transformer leak-
	age
VIRT Transformer	
Core	EQ20+EQ20/ML91-S, 0.127 mm gap
	on all legs
Primary windings	$N_p=10 - 450/48$ Litz wire wound in
	three layers $(4/4/2)$. 3.3mm separation
	to secondary windings.
Secondary windings	Two parallel-connected half-turn sec-
	ondaries each comprising 8 paralleled
	450/48 Litz wire segments.
dc Bus Connections	
V _o left-side	1.6m Ω in series with 40nH
Ground left-side	1.6m Ω in series with 40nH
V _o right-side	$0.9 \mathrm{m}\Omega$ in series with $60 \mathrm{nH}$
Ground right-side	$0.9 \mathrm{m}\Omega$ in series with $60 \mathrm{nH}$

TABLE IV: Components used in prototype for Case Study 2.

The model can also be used to evaluate highly asymmetrical arrangements. To demonstrate this, the FB/FB mode described above is re-evaluated but with the right-side dc bus connections removed (i.e. $R_{VoR} \rightarrow \infty$ and $R_{GR} \rightarrow \infty$). Fig. 15 compares experiment to simulation and again good agreement between them is seen. Importantly, the bus connection asymmetry does not significantly change the behaviour of the converter except for reducing the ac current that is induced on the remaining dc bus connections (and changing its wave shape). It is again suspected that differences in wave shape are attributable to finer details of the switching circuit which are not accounted for in the model, or to sensitivity in the estimate of the external leakage reluctance and the bus connection impedance as discussed in Section V-D. Ultimately, in terms of practical impact on design, these ac bus currents are estimated to be very small and measurement confirms this.

2) HB/HB Mode: The HB/HB mode can be modeled using the same procedure as in the FB/FB mode, and the resulting circuit is the same except that the rectifiers are connected as half-bridges (i.e. Q_1/Q_2 and Q_7/Q_8 operate in-phase as halfbridge rectifiers. Q_4 and Q_6 are held on while Q_3 and Q_5 are held off) and the blocking capacitors must be included in the simulation model. These can be added directly to the schematic in Fig. 11, in the same manner as described in Section V-B. The converter interfaces a 380V input to a 9V/45W output. Fig. 16 compares the experimental results to those obtained from a PLECS simulation. There is again good matching between the model and experiment, though there



<complex-block>

 Input connector

 Vol. Connection

 GR Connection

Fig. 13: Experimental prototype used in Case Study 2. (a) Top. (b) Bottom.

is an additional unexpected curvature in the experimental dc bus currents associated with the left dc bus connections. The errors in peak-to-peak values are similar for each bus current as in FB/FB mode (18-51%) consistent with there being a sensitivity to measuring the relatively small dc bus connections or the estimate of the external leakage reluctance. These errors are explored in Section V-D. Critically, the ac current induced in the bus connections again negligibly increases their rms current carrying requirement, and the triangular currents have a fundamental component at the switching frequency of approximately 0.35Apk, much lower than the approximately 8.4Apk carried in the half-turns – these insights are well captured by the simulation model.

The right-side dc bus connections are again removed and the results in Fig. 17 are obtained. This yields a larger error between the simulated and measured circulating currents (e.g.



Fig. 14: Comparison between experimental (solid blue lines) and simulated results (dashed black lines) for Case Study 2, FB/FB mode.



Fig. 15: Comparison between experimental (solid blue lines) and simulated results (dashed black lines) for Case Study 2, FB/FB mode with right-side bus connections removed.



Fig. 16: Comparison between experimental (solid blue lines) and simulated results (dashed black lines) for Case Study 2, HB/HB mode.

0.7Ap-p measured vs. 0.3Ap-p estimated) compared to the removal of the right-side bus connections when operating in the FB/FB configuration, and this error is explored in Section V-D. Ultimately, this measured current is again negligibly small in comparison to the dc current that is carried by these connections (approximately 2.5A) and compared to the peak current in the windings (approximately 8.4Apk) – information obtained from the model provides useful insight into its operation and the existence of these bus currents.

D. Case Study 2: Model Sensitivity and Tuning

The model outputs match well with experiment, but there are some discrepancies in the estimates of the bus-connection currents. Unlike the sensitivity exploration for Case Study 1 (ref. Section IV-B), the model here is highly coupled, involves many more parameters, and is not LTI, impeding a quantitative description of its sensitivity to the parameter estimates. Instead, in this section the model parameters are 'tuned' for better matching to the experiment, within a reasonable physical basis, and the qualitative effect of changing a given parameter is described. It is emphasized that the intent here is not to select parameters that yield waveforms which exactly match with experiment in each of the four cases, but to show how certain reasonable errors in estimating the model parameters can affect the model output. The changes in the 'tuned' model are:

1) Increasing the external reluctance estimate, \mathscr{R}_e , by 1.5 times, which reduces the ac magnitudes of all the bus currents. As discussed in Section IV-B, the nature of this external reluctance path makes it inherently difficult to accurately estimate, and an error on the order of 50% is believed by the authors to be reasonable.





Fig. 17: Comparison between experimental (solid blue lines) and simulated results (dashed black lines) for Case Study 2, HB/HB mode with right-side bus connections removed.

- 2) Increasing the inductance estimate of the two bottom-side dc bus connections, the left-side V_o connection and the right-side ground connection, by 10nH, which reduces the ac current in those connections, and increases the ac current in the right-side V_o connection and the left-side ground connection. It is reasonable to assume that these connections have higher inductance since they include the additional inductance associated with traversing through the PCB. Furthermore, an error of 10nH is reasonable given the relatively low inductances being assessed, and the importance of the physical orientation of the connections in determining that value.
- 3) Increasing the resistance estimate of the left-side bus connections from $1.6m\Omega$ to $2.25m\Omega$, which reduces the dc current flowing through the left-side connections, and increases the current in the right-side connections. The left-side includes the connections on the PCB, and an error here could be attributable to the approximate nature of the estimate, the neglect of ac resistance effects in the PCB connections [26], or a sensitivity in measuring the resulting $0.65m\Omega$ resistance difference.
- 4) Accounting for the differences in the capacitance of the ceramic capacitors in the 5V and 9V cases owing to their ferroelectric nature [27], [28], and modeling the physical distribution of the capacitors by including a 0.5nH parasitic inductance between the half-bridges. These have the effect of changing the wave-shape of the bus currents to be more 'curved' and less triangular. This change is discussed in more detail in Appendix A.

The tuned results for the four cases are shown in Figs. 18, 19, 20, and 21 and there is better agreement between the model and experiment. In particular, the model captures part of the

Fig. 18: Comparison between experimental (solid blue lines) and simulated results after tuning (dashed black lines) for Case Study 2, FB/FB mode.

'curved' i_{GL} and i_{VoL} waveshapes in Figs. 20 and 21, related to modeling the distributed decoupling capacitors. Errors in the dc current level of 0.1-0.2A may be attributable to tolerances in zeroing the TCP202 current probes. There remains a significant error in estimating the bus currents in the HB/HB case with right-side connections removed. In particular, the predicted i_{VoL} appears to be 180 degrees out-of-phase. It is possible that this operating point is near a resonance related to the parasitic inductances on the PCB and the distributed capacitors, which would account for an increase in amplitude and a change in phase. Certain combinations of these parameters (e.g. tripling the decoupling inductance) do appear to yield a resonance in the model which results in these bus current amplitudes being closer to what is measured in experiment. The differences in capacitance between the 5V and 9V cases could also explain why this effect is only seen in the 9V case. This may be a useful point for future investigation, though it is sensitive to accurate estimates of these parameters. Ultimately, while these refinements produce a more accurate description of the physical system, the estimates obtained without this tuning remain effective for design, demonstrate the accuracy that can be obtained using straightforward estimates of the model parameters, and enable improved understanding of the operation of this coupled electronic and magnetic system.

VI. CONCLUSION

This paper presents a modeling approach for coupled electronic and magnetic systems (CEMSs), including the Variable Inverter/Rectifier Transformer (VIRT). These CEMSs are magnetic components in which electronics complete the conductive loops around the core. Their tight coupling between the magnetic and electronic domains make them ill-suited for





Fig. 19: Comparison between experimental (solid blue lines) and simulated results after tuning (dashed black lines) for Case Study 2, FB/FB mode with right-side bus connections removed.



Fig. 20: Comparison between experimental (solid blue lines) and simulated results after tuning (dashed black lines) for Case Study 2, HB/HB mode.

Fig. 21: Comparison between experimental (solid blue lines) and simulated results after tuning (dashed black lines) for Case Study 2, HB/HB mode with right-side bus connections removed.

application of conventional modeling techniques. While these systems are emerging and have been employed in numerous studies, no previous work has proposed a general modeling framework through which to synthesize their electrical circuit representations. The proposed approach takes advantage of the dual interpretation of a 2D representation of the CEMS as either a conventional electrical circuit schematic or a description of the physical topology of the system, and, unlike earlier proposals for their modeling, the resulting electrical circuit representation can be made without requiring any explicit assumption on system symmetry, rectifier construction, or current flow in external connections made around the transformer. The method is applied to two case studies, one in which the secondary comprises a simple but ambiguous resistive network, and another which evaluates a VIRT employed in a 380-5V or 9V stacked-bridge LLC dc/dc converter prototype. In both cases, the experimental results match well with PLECS simulations of the derived electrical models. The proposed approach captures details which have not been studied in prior investigations of the VIRT and other fractional-turn transformers. Namely, the model allows potential ac currents induced on wrapping dc connections to be estimated. These currents are shown to be relatively small in experiment and a simplified model of the VIRT employing the fundamental harmonic approximation provides analytical insight into the key determiners of the magnitude of this current. Highly asymmetric VIRT constructions are also shown to be well modeled. Errors between the models and experiment are reasonably attributed to difficulties in accurately estimating certain model parameters. The proposed approach is suitable both for assessing finer details of the VIRT and as a framework



Fig. 22: Updated rectifier models to account for local capacitor distributions. (a) Upper rectifier. (b) Lower rectifier.

for deriving and understanding new CEMS implementations.

APPENDIX A DECOUPLING CAPACITOR DISTRIBUTION

The accuracy of the model can be improved by accounting for the differences in capacitance between the 5V and 9V cases owing to the different dc biases applied to the capacitors and their different operating frequencies. In the 5V case, the updated estimates are $C_o = 148\mu$ F, $C_{block} = 15.6\mu$ F, and $C_d = 8.8\mu$ F, while in the 9V case they are $C_o = 176\mu$ F, $C_{block} = 14.7\mu$ F, and $C_d = 7.4\mu$ F¹⁰ [27], [28].

A further improvement is to account for the physical displacement of these capacitors on the PCB. Fig. 13 shows that each bridge interfaces to its own local decoupling capacitor, while the main output capacitor is physically located next to Q_3 . The connections between the low side switches and the ground node of the decoupling capacitors are low inductance because they return on a plane on the second layer of the PCB (approximately 4 mils of vertical separation). However, the V_o nodes of the decoupling capacitors (e.g. next to Q_5 and Q_7) are connected on the third layer of the PCB, resulting in approximately 1.2mm of vertical separation. The resulting inductance of this connection is approximately 0.5-1.5nH, with the lower value used in Section V-D owing to it yielding good matching. This is implemented in the model as shown in Fig. 22. A strength of the modeling framework is that these kinds of physical details can be added in a straightforward manner.

ACKNOWLEDGMENT

This work was supported by the Cooperative Agreement between the Masdar Institute of Science and Technology (Masdar Institute), Abu Dhabi, UAE and the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA - Reference 02/MI/MIT/CP/11/07633/GEN/G/00. The authors also thank Plexim GmbH for generously providing access to their PLECS software.

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¹⁰Although the higher dc bias yields a larger degradation in capacitance at 9V, the higher operating frequency means the capacitor operates closer to its resonance – this is accounted for as an increase in the effective capacitance as per the manufacturer's datasheet and may be another source of modeling error.

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