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Enumeration and Analysis of DC-DC Converter Implementations based on Piezoelectric Resonators

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***Abstract*—Demand for power electronics with smaller volume, lighter weight, and lower cost will eventually require new converter energy storage technologies with fundamentally higher power density and efficiency limits. This motivates investigation into piezoelectric resonators (PRs), which offer very high power density and efficiency capabilities and significantly improved scaling properties compared to magnetics. PRs have been used in power conversion previously, but the realm of possible converter implementations using only PRs for energy storage has seen little exploration. In this work, we enumerate and evaluate dc-dc converter topologies and switching sequences that best utilize a PR as the only energy storage component, and that enable low-loss resonant "soft charging" of the PR's input capacitance and voltage regulation capability. To compare these implementations, we present analysis techniques for their operation and periodic steady state solutions considering practical constraints. In addition, we provide useful techniques for estimating PR utilization and efficiency, which we validate experimentally in a 200-100 V, 25 W rated prototype. This prototype exhibits peak efficiency >99% as well as high efficiency (≥96%) across a wide range of operating conditions, illustrating the promise of PR-based converters for high voltage, low power applications.**

This paper is accompanied by an instructional video for selecting and analyzing PR-based dc-dc converter implementations.

***Index Terms*—converter topologies, dc-dc power converters, piezoelectric resonators, piezoelectric transducers, switching sequences, soft charging, zero voltage switching**

I. Introduction

Power electronics face ever-increasing demands for miniaturization, integration, and lower cost that are becoming challenging to meet with conventional design strategies. Miniaturization tends to be limited by the sizes and performance of energy storage components, especially magnetics, which typically comprise a large portion of a converter's volume. Significant advances in power density have been realized through approaches that minimize the sizes of magnetics (e.g., higher switching frequencies, improved magnetic materials/design [3]–[5]). However, the achievable power densities of magnetics fundamentally decrease as volume reduces, inherently impeding miniaturization [6]. Switched capacitor converters and their hybrid counterparts (e.g., [7]–[10]) have achieved record-high power densities, but these designs nonetheless require magnetic components for efficient voltage regulation.

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Hence, an opportunity exists for new energy storage mechanisms in power conversion that can offer major advances in achievable power density with high efficiency. One prospect is piezoelectric energy storage, which stores energy in the mechanical inertia and compliance of a piezoelectric material and can be realized in the form of single-port piezoelectric resonators (PRs) or multi-port piezoelectric transformers (PTs). Piezoelectric components have significantly improved scaling properties compared to magnetics, and emerging piezoelectric materials such as lithium niobate show very high promise in both achievable power density and achievable efficiency [11], [12]. In addition, piezoelectrics offer highly-planar form factors, natural isolation barriers (PTs), batch fabrication capabilities, and the potential for a high degree of integration.

While piezoelectric materials have been used extensively for sensing, actuation, transduction, and energy harvesting applications, their adoption in power conversion has been more limited. The concept has a long history [13], and PTs have seen widespread use in fluorescent back light drivers, often augmented with one or more magnetic component(s). The use of PTs in power converters has been explored similarly with external magnetic components to help achieve zero voltage switching (ZVS) [14], though this reduces their potential power density advantages. Magnetic-less converter variations with ZVS have been realized using both PTs (e.g., [15]–[21]) and PRs (e.g., [22]–[28]), but typically with limited power and/or performance capability and without investigation into the full realm of possible converter implementations.

In this paper, we conduct a systematic enumeration and downselection of dc-dc converter switching sequences and topologies that best leverage PRs as their only energy storage components. In particular, we focus on switching sequences that facilitate low-loss resonant charging/discharging ("soft" charging) of the PR's input capacitance and provide voltage regulation capability. To analyze and compare implementations, we demonstrate methods for mapping PR state trajectories across a switching cycle and solving for their periodic steady state solutions with practical constraints. We then evaluate PR utilization with each implementation and provide low-computation tools for estimating efficiency. An experimental prototype based on a commercially-available PR demonstrates promising implementations and validates the proposed analysis techniques. Through its effective utilization of the PR, this prototype achieves significantly improved performance compared to previous PR-based converter designs.

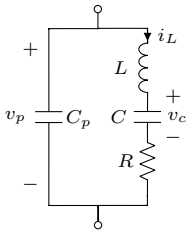

Fig. 1. Butterworth-Van Dyke circuit model for PRs [29], [30].

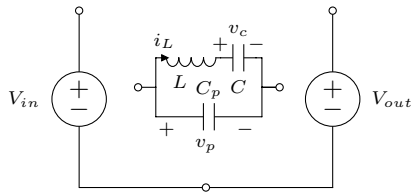

Fig. 2. Common-negative system considered for switching sequence enumeration, illustrated with an ideal PR.

II. Switching Sequence Enumeration

A PR is commonly modeled using the Butterworth-Van Dyke circuit model shown in Fig. 1, which serves as a basis for how we conceptualize the PR's behavior. This model contains the PR's physical input capacitance C_p in parallel with an LCR branch that models its electromechanical resonance properties [29], [30]. In this enumeration process, we aim to identify converter switching sequences that enable soft charging of C_p at all voltage transitions to minimize switching loss.

We begin with a non-inverting "common-negative system" as shown in Fig. 2 that contains only a PR for energy storage (these concepts also apply to other topologies including common-positive variants). There are a finite number of ways the PR's terminals can be connected in this source/load system, and each of these connections defines a possible *stage* of a switching cycle. These stages can be categorized as:

- Connected stages: the PR's terminals are connected to the source/load system such that v_p is fixed (denoted with capital V_p) at some combination of V_{in} and/or V_{out}, illustrated in Figs. 3(a)-(f).
- Zero stages: the PR's terminals are short-circuited ($V_p = 0$) as shown in Fig. 3(i).
- Open stages: the PR's terminals are open-circuited, allowing v_p to increase or decrease through resonance as shown in Figs. 3(g)-(h).

Connected stages allow the PR to interact with the source/load system, while zero and open stages are useful for redistributing energy within the PR. We permute these stage types to create *switching sequences*, defined as order-specific arrangements of the stages described above across a switching period. To facilitate soft charging of C_p at each stage transition, this permutation considers only switching sequences that alternate connected/zero stages with open stages. Thus, we refer to a switching sequence by the order of its connected/zero stages named by PR terminal voltage (V_p), assuming an open stage between each (e.g., V_{in}, V_{in}-V_{out}, V_{out}). We further constrain this enumeration for switching sequences with:

1) A minimum number of stages.
2) At least one connection to each of V_{in} and V_{out}.
3) At least two connected stages (to balance energy transfer to/from the PR over a switching period).
4) No repetition of the same connected/zero stage.

These criteria limit the search to switching sequences with only even numbers of stages, with a minimum of four (including open stages). We differentiate between duplicate sequences as follows: Rearranging the order of a switching sequence's stages results in a different switching sequence,

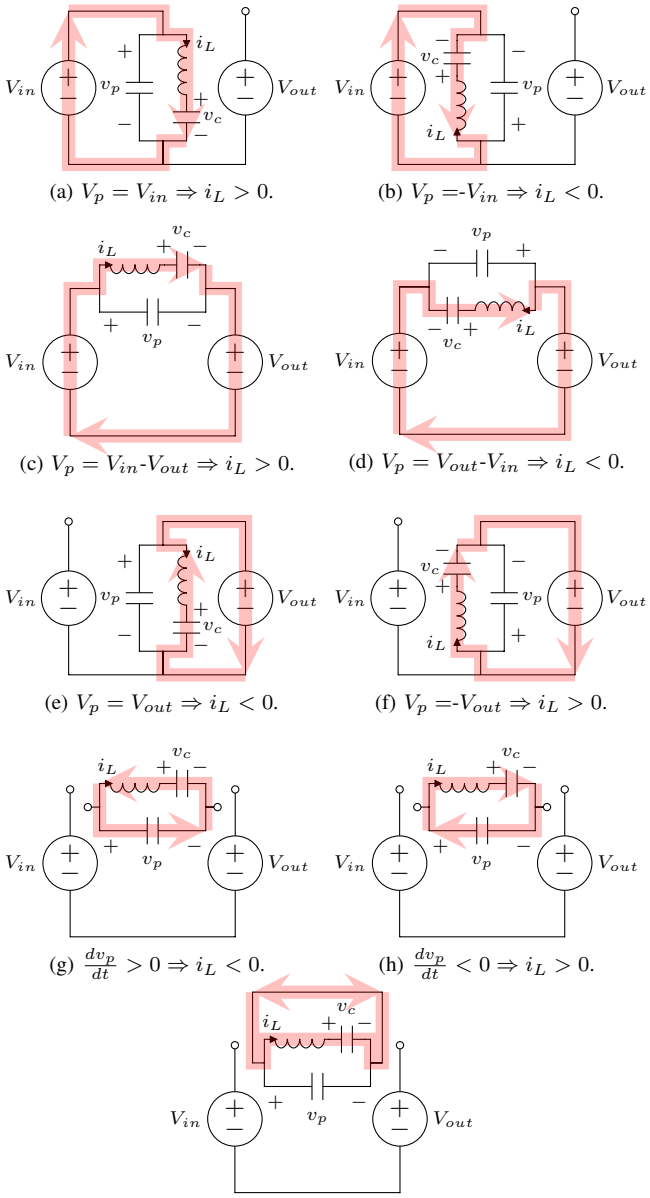

Fig. 3. Assumed current paths for each connected stage (a)-(f), open stage (g)-(h), and zero stage (i), illustrated with an ideal PR.

whereas rotating the stages (in the same order) to a different "first" stage results in the same switching sequence. Further, inverting *all* stages of a switching sequence results in the same switching sequence (with opposite PR polarity). Enumerating all possible sequences and filtering the results according to these criteria yields 7 distinct four-stage switching sequences and 33 distinct six-stage sequences (full list in Appendix A).

III. Switching Sequence Downselection

The enumerated set of switching sequences can be reduced based on physical requirements for power conversion and practical considerations. For this downselection process, we make the assumption that positive average power flow *from* V_{in} and/or *to* V_{out} is desired *for each connected stage*. For this to be true, i_L must be on average positive during connected

TABLE I
EXAMPLE i_L POLARITY MAPPINGS FOR $V_{in} > 2V_{out}$

V_p sequence A:	V_{in}	open	$V_{in}-V_{out}$	open	V_{out}	open
i_L polarity:	+	+	+	+	-	-
V_p sequence B:	V_{in}	open	$V_{out}-V_{in}$	open	$-V_{out}$	open
i_L polarity:	+	+	-	-	+	-

stages where V_p = V_{in}, V_{in}-V_{out}, or -V_{out} and on average negative for connected stages where V_p = -V_{in}, V_{out}-V_{in}, and V_{out}. Average i_L polarity constraints also apply to open stages, which require a particular charge redistribution to charge/discharge v_p. Positive i_L removes charge from C_p and therefore decreases v_p, while negative i_L increases v_p. These assumed current polarities are illustrated for each stage type in Fig. 3 (zero stages have no inherent i_L polarity requirement).

A. PR Resonant Cycle

We first focus on switching sequences that can be completed in only one PR resonant period (one cycle of energy exchange between L and C). A sequence that spans more than one resonant period would require more redistribution of energy within the PR during open and zero stages (still dissipating energy in R), higher and/or bidirectional switch blocking requirements (if v_p peaks during an open stage), or connected stages with significant reverse power flow to avoid these.

To investigate this, the aforementioned i_L polarity constraints can be mapped for each stage of a switching sequence as shown in Table I, where + and - indicate positive or negative i_L as required by the necessary charge transfer. For a switching sequence to be completed in one PR resonant cycle, it must require only one span (one or multiple stages back-to-back) of positive i_L and only one span of negative i_L like Sequence A in Table I. Sequence B requires multiple spans of each and therefore traverses more than one cycle. Filtering the potential switching sequences to only those that can be completed in one cycle leaves 7 four-stage and 20 six-stage switching sequences for each of $V_{in} > V_{out}$ and $V_{in} < V_{out}$.

B. PR Energy and Charge Balance

Periodic steady state operation requires balance of both energy and charge on the PR across the switching period [23]. For six-stage switching sequences (easily adapted to four-stage), the following Conservation of Energy (CoE) equation must hold. For the n^{th} stage, E_n is the energy delivered to the PR, V_{pn} is a constant value of v_p, and q_n equals the net charge transferred by i_L (q_n has the same polarity specified for i_L):

$$E_1 + E_3 + E_5 = V_{p1}q_1 + V_{p3}q_3 + V_{p5}q_5 = 0 \tag{1}$$

Switching sequences for which the energy terms in this equation are either all positive or all negative (ie. the only solution is $q_1 = q_3 = q_5 = 0$) are not capable of balancing the PR's energy and can therefore be eliminated.

Furthermore, the following Conservation of Charge (CoC) equations must hold for C_p and C, respectively:

$$q_2 + q_4 + q_6 = 0 \tag{2}$$

$$q_1 + q_2 + q_3 + q_4 + q_5 + q_6 = 0 \tag{3}$$

Combining these two equations shows that the charge transfer during connected/zero stages must also be balanced:

$$q_1 + q_3 + q_5 = 0 \tag{4}$$

Inserting (4) into (1) results in a general equation that must be satisfied to ensure energy balance and charge balance on the PR for a given switching sequence. The solution to this equation *with correct q polarities* yields the complete voltage conversion range for which this balance holds and the switching sequence is useful. Appendix B contains an example voltage conversion range derivation using this procedure, and the conversion ranges for the final proposed switching sequences are summarized in Table II. Switching sequences for which this general equation cannot be satisfied without $q_1 = q_3 = q_5 = 0$ are not capable of both energy and charge balance and can be eliminated. Switching sequences for which only specific voltage conversion ratios can satisfy this equation (e.g., $V_{in} = V_{out}$ or $V_{in} = 2V_{out}$) cannot regulate voltage and are therefore also removed. Filtering according to these criteria eliminates all four-stage switching sequences; *no four-stage switching sequences can satisfy our assumptions outside of fixed voltage conversion ratios*. By contrast, 9 six-stage sequences (each with step-up and step-down versions) are capable of balancing the PR's energy and charge across wide ranges of voltage regulation.

C. Switch Implementation

The circuit topologies and switch implementations needed to realize these switching sequences vary widely in terms of switch quantity and voltage blocking capability. A converter with a high number of switches is more complex to implement, and switches that block bidirectional voltage are difficult to physically realize. In general, each distinct terminal connection requires its own switch, and there are three node options (positive input, positive output, ground) to which both terminals can be tied for zero stages. For the six-stage sequences in this study, implementations that require less than or more than four switches require at least one bidirectional voltage blocking switch. If we filter to switching patterns that only require four unidirectional-blocking switches (inclusive of three-switch topologies with one bidirectional-blocking switch), 5 switching sequences prevail each for step-up and step-down operation. An alternative enumeration/downselection strategy beginning with this practical implementation assumption is described in Appendix C and yields the same result. The remainder of this paper focuses on these switching sequences, summarized in Table II.

IV. RESULTING IMPLEMENTATIONS

Table II summarizes the step-up and step-down versions of the 5 switching sequences reached in Section III along with their associated topologies and constraints; details regarding this information are provided below. The sequences for $V_{in} > V_{out}$ each have time-reversed duals for $V_{in} < V_{out}$, resulting in some sequences that are the same for both cases while

TABLE II
SUMMARY OF PROPOSED SWITCHING SEQUENCES, TOPOLOGIES, AND CONSTRAINTS

Switching Sequence	Feasible Voltage Conversion Range	General Practical Constraints	Topology (Fig. 4)	Modification for Soft Switching (required if only 2 active switches used)	K
V_{in}-V_{out}, *Zero*, V_{out}	$V_{in} > 2V_{out}$	$i_{L1}, i_{L4} = 0$ ⬠	(a)*	$i_{L4}, i_{L6B} = 0$, $V_{p6B} = V_{in}$ ○	$\frac{V_{in}}{2(V_{in}-V_{out})}$
	$2V_{out} > V_{in} > V_{out}$	$i_{L3}, i_{L6} = 0$ ⬠	(a)	$i_{L3}, i_{L6B} = 0$, $V_{p6B} = V_{in}$ ○	$\frac{V_{in}}{2V_{out}}$
V_{in}, V_{in}-V_{out}, V_{out}	$2V_{out} > V_{in} > V_{out}$	$i_{L1}, i_{L4} = 0$ ⬠	(a)	$i_{L1}, i_{L4B} = 0$, $V_{p4B} = 0$ ○	$\frac{V_{in}}{2V_{out}}$
V_{in}-V_{out}, -V_{out}, *Zero*	$V_{in} > V_{out}$	$i_{L1}, i_{L4} = 0$ □	(c)†	$i_{L1}, i_{L4B} = 0$, $V_{p4B} = -V_{in}$ △	$\frac{1}{2}$
			(e)*	$i_{L4}, i_{L6B} = 0$, $V_{p6B} = V_{in}$ ◇	
			(f)*	No change	
V_{in}, *Zero*, V_{out} (explored in [23])	$V_{in} < V_{out}$	$i_{L3}, i_{L6} = 0$ ■	(b)*	$i_{L2B}, i_{L6} = 0$, $V_{p2B} = V_{in}$-V_{out} ▲	$\frac{1}{2}$
			(d), (i)*	No change	
	$V_{in} > V_{out}$	$i_{L1}, i_{L4} = 0$ □	(c)	$i_{L1}, i_{L4B} = 0$, $V_{p4B} = V_{out}$-V_{in} △	
			(a), (h)*	No change	
V_{in}, -V_{out}, *Zero*	Any	$i_{L1}, i_{L4} = 0$ ✳	(e)	No change	$\frac{\max(V_{in}, V_{out})}{2(V_{in}+V_{out})}$
V_{in}, *Zero*, V_{out}-V_{in}	$2V_{in} < V_{out}$	$i_{L3}, i_{L6} = 0$ ⬟	(d)	$i_{L3}, i_{L6B} = 0$, $V_{p6B} = V_{out}$ ●	$\frac{V_{out}}{2(V_{out}-V_{in})}$
	$V_{in} < V_{out} < 2V_{in}$	$i_{L1}, i_{L4} = 0$ ⬟	(d)*	$i_{L4}, i_{L6B} = 0$, $V_{p6B} = V_{out}$ ●	$\frac{V_{out}}{2V_{in}}$
V_{in}, V_{out}-V_{in}, V_{out}	$V_{in} < V_{out} < 2V_{in}$	$i_{L3}, i_{L6} = 0$ ⬟	(d)*	$i_{L2B}, i_{L6} = 0$, $V_{p2B} = 0$ ●	$\frac{V_{out}}{2V_{in}}$
V_{in}, V_{in}-V_{out}, *Zero*	$V_{in} < V_{out}$	$i_{L1}, i_{L4} = 0$ ■	(b)*	$i_{L4}, i_{L6B} = 0$, $V_{p6B} = V_{out}$ ▲	$\frac{1}{2}$
			(e)	$i_{L1}, i_{L4B} = 0$, $V_{p4B} = -V_{out}$ ♦	
			(g)*	No change	

(*) can be realized with only two active switches, and (†) requires opposite v_p polarity. Markers next to i_L constraints correspond to Fig. 12.

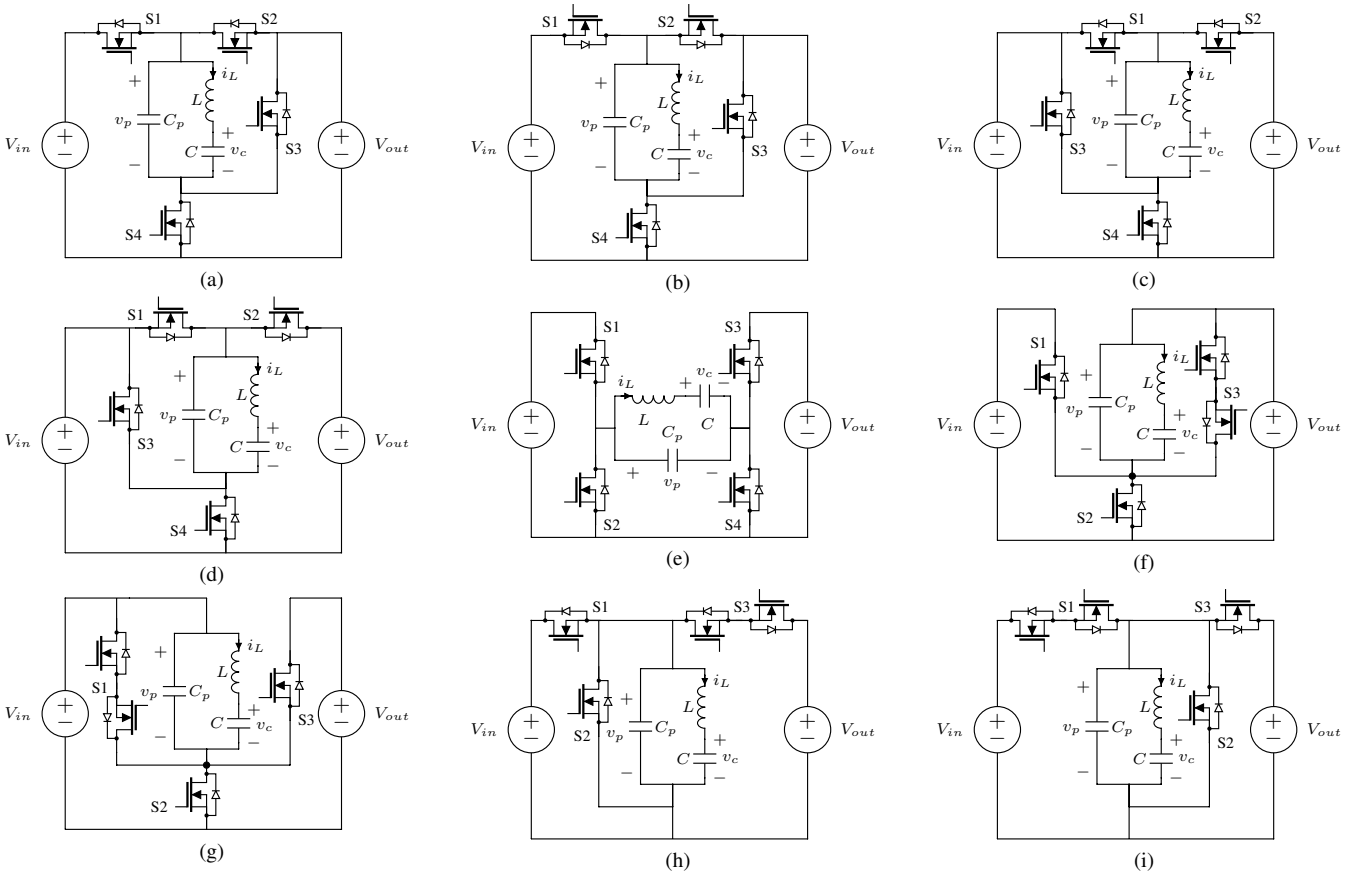

Fig. 4. Derived converter topologies requiring only four unidirectional-blocking switches. All switches are displayed as MOSFETs, but many can be implemented with diodes (specific to the switching sequences). Switching sequences and other details for these topologies are displayed in Table II.

others are different (amounting to 8 total distinct sequences). The 9 topologies for realizing these sequences are displayed in Fig. 4. It should be noted that some of these topologies have two switch nodes (ie. both PR terminals each connect to two source/load system nodes), and some have only one (ie. the other PR terminal is fixed).

The attached instructional video contains suggestions for selecting and analyzing a PR-based converter implementation using the information in Table II. The supported voltage conversion ranges are calculated as described in Section III-B. The general practical constraints refer to the necessary i_L zero crossings for all-positive instantaneous power transfer with unidirectional-blocking switches described in Section VII-A, where i_{Ln} refers to i_L at the start of the n^{th} stage. The zero crossing modifications for soft switching are those described in Section VII-B, and likewise refer to i_L and V_p at the start of the indicated stage. The symbols next to the i_L constraints correspond to the efficiency curves in Fig. 12, and K refers to the charge transfer utilization factor described in Section VIII-A. Topologies (*) can be realized with only two active switches, and topology (†) requires opposite v_p polarity.

V. State Plane Visualization

For each switching sequence, we can visualize the internal behavior of the PR and how it interacts with the source-load system by plotting its state (v_p, v_c, and i_L) trajectories on a pair of state planes as shown in Fig. 5 (this technique is commonly used for resonant converter analysis [31]–[36]). The assumed i_L polarities for each stage as mapped in Table I can be used to expedite this process; the stages directly relate (in order) to the positive and negative i_L portions of the state planes. The *starting point* of each stage is indicated by number label, and the positions of these labels correspond to the numbered variable states used to solve for a periodic steady state solution in Section VI. For periodic steady state operation, the final variable states must equal the initial variable states, creating complete loops on the state planes. To ensure soft charging of C_p, v_p must resonate to exactly V_p for the next connected/zero stage in time for that stage to begin. The state planes of Fig. 5 correspond to the time-domain waveforms of Fig. 6, which exhibit these desired behaviors. The attached instructional video contains stage-by-stage construction of these example state planes.

During all connected/zero stages (1, 3, and 5) on the state planes, v_p stays constant (V_p) at some combination of $\pm V_{in}$, $\pm V_{out}$, and 0 depending on the PR terminal connections. L and C resonate in the equivalent circuit of Fig. 7(a) or 7(b), with i_L and v_c exhibiting LC-normalized circular arcs (if with no loss) around a center point of (0, V_p) on the i_L vs. v_c plane. i_L reflects the same vertical change on the i_L vs. v_p plane at constant V_p. The PR acquires and releases energy during connected stages, and whether its energy increases or decreases depends on the polarities of V_p and i_L.

During all open stages (2, 4, and 6), all three state variables participate in resonance, and the effective capacitance reduces to the series combination of C_p and C:

$$C_{eff} = \frac{C_p C}{C_p + C} \tag{5}$$

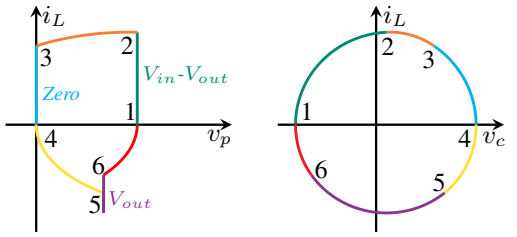

Fig. 5. State plane example for switching sequence V_{in}-V_{out}, *Zero*, V_{out} with V_{in} = 100 V, V_{out} = 40 V, and P_{out} = 6 W. Numbers 1-6B correspond to the time-domain points indicated in Fig. 6. PR parameters: Table III.

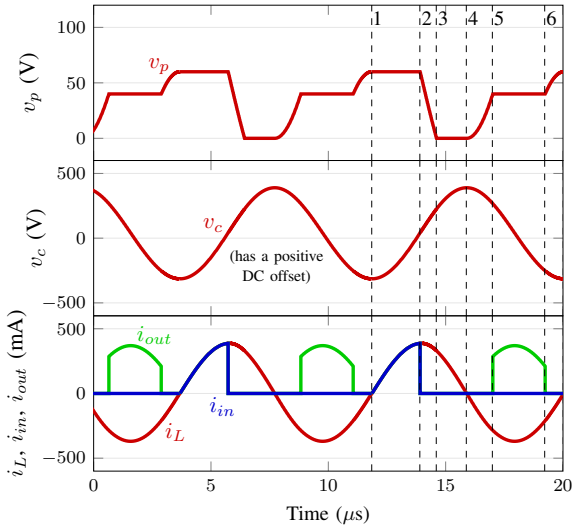

Fig. 6. Time-domain waveforms for switching sequence V_{in}-V_{out}, *Zero*, V_{out} with V_{in} = 100 V, V_{out} = 40 V, and P_{out} = 6 W. Numbers 1-6B correspond to the state transition points in Fig. 5.

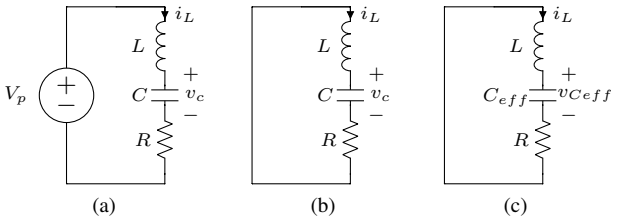

Fig. 7. Resonant circuits for (a) connected stages, (b) zero stages, and (c) open stages.

The center of resonance on the state plane during open stages is less straightforward. i_L is still centered around 0, and the center of resonance for v_{Ceff} is also 0, yielding the resonant circuit in Fig. 7(c). This mandates that the center of resonances (V_o) for v_p and v_c both be equal to the following function of capacitance and initial states for the stage, using stage 2 as an example (full derivation in Appendix D):

$$V_o = \frac{C_p v_{p2} + C v_{c2}}{C_p + C} \tag{6}$$

The C_p terms in the above equations can be modified to include parasitic capacitance if desired, which is described in Appendix E. R does not affect the center of resonance for either connected or open stages, but it does damp the resonance (and therefore dissipates energy) during both.

VI. Periodic Steady State Solution

Quantifying variable states and their exact locations on a state plane requires solving the six-stage system for periodic steady state. The ideal version of this solution (neglecting R) can be obtained with light computation and provides a close estimate of the exact solution to the extent that $R \to 0$. The exact periodic steady state solution (considering R) must be obtained numerically as described in Appendix F. The below analysis does not consider the effects of parasitic capacitances in the circuit (e.g., switch capacitances); these can be added by modifying C_p as described in Appendix E.

A. Ideal Solution

We can solve for the ideal periodic steady state solution for a given switching sequence using equations that enforce CoE and CoC across the switching cycle, assuming the final variable states equal the initial variable states and that v_p always reaches the voltage necessary to soft-charge C_p. These equations rely only on the state variable values at each switching stage transition point, with their subscript numbers indicating the stage that follows (corresponding to the number labels in Fig. 5). Since v_p is defined for each of these points, there are two total variables for each stage (v_c and i_L).

Connected stages have the following CoE constraint, where v_p is defined (V_p) based on the PR's terminal connections. Intuitively, V_p can be considered the DC voltage offset for C as it resonates with L.

$$C(v_{c1} - V_p)^2 + Li_{L1}^2 = C(v_{c2} - V_p)^2 + Li_{L2}^2 \tag{7}$$

Open stages for the PR have both a CoE constraint and a CoC constraint since v_p changes through resonance with the PR's other elements.

$$C_pV_{p2}^2 + Cv_{c2}^2 + Li_{L2}^2 = C_pV_{p3}^2 + Cv_{c3}^2 + Li_{L3}^2 \tag{8}$$

$$C_p(V_{p3} - V_{p2}) = -C(v_{c3} - v_{c2}) \tag{9}$$

These equations can be solved using an analytic solver constrained by the i_L polarity requirements in Section III. Six-stage sequences have three connected stages and three open stages, which translate to nine total equations and twelve variables before applying practical constraints (further described in the attached instructional video).

B. Ideal Switching Times

Once an ideal periodic steady state solution has been obtained, the time duration of each stage can be calculated using the exact variable states at each stage transition. A simple strategy for this involves multiplying the resonant period of a given stage's equivalent circuit times the proportion of its resonant period completed during the stage. For a connected stage, this translates to calculating the angle between the two vectors created by the stage's start and end points (both referenced to the center of resonance (V_p,0)) on the i_L vs. v_c normalized state plane. If a connected stage occurs in only one quadrant of the state plane, that angle can be calculated and used to calculate the stage's time duration as follows:

TABLE III
Assumed PR Model Parameters [37]

Parameter:	C_p	L	C	R	f_{res}
Value:	4.3 nF	1.4 mH	1.4 nF	$\leq$ 2.4 Ω	114 kHz

$$t_1 = \sqrt{LC}\left(\tan^{-1}\left(\frac{i_{L2}\sqrt{L/C}}{v_{c2} - V_p}\right) - \tan^{-1}\left(\frac{i_{L1}\sqrt{L/C}}{v_{c1} - V_p}\right)\right) \tag{10}$$

Similarly, the time duration of an open stage can be calculated using the angle between the vectors created by the stage's i_L and inductor voltage (V_p-v_c) start and end points (both referenced to (0,0)). This takes the following form for an open stage in one quadrant of the i_L vs. $V_p - v_c$ state plane, and can then be multiplied by the LC_{eff} resonant period to calculate time duration:

$$t_2 = \sqrt{LC_{eff}}\left(\tan^{-1}\left(\frac{i_{L3}\sqrt{L/C_{eff}}}{V_{p3} - v_{c3}}\right) - \tan^{-1}\left(\frac{i_{L2}\sqrt{L/C_{eff}}}{V_{p2} - v_{c2}}\right)\right) \tag{11}$$

For any stage that spans more than one quadrant of the state plane, this strategy for calculating stage time duration still applies but one must consider each quadrant when calculating the angle between the vectors.

VII. Practical Constraints

Degrees of freedom in the periodic steady state system of equations can be used to apply constraints for desired operation. In this work, we implement constraints that improve performance by requiring only positive instantaneous power transfer and, in some cases, zero-voltage soft switching (ZVS) of the transistors serving as switches.

A. Positive Instantaneous Power Transfer

The general i_L polarity assumptions in Section III can be extended to require these i_L polarities for the entirety of each stage, ensuring all-positive *instantaneous* power transfer. Constraining for only positive instantaneous power transfer both from the source and to the load removes loss due to current durations that do not provide net energy transfer between the PR and the source/load system. With unidirectional voltage blocking switches, this constraint requires v_p to resonate to exactly its desired voltage, without overshoot, during open stages before the highest and lowest V_p connections. Also, i_L must change polarity exactly when v_p reaches the desired voltage for those stages as exemplified in the state plane of Fig. 5. This defines the i_L zero crossing point for one or both halves of the resonant cycle.

Some switching sequences have a zero stage either during or surrounding an i_L zero crossing, so the definition of the exact crossing point does not affect instantaneous power transfer to or from the source/load system. In these cases, the zero stage itself can also be constrained for only single direction current flow to prevent unnecessary current segments, with the polarity of i_L determined by CoC equation (4).

Thus, the two i_L zero crossing points can be defined for all switching sequences, and resulting i_L variable constraints are

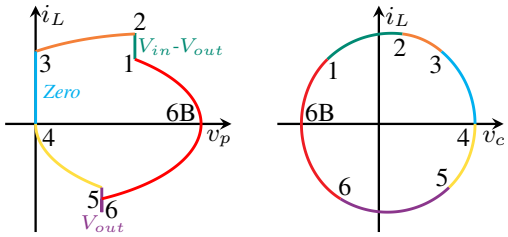

Fig. 8. State plane example for soft-switched sequence V_{in}-V_{out}, *Zero*, V_{out} with V_{in} = 100 V, V_{out} = 40 V, and P_{out} = 6 W. Numbers 1-6B correspond to the time-domain points indicated in Fig. 9. PR parameters: Table III.

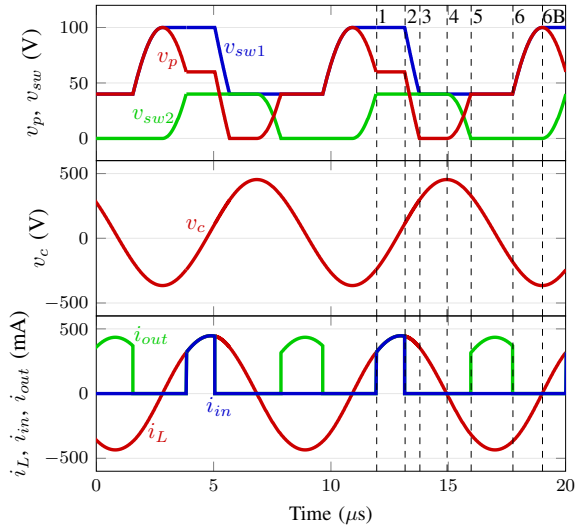

Fig. 9. Time-domain waveforms for soft-switched sequence V_{in}-V_{out}, *Zero*, V_{out} with V_{in} = 100 V, V_{out} = 40 V, and P_{out} = 6 W. v_{sw1} and v_{sw2} refer to the switch nodes between S1, S2 and S3, S4, respectively, in Fig. 15. Numbers 1-6B correspond to the state transition points in Fig. 8.

summarized under "General Practical Constraints" in Table II. They reduce the degrees of freedom in the periodic steady state system of equations to only one, which can be used to modulate power.

B. Soft Switching

All of the viable implementations summarized in Table II facilitate soft charging of the PR, but not necessarily ZVS of the switches. Topologies that have only one switch node (ie. one terminal of PR is tied to the source/load system) inherently require ZVS in order to soft charge the PR since C_p and all switch capacitances exist between the same switch node and a fixed DC voltage. Thus, ZVS naturally occurs across the entire six-stage switching sequence for topologies (f)-(i) in Fig. 4.

For topologies that have two switch nodes (ie. neither terminal of PR is tied to the source/load system as in topologies (a)-(e) of Fig. 4), six-stage sequences require at least one open stage during which both switch nodes change voltage. Barring specific conversion ratios, the necessary voltage changes at each of the two nodes tend to require different time durations and/or opposite i_L polarities during this open stage.

ZVS can be ensured for topologies (a)-(e) of Fig. 4 if the open stage during which both nodes change voltage is *split into two sections*. For the general case, this two-part open stage can be used to change the two node voltages one at a time, with a V_p constraint at the transition point. This way, one of the PR terminals is always clamped at a DC voltage during the open stage, and the transition between the two parts of the open stage can take place at a zero crossing for i_L if the two nodal voltage transitions require opposite i_L polarities. Fig. 8 illustrates this concept with the soft-switched version of the V_{in}-V_{out}, *Zero*, V_{out} switching sequence in topology (a) of Fig. 4, with corresponding time-domain waveforms shown in Fig. 9. During its two-segment sixth stage, this implementation must resonate v_p up to V_{in} for ZVS turn-on of S1 (at point 6B) before reducing v_p to V_{in}-V_{out} for soft switching of S3.

Altering an open stage in this way to achieve soft switching in topologies (a)-(e) requires modification of the i_L zero-crossing constraints for all-positive instantaneous power transfer with unidirectional blocking switches. These modifications are displayed in Table II along with the V_p constraint for the i_L zero crossing between the open stage's two parts (subscript "B" indicates this transition point). This V_p constraint suggests the presence of a potential fourth connected stage (and therefore an eight-stage switching sequence) if held for longer than infinitesimal time duration, which is explored in Appendix G.

C. Minimal Active Switches

Fig. 4 shows active switch implementations for all switches, but at least one switch in each topology can be replaced with a diode to reduce control complexity. There are two zero crossings for i_L each cycle, and a switch that turns off at a zero crossing to satisfy the i_L constraints in Table II can be implemented with a diode if it also blocks voltage in the appropriate direction. This is the case for one switch each in Figs. 4(f)-(i), reducing the number of active switches to two (counting the bidirectional blocking pair as one switch) for these topologies. Topologies (a), (b), (d), and (e) can also be reduced to only two active switches for certain switching sequences, with the other two switches realized with diodes. These implementations require (and ensure) soft switching with the current constraints in Table II, which greatly reduces the complexity imposed by those constraints. All topology and switching sequence combinations that can be implemented using only two active switches are distinguished with (*) next to their required current constraints in Table II.

VIII. PR Utilization

The efficiency of a PR-based converter depends on not only on the PR's properties (e.g., material, dimensions, loss factors, etc.) but also how effectively its implementation uses it to process energy. To evaluate this, we examine the charge transfer pattern of each switching sequence with respect to the PR's resonant cycle and its implications for the PR's amplitude of resonance and energy processing capability.

A. Charge Transfer Utilization Factor (K)

The proposed implementations in Table II vary widely in how they utilize the PR's resonant cycle. For $V_{in} > V_{out}$, some sequences such as V_{in}-V_{out}, *Zero*, V_{out} spend the majority of

the PR resonant cycle delivering energy to the load (ie. energy is delivered during both positive and negative i_L), while others such as V_{in}, -V_{out}, *Zero* devote more than an entire half-cycle to open and zero stages.

Productive use of the PR's resonant cycle can be quantified with a "charge transfer utilization factor", K, which we define as the proportion of all connected/zero stage charge transfer that is delivered to the output for $V_{in} > V_{out}$ or sourced from the input for $V_{out} > V_{in}$. This fraction can be simplified to a function of only V_{in} and V_{out} using the CoE and CoC equations for a given sequence.

Here we derive K for sequence V_{in}, V_{in}-V_{out}, V_{out}, which delivers charge to the output during stages 3 and 5:

$$K = \frac{|q_3| + |q_5|}{|q_1| + |q_3| + |q_5|} = \frac{|q_3| + |q_5|}{2|q_5|} \tag{12}$$

An expression for q_3 as a function of q_5 can be derived from CoE-CoC expression (26), re-written with q_3 and q_5:

$$V_{in}(|q_5| - |q_3|) + (V_{in} - V_{out})|q_3| - V_{out}|q_5| = 0 \tag{13}$$

$$\Rightarrow |q_3| = \frac{V_{in} - V_{out}}{V_{out}}|q_5| \tag{14}$$

Inserting (14) into (12) yields K as a function of V_{in} and V_{out}:

$$K = \frac{V_{in}}{2V_{out}} \tag{15}$$

The K expressions derived for all of the switching sequences are displayed in the rightmost column of Table II. A higher charge transfer utilization factor K implies that a switching sequence's connected stages use the PR's resonant cycle more effectively, requiring less charge circulation to deliver the same quantity of energy to the load.

B. Total Charge Transfer

The total charge that must be transferred through the PR during each resonant cycle can be partitioned into charge transfer required of connected/zero stages (Q_{conn}) and open stages (Q_{open}). The charge that must be transfered by i_L during only the connected/zero stages (Q_{conn}) of a switching sequence is the following function of K:

$$Q_{conn} = \frac{Q_{out}}{K} = \frac{E_{out}}{KV_{out}} = \frac{P_{out}}{fKV_{out}} \tag{16}$$

Open stages do not deliver charge to the output but collectively charge/discharge C_p across its full voltage range V_{pp}, so the charge transferred by i_L during open stages is:

$$Q_{open} = 2C_pV_{pp} \tag{17}$$

Thus, the total magnitude of charge that must be transferred by i_L during each resonant cycle (Q_{total}) is the sum:

$$Q_{total} = Q_{conn} + Q_{open} = \frac{P_{out}}{fKV_{out}} + 2C_pV_{pp} \tag{18}$$

These charge transfer calculations enable estimation of several PR energy and efficiency characteristics as explored in the remainder of this section and Section IX. If desired, the effects of parasitic capacitances can be added by modifying C_p as described in Appendix E.

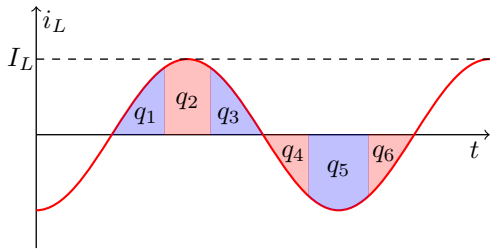

Fig. 10. Sinusoidal approximation of i_L based on the charge transfer q_n required of each stage.

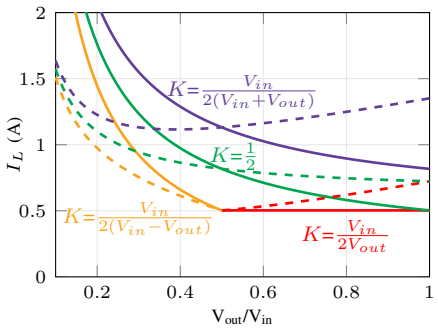

Fig. 11. I_L vs. $\frac{V_{out}}{V_{in}}$ for various K as calculated in (20) with constant V_{in} = 100 V (solid lines) or constant V_{out} = 50 V (dashed lines). P_{out} = 10 W, V_{pp} = V_{in}, and f (assumed f_{res}) and C_p correspond to the PR in Table III.

C. Amplitude of PR Resonance

The magnitude of charge transferred by i_L each resonant cycle (Q_{total}) can be extended to estimate the PR's maximum i_L, denoted as I_L. I_L can be considered a metric for the PR's amplitude of resonance, which has implications for energy storage, loss, and efficiency. If we approximate i_L to be sinusoidal as shown in Fig. 10, I_L can then be calculated by equating Q_{total} to the integral of i_L:

$$Q_{total} = 2\int_0^{\frac{1}{2f}} i_L dt = 2\int_0^{\frac{1}{2f}} I_L \sin(2\pi ft)dt = \frac{2I_L}{\pi f} \tag{19}$$

$$\Rightarrow I_L = \frac{\pi}{2} f Q_{total} = \pi\left(\frac{P_{out}}{2KV_{out}} + fC_pV_{pp}\right) \tag{20}$$

This I_L expression provides key insight into the factors that determine the PR's amplitude of resonance. Only the open stage term in this equation is dependent on PR parameters; the connected/zero stage term depends exclusively on the operating point and switching sequence. For a given PR and operating point, higher charge transfer utilization K results in the same P_{out} delivery with a lower I_L. Also, I_L increases as P_{out} alone increases and vice-versa, but I_L remains unaffected if $\frac{P_{out}}{V_{out}}$ (ie. the average output current) stays the same.

Fig. 11 plots I_L as a function of voltage conversion ratio for constant power in the step-down case and reveals significant variability with respect to the K values in Table II. I_L generally increases as the voltage conversion ratio decreases, which is more drastic as V_{out} is varied since $\frac{P_{out}}{V_{out}}$ also increases in that case. K=$\frac{V_{in}}{2(V_{in}-V_{out})}$ and K=$\frac{V_{in}}{2V_{out}}$ clearly produce the lowest I_L for both the constant-V_{in} and constant-V_{out} sweeps. Thus, switching sequences associated with these K values require the lowest amplitude of resonance in the PR.

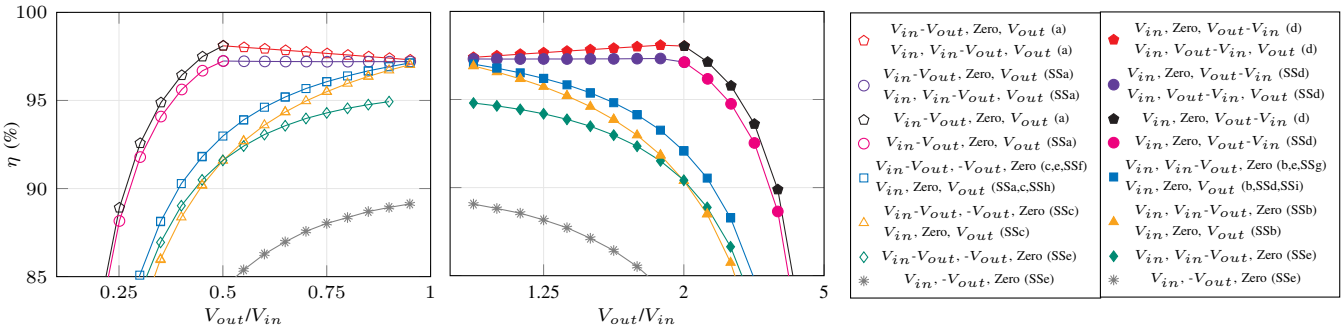

Fig. 12. Calculated efficiency vs. $\frac{V_{out}}{V_{in}}$ of the exact periodic steady state solution (Appendix F) for the PR in Table III when used in the proposed implementations of Table II. Max(V_{in},V_{out}) = 100 V and P_{out} = 10.0 W. The line markers point to the symbols next to the operation constraints for i_L in Table II; these correspond to each efficiency curve's specific switching sequence and topology (summarized in the legend, where SS indicates soft switching).

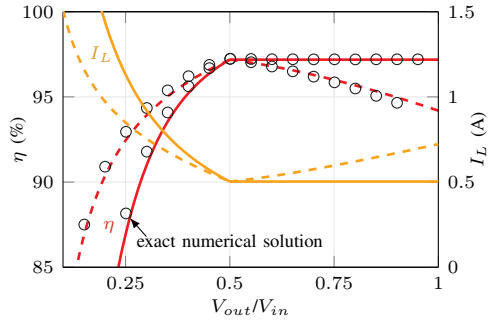

Fig. 13. Estimated I_L (20) and efficiency (23) vs. $\frac{V_{out}}{V_{in}}$ for the PR in Table III with constant V_{in} = 100 V (solid lines) or constant V_{out} = 50 V (dashed lines). P_{out} = 10 W and $f_{assumed}$ = 131 kHz (open-stage frequency). The exact, numerically-solved efficiency points are overlaid on the estimated trends for direct comparison.

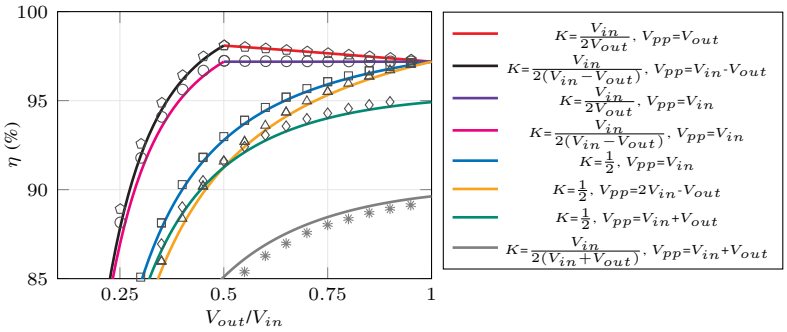

Fig. 14. Estimated efficiency vs. $\frac{V_{out}}{V_{in}}$ using (23) for the PR in Table III with V_{in} = 100 V and P_{out} = 10.0 W. Different K and V_{pp} combinations are delineated by color, and the calculated points in Fig. 12 are overlaid on the estimated trends for direct comparison.

D. PR Energy Storage and Loss

I_L is the value of i_L at its assumed-sinusoidal peak, which is the point in the resonant cycle at which L holds all of the energy stored in the PR's LCR branch. Thus, the mechanical energy stored in the PR (E_{stored}) for a given switching sequence and operating point can be estimated using:

$$E_{stored} \approx \frac{1}{2} L I_L^2 \tag{21}$$

Similarly, the mechanical energy lost during each cycle of the PR (E_{loss}) can be estimated using I_L as follows:

$$E_{loss} \approx \int_0^{\frac{1}{f}} i_L(t)^2 R dt = \int_0^{\frac{1}{f}} (I_L \sin(2\pi f t))^2 R dt = \frac{1}{2f} I_L^2 R \tag{22}$$

Minimizing I_L translates to less energy storage and loss, both of which are proportional to I_L^2. Thus, I_L can be used as a general metric for comparing energy processing capability during the design process, with lower I_L values for a given operating point being more desirable.

IX. Efficiency Comparison

To further evaluate the proposed implementations in Table II, we calculate and compare PR efficiency using the exact periodic steady state solution considering R in Appendix F. The result confirms the implications of (20) and (22) and shows their utility for calculating an efficiency approximation that compares closely with the exact solution.

A. Efficiency by Implementation

Fig. 12 plots calculated PR efficiency (only the PR - not the full converter) as a function of voltage conversion ratio for a given PR and fixed power when used in each of the configurations listed in Table II. These calculations are made based on the *exact* periodic steady state solution of Appendix F, assuming the measured PR parameters in Table III. Fig. 12 reveals significant efficiency differences among the implementations, but these variations align with the characteristics that minimize I_L in (20), especially K. High efficiency tends to be correlated with:

- Connected stages involving V_{out} (for $V_{in} > V_{out}$) or V_{in} (for $V_{out} > V_{in}$) spanning a greater portion of the PR resonant cycle.
- No zero stage, or minimal zero stage charge transfer.
- Less charge transfer during open stages (i.e. smaller V_{pp}).

Sequences V_{in}, V_{in}-V_{out}, V_{out} and V_{in}-V_{out}, *Zero*, V_{out} advantageously utilize both the positive and negative i_L halves of the PR resonant cycle for energy transfer to the output, and they require the lowest V_{pp} (V_{out} as-is or V_{in} with soft switching) across the switching cycle in their operating regions. These sequences are the most effective for the step-down case, as predicted by I_L and now confirmed with exact efficiency in Fig. 12.

In the state plane context, sequences that have identical efficiencies as a function of voltage conversion ratio have shifted versions of the same i_L profile. For example, V_{in}, V_{in}-

V_{out}, V_{out} and V_{in}-V_{out}, *Zero*, V_{out} have the same state planes rotated by 180° and V_p-shifted by V_{out}. These sequences also have the same K and V_{pp}, which is consistent with producing the same I_L for a given PR and operating point in (20) and therefore the same loss in (22).

Fig. 12 also shows that the modifications required for ZVS in topologies Fig. 4(a)-(e) result in a slight efficiency drop for the PR, which can be attributed to the additional v_p swing in the two-part open stage (and therefore higher V_{pp} in (20)). This v_p swing warrants additional charge transfer during open stages, requiring a higher I_L (and therefore higher loss in the PR) for the same energy transfer to the load. Thus, a tradeoff exists between this PR efficiency drop and the loss that would be incurred by hard switching in these topologies.

It should be noted that the proportion of energy output per cycle that is directly transferred from V_{in} to V_{out} during the same connected stage (and therefore not stored in the PR) was *not* found to be deterministic for high efficiency; this is further explored in Appendix H.

B. Efficiency Estimation

To the extent that i_L is sinusoidal, the analysis of Section VIII-D can be extended to estimate the efficiency of an operating point using only (20) as follows:

$$\eta \approx \frac{P_{out}}{P_{out} + fE_{loss}} = \frac{P_{out}}{P_{out} + \frac{1}{2} I_L^2 R} \tag{23}$$

This relationship is illustrated in Fig. 13 with I_L and efficiency estimates as functions of $\frac{V_{out}}{V_{in}}$ for fixed V_{in} (solid lines) and for fixed V_{out} (dashed lines). To evaluate the validity of (23), the exact, numerically-obtained efficiency points are overlaid for direct comparison. Fig. 13 reveals striking similarity between the two methods for predicting efficiency, attesting to the close representation of the PR's resonant behavior obtained through (20). This suggests that reasonable energy storage, loss, and efficiency estimations can be accessed with (20) without the computational burden of numerically solving the exact periodic steady state system. Fig. 14 plots these estimates for the same step-down operating ranges and implementations compared in Fig. 12, with the points from Fig. 12 overlaid for direct comparison. The attached instructional video further contextualizes this estimation technique with the analysis of Section VIII.

X. Example Implementation

We illustrate an example converter implementation using the topology in Fig. 4(a) and the PR modeled in Table III. Table II shows that this topology serves switching sequences V_{in}-V_{out}, *Zero*, V_{out} and V_{in}, V_{in}-V_{out}, V_{out}, which have the highest K values for step-down designs and therefore the most desirable efficiencies. The soft-switched version of V_{in}-V_{out}, *Zero*, V_{out} can be reduced to just two active switches for $V_{in} > 2V_{out}$ as pictured in Fig. 15 while maintaining all-positive instantaneous power transfer with unidirectional-blocking switches. Thus, this implementation has both performance and practicality advantages relative to others for step-down designs.

The PR was selected based on the following criteria among available parts from APC International [37]: (1) material with a high mechanical quality factor and (2) resonant frequency in the low hundreds of kHz (for ease of initial demonstration). We acquired samples of three ready-to-ship products, obtained estimates of their model parameter values using an impedance analyzer, solved for their relative efficiencies, and selected the APC International part 790 (844 material disc, diameter 19.8 mm, thickness .8 mm, radial vibration mode) as the best candidate for demonstration (parameters in Table III).

The prototype (pictured in Fig. 16) is implemented on a two-layer 1-oz copper board with the parts shown in Table IV. Its layout has parallel FET and diode footprints for S3 and S4 so either can be accommodated as shown in Fig. 15. We test each switching sequence using only the minimum required active switches (summarized in Table V), with S3 and S4 implemented as diodes when feasible. Testing in the $\frac{V_{out}}{V_{in}} < 0.5$ region permits use of both diodes at all times. For

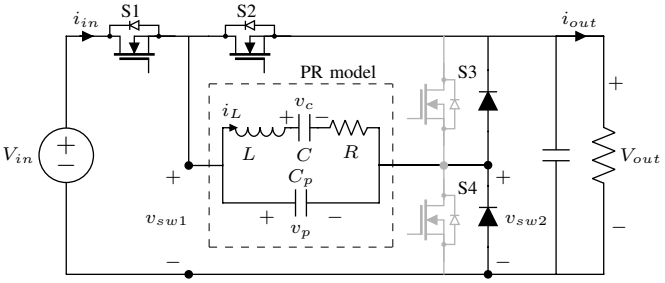

Fig. 15. Example implementation of the topology in Fig. 4(a), showing S3 and S4 implemented as active switches (grayed out) or diodes.

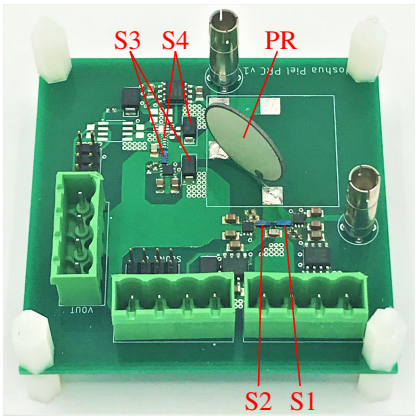

Fig. 16. Prototype circuit board for the implementation in Fig. 15.

TABLE IV
Prototype Parts List

Component	Part
PR	APC International part 790
Active Switch	EPC 2019 GaN FET
Schottky Diode	ON Semiconductor NRVSTA4100
Gate Driver	Texas Instruments UCC27611

TABLE V
High-Efficiency Step-Down Switching Sequences

Switching Sequence	Voltage Conversion Range	Active Switches
V_{in}-V_{out}, *Zero*, V_{out}	$V_{in} > 2V_{out}$	S1, S2
	$2V_{out} > V_{in} > V_{out}$	S1, S2, S3
V_{in}, V_{in}-V_{out}, V_{out}	$2V_{out} > V_{in} > V_{out}$	S1, S2, S4

testing in the $\frac{V_{out}}{V_{in}} > 0.5$ region, both the S3 and S4 FETs are populated but only used as listed in Table V.

An isolated supply powers the gate circuitry for S1 and S2. We operate this prototype with open-loop control of all gate signals and a constant-voltage load. For each operating point, the converter's switching times are tuned for ZVS, soft charging of the PR, and all-positive instantaneous power transfer. Assuming operation is at a fixed power or frequency, there is a unique tuning point that satisfies these conditions for a six-stage sequence. The PR's properties change with temperature, so all data points are acquired at ≤ 40 °C and not necessarily at thermal equilibrium for higher-loss operating points.

XI. Experimental Results

We experimentally demonstrate implementations described herein using the prototype and operation procedures of Section X. Only the V_{in}-V_{out}, *Zero*, V_{out} switching sequence can serve the $\frac{V_{out}}{V_{in}} < 0.5$ operating region, so we use this region to illustrate the switching sequence's functionality and validate the analysis of Sections V - IX. In the $\frac{V_{out}}{V_{in}} > 0.5$ region, we compare the V_{in}-V_{out}, *Zero*, V_{out} and V_{in}, V_{in}-V_{out}, V_{out} sequences and demonstrate the flexibility they provide. The eight-stage domain between these sequences in the $\frac{V_{out}}{V_{in}} > 0.5$ region is explored experimentally in Appendix G.

A. Waveforms

Experimental waveforms for various operating points with $\frac{V_{out}}{V_{in}}$ less than 0.5 are displayed in Figs. 17 and 18. These waveforms greatly resemble the desired waveforms shown in Fig. 9, which directly compare to the operating point of Fig. 17(b). All waveforms exhibit ZVS and soft charging of the PR, as indicated by the resonant transitions and the exact v_p swing up to V_{in}. Some operating points have smooth waveforms, while others contain a small 2.5 MHz ripple as shown in Fig. 18(b) due to excitation of the PR's thickness vibration mode. Figs. 17(b) and 18(c) have nearly-identical switching times and are indistinguishable if scaled by voltage, demonstrating linear behavior in this regard. These concepts also apply to waveforms in the $\frac{V_{out}}{V_{in}} > 0.5$ operating region, some of which are displayed in Fig. 27 of Appendix G.

Fig. 17 illustrates how the switching sequence adapts as $\frac{V_{out}}{V_{in}}$ decreases from 0.48 to 0.2 for the same power output. At $\frac{V_{out}}{V_{in}} = 0.48$ (Fig. 17(a)), the zero stage (stage 3) is almost nonexistent, and the voltage waveforms appear close to symmetric. As $\frac{V_{out}}{V_{in}}$ decreases, the zero stage becomes progressively more prominent until it dominates the V_{in}-V_{out} stage as shown for $\frac{V_{out}}{V_{in}} = 0.2$ in Fig. 17(c). This is how the switching sequence regulates voltage.

Fig. 18 shows how the switching sequence changes as power increases from 1 W (Fig. 18(a)) to 24 W (Fig. 18(c)) at the same input and output voltage. At 1 W, the connected stages are barely visible; almost all of the PR's resonant cycle is used for charge transfer during the open stages. As power increases, this charge transfer requires less time, and the connected stages become more prominent.

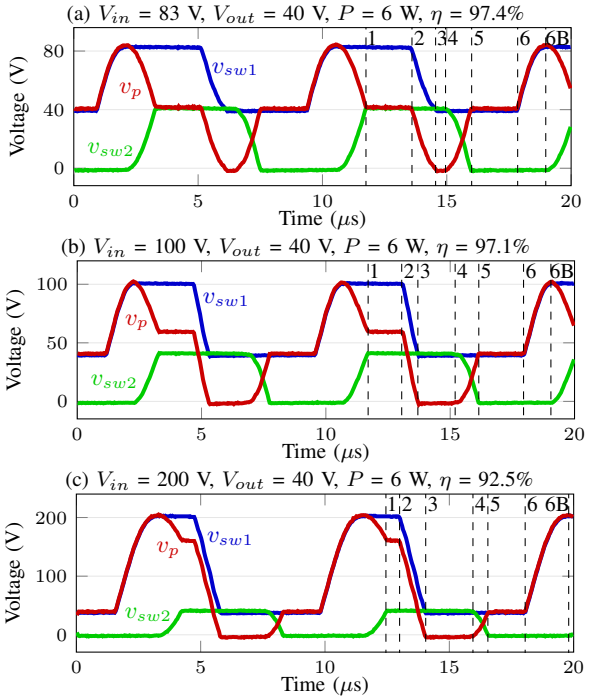

Fig. 17. Experimental waveforms for switching sequence V_{in}-V_{out}, *Zero*, V_{out} at various $\frac{V_{out}}{V_{in}}$ with the prototype described in Section X. Numbers 1-6B correspond to the state transition points in Fig. 8.

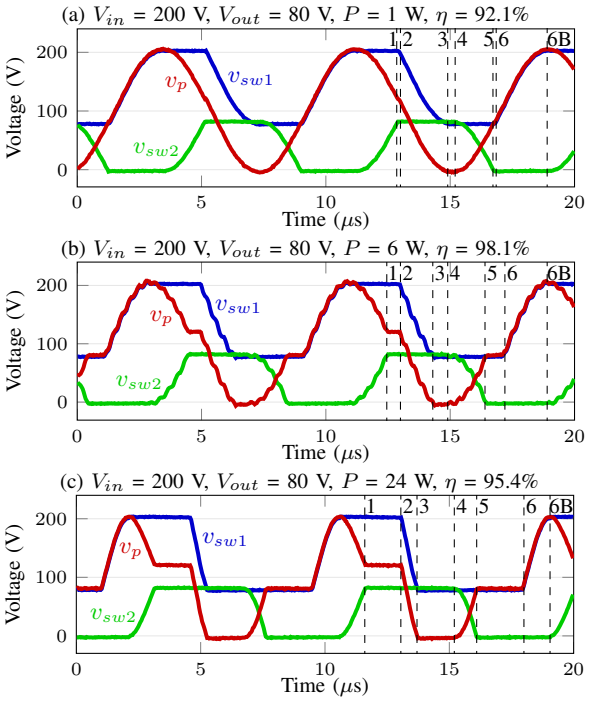

Fig. 18. Experimental waveforms for switching sequence V_{in}-V_{out}, *Zero*, V_{out} at various power levels with the prototype described in Section X. Numbers 1-6B correspond to the state transition points in Fig. 8.

B. Gain

Fig. 19 plots the experimental $\frac{V_{out}}{V_{in}}$ as a function of frequency for different power levels in the $\frac{V_{out}}{V_{in}} < 0.5$ region. Fig. 23 does the same for $\frac{V_{out}}{V_{in}} > 0.5$ and shows that the two sequences serving this region operate at nearly-identical frequencies for a given operating point. For the same $\frac{V_{out}}{V_{in}}$,

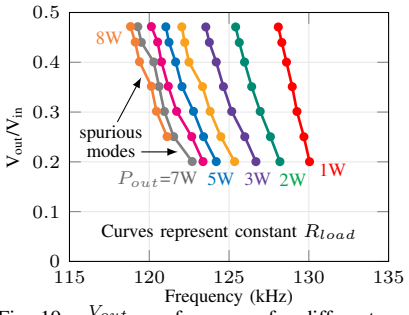

Fig. 19. $\frac{V_{out}}{V_{in}}$ vs. frequency for different power levels (labeled) at the same V_{out} = 40 V. Same operating points as Fig. 20.

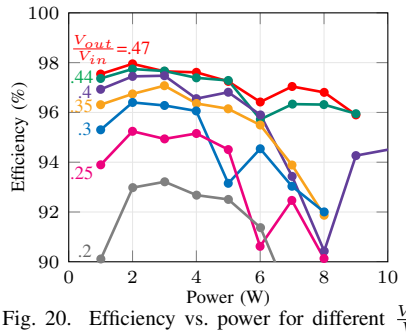

Fig. 20. Efficiency vs. power for different $\frac{V_{out}}{V_{in}}$ ratios (labeled) at the same V_{out} = 40 V. Same operating points as Fig. 19.

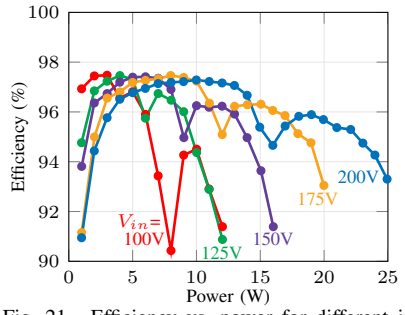

Fig. 21. Efficiency vs. power for different input voltages (labeled) at the same $\frac{V_{out}}{V_{in}}$ = 0.4. Same operating points as Fig. 22.

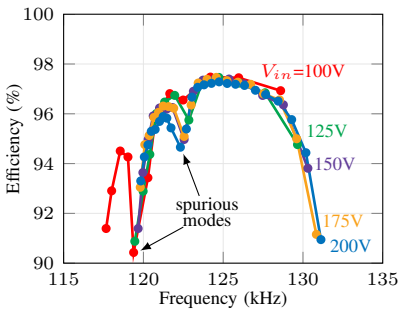

Fig. 22. Efficiency vs. frequency for different input voltages (labeled) at the same $\frac{V_{out}}{V_{in}}$ = 0.4. Same operating points as Fig. 21.

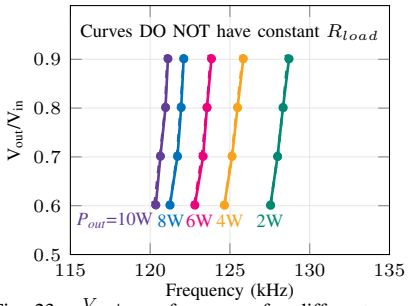

Fig. 23. $\frac{V_{out}}{V_{in}}$ vs. frequency for different power levels (labeled) with V_{in}-V_{out}, *Zero*, V_{out} (solid lines) and V_{in}, V_{in}-V_{out}, V_{out} (dashed lines) at V_{in} = 100 V. Same operating points as Fig. 24.

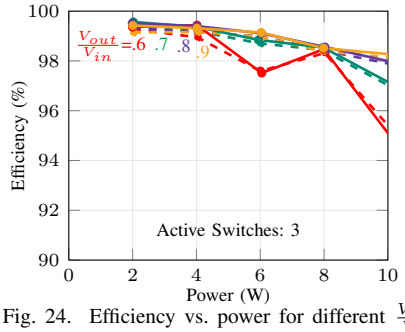

Fig. 24. Efficiency vs. power for different $\frac{V_{out}}{V_{in}}$ with V_{in}-V_{out}, *Zero*, V_{out} (solid lines) and V_{in}, V_{in}-V_{out}, V_{out} (dashed lines) at V_{in} = 100 V. Same operating points as Fig. 23.

higher-power loads require frequencies closer to the resonant frequency (at the lower end of the frequency range). These maps illustrate how frequency may be used to regulate power at a constant $\frac{V_{out}}{V_{in}}$ or vice versa, using the final degree of freedom in the periodic steady state solution as discussed in Section VII.

C. Efficiency

To evaluate performance, we conduct data sweeps over various $\frac{V_{out}}{V_{in}}$, load, and frequency conditions beginning with V_{in}-V_{out}, *Zero*, V_{out} in the $\frac{V_{out}}{V_{in}} < 0.5$ region. Before we discuss efficiency, it should be noted that Fig. 19 exhibits discontinuities at frequencies close to 120 kHz and 122.5 kHz, at which the PR operates in an undesired alternate vibration mode. These "spurious" modes cause downward spikes in efficiency as shown in Fig. 22 , and their existence is entirely dependent on the construction and mounting of the PR (outside the scope of this work) [1]. Thus, the discussion in this section examines the observed efficiency trends ignoring these modes.

In Fig. 20, we plot efficiency as a function of power for different $\frac{V_{out}}{V_{in}}$ less than 0.5. Efficiency increases as $\frac{V_{out}}{V_{in}}$ approaches 0.5, which demonstrates the role of the charge transfer utilization factor K in (20). At $\frac{V_{out}}{V_{in}}$ = 0.5, K reaches its maximum for this operating range, which translates to lowest I_L and therefore lowest loss.

We then plot the efficiency as a function of power for various V_{in} and V_{out} combinations all with the same $\frac{V_{out}}{V_{in}}$ ratio (and therefore constant K) in Fig. 21. At higher voltages, higher power levels can be reached with similar efficiencies, indicating that efficiency is closely related to current. This is described by the $\frac{P_{out}}{V_{out}}$ term in (20), whose first term does not change as long as $\frac{P_{out}}{V_{out}}$ remains the same. The power level at which efficiency peaks also rises as voltage rises in Fig. 21, suggesting an "optimal" $\frac{P_{out}}{V_{out}}$ (the open stage term dominates at lower power levels and vice versa).

Fig. 22 contains the efficiency data in Fig. 21 plotted again vs. switching frequency (still all with the same $\frac{V_{out}}{V_{in}}$ and K) and reveals strikingly similar efficiency sweeps for all input/output voltage combinations. At a single frequency and $\frac{V_{out}}{V_{in}}$, both the connected stage and open stage terms in (I_L) increase linearly with voltage, as does the resulting I_L. P_{out} increases quadratically with voltage, and if loss is closely related to I_L^2, loss also increases quadratically with voltage. Thus, the same efficiency results regardless of voltage level as long as frequency and $\frac{V_{out}}{V_{in}}$ are identical. Fig. 22 demonstrates this behavior and therefore further validates (20) and the close relationship between I_L and loss.

Fig. 24 compares efficiency as a function of power for various $\frac{V_{out}}{V_{in}}$ greater than 0.5 for V_{in}-V_{out}, *Zero*, V_{out} (solid lines) and V_{in}, V_{in}-V_{out}, V_{out} (dashed lines) with constant V_{in}. Fig. 24 demonstrates that these two switching sequences have essentially identical efficiencies even as power and $\frac{V_{out}}{V_{in}}$ vary, and that efficiency has practically no dependence on $\frac{V_{out}}{V_{in}}$ in this region of operation. Both of these behaviors again confirm the influence of K on performance; K is identical for both sequences and removes the dependence of I_L on V_{out} in this region. Thus, this PR-based converter implementation may be used in this operating region for a significant range of voltage

[1]Efficiency drops are also observed in [23] due to harmonic content in i_L.

regulation with little change in efficiency.

XII. Conclusion

This systematic enumeration and downselection of PR-based dc-dc converter implementations has revealed eight distinct six-stage switching sequences and nine practical converter topologies. These implementations rely solely on a single PR for power stage energy storage, which enables realization of the PR's full power density and efficiency advantages compared to other energy storage mechanisms. The considered switching sequences support voltage regulation as well as resonant "soft charging" of the PR's input capacitance between connected stages in order to reduce switching loss. This, coupled with soft switching all switches, will allow efficient operation of these implementations at higher switching frequencies.

The presented analysis methods provide means to easily visualize, constrain, and evaluate the operation of these proposed implementations. Experimental testing validates that the proposed implementations facilitate resonant soft charging of the PR's capacitance, ZVS on all switches, and all-positive instantaneous power transfer, resulting in efficiencies of $\geq$96% across a wide range of operating points and peak efficiencies of >99%. The PR in this prototype is a commercially-available component, so even better performance and power density may be reached with a PR custom-designed for power conversion. Thus, it can be concluded that PR-based converter implementations are promising alternatives to those based on traditional energy storage mechanisms and may be a route to miniaturization for high voltage, low power applications.

Appendix A
Full List of Switching Sequences

Tables VI and VII contain the complete sets of four- and six-stage switching sequences enumerated in Section II, along with the Section III sub-section in which they are eliminated for $V_{in} > V_{out}$, $V_{out} > V_{in}$. The final switching sequences shown in Table II are marked with $*$.

TABLE VI
All Enumerated Four-Stage Switching Sequences

V_{in}, V_{in}-V_{out}	B,B	V_{in}-V_{out}, V_{out}-V_{in}	B,B
V_{in}, V_{out}-V_{in}	B,B	V_{in}-V_{out}, V_{out}	B,B
V_{in}, V_{out}	B,B	V_{in}-V_{out}, -V_{out}	B,B
V_{in}, -V_{out}	B,B		

Appendix B
Example Voltage Conversion Range Derivation

We derive the range of voltage conversion ratios compatible with example switching sequence V_{in}, V_{in}-V_{out}, V_{out}, using the CoE equation (1) and the CoC equation (4). For this switching sequence, the i_L polarity assumptions made at the beginning of Section III require q_1 and q_3 to be positive and q_5 to be negative. Thus, equations (1) and (4) become:

$$V_{in}|q_1| + (V_{in} - V_{out})|q_3| - V_{out}|q_5| = 0 \tag{24}$$

$$|q_1| + |q_3| = |q_5| \tag{25}$$

TABLE VII
All Enumerated Six-Stage Switching Sequences

V_{in}, -V_{in}, V_{in}-V_{out}	A,A	V_{in}, -V_{out}, V_{in}-V_{out}	A,A
V_{in}, -V_{in}, V_{out}-V_{in}	B,C	V_{in}, -V_{out}, V_{out}-V_{in}	C,C
V_{in}, -V_{in}, V_{out}	B,C	V_{in}, -V_{out}, V_{out}	C,B
V_{in}, -V_{in}, -V_{out}	A,A	V_{in}, -V_{out}, Zero	$*$,$*$
V_{in}, V_{in}-V_{out}, V_{out}-V_{in}	B,C	V_{in}, Zero, V_{in}-V_{out}	A,B
V_{in}, V_{in}-V_{out}, V_{out}	$*$,B	V_{in}, Zero, V_{out}-V_{in}	B,$*$
V_{in}, V_{in}-V_{out}, -V_{out}	B,B	V_{in}, Zero, V_{out}	$*$,$*$
V_{in}, V_{in}-V_{out}, Zero	B,$*$	V_{in}, Zero, -V_{out}	B,B
V_{in}, V_{out}-V_{in}, V_{in}-V_{out}	A,A	V_{in}-V_{out}, V_{out}-V_{in}, V_{out}	C,B
V_{in}, V_{out}-V_{in}, V_{out}	B,$*$	V_{in}-V_{out}, V_{out}-V_{in}, -V_{out}	A,A
V_{in}, V_{out}-V_{in}, -V_{out}	A,A	V_{in}-V_{out}, V_{out}-V_{in}, Zero	B,B
V_{in}, V_{out}-V_{in}, Zero	B,A	V_{in}-V_{out}, V_{out}, -V_{out}	A,A
V_{in}, V_{out}, V_{in}-V_{out}	A,A	V_{in}-V_{out}, V_{out}, Zero	A,B
V_{in}, V_{out}, V_{out}-V_{in}	A,A	V_{in}-V_{out}, -V_{out}, V_{out}	C,B
V_{in}, V_{out}, -V_{out}	A,A	V_{in}-V_{out}, -V_{out}, Zero	$*$,B
V_{in}, V_{out}, Zero	A,A	V_{in}-V_{out}, Zero, V_{out}	$*$,B
		V_{in}-V_{out}, Zero, -V_{out}	B,A

Inserting (25) into (24) yields the general equation that must be satisfied to ensure energy and charge balance on the PR with this switching sequence:

$$V_{in}|q_1| + (V_{in} - V_{out})|q_3| - V_{out}(|q_1| + |q_3|) = 0 \tag{26}$$

The complete set of V_{in} and V_{out} combinations for which q_1 and q_3 can be calculated to satisfy this general equation is bound by the requirement that V_{out} is a weighted average of V_{in} and V_{in}-V_{out}. This translates to the ranges $V_{in} > V_{out}$ and $V_{out} > V_{in}$-V_{out}, which combine into $2V_{out} > V_{in} > V_{out}$. Thus, this is the range of voltage conversion ratios that are supported by switching sequence V_{in}, V_{in}-V_{out}, V_{out} assuming the aforementioned constraints.

Appendix C
Alternative Topology-based Enumeration

One alternative enumeration approach begins with the realm of *topologies* that can be derived from Fig. 2, constrained by practical assumptions. The following source/load connection quantities are possible for each PR terminal:

- One source/load connection: allows a fixed node with no switches.
- Two source/load connections: creates a switch node that requires two unidirectional-blocking switches.
- Three source/load connections: creates a switch node that requires two unidirectional-blocking and one bidirectional blocking switch (for the middle-voltage node).

Since a six-stage switching sequence has three connected stages, it requires a minimum of four total terminal connections for the PR. This can be constructed with either one terminal having one connection (a fixed node) and the other having three connections (a switch node) or both terminals having two connections each (two switch nodes). Both of these configurations can be implemented with four unidirectional blocking switches, which is the fewest number for a six-stage switching sequence. Assuming this simplicity is desired, the domain of relevant topologies can be confined to these configurations.

Enumerating topologies with two switch nodes yields Figs. 4(a)-(e) plus one additional structure with both PR terminals

each having connections to the positive nodes of V_{in} and V_{out}. This amounts to four distinct structures if the blocking directions of the switches are left ambiguous. The structures in Figs. 4(a)-(e) can each support four distinct connected stages, while the additional structure can only support three (since it supports two ways to achieve a zero stage).

The realm of potential switching sequences for a topology can be enumerated by permuting the structure's possible connected stages. For Figs. 4(a)-(e), this results in eight distinct six-stage switching sequences each (as defined by the assumptions in Section II). These switching sequences can then be downselected based on the same resonant cycle and energy/charge balance requirements described in Section III. This process eliminates all but four sequences each for Figs. 4(a)-(d), all but three sequences for Fig. 4(e), and all potential sequences for the additional derived structure. The downselection result is the same as that displayed in Fig. 4 and Table II for these topologies, and the same process applies to Figs. 4(f)-(i).

Appendix D
Open Stage Center of Resonance Derivation

The center of resonance on a state plane for v_p and v_c during open stages (denoted V_o) can be derived from the energy stored in C_p and C that does not participate in the open-stage resonance. This is calculated by subtracting the energy in C_{eff} from the energy in C_p and C at the beginning of the open stage (dependent on the variable states when the stage begins) as follows, using stage 2 in Fig. 5 as an example:

$$E_{Ceff} = \frac{1}{2}C_{eff}(v_{p2} - v_{c2})^2 \tag{27}$$

$$E_{Cp} + E_C = \frac{1}{2}C_p v_{p2}^2 + \frac{1}{2}C v_{c2}^2 \tag{28}$$

$$E_{Cp} + E_C - E_{Ceff} = \frac{(C_p v_{p2} + C v_{c2})^2}{2(C_p + C)} \tag{29}$$

The center of resonance V_o is then the voltage for which the energy in C_p and C equal this value:

$$\frac{1}{2}C_p V_o^2 + \frac{1}{2}C V_o^2 = \frac{(C_p v_{p2} + C v_{c2})^2}{2(C_p + C)} \tag{30}$$

$$\Rightarrow V_o = \frac{C_p v_{p2} + C v_{c2}}{C_p + C} \tag{31}$$

To consider parasitic capacitances in the circuit, C_p can be modified as described in Appendix E.

Appendix E
Considering Parasitic Capacitance

In a realistic implementation, there are additional parasitic capacitances (e.g., switch capacitances) between each switch node and AC ground. These capacitances do not affect resonant behavior during connected stages, but they can play a significant role in the resonance of open stages. Fig. 25 contains the open stage resonant circuits when parasitic capacitances are present at one or both terminals of the PR, where C_{parA} and C_{parB} are the sums of all capacitances between switch nodes A or B (respectively) and AC ground. To consider these capacitance in the analysis herein, C_p can be modified to include them as follows:

$$C_{p+A} = C_p + C_{parA} \tag{32}$$

$$C_{p+A+B} = C_p + \frac{C_{parA}C_{parB}}{C_{parA} + C_{parB}} \tag{33}$$

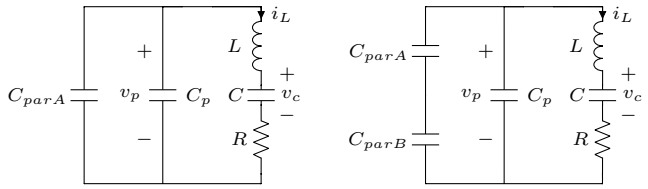

Fig. 25. Resonant circuits considering parasitic capacitances at (a) one PR terminal and (b) both PR terminals.

Appendix F
Exact Periodic Steady State Solution

The periodic steady state solution obtained in Section VI does not consider the effects of R. Adding power dissipation terms to the CoE equations requires time-domain integration of i_L^2, which is complex to implement using only the transition point state variables in the ideal system of equations. Instead, if an exact periodic steady state solution considering R is desired, the time-domain system of differential equations governing the PR's states can be solved symbolically for each stage (producing solutions with complex exponentials) and assembled into a system of equations representing the whole switching sequence. Then, this system of equations can be solved numerically *using the ideal periodic steady state solution as its starting point*, which is vital for reliable convergence.

Connected stages can be described by the following differential equations, where v_p is constant (V_p):

$$\frac{dv_c}{dt} = \frac{i_L}{C} \tag{34}$$

$$\frac{di_L}{dt} = \frac{V_p - v_c - Ri_L}{L} \tag{35}$$

Open stages have these same equations plus an additional equation to describe the change in v_p.

$$\frac{dv_p}{dt} = \frac{-i_L}{C_p} \tag{36}$$

With two equations for each connected stage and three equations for each open stage, this time-domain system has fifteen equations for a six-stage switching sequence. Its unknowns are the same transition point variable states plus the six time durations of each stage, amounting to 18 total variables. This method for obtaining an exact periodic steady state solution considering R is much more computation-heavy than the ideal solution and should therefore only be pursued if an exact solution is absolutely necessary. We have employed it to calculate and compare expected PR efficiencies in Section IX.

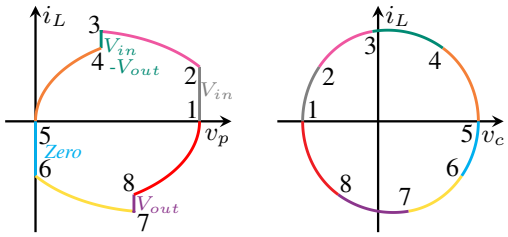

Fig. 26. State plane example for sequence V_{in}, V_{in}-V_{out}, *Zero*, V_{out} with V_{in} = 100 V, V_{out} = 60 V, and P_{out} = 6 W. PR parameters: Table III.

Appendix G
Expansion to Eight-Stage Switching Sequences

As discussed in Section VII-B, achieving ZVS with a six-stage switching sequence in topologies with two switch nodes (Figs. 4(a)-(e)) requires splitting an open stage into two sections, allowing the two terminal nodes to change voltage sequentially. The infinitesimal-duration boundary between these two sections is constrained at a defined V_p, which suggests the potential for a fourth connected stage at that point (creating an eight-stage switching sequence). Notably, if all modified six-stage switching sequences for a given topology in Figs. 4(a)-(e) are expanded to include this specific fourth connected stage, *all sequences yield the same eight-stage switching sequence* (same stages in the same order). Thus, all six-stage sequences proposed herein for a given topology are different segments of the same eight-stage sequence:

- Figs. 4(a)-(b): V_{in}, V_{in}-V_{out}, Zero, V_{out} (Fig. 26)
- Figs. 4(c)-(d): V_{in}, Zero, V_{out}-V_{in}, V_{out}
- Figs. 4(e): V_{in}, V_{in}-V_{out}, -V_{out}, Zero

This relationship between a topology's six-stage and eight-stage sequences suggests a multi-dimensional space of operating modes with varying durations for each of the four potential connected stages. The six-stage sequences are the boundaries for this space, and the eight stage sequence spans from one boundary to another. The efficiency comparison of six-stage switching sequences conducted in Section IX compares the extremes of this space and points to the corners of it that most effectively use the PR. Intentional use of the eight-stage sequence provides added flexibility for tuning and an additional degree of freedom for regulation while maintaining soft charging, ZVS, and positive instantaneous power flow.

To search for other potential eight-stage sequences, we can enumerate sequences for each topology structure as suggested in Appendix C. This yields 8 sequences for each of the 3 structures (24 total), but only the 3 eight-stage sequences listed above survive downselection for one PR resonant cycle and energy/charge balance.

To demonstrate the V_{in}, V_{in}-V_{out}, Zero, V_{out} eight-stage sequence, we experimentally traverse the region between V_{in}-V_{out}, Zero, V_{out} and V_{in}, V_{in}-V_{out}, V_{out} while keeping V_{in}, V_{out}, and P_{out} constant. This requires incrementally increasing and decreasing the zero stage and V_{in} stage time durations and adjusting frequency to maintain a tuned operating point. Fig. 27(b) displays waveforms for V_{in}, V_{in}-V_{out}, Zero, V_{out}, while Figs. 27(a) and 27(c) display waveforms for the two six-stage sequences (all at the same operating point). These

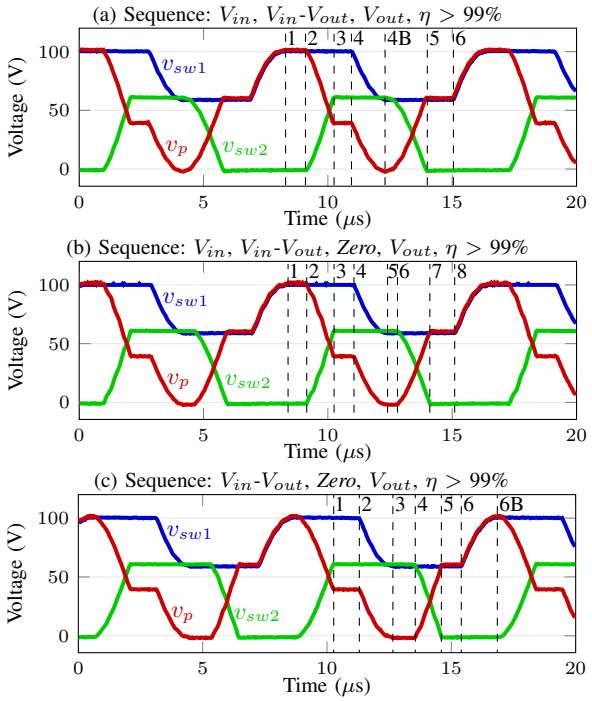

Fig. 27. Experimental waveforms of different switching sequences for V_{in} = 100 V, V_{out} = 60 V, P = 4 W, with the prototype described in Section X. Numbers 1-6B for (b) correspond to the state transition points in Fig. 26.

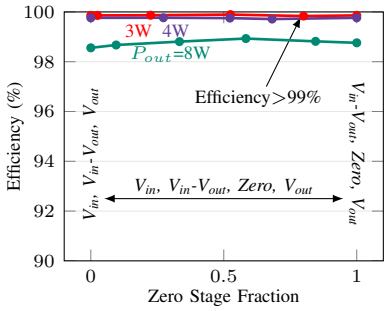

Fig. 28. Experimental efficiency vs. zero stage fraction (1 = maximum duration) for eight-stage sequence for V_{in} = 100 V, V_{out} = 60 V, and constant power.

waveforms exhibit ZVS, soft charging of the PR, and all-positive instantaneous power transfer as desired. Fig. 28 plots efficiency across the continuous eight-stage region at a single operating point and shows that efficiency is virtually constant as the V_{in} and zero stages trade time duration. This aligns with the eight-stage sequence also having an identical charge transfer utilization factor K to those of the boundary six-stage sequences (K=$\frac{V_{in}}{2V_{out}}$) in this region of operation. Thus, the eight-stage region between the two six-stage sequences provides similar operating behavior with an added degree of control flexibility. The operating points of Figs. 27 and 28 engage all four of the converter's active switches (including the six-stage sequences for direction comparison), resulting in the highest reported efficiencies (>99%) for this prototype.

Appendix H
Proportion of Direct Energy Transfer

The proportion of direct energy transfer for a given switching sequence and operating point can be derived using the

same CoE and CoC concepts used in Section III-B and Appendix B. In one cycle, sequence V_{in}-V_{out}, Zero, V_{out} delivers $V_{out}|q_1|$ directly from input to output and $V_{out}|q_5|$ to the output from energy stored in the PR. Thus, the proportion of direct energy transfer is $\frac{|q1|}{|q1|+|q5|}$. This can be derived from the CoE equation for V_{in}-V_{out}, Zero, V_{out} as follows:

$$(V_{in} - V_{out})|q_1| = V_{out}|q_5| \tag{37}$$

$$\Rightarrow \frac{|q_1|}{|q_1| + |q_5|} = \frac{V_{out}}{V_{in}} \tag{38}$$

The same applies to V_{in}, V_{in}-V_{out}, V_{out}, whose proportion of direct energy transfer is $\frac{|q3|}{|q3|+|q5|}$. This can be derived beginning with (13) and results in:

$$\Rightarrow \frac{|q_3|}{|q_3| + |q_5|} = 1 - \frac{V_{out}}{V_{in}} \tag{39}$$

Thus, V_{in}, V_{in}-V_{out}, V_{out} and V_{in}-V_{out}, Zero, V_{out} have opposite proportions of direct energy transfer, yet still produce the same efficiency in Fig. 12.

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