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Bus Converter using Isolation Capacitance for ZVS and Invariant Operation

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***Abstract*—Many power distribution architectures, including the now-popular "isolated bus" architecture, call for a small and efficient unregulated dc transformer stage. Typical isolated converters can be both small and efficient through high frequency operation and soft switching, but timing and control can be challenging as switching frequencies increase. We present an isolated bus converter which achieves ZVS for both inverter and rectifier switches with equal and constant dead times regardless of load, greatly simplifying control. It accomplishes this by using additional capacitors to aid the magnetizing current in commutating switch voltages during the dead time. The converter's operation and advantages are verified with a $1.4\,\mathrm{MHz}$ prototype. The converter operates from $36\,\mathrm{Vdc_{in}}$ to $12\,\mathrm{Vdc_{out}}$ at up to $36\,\mathrm{W}$ rating and achieves $> 94.5\,\%$ peak efficiency with $300\,\mathrm{W/in^3}$ power density.**

***Index Terms*—dc-dc power conversion, isolation technology, hf transformers**

I. Introduction

ADVANCES in power distribution systems (e.g., for telecommunications, data centers, and dc distribution systems) have been driven by a demand for higher efficiency, smaller volume, and lower cost. One approach to high performance architectures is to judiciously divide power processing tasks (voltage transformation, regulation, isolation) among multiple stages, each of which performs its more limited task very well. One popular example is known as the intermediate-bus architecture, which incorporates an isolated bus converter stage (or dc transformer) that provides isolation and voltage transformation but without regulation capability. The isolated bus stage has very focused design goals, allowing for high efficiency and density for the whole system [2]–[8]. Moreover, there are many other power conversion architectures and applications in which the isolation and/or transformation function of the power electronics can be separated from the ability to regulate power [3], [9]–[14]. Practical applications of such systems depend upon bus converters having small size and low loss.

High efficiencies and densities have been achieved through high frequency operation, which has been enabled by advances in components and devices. Gallium-nitride (GaN) transistor technology facilitates higher frequency operation with improved transistor figures of merit (e.g., $R_{on} \times C_{oss}$ [15] or $\sqrt{R_{on} Q_g}$ [16], [17]), such that low-loss soft switching can be realized at high frequency [3], [18]–[23]. Magnetic materials have also been shown to have sustained or improved performance at MHz frequencies [24], [25], permitting continued miniaturization through increases in frequency.

Nevertheless, leveraging the achievable performance of these devices requires converters to have very precise control to achieve, e.g., soft switching and high-resolution duty ratios. For many existing converter topologies and control techniques, at ever increasing frequencies, this is a serious limitation. For more details, refer to Section II.

In this paper, which is an extension of [1], we propose a technique for achieving ZVS and synchronous rectification in isolated bus converters. The approach permits constant and equal dead time for both the rectifier and the inverter switches independent of load. This feature directly addresses the challenge of maintaining ZVS operation with accurate switch timing in the MHz frequency range. Section III of the paper introduces the new bus converter topology and illustrates its operation, design considerations, and advantages. Section IV of the paper demonstrates an implementation of the converter operating at $1.4\,\mathrm{MHz}$ and presents experimental verification of the above advantages. Finally, in Section V we conclude that the proposed approach is a viable technique for implementing efficient and dense isolated bus converers.

II. Limitations of Existing Converters

Conventional dc-dc converter topologies can achieve high density and efficiency; however, as switching frequencies increase, conventional control techniques become very challenging. This is especially true when the converter must be isolated and handle variations in voltage and especially load.

For example, there are many resonant converter topologies processing (quasi) sinusoidal currents that may be useful for isolated bus conversion (e.g., series-resonant [26], parallel-resonant [27], and LLC [28]–[32]). While many of these converters can be designed with diode-based rectifiers, synchronous rectifiers are often needed for higher efficiency (e.g., [2], [33]). In these converters, achieving sufficiently accurate rectifier switch timing is very challenging, especially with changing loads or voltages.

One approach is to control the rectifier transistors to behave like diodes using only information available on the secondary

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side (like transistor v_{ds}). While many commercial control / driver ICs (e.g., [34]) are available for this purpose, the underlying technique has limitations at high frequencies. First, parasitics make it difficult to achieve the necessary switch timing using v_{ds} measurements. In addition, achieving fast voltage comparisons with low overdrive voltages consumes large control powers [35]–[37]. As both of these concerns are exacerbated as frequency increases, there is significant difficulty in making this self-sensing synchronous rectification approach work well in the multi-MHz regime.

Direct control of the rectifier switches (e.g., from the primary side) is another means of realizing synchronous rectification for bus converters. However, this becomes challenging for these topologies at high frequencies, since the exact timing required for ZVS turn on, dead-time control, etc., usually varies with operating condition, and must be managed precisely across an isolation barrier. Control timing (and its variation with operating condition) thus becomes an increasingly challenging problem as frequency increases.

An alternative to resonant topologies in the bus converter (or dc transformer) application is the dual-active-bridge (DAB) converter (e.g, [33]). In this topology there is active control of the timing of the inverter switches relative to the rectifier switches (such that the rectifier switches are not operated like diodes, but do achieve ZVS). One can achieve quasi-trapezoidal current waveforms that provide very low rms currents in the devices and transformer, yielding low conduction dissipation [38], [39]. However, the driving signals require complex and accurate control circuitry with variable dead time, duty ratio, and phase shift for various loads and input voltages. This becomes increasingly difficult at high frequency and imposes heavy constraints on the achievable frequency, especially considering the timing delay and timing variability among signals crossing the isolation barrier.

Overall, there is a difficulty in operating many conventional isolated converters with synchronous rectification at high frequency because of the complexities of achieving the necessary control timing among all of the switches when working across the isolation barrier. This highlights the need for new topologies and control approaches that are more suitable to this frequency range, and which will remain effective as switching frequencies continue to increase.

III. Proposed Bus Converter topology

The proposed converter (Fig. 1) is intended to relieve the difficulty in timing and control at MHz frequencies. It is designed to act as a dc transformer in which the voltage conversion ratio is fixed and no regulation capability is required.[1] The converter comprises a full-bridge inverter, transformer, resonant tank, full-bridge synchronous rectifier, and capacitors interconnecting primary and secondary side switching nodes. The capacitors $\mathrm{C_{y1}}$ and $\mathrm{C_{y2}}$ are implemented with Y-rated safety capacitors to meet galvanic isolation requirements.

[1]In our intended application the converter is used as a bus converter, in which the input voltage is (at least approximately) fixed in addition to conversion ratio, though it can operate well at variable input voltages within limitations constrained by device capacitance nonlinearities.

The operation of the proposed converter topology naturally absorbs the leakage and magnetizing inductances of the transformer as well as the device and transformer capacitances, making it suitable for high-frequency operation. In considering the transformer parasitics, we use the "cantilever model" [40] of the transformer, namely a single leakage inductance L_{nr}, a single magnetizing inductance L_n, and a non-physical turns ratio $N:1$.[2]

In Fig. 1, $\mathrm{C_a}$ and $\mathrm{C_b}$ are the output capacitances of the inverter and rectifier switches (plus any added capacitance). For the selected operating frequency, the leakage inductor $\mathrm{L_{nr}}$ and capacitor $\mathrm{C_{nr}}$ form a resonant tank, such that current ideally flows only at the fundamental frequency, $i_{nr} = I_{nr}\sin(2\pi f_{sw}t)$. In addition, all of the switches are synchronized and controlled by the S1 and S2 gate signals as shown in Fig. 1.

A. Operation

Fig. 2 illustrates the ideal switch timing and operating waveforms of the proposed isolated bus converter. The resonant tank (composed of inductor $\mathrm{L_{nr}}$ and capacitor $\mathrm{C_{nr}}$) is tuned to the selected operating frequency, such that the current $\mathrm{i_{nr}}$ is approximately sinusoidal. The converter operates at fixed frequency and all the switches are operated to have the same duty ratio with a fixed dead time. It is important to note that the converter operates *at* the resonant frequency, not above it as in many other resonant converters. The resonant current therefore does not aid in obtaining soft switching; ZVS is instead achieved through the magnetizing current [41], [42].

To simplify the analysis, we assume 100% efficiency and small dead time between signals S1 and S2 such that no significant power is transferred through C_{y1} and C_{y2}. With these assumptions, the converter cycles through four states as shown in Fig. 2, with the polarity of the voltages and currents as illustrated in Fig. 1. Ignoring the dead time, the magnetizing current is triangular and the resonant current is sinusoidal:

$$i_n = \begin{cases} \frac{V_{in}}{L_n}(t - \frac{T}{4}) & 0 < t < \dfrac{T}{2} \\ -\frac{V_{in}}{L_n}(t - \frac{3T}{4}) & \frac{T}{2} < t < T \end{cases} \tag{1}$$

$$i_{nr} = I_{nr}\sin(2\pi f_{sw}t) = \frac{\pi}{2}\frac{V_{out}}{R}\sin(2\pi f_{sw}t) \tag{2}$$

During the dead time, the magnetizing current is at its peak, while the resonant current is nearly zero.

The magnetizing current is used to commutate switch voltages and achieve ZVS, and analyzing this process reveals the need for C_{y1} and C_{y2}. Without them, the magnetizing current (as modeled) would charge/discharge the inverter switch capacitances, but would have no path to charge/discharge the rectifier switch capacitances. We could rely on the resonant current i_{nr} to achieve ZVS on the secondary side, but this

[2]The cantilever model provides more clarity here, though it is mathematically equivalent to the more common T-model.

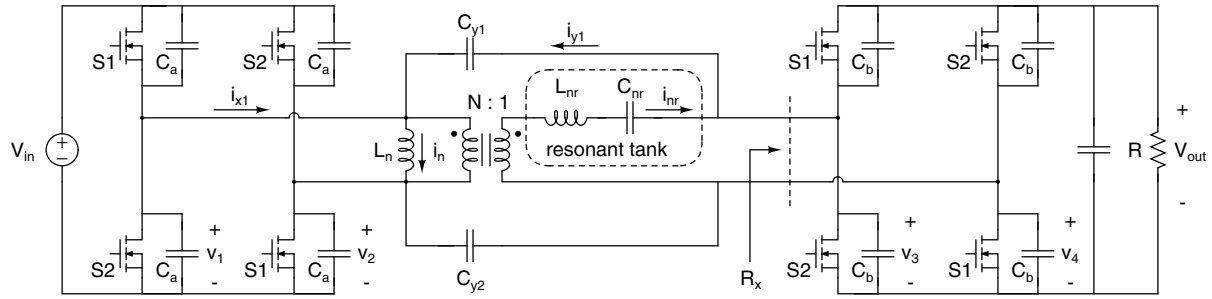

Fig. 1. The proposed isolated converter topology, comprising a full-bridge inverter, transformer, resonant tank, full-bridge synchronous rectifier, and Y-rated capacitors interconnecting corresponding inverter and rectifier switch sets.

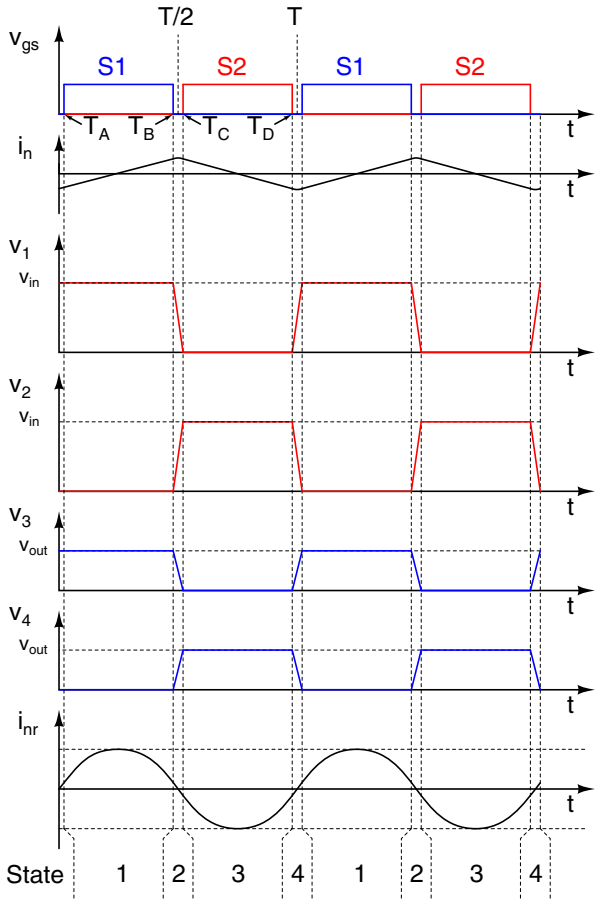

Fig. 2. The waveforms describe the voltage and current of the proposed isolated bus converter topology shown in Fig. 1. The isolation capacitor currents are equal in magnitude to a fraction of the magnetizing current (see Fig. 3) during the brief dead time (approximately constant); they are zero otherwise. Note that the only waveform that varies with power is I_{nr}, which simply decays to zero magnitude as power is decreased.

would make ZVS conditions depend on the load.[3] Instead, the addition of C_{y1} and C_{y2} gives the magnetizing current a path to charge/discharge capacitances on the inverter *and* rectifier switches, allowing the converter to decouple the goals of achieving ZVS and delivering power.

In this way, ZVS is achieved independent of load conditions. The resonant current processes power to the output, while the magnetizing current does not. Thus, as the load changes, the magnitude of the resonant current $|i_{nr}|$ will vary but the magnetizing current will not. Since ZVS is achieved purely through the magnetizing current (the resonant current is nearly zero during the dead time), ZVS is guaranteed for the same dead time independent of load.

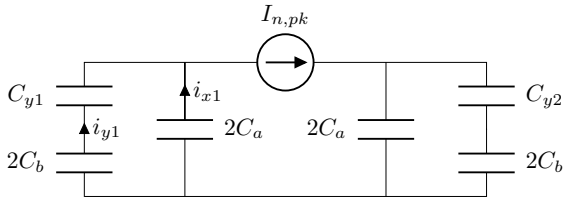

Fig. 3. Equivalent incremental circuit model during the dead time. The magnetizing current is at its peak and assumed constant for the short dead time. With C_{y1} and C_{y2}, both the primary and secondary switch capacitances can commute charge to achieve ZVS.

B. Selecting C_y

For the desired operation as illustrated above, the Y-rated capacitors (generally more capacitance than occurs naturally in the transformer) need to be selected properly to achieve ZVS conditions for all of the switches while using the same, constant dead time. During the dead time (when all of the switches are off), the current through the switches and resonant tank is close to zero. The magnetizing current, which is at its peak $I_{n,pk}$ ($\approx$ constant), flows through inverter switch capacitances (C_a), Y-rated capacitors (C_{y1} and C_{y2}), and rectifier switch capacitances (C_b) as shown in Fig. 3. For a constant dead time, a fixed charge $Q = I_{n,pk}T_{dead}$ will be transferred, and the voltage changes on the primary and secondary switches will be:

$$\Delta V_a = \frac{Q}{2C_a + C_2} \quad (= V_{in} \text{ for ZVS}) \tag{3}$$

$$\Delta V_b = \frac{\frac{C_2}{C_2+2C_a}Q}{2C_b} \quad (= \frac{V_{in}}{N} \text{ for ZVS}) \tag{4}$$

[3]The converter could be designed with sufficient resonant current to achieve ZVS with constant dead time in above-resonant operation. However at higher loads, the transition would be achieved quickly and the body diodes of the rectifier switches would conduct for much of the dead time. The loss associated with diode conduction becomes more acute at low voltage (where the diode drop is significant) and at high frequency (where the dead time is a larger fraction of a cycle).

where C_2 is the equivalent capacitance of C_y and $2C_b$ in series.

Solving the above equations for the correct value of C_y that precisely provides ZVS for the inverter and rectifier switches in the allotted dead time yields:

$$C_y = \frac{2C_b}{N-1} \tag{5}$$

C. Selecting T_{dead} and L_n

We can estimate the required dead time for the converter from the equations above. Continuing to treat the magnetizing current as nearly constant during the short dead time, its value is:

$$I_{dead} \approx I_{n,pk} \approx \frac{V_{in}T}{4L_n} \tag{6}$$

Then, the required dead time can be calculated as

$$T_{dead} = \frac{Q_{zvs}}{I_{n,pk}} = \frac{8L_n(C_a + C_b/N)}{T} \tag{7}$$

where Q_{zvs} is the charge transfer necessary to achieve ZVS from (3) and (4), with the correct C_y used to compute C_2.

It is desirable to maintain T_{dead} short while keeping $I_{n,pk}$ low for good efficiency; from (7), these goals are in conflict. Thus, L_n and T should be selected to appropriately balance these goals for a given application. Nevertheless, it should be emphasized that the required dead time is easily calculated and is independent of load.

As a bound on this tradeoff, note that during the dead time we want the magnetizing current to be large relative to the main (sinusoidal) power delivery current so that the main power delivery current does not affect ZVS. For this purpose, the magnetizing inductance needs to satisfy (10) at full load.

$$i_n(t)\ |_{t=T_{dead}/2} \ > \ \frac{i_{nr}(t)}{N}\ |_{t=T_{dead}/2} \tag{8}$$

$$\Rightarrow \frac{V_{in}}{L_n}\frac{T}{4} \ > \ \frac{\pi}{2}\frac{V_{out}}{NR}\sin(\pi\frac{T_{dead}}{T}) \simeq \frac{\pi^2}{2}\frac{P_{out}T_{dead}/T}{V_{in}} \tag{9}$$

$$\Rightarrow \quad L_n < \frac{V_{in}^2\ T}{2\pi^2 P_{out}\ T_{dead}/T} \tag{10}$$

Rearranging, the dead time and magnetizing inductance are bounded above:

$$\frac{T_{dead}}{T} < \frac{2V_{in}}{\pi}\sqrt{\frac{1}{P_{out}T}(C_a + C_b/N)} \tag{11}$$

$$L_n = \frac{T_{dead}T}{8(C_a + C_b/N)} < \frac{V_{in}T^{\frac{3}{2}}}{4\pi}\sqrt{\frac{1}{P_{out}(C_a + C_b/N)}} \tag{12}$$

For numerical context, in our prototype operating with tens of volts, tens of watts, and at about 1 MHz, we found $T_{dead}/T < 0.088$ and $L_n < 14.7\,\mu\text{H}$.

Finally, the upper bound on L_n puts a lower bound on $I_{n,pk}$,

$$I_{n,pk} = \frac{V_{in}T}{4L_n} > \pi\sqrt{\frac{P_{out}(C_a + C_b/N)}{T}} \tag{13}$$

The designer may be interested in the ratio of resonant current to magnetizing current, as the ratio of power delivery current to circulating current has bearing on efficiency. Bounded by the minimum allowable magnetizing current, this ratio comes to

$$\frac{I_{nr}}{I_{n,pk}} < \sqrt{\frac{T}{(C_a + C_B/N)R}} \tag{14}$$

where the principal ratio of interest is the $R_{out} \times C_{switch}$ time constant relative to the total period.

D. Selecting Resonant Q

Another design consideration is selecting the quality factor (Q) of the resonant tank, which is given by

$$Q = \frac{1}{R_x}\sqrt{\frac{L_{nr}}{C_{nr}}} \quad \text{where} \quad R_x = \frac{8}{\pi^2}R \tag{15}$$

where R_x is the effective impedance looking into the synchronous rectifier from the resonant tank [26] and R is the equivalent dc resistance loading the output of the bus converter.

Larger values of Q yield more sinusoidal currents, but require large L_{nr} and larger resonant voltages across C_{nr}. For a given Q the voltage across the resonant capacitor is simply Q times the fundamental voltage applied to the equivalent resonant circuit formed by L_{nr}, C_{nr}, and R_x:

$$|v_{C_{nr}}| = Q \times \frac{4}{\pi}V_{out} = Q \times \frac{4}{\pi}\frac{V_{in}}{N} \tag{16}$$

To avoid using high-voltage resonant capacitors and large leakage inductances, we prefer the lowest Q resonant tank that reasonably behaves as described in Fig. 2 across the application's load range. Because Q decreases at light load, there is a natural tradeoff between light-load performance (which benefits from higher L_{nr}/C_{nr}) and full-load performance (which benefits from lower L_{nr}/C_{nr}).

Nevertheless, resonant tanks having quite low Q will still ensure that the resonant current is sufficiently small and crossing zero during the dead time, which are the requirements for the above analysis to be valid. Indeed, as can be seen in the simulations in Fig. 4, quality factors as low as 0.1 are sufficient to ensure proper operation. In our prototype, for example, we demonstrate the effectiveness of the converter with $Q = 0.16$ at full load, which provided an appropriate balance of light-load performance, full-load performance, and size for the intended application.

E. Using loss to select switches and transformer turns

Losses in the converter are primarily due to conduction and to core loss. Switching losses are not included as all switches turn on with ZVS and turn off with sufficient switch capacitance to snub the transition. The rms currents and losses are derived in Appendix A; we quote the important conclusions here for discussion.

The mean-square current in one of the inverter switches is given by

$$I_{sw,a,rms}^2 = \left(\frac{1}{6}I_{n,pk}^2 + \frac{\pi^2 V_{out}^2}{16R^2N^2}\right)$$
$$> \frac{1}{6}\frac{\pi^2 P_{out}}{T}(C_a + C_b/N) + \frac{1}{16}\frac{\pi^2 P_{out}^2}{V_{in}^2} \tag{17}$$

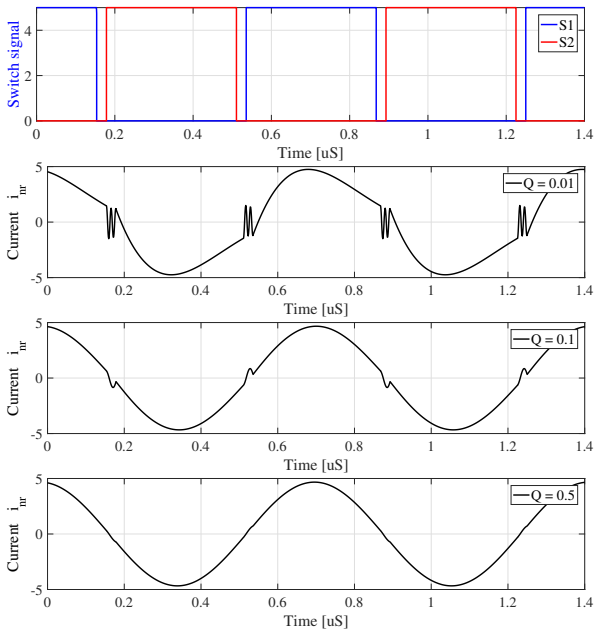

Fig. 4. Simulated resonant tank currents for various quality factors. Quality factors as low as 0.1 yield near-ideal resonant current.

where, in the inequality, we have used the minimum value for $I_{n,pk}$. The mean-square current in the primary winding is given by

$$I_{p,rms}^2 = \left(\frac{1}{3}I_{n,pk}^2 + \frac{\pi^2 V_{out}^2}{8R^2N^2}\right) > \frac{1}{3}\frac{\pi^2 P_{out}}{T}(C_a + C_b/N) + \frac{1}{8}\frac{\pi^2 P_{out}^2}{V_{in}^2} \quad (18)$$

where we have again used the minimum for $I_{n,pk}$ in the inequality. The mean-square current in one of the rectifier switches is given by

$$I_{sw,b,rms}^2 = \frac{1}{16}\frac{\pi^2 P_{out}^2}{V_{in}^2} \quad (19)$$

The mean-square current in the secondary winding is given by

$$I_{s,rms}^2 = \frac{1}{8}\frac{\pi^2 P_{out}^2}{V_{in}^2} \quad (20)$$

Finally, core loss is given by

$$P_{core} = V_{core} \times kB_{ac,pk}^{\beta} = V_{core} \times k\left(\frac{V_{in}T}{4N_pA_c}\right)^{\beta} \quad (21)$$

where V_{core} is the core volume, and k and β are the Steinmetz loss parameters associated with the core material at the operating frequency.

These equations highlight the design tradeoffs associated with switch selection. While switch resistance causes loss directly, reduced switch resistance implies increased switch capacitance (for a given technology), which requires more primary current to achieve ZVS and therefore more loss in the primary winding and in the inverter switches. Only the secondary winding loss and the core loss are unaffected by this choice.

The other principle tradeoff pertains to the number of turns on the transformer, where increased number of turns (for a given L_n) increases copper loss and reduces core loss (and *vice versa*). The switch losses are unaffected by this tradeoff.

These decisions must be examined in detail for given specifications and design goals. For example, because different loss components scale differently with power, there is a tradeoff between light load and full load efficiency. There is no single optimal version of the converter.

F. Advantages

The proposed isolated bus converter has several advantages over conventional topologies. First, the switch control circuitry and timing are greatly simplified because ZVS conditions occur simultaneously for both inverter and rectifier switches for all load conditions (for comparison with the series resonant converter, for example, see Appendix B). The converter achieves this by completely segregating the current which accomplishes ZVS (the magnetizing current i_n) from the current used for power delivery (the resonant current i_{nr}). As explained previously, this allows the dead time to be constant with respect to power and the same for both the inverter and rectifier. Once the switch components, transformer, and specifications of the converter are decided, the switch driving signals can be specified to have this single dead time. Further adaptive dead-time control is rendered unnecessary. This is especially important at high-frequency as precise control becomes more difficult.

The second advantage is reliably achieving ZVS for the rectifier switches, even at high frequency. This is made possible by the inclusion of the Y-rated capacitors interconnecting inverter and rectifier switches. Moreover, the current utilized for energy transfer is very low at the switching instants and turn-off is snubbed by C_a and C_b, providing many of the benefits usually associated with ZCS. Guaranteeing soft turn-on and relatively soft turn-off for all switches at any load permits high efficiency operation compared to many conventional resonant converters. As frequencies increase, this advantage becomes more important.

IV. Implementation and Experimental Results

To validate the above operation and advantages, we designed a prototype converter to convert 36 Vdc to 12 Vdc at up to 36 W. These specifications are drawn from the application in which the proposed bus converter will be used, but it should be emphasized that the topology's potential application is not limited to this voltage range, step-down ratio, or power level.

A. Prototype Converter Implementation

The selected components for the prototype converter are described in Table I. We used gallium-nitride (GaN) high-electron-mobility transistors (HEMT) driven by LM5113 half-bridge driver ICs. Two switching signals are generated (S1 and S2), both at 1.4 MHz frequency with a 16.66 ns dead time

between them[4]. We selected 680 pF, Y-rated capacitors for C_{y1} and C_{y2} as these are commercially available and close to the required capacitance from (5). The designer could add capacitance across the switches to get a precise match or to linearize C_a and C_b, at the cost of requiring somewhat higher magnetizing current to achieve ZVS.

We implemented the transformer using 3F45 core material with an EQ13 core structure and evenly-split gap (i.e. center post and side legs are all gapped by 0.28 mm). The transformer had 12 layers of 2 oz copper PCB traces, with six turns for the primary and two turns for the secondary as demonstrated in Fig. 6.

TABLE I
SPECIFICATIONS AND COMPONENTS OF THE PROTOTYPE CONVERTER

Specification	
Input Voltage	36 Vdc
Output Voltage	12 Vdc
Output Power	up to 36 W
Switch and Driver IC	
Inverter	GaN switch EPC 2014C Coss ≃ 150 pF
Rectifier	GaN switch EPC 2015C Coss ≃ 700 pF
Driver IC	LM5113 half-bridge driver, TI
Y-rated capacitors	
C_{y1}, C_{y2}	680 pF Y3 X7R 250 Vac (rating) and 1500 Vac (withstand), Johanson Dielectrics
Transformer	
Core	Ferroxcube 3F45 EQ13 with 0.28 mm gap
Number of Turns	6 : 2 (i.e, $N \approx 3$)
Winding	Planar structure with 62 mil thickness PCB, 12 layers of 2 oz copper (Fig. 6)
L_n	5.8 µH (measured from primary side)
L_{nr}	60 nH (estimated)
C_{nr}	0.22 µF C0G/NPO 50 V, TDK
Control	
Microcontroller	TMS320F28035, TI (for prototyping)
Switching Frequency	1.4 MHz
Dead time	16.66 ns

We used the leakage inductance[5] (≈ 60 nH) as the resonant inductance, and selected a 0.22 µF resonant capacitor through the tuning process described below (using a C0G/NPO capacitor with low dissipation factor). From the tuned resonant capacitance and the selected operating frequency, the quality factor Q was around 0.16 at full load. Fig. 5 shows the top and bottom sides of the implemented prototype converter including the components described above.

B. Resonant Tuning

To operate the prototype converter as described in Section III, the resonant tank of the converter should be tuned at the operating frequency. If the leakage inductance of the transformer is used as the resonant inductor, its small inductance may be difficult to measure and some tuning of C_{nr}

[4]From (7), an actual dead time of ∼25 ns is required, which can be discerned in Figs. 8-9. However, the turn-on/turn-off and delay time mismatches from the LM5113 require that the digital input signal have the shorter dead time of ∼17 ns, which is reported here for replicability.

[5]The leakage inductance of the primary was small enough to ignore. This makes the components of the cantilever model approximately equal to those of the T model, including the turns ratio.

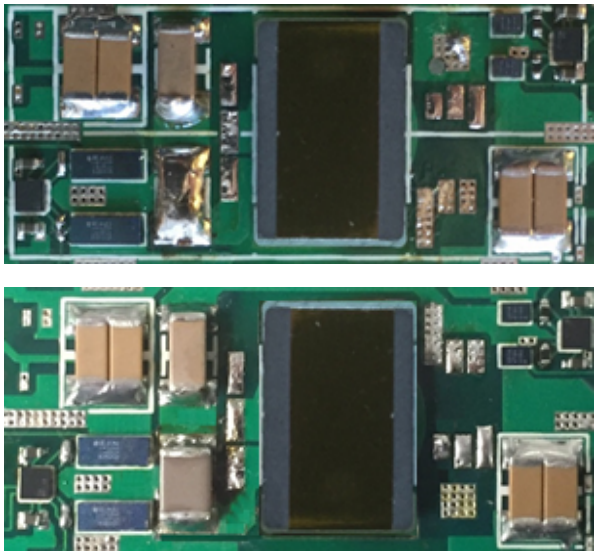

Fig. 5. Top and bottom sides of the prototype converter. The main power stage has a size of 1.2 in × 0.6 in × 0.17 in, yielding a power density of 300 W/in^3.

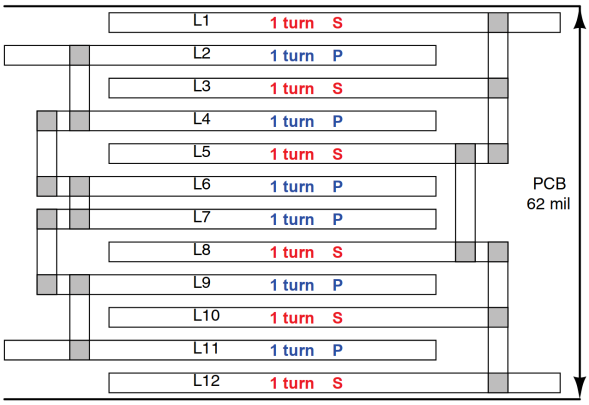

Fig. 6. Transformer layer configuration of the prototype converter. The primary winding has 6 turns, each on a separate layer (94 mil traces). The secondary winding has 2 turns, each formed of 3 parallel traces on separate layers. All windings are realized with 2 oz copper.

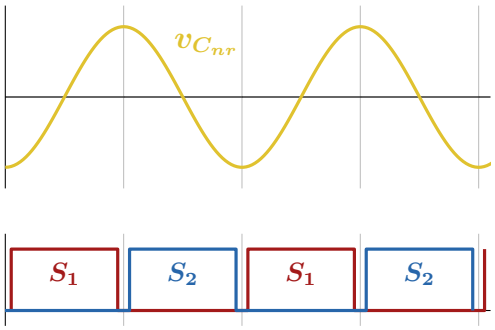

Fig. 7. Expected waveforms when the resonant frequency and operating frequency are properly tuned. The resonant tank can be tuned by measuring the phase of the resonant capacitor voltage referenced to the control signals.

or frequency may be necessary. Nevertheless, this process only need be completed once for a given design, at least for planar magnetic implementations with highly repeatable leakage inductance. Tuning can be achieved without HF current measurements by instead measuring the voltage across the resonant capacitor; at resonance, v_{cr} should be 90° out of phase with the S1 and S2 gate signals as shown in Fig. 7.

C. Experimental Results

Figs. 8-9 illustrate experimental converter waveforms at 36 W and 18 W loads respectively. As described in Section III-F, the converter operates at constant frequency (1.4 MHz) and dead time and maintains ZVS as load varies.

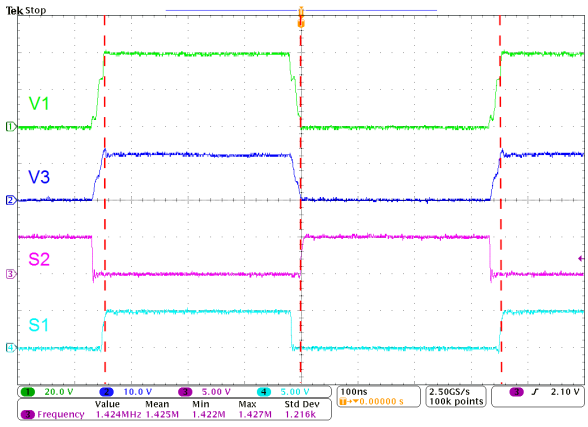

Fig. 8. Experimental waveforms at full load. The primary and secondary switches achieve ZVS (red dashed lines) at the same time using the same control signals.

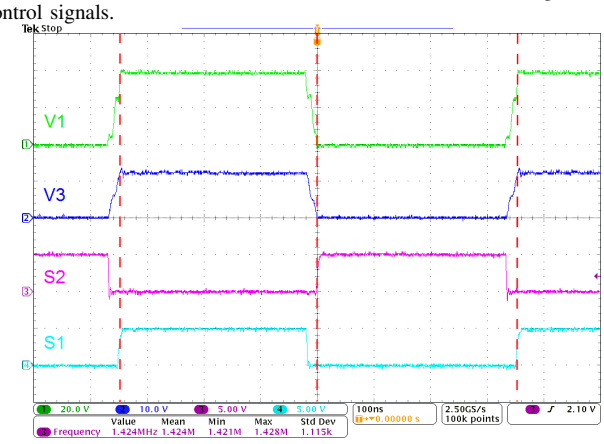

Fig. 9. Experimental waveforms at half load. Compared with the full-power case (Fig. 8), the primary and secondary switches still achieve ZVS (red dashed lines) even though the same control signals are used.

Fig. 10 shows a captured thermal image from a FLIR E6 infrared camera with the converter operating at full load in a ∼25 °C environment without active cooling. It can be seen that the peak temperature rise observed is less than 20 °C above ambient. The majority of the loss can be seen to come from the transformer, which is reasonable considering the soft switching operation of the switches.

With the aid of zero-voltage switching operation and maintaining ZVS independent of the load level, the prototype converter shows $> 94\,\%$ efficiency over a wide load range (Fig. 11), yielding a high power density of $300\,\mathrm{W/in^3}$. Note that the decrease in efficiency at very light load is only partly caused by waveform distortion at low Q; in large part, it is caused by the resonant current (which processes the power) becoming small relative to the magnetizing current (which processes no power but does cause copper/core loss which is independent of load). The experimental efficiency is predicted in Fig. 11 at even lighter loads by assuming that loss remains constant at the same level as the 8.5 W experimental data point, a good assumption given that the dominant loss at light-load arises from the constant magnetizing current. Since some losses will in fact decrease with power, this represents a conservative prediction.

Finally, recall that this technique was intended to simplify control. This is demonstrated here by noting that the dead time was the same for both inverter and rectifier switches. Its value, once set, was held constant across all operating conditions and no adaptive dead-time control was necessary. This is a significant advantage for operating well into the MHz regime and beyond.

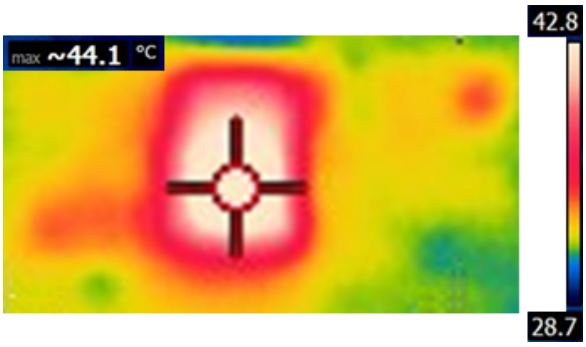

Fig. 10. Infrared thermal image of the converter operating at full power in a 25 °C ambient without active cooling. Low temperature rise is achieved and low switch losses in particular are expected from achieving ZVS (compare to Fig. 5).

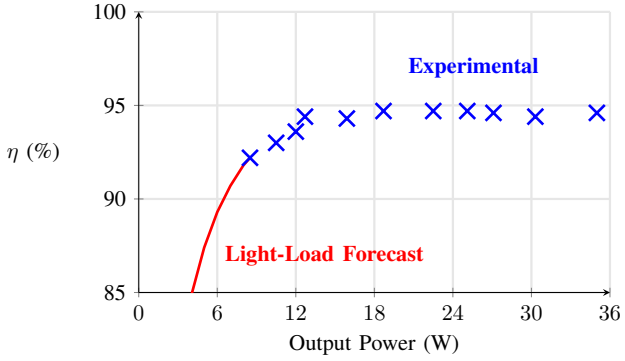

Fig. 11. Experimental efficiency of the prototype converter across power, showing high efficiency for a wide load range since ZVS is maintained; constant magnetizing current causes efficiency droop at light load, which is forecast to lighter-load conditions by assuming constant loss.

V. Conclusion

We proposed a capacitively-aided zero voltage switching (ZVS) technique for isolated bus converters, intended to simplify control and achieve high performance at ever-increasing

switching frequencies. The proposed technique has the advantages of achieving ZVS turn-on and low-current turn-off with synchronous rectification – all with load-independent timing of the inverter and rectifier switches. This matched control timing for both the inverter and rectifier switches is achieved through the use of Y-rated capacitors interconnecting the inverter and rectifier switch nodes. With properly selected interconnecting capacitors, the ZVS conditions for inverter and rectifier switches occur at the same time, and the required dead time for ZVS operation becomes independent of the load of the converter. These characteristics greatly simplify control, especially when the converter operates at high frequency where control timing is a major design constraint. The proposed approach is demonstrated in a prototype converter which operates from $36\,\mathrm{Vdc}$ to $12\,\mathrm{Vdc}$, at up to $36\,\mathrm{W}$ load at a fixed switching frequency of $1.4\,\mathrm{MHz}$. Experimental results support the efficacy of the proposed approach, including ZVS soft switching for all devices, load independent control, and excellent efficiency over a wide load range. The prototype converter achieves higher than $94.5\,\%$ efficiency across a significant load range with a high $300\,\mathrm{W/in^3}$ power density, with substantial thermal margin.

Appendix A
Loss Analysis

Due to the constant operation of the converter, the rms currents are easily calculable and can be used to predict loss as a function of voltage and power.

Consider the inverter switches driven by the S1 signal (due to symmetry, the switches driven by S2 will have the same rms current). Their current is

$$i_{sw,a} = \frac{V_{in}}{L_n}\left(t - \frac{T}{4}\right) + \frac{\pi V_{out}}{2R}\frac{1}{N}\sin\left(\frac{2\pi}{T}t\right) \qquad (22)$$

from $t = 0$ to $t = T/2$, and zero otherwise. Their rms current is therefore

$$\begin{aligned} I_{sw,a,rms} &= \sqrt{\frac{1}{T}\int_0^{T/2} \frac{V_{in}^2}{L_n^2}\left(t-\frac{T}{4}\right)^2 + \frac{\pi^2 V_{out}^2}{4R^2N^2}\sin^2\left(\frac{2\pi}{T}t\right) + \frac{V_{in}V_{out}}{L_nRN}\left(t-\frac{T}{4}\right)\sin\left(\frac{2\pi}{T}t\right)\; dt} \\ &= \sqrt{\frac{1}{96}\frac{V_{in}^2T^2}{L_n^2} + \frac{\pi^2P_{out}^2}{16V_{in}^2} + 0} \\ &= \sqrt{\frac{1}{6}I_{n,pk}^2 + \frac{1}{4}\left(\frac{I_{nr}}{N}\right)^2} \\ &= \sqrt{\frac{1}{2}I_{n,rms}^2 + \frac{1}{2}\left(\frac{I_{nr,rms}}{N}\right)^2} \end{aligned} \qquad (23)$$

The primary current into the transformer is found similarly by integrating across the whole period.

$$\begin{aligned} I_{p,rms} &= \sqrt{\frac{1}{T}\int_0^T \left(\frac{V_{in}}{L_n}\left(t-\frac{T}{4}\right) + \frac{\pi V_{out}}{2R}\frac{1}{N}\sin\left(\frac{2\pi}{T}t\right)\right)^2 dt} \\ &= \sqrt{\frac{1}{48}\frac{V_{in}^2T^2}{L_n^2} + \frac{\pi^2P_{out}^2}{8V_{in}^2} + 0} \\ &= \sqrt{\frac{1}{3}I_{n,pk}^2 + \frac{1}{2}\left(\frac{I_{nr}}{N}\right)^2} \\ &= \sqrt{I_{n,rms}^2 + \left(\frac{I_{nr,rms}}{N}\right)^2} \end{aligned} \qquad (24)$$

The rectifier switch currents are found in the same way, with only the contribution from the resonant current:

$$\begin{aligned} I_{sw,b,rms} &= \sqrt{\frac{1}{T}\int_0^{T/2} \left(\frac{\pi V_{out}}{2R}\sin\left(\frac{2\pi}{T}t\right)\right)^2 dt} \\ &= \frac{1}{4}\frac{\pi P_{out}}{V_{out}} \\ &= \sqrt{\frac{1}{2}I_{nr,rms}^2} \end{aligned} \qquad (25)$$

And the secondary current from the transformer is equal to the resonant current, which yields:

$$\begin{aligned} I_{s,rms} &= I_{nr,rms} \\ &= \sqrt{\frac{\pi^2V_{out}^2}{8R^2}} = \sqrt{\frac{\pi^2P_{out}^2}{8V_{out}^2}} \end{aligned} \qquad (26)$$

Conduction losses from the above currents can be found using the switch resistances and the transformer ac resistance matrix.[6] Switching loss is not included in this analysis, as every switch turns on with ZVS and turns off with sufficient switch capacitance to snub the transition.

Finally, core loss can be estimated from the peak magnetic field in the core:

$$B_{ac,pk} = \frac{I_{n,pk}L_n}{N_pA_c} = \frac{V_{in}T}{4N_pA_c} \qquad (27)$$

where N_p is the number of primary turns (for the magnetizing inductance L_n referred to the primary) and A_c is the cross-sectional area of the core. Core loss can then be found approximately using the Steinmetz equation $P_{core} = V_{core} \times kB_{ac,pk}^{\beta}$, where V_{core} is the core volume and k and β are parameters of the core material at the operating frequency.

Appendix B
Comparison to Series Resonant Converter

Because the proposed converter topologically resembles the series resonant converter (SRC), it may be profitable to compare the two converters in simulation.

[6]The ac resistance matrix of the transformer is the most prone to estimation error, as one cannot necessarily assume that current and flux densities are well distributed. A naïve one-skin-depth-conduction assumption underestimates the experimental loss in the transformer in this work, for example.

Parameters for the comparison systems are given in Table II, with parameters from the proposed converter taken from the prototype presented in the paper.

The SRC, as it is typically operated, has ignorably large magnetizing inductance and is operated above resonance to achieve ZVS. Thus, several changes must be made to the converter parameters to achieve a fair comparison. First, although the same transformer core and material are used, the turns ratio must be slightly closer to 1 (so the SRC can operate above resonance) and the transformer for the SRC is ungapped to increase magnetizing inductance.

In addition, the SRC is a variable frequency converter; the proposed converter is not. To achieve the fairest possible comparison, the SRC must be restricted to a somewhat narrow frequency range, implying a significantly higher resonant characteristic impedance Z_0. As such, in the SRC, an additional inductor beyond the leakage inductance is required with an assumed Q_L of 300. It should be noted that even a narrow frequency range is still often a significant disadvantage compared to a single-frequency converter.

TABLE II
PARAMETERS FOR CONVERTER COMPARISON

	Proposed	Series Resonant
Turns	6:2	5:2
Primary Resistance	15 mΩ	12.5 mΩ
Secondary Resistance	2 mΩ	2 mΩ
Primary Switch Resistance	32 mΩ	32 mΩ
Secondary Switch Resistance	8 mΩ	8 mΩ
Steinmetz parameter k [25]	0.03	0.006-0.103
Steinmetz parameter β [25]	2.55	2.55
Resonant Inductance	60 nH	3 µH
Resonant Capacitance	220 nF	30 nF
Z_0	0.5 Ω	10 Ω
Resonant Inductor Q_L	-	300
Magnetizing Inductance	5.8 µH	50 µH

The primary comparison to be made between the SRC and the proposed converter is in control. To achieve high efficiency, both converters are operated with timings that achieve ZVS and minimize diode conduction time on the secondary switches. The proposed converter is operated with fixed timing at fixed frequency, as shown in Figs. 12-13. By contrast, the SRC must vary both frequency and on-time to maintain fixed conversion ratio and low diode conduction time as a function of load. This is an especially difficult challenge in practice for high switching frequencies, which are desirable for miniaturization.

The two converters may also be compared in terms of efficiency. While the proposed converter requires more magnetizing current to achieve ZVS, the SRC requires higher resonant current to achieve the same effect (and additional losses in the resonant path). This can be seen in the light-load and full-load performance of the two converters (Figs. 14-15). While there is some efficiency tradeoff at light load between the two converters (in this example incarnation), the much more significant effect is seen at full load where the losses in the resonant path greatly reduce the performance of the SRC.

The high Z_0 of the SRC is likewise problematic when examining the resonant capacitor, which must store much more

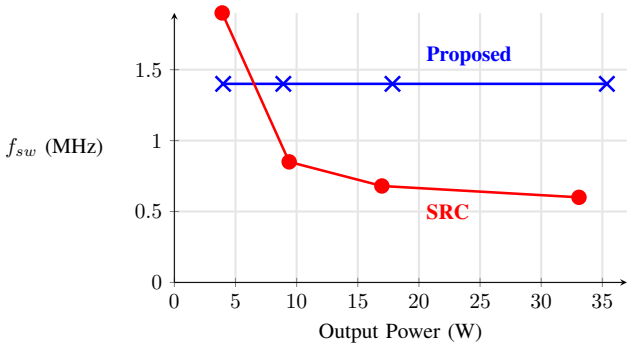

Fig. 12. Simulated switching frequency f_{sw} of the proposed converter and the SRC, contrasting the constant timing operation of the proposed converter with the variable-frequency nature of the SRC.

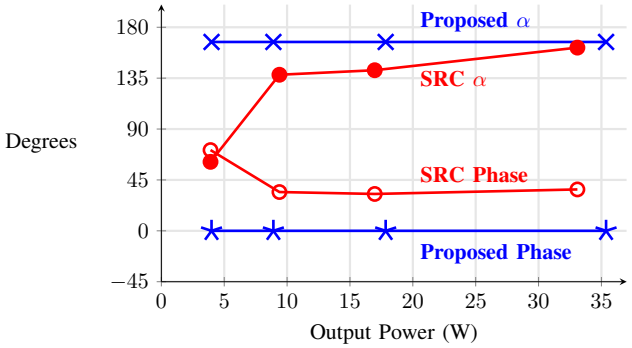

Fig. 13. Simulated conduction angle α and phase shift of the secondary switches to achieve ZVS with minimal diode conduction, contrasting the load-invariant operation of the proposed converter with the highly load-dependent operation of the SRC. Because the SRC depends upon the resonant current to achieve ZVS, the conduction angle decreases with load, which also causes losses without transferring power.

energy (Fig. 16) and withstand much higher voltages (Fig. 17) than in the proposed converter. These have implications for the size and cost of the resonant components, and high peak voltages may impact part availability and PCB spacing in some applications.

A. Other alternatives

It may also be profitable to consider two more operation alternatives with identical circuit parameters. First, we may investigate what happens when the isolation capacitors are removed from the proposed converter with no change in operation. Second, we may investigate how the converter would behave if the secondary switches could be controlled as ideal diodes. We set up each case at full power (36 W) and observe circuit behavior as power is decreased, as seen in Fig. 18. Timing is not changed as power is decreased, except in the second case to maintain ideal diode behavior on the secondary.

The proposed converter achieves the lowest rms inductor current and most reliable waveforms as power is decreased. Merely removing the capacitors causes a phase shift in resonant current which helps achieve ZVS on the secondary but works against achieving ZVS on the primary (the magnetizing current is large enough in this case to overcome the negative

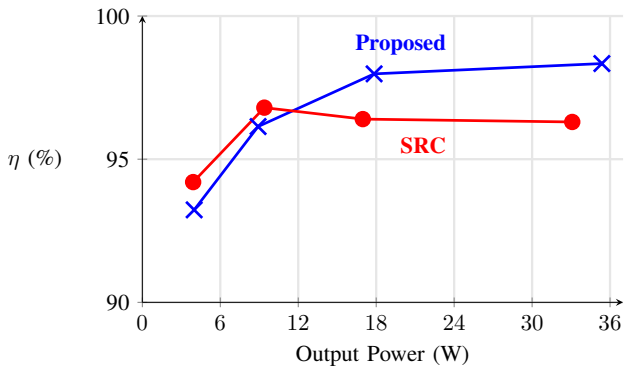

Fig. 14. Simulated efficiency for the proposed converter, showing comparable light-load behavior with greatly improved full-load efficiency for the proposed converter.

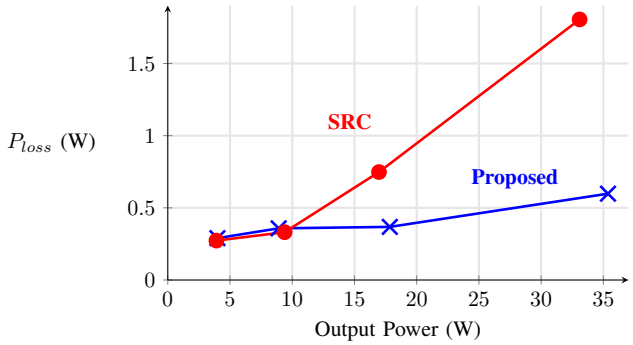

Fig. 15. Simulated losses corresponding to the efficiencies in Fig. 14, highlighting that the volume-setting peak losses in the SRC are significantly higher than in the proposed converter.

tank current even at full power, but may not be in every case). The phase offset in the tank current results in low power factor and needless transfer of charge (i.e. high rms current per unit power). Finally, operating the converter with no capacitors and ideal diodes on the secondary exhibits the worst results. Long dead times are required to allow the small tank current to charge the secondary parasitic capacitances, resulting in poor waveforms as power is decreased. In addition, the timing on the secondary requires a dead time change of 110 ns and an equivalent time-shift change of 55 ns as power is decreased from 36 W to 9 W. This violates the desired invariant control that the proposed converter provides. In general, converter behavior across power is not well controlled in these alternate cases. As power is decreased beyond the moderate 25 % load presented here, these disadvantages become more severe.

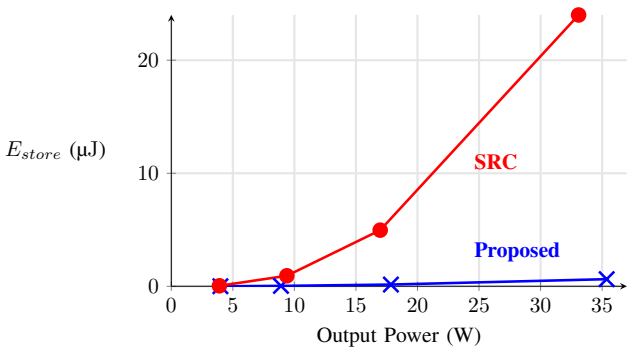

Fig. 16. Simulated resonant energy storage (which corresponds to volume of the resonant elements), constrasting the high energy storage of the SRC (due to its high Z_0 requirement) as opposed to the proposed converter.

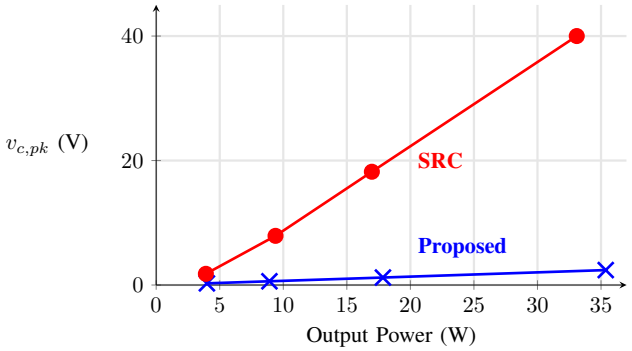

Fig. 17. Simulated peak resonant capacitor voltages (which may set spacing and part availability for some applications), contrasting the high voltages in the SRC (due to its high Z_0 requirement) as opposed to the proposed converter.

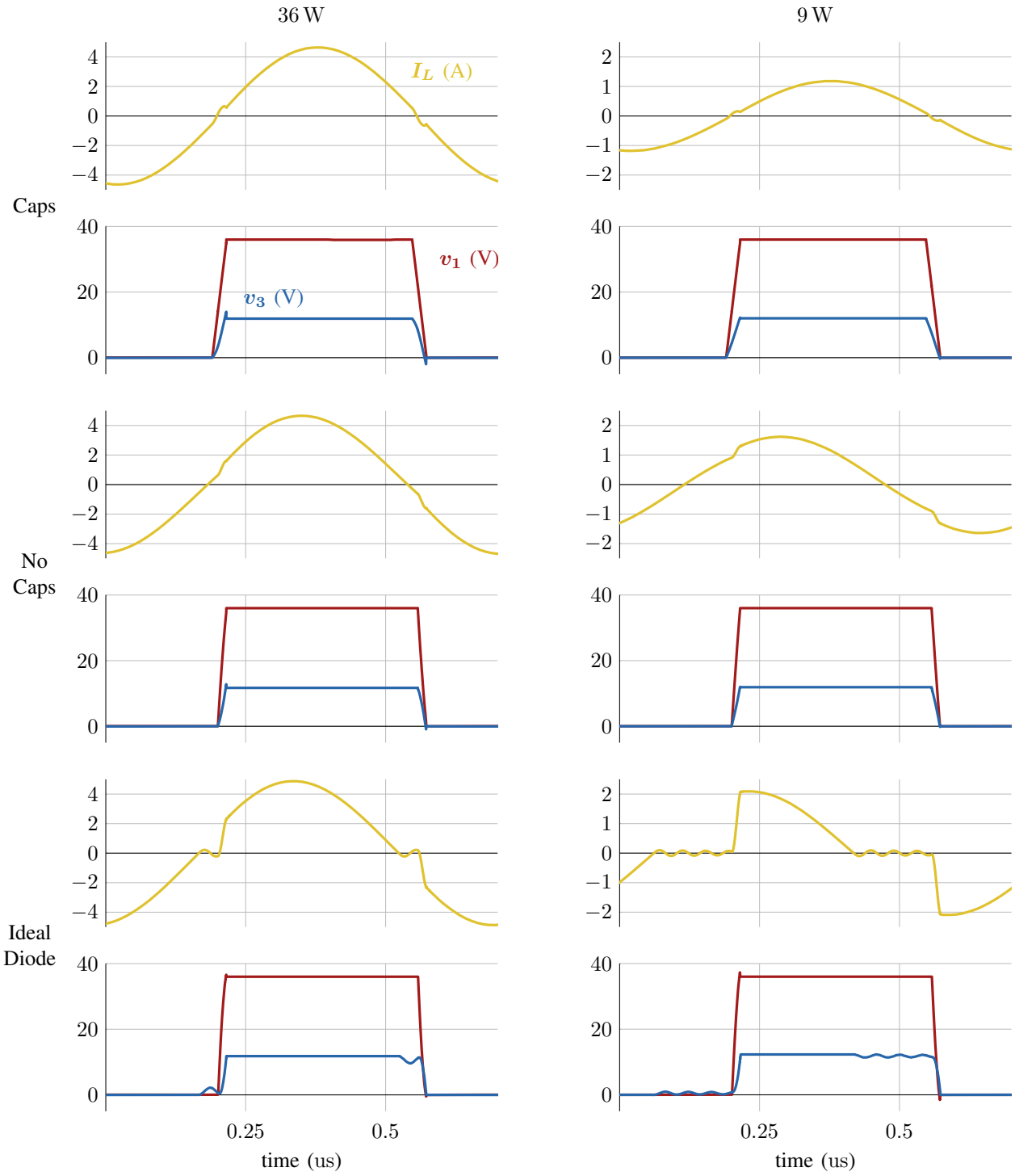

Fig. 18. Simulated results from the proposed converter ("caps"), from the proposed converter with identical components and the isolation capacitors removed and optimized dead time ("no caps"), and from the proposed converter with the secondary devices controlled to act as ideal diodes ("ideal diode"). For the first two cases, operating parameters are set for the 36 W case and are not changed for the 9 W case. Only the secondary timing is changed to maintain ideal diode behavior in the third case. The proposed converter exhibits the best results.

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