# A 380-12V, 1kW, 1MHz Converter Using a Miniaturized Split-Phase, Fractional Turn Planar Transformer

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Abstract—High step-down, high output current converters are required in many common and emerging applications, including data center server power supplies, point-of-load converters, and electric vehicle charging. Miniaturization is desirable but challenging owing to the high-step-down transformer ubiquitously used in these converters. In this work, a miniaturized split-phase half-turn transformer is demonstrated which leverages the wellestablished parallelization benefit of employing multiple phases, as in a matrix transformer, with the dramatic reduction in copper loss associated with the relatively new Variable Inverter/Rectifier Transformer (VIRT) architecture. While these techniques have been described in earlier studies, their combination has not been well explored. A detailed design procedure is described and is used to develop a 97.7% peak efficiency, 97.1% full-load efficiency prototype having a transformer that is 12-36% smaller than best-in-class designs in the literature at the same power level, while also being more efficient. This work showcases the miniaturization benefit of employing multi-phase, fractional-turn transformers in high step-down, high output current applications and provides comprehensive guidance to designers interested in applying and extending these techniques.

*Index Terms*—Data center server power supply, LLC converter, Variable Inverter/Rectifier Transformer, VIRT, fractional turn, half-turn, high step down, multi-phase, split-phase

#### I. INTRODUCTION

Many applications rely on high voltage step-down converters capable of delivering high output current, including data center server power supplies, 48V to point-of-load converters, and electric vehicle chargers. Power density is a critical performance metric in these applications, as a miniaturized converter allows for more of the limited system volume to be allocated to the targeted functionality (e.g. storage and computational ability in a server). The inherent challenge of miniaturization is that as volume is decreased, loss must also decrease in order to satisfy thermal limits in the smaller form factor. Power magnetic components are especially challenging to miniaturize as magnetic scaling laws fundamentally work against achieving high efficiency at small sizes [1].

Transformers are ubiquitously employed in high step-down, high output current converters, and present a critical bottleneck toward miniaturization. The recent emergence of highperformance, high-frequency magnetic materials presents the opportunity for significant gains in miniaturization by operating in the 1-10 MHz regime [2]. However, the following key challenges must be addressed:

- At high frequencies the current carrying capability of copper is greatly diminished by skin- and proximity effects. This is problematic at high current as copper loss can dominate and make it especially challenging to employ a small form factor.
- 2) In high step-down transformers, a high primary turns count is required. It is difficult to accommodate these turns in a miniaturized form factor owing to insulation and/or practical turn-to-turn spacing requirements, especially in planar magnetic designs in which windings are implemented on a printed circuit board (PCB). This further aggravates copper loss in addition to the inherent challenge of high current operation.
- 3) Planar magnetic designs are especially promising for transformer miniaturization, offering strong advantages in terms of manufacturability, repeatability, and cost compared to wire-wound alternatives [3]. However, they present challenges in this regime owing to poor window fill factor and the potential for high inter- and intrawinding capacitance. Furthermore, high-current, highfrequency planar windings can incur large loss in their terminations (i.e. in the copper traces and vias that connect the windings to the rest of the circuit), especially in highly interleaved designs [4].

One attractive means to address these challenges is to decompose the transformer into multiple smaller transformers having a series-primary, parallel-secondary connection. In doing so, the current rating and step-down requirement of each transformer is reduced, mitigating the challenges of high current carrying and high turns count. This is the central paradigm behind miniaturization in "cellular" converters, which place multiple converter stages in parallel [5], and in the matrix transformer (MT) concept, which employs a multi-element series-primary, parallel-secondary transformer within a single conversion stage [6]. This paradigm has been explored at length in the literature, and optimized prototypes have been developed with high power density, highlighting the benefits of transformer parallelization. However, magnetic scaling laws work against the distribution of a single large magnetic component into multiple smaller ones [1]. Thus, from the perspective of transformer miniaturization, there may be opportunities for improvements over these distributed

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Fig. 1: LLC DCX schematic.

transformer architectures.

Another promising concept is the Variable Inverter/Rectifier Transformer (VIRT) [7], [8]. This is a recently proposed architecture that builds on a new paradigm in which magnetic and electronic systems are hybridized, viewed and designed as one coupled system, rather than their conventional treatment as separate elements. Note, for example, that in the popular LLC dc transformer (DCX) topology shown in Fig. 1, the transformer connects to the output via rectifiers. In the VIRT architecture, the step-down capability of the transformer is increased not by employing elemental transformers having a series-primary connection, but by carefully distributing the rectifiers around the magnetic core. In doing so, the effective turns ratio of the transformer is increased. For example, [8] showcases a 'half-turn' implementation in which a 24:1 stepdown ratio is achieved with one magnetic core and 12 primary turns, behaving as if a 'half-turn' is wound on the secondary<sup>1</sup>, and also illustrates how other 'fractional turn' secondaries can be realized, including a 'quarter-turn' secondary implementation. In the VIRT approach, the current in the secondary windings, and the ac conduction length, is reduced, greatly reducing copper loss. These benefits come at the price of increased core loss, but this can be a favourable trade-off in copper-loss dominated high-step-down, high-current transformers.

It should be emphasized that in the VIRT 'fractional turn' transformer concept, the secondary winding still comprises one net turn<sup>2</sup>. The electronics connecting to the partial turn segments allow the output voltage to be inserted multiple times into the single secondary loop, and this increases the *effective* turns ratio of the transformer. The name 'half-turn' is used both to reflect that the connecting electronics partition the single secondary winding into two halves and to reflect the fact that  $N_p/2$  primary turns can be used to achieve  $N_p$ : 1 step-down, *mathematically* equivalent to the secondary comprising "half a turn".

From the initial proposal of the VIRT in [7], additional studies have evaluated a half-turn [11], [12], and quarter-turn transformer (QTT) using center-tapped rectifiers (CTRs) in a 380-12V, 1kW data center server power supply application [13]. The use of a CTR reduces the number of switches that are required, but increases the copper loss of the transformer

compared to a full-bridge rectifier [14], diminishing a central benefit of the fractional-turn technique.

Another recent work describes a different concept for a "fractional turn" in which it is proposed that a transformer can be wound with a secondary having a winding length that is less than one full turn [15]. That work employs a modification of the matrix transformer concept in which four CTRs are paralleled around a single UI core, rather than the original proposal of two CTRs paralleled around a single UI core [6], [16]. Therefore, as expected for a matrix transformer, the transformer in [15] requires 16 primary turns to achieve 16:1 step-down. The proposed "fractional turn" behaviour is derived by distributing the rectifiers around the core, allowing them to be connected though only a fraction of the core window length. It is argued that this decreases conduction loss. However, the application of Faraday's law requires the identification of complete physical loops, and current must flow in closed loops. Thus, current will return in the connections made outside the core window, with corresponding contributions to conduction loss. These windings are therefore 'fractional' only in the sense that a fraction of the full loop traversed by the secondary current is inside the core window. The proposal of "fractional turns" in [15] is fundamentally different from the previously established definitions for fractional-turn transformers [8]. To avoid confusion, it is emphasized that in the fractional-turn transformers described in this work, complete secondary loops are always defined and an  $N_p$ : 1 conversion ratio is achieved with fewer than  $N_p$  primary turns.

This paper evaluates the miniaturization potential of a transformer which combines the well-explored concept of increasing transformer phase count with the relatively new VIRT fractional-turn concept. These techniques offer distinct loss trade-offs, and this paper also describes a framework to intuitively understand the inherent loss trade-offs that are made when moving between these techniques, and when combining them. This study greatly expands on our earlier work in [17], which presents a comparative basis to evaluate the use of fractional-turns and multiple phases for transformer miniaturization.

Section II provides an overview of the multi-phase VIRT and provides an intuitive framework to understand its loss trade-offs. Section III discusses in detail the critical design considerations for developing a high performance split-phase half-turn VIRT (SPHTV) and proposes a recommended design procedure. Section IV discusses the layout considerations involved in developing a high-performing prototype. Section V presents the experimental results, demonstrating a peak power-stage efficiency of 97.7% achieved in a transformer and rectifier box volume of 14.2cm<sup>3</sup>. The performance of the transformer is compared to the highest performing state-ofthe-art implementations of 380-12V, 1kW transformers in the literature and it is shown to achieve higher efficiency in a lower volume. Thus, this work demonstrates the high performance capability of a multi-phase, fractional-turn transformer for achieving miniaturization in high-current, high step-down converters.

<sup>&</sup>lt;sup>1</sup>This effective turns ratio is also variable via control over the operation of the rectifier switches, though this functionality is not employed in the fixed-gain DCX case study of this work.

<sup>&</sup>lt;sup>2</sup>The name 'fractional turns' was first proposed by Perica [9] and Dixon [10] to refer to transformers having physical turns ratios smaller than their conversion ratios (originally derived by employing a full turn coupling fractional flux).



Fig. 2: Derivation of the split-phase transformer. (a) Two single phase transformers with primaries carrying equal current are wound to produce opposing flux in their respective outer legs. (b) The cores are combined to form a split-phase transformer, taking advantage of flux cancellation in the core legs. The dimensions of the core are indicated, with the unlabeled dimension *a* being the length of the core (i.e. the depth of the core into the page).  $\mu_c$  is the permeability of the core.

# II. OVERVIEW OF MULTI-PHASE AND FRACTIONAL TURN TRANSFORMERS

A split-phase transformer can be constructed from two single-phase transformers, each wound such that they produce equal and opposite flux in their outer legs as illustrated in Fig. 2. These separate transformers can be combined into a single, smaller, core by taking advantage of the equal and opposite flux in their outer legs<sup>3</sup>. This kind of core flux cancellation is a hallmark of integrated multi-phase transformers, and has been employed in matrix [18] and three-phase [19] builds.

### A. Loss Trade-offs

Note that the derivation of the split-phase transformer in Fig. 2 makes no assumption on whether or not fractional turns are employed. This emphasizes the distinct nature of the two techniques. The development of multi-phase or matrix transformers relies on duplication of an "elemental" transformer and creates the opportunity to leverage equal and opposite flux flows to reduce overall core size. The VIRT architecture instead relies on a symmetric distribution of rectifiers around a magnetic core. These techniques offer different scalings between core- and copper loss, and in different applications one of the two techniques, or a combination of them, is best suited for miniaturization. The study initially published in

[17], and summarized in Fig. 3, provides a framework for determining which combination is best for a given application, and shows, for example, that the SPHTV is well-suited for the 12V, 1kW application explored in this work. For completeness, this comparison is reproduced in Appendix A.

To provide intuition on what these distinct techniques offer a designer, Fig. 3 summarizes their core and copper loss trade-offs assuming the same core dimensions are used [17]. A designer can associate adding phases with a linear tradeoff of core and copper loss (e.g. moving from single-phase to two phases yields approximately half the copper loss and twice the core loss) while increasing the degree of fractional turn (e.g. no VIRT to half-turns to quarter-turns) can be viewed as an exponential trade-off of these losses (e.g. a halfturn increases core loss by  $2^{\beta}$ , where  $P_v = k f^{\alpha} B^{\beta}$  is the Steinmetz equation for core loss<sup>4</sup>, but decreases copper loss by more than a factor of 4). In practice, a designer would re-optimize the transformer's dimensions to minimize loss, and in doing this the simple relationships described above no longer hold. However, they can provide intuition as a kind of "gear change" for copper- and core loss. For example, if an optimized transformer is copper loss dominated after adding a second phase to the design, a designer can try a deeper tradeoff by shifting to a fractional turn design, and then continue to add phases and/or degrees of fractional turns until a loss minimum has been reached.

## B. Split-phase Half-turn VIRT Circuit Model

Consider the cross-section shown in Fig. 2b. Assume that the same current  $i_p$  flows in each primary winding and that the secondary half-turns<sup>5</sup> and the connecting rectifiers are laid out in a symmetric fashion about the center of the transformer. Each primary phase generates the same flux in the two inner posts and this flux flows through the core as shown by the dashed red lines. Assuming that the core has a permeability much larger than free space, the magnetomotive force ( $\oint H \cdot dl$ ) around each set of four primary turns and one half-turn is identical. Thus, by Ampère's Law, the currents  $i_1, i_2, i_3$ , and  $i_4$ are equal to one another. This is a consequence of symmetry: no further assumption must be made about the physical connection of the secondary half-turns. For example, in a non-fractional-turn split-phase transformer,  $i_1 = i_2$  because these currents flow in the same conductor; in the SPHTV,  $i_1 = i_2$  by symmetry, even if they are not directly connected. A VIRT design takes advantage of this fact by connecting each of these secondary half-turns to rectifiers, enabling increased voltage step-down of the transformer [8]. The physical design considerations associated with achieving this symmetry are discussed in Section IV.

From the physical current flows in Fig. 2b, the magnetic circuit model in Fig. 4a can be derived. The MMF sources associated with the currents in the secondary,  $i_s$ , are shown in

<sup>&</sup>lt;sup>3</sup>Note that this is only a particular example of flux cancellation; the technique can be leveraged for other core shapes and winding orientations in order to eliminate desired core sections.

 $<sup>{}^{4}\</sup>beta$  is typically between 2 and 3.

<sup>&</sup>lt;sup>5</sup>Because the secondary conductors in the core window do not directly form closed loops (they are closed by the switching rectifiers), it is most appropriate to describe them as conductors rather than 'turns'. However, the term 'half-turn' is used for consistency with the standard nomenclature of a transformer.



Fig. 3: Example loss trade-off between copper- and core loss associated with increasing the number of parallel phases and increasing the degree of fractional turns in a transformer. These simple relationships only hold if the same core dimensions are used [17], but they provide useful intuition on the scaling benefit of a given technique.  $\beta$  is the Steinmetz coefficient associated with flux-density.

series with the primary MMF sources, reflecting the fact that these currents form closed loops around the inner core legs (flowing through the local decoupling capacitors of each halfbridge rectifier). Note that  $N_p$  in this model is the number of primary turns around each center-post. For example, in Fig. 2b  $N_p$  is four. This model includes three additional features: two external reluctances accounting for the fact that there is a finite reluctance path for flux through the space around the core, and a transferance element  $\mathscr{L}_{ext}$  [20] to model the fact that a conductive loop may exist around the transformer. For example, dc connections may be required between all of the rectifiers in order to tie them to a single output bus, and these constitute a conductive loop having some resistance  $R_{conn}$ . Noting that the external reluctance is likely to be much larger than the core reluctances, and that the transferance provides additional impedance to this external flux, it is assumed that negligible flux flows through this external path.

The magnetic circuit model in Fig. 4a also demonstrates the importance of having both gaps  $g_1$  and  $g_2$  in the transformer. If  $g_2$  is removed, then the reluctance between the two center posts,  $4\mathscr{R}$ , reduces to zero. This would cause all of the generated center-post fluxes to travel through this part of the core rather than being shared with the outer legs, increasing



**Fig. 4:** Magnetic circuit and equivalent electrical model of the SPHTV. (a) Magnetic circuit including external reluctances and a transferance associated with dc connections between the rectifiers. (b) Electrical circuit model of the split-phase transformer assuming negligible flux in the external branches. This is the model derived by directly mapping the magnetic circuit in Fig. 4(a) to an electrical circuit, using conventional transformation methods [21], applying symmetry, and combining elements.

core loss<sup>6</sup>.

The resulting electrical circuit model can be determined from the magnetic circuit model in a straightforward manner using the methods of [21], and applying circuit symmetry to combine terms; the result is shown in Fig. 4b. The rectifiers are connected to this electrical model under the constraint that  $v_p$  equals  $4N_pv_o$ . The resulting SPHTV electrical model with series connected primary windings is shown in Fig. 5. Note that each transformer in Fig. 4b is mapped to a transformer having two secondary windings in Fig. 5, and each transformer secondary winding is connected to a full-bridge rectifier. This satisfies the electrical model constraint and is identical to the model for a single-phase VIRT [8]. A lumped primary-referred leakage inductor is also included, associated with leakage flux in the transformer. Half-bridges A1, B1, C1, and D1 are operated with the same duty cycle and 180 degrees out of phase with A2, B2, C2, and D2. Because of this symmetric operation, the schematic of Fig. 5 can be simplified to that of Fig. 1 with a transformer turns ratio  $N_p: N_s = N_p: 1/4^7$ .

# III. DESIGN CONSIDERATIONS AND PROCEDURE

This section discusses the design considerations involved in building a high-performing, miniaturized LLC DCX prototype using a SPHTV. The iterative design procedure is outlined in Fig. 6 and is explained in the indicated sections. It is assumed that the designer has selected a target switching frequency,  $f_s$ , and core material such that a high magnetic material performance factor is achieved [2]. In the demonstrated design,  $f_s = 1$ MHz and Hitachi Metals ML91S core material is used.

<sup>&</sup>lt;sup>6</sup>In essence, setting  $g_2 = 0$  results in the core behaving like a UI core. Such a configuration would require a taller transformer height to carry the higher flux in the endplates and this is not preferred for miniaturization. The larger footprint of the combined E-core structure of Fig. 2b is well utilized since the connecting rectifiers can sit in the box volume of the transformer.

<sup>&</sup>lt;sup>7</sup>Since  $N_p$  in the model is taken to be the number of primary turns around each center-post, this means that a total of 8 primary turns are wound to achieve 16:1 step-down as expected from the half-turn operation of the VIRT.



**Fig. 5:** SPHTV circuit model. The primary winding comprises two sets of  $N_p$  turns wound in series around the center posts.  $L_M = N_p^2 / \mathscr{R}$  (ref. Fig. 4a) and the primary-referred leakage is represented by the lumped value  $L_{lk}$ . The relationships between the dc output current and the peak of the winding currents are shown in blue.



**Fig. 6:** Iterative design procedure for developing an LLC DCX with a SPHTV. Square brackets indicate the section in the paper that discusses the associated design step.

# A. Planar Transformer Implementation

There are many possible implementations for a planar transformer, with many variables that can, in principle, be controlled including: number of layers, distribution of windings on layers and degree of interleaving, copper thicknesses, spacing between layers, and overall board thickness. The approach followed in this work is to employ the simplest possible stack-up. In particular, in this design, a planar transformer with a non-interleaved Secondary-Primary-Primary (SPP) stack-up is used as illustrated in Fig. 2b. This design uses the default 4 layer specification of the PCB manufacturer: 1.6mm (63 mil) board thickness and manufacturer-standard layer spacings (0.22 mm, 1 mm, and 0.22 mm) between layers 1 and 2, 2 and 3, and 3 and 4, respectively). This selection has a number of advantages over a higher layer count, interleaved design:

- 1) It is a very simple implementation, and avoids the complexity and cost of a high PCB layer count.
- 2) Window fill factor is improved as the number of layer spacings is minimized. Note, for example, that in a PCB having 3oz copper layers (4.2 mil thick), layer spacings of 10 or 30 mils are 2.3 or 12.2 times larger than the conductor thickness, respectively [3].
- 3) No high-current vias are required through the length of the board, as may be the case if a more highly interleaved design is used (e.g. SPSPS). These vias, and the resulting requirements on termination design, can yield a dramatic increase in loss [4].
- 4) Inter-winding capacitance is minimized as there is only one primary-to-secondary facing layer and the distance between these layers can be made relatively large [3].
- 5) The relatively large leakage inductance in a noninterleaved design is useful for maintaining a reasonable resonant capacitance value in an LLC converter.

The key challenge of an SPP design is that a single layer of copper must carry the large secondary current. This challenge can only be quantitatively assessed after the transformer has been designed and its losses estimated. Thus, the approach followed in this work is to begin with this simple stack-up, complete the design, and then only add additional winding complexity if the estimated performance of the transformer is insufficient. The transformer design comparison in Appendix A suggests that an SPHTV with an SPP winding can achieve very high efficiency in a low volume, and thus a more complicated stack-up is not needed. Ultimately, as discussed in Section V, the experimental performance of the transformer is very high and this provides strong evidence that the approach of using the simplest stack-up, and reaping the associated benefits described above, can be a highly effective means of achieving transformer miniaturization<sup>8</sup>.

Another important point is that, because PCBs are constructed with an even number of layers, a four layer board must be used even though only three layers are required. To

<sup>&</sup>lt;sup>8</sup>Should a designer be interested in exploring more complicated transformer winding stack-ups, the following are recommended resources for understanding the trade-offs in terms of: via and termination loss [4], inter-winding capacitance [22], and leakage inductance [23]. Trade-offs for cost and window fill factor can be obtained from discussion with the PCB manufacturer.

take advantage of all four layers, an SPPS interleaved stackup could be used where each secondary winding is directly connected to its own set of rectifiers, a technique which has been employed in the literature for center-tapped rectifiers [6] and full-bridge rectifiers [24]. This arrangement can take full advantage of the conduction capability of the PCB, improves the ac resistance of the primary, and avoids problematic highcurrent ac terminations<sup>9</sup>. However, this SPPS arrangement doubles the number of switches that are required, increases the inter-winding capacitance, and requires an additional set of gaps to ensure equal current sharing between the secondary layers. For simplicity, and because a high-performing design is achievable, an SPP build is used in this work<sup>10</sup>.

Ultimately, as with other high-performance magnetics designs, the selection of the planar transformer implementation is iterative. The recommended design procedure is shown in Fig. 6. It is suggested to begin with the simplest possible stackup, complete the rest of the design, and then re-iterate with an SPPS design if efficiency or thermals are unacceptable. If that is insufficient, or if one wishes to preserve the benefits of an SPP design, the designer can instead try additional phases and/or increasing the degree of fractional turn and/or a more complicated winding stack-up.

1) Copper Thickness: Because the SPP stack-up is noninterleaved, the inner primary layer experiences higher magnetic fields than the two outer layers. Using Dowell's equation [23], it can be determined that if 3oz copper is used on the inner layer, its ac resistance factor is 3.5. If 2oz copper is used, its ac resistance factor is 1.6. Thus, a 3/2/2/3 oz stack-up is used as it results in lower ac resistance than using 3oz copper on all layers.

# B. Transformer Turns Selection and Initial Current Estimates

When operated at resonance, the voltage gain of the LLC DCX using a SPHTV is

$$\frac{V_o}{V_{in}} = \frac{1}{2} M_{g,LLC} \frac{1}{4N_p} \tag{1}$$

where  $M_{g,LLC}$  is the voltage gain of the resonant tank. The required gain is 3/95, corresponding to  $M_{g,LLC}/N_p = 15.83$ . Since there must be an integer number of primary turns,  $N_p =$ 4 is selected to yield an effective turns ratio of 16:1. A very small voltage gain of 1.01x is required from the LLC resonant tank in order to achieve the desired 12V output, and this can be achieved by operating the converter slightly below resonance. This is a minor requirement on LLC design, but has the effect of constraining the ratio between the magnetizing and resonant inductance values  $L_n = L_m/L_r$  [25].

The LLC must be designed to enable zero voltage switching of the inverter switches and achieve the requisite gain near 1MHz operation. Also, the leakage inductance of the transformer should be the value of  $L_r$ . To estimate this inductance, the transformer dimensions must be known, but these dimensions are themselves selected based on the current flows in the LLC. As a first step in this iterative design process, one can use the Fundamental Harmonic Approximation (FHA) to estimate the value of the currents in the windings [25]. For the secondary half-turns,

$$i_{s,rms} = \frac{1}{4} \frac{\pi}{2\sqrt{2}} I_o,$$
 (2)

which is the same as for the single-phase full-bridge LLC DCX but with the factor of 1/4 scaling associated with the SPHTV. For the primary turns,

$$i_{p,rms} = \frac{1}{4N_p} \frac{\pi}{2\sqrt{2}} I_o.$$
 (3)

This omits the magnetizing current, which cannot be estimated until an initial transformer design is selected. However, this value provides a useful starting point for design.

#### C. Inverter Switch Selection

At 1MHz and with a 380V blocking requirement, GaN devices have a superior  $R_{on} * C_{oss}$  figure of merit compared to their silicon counterparts, and the highest performing prototypes in the literature have employed these devices [6], [13]. There are two critical non-idealities that are important when operating a high voltage GaN FET at high frequency: dynamic on-resistance [26], which can greatly increase the switch's conduction loss, and  $C_{oss}$  loss [27] which occurs for large voltage slew-rates during soft-switching. Based on an assumed 5x multiplier in on-resistance over datasheet values, the 650V GS66516T switch, being the lowest on-resistance option available at the time of design, is selected. This device has an estimated charge-equivalent  $C_{oss}$  [28] of 305pF.

## D. Rectifier Switch Selection

The rectifiers operate as synchronous rectifiers (i.e. they are operated to mimic the switching of a diode). These switches need only block 12V, and at this voltage silicon switches are competitive. The converter must deliver 83.3A to the output at 1kW. In the full-bridge LLC DCX of Fig. 1, this corresponds to a switch rms current of approximately  $\pi I_o/4$ , or 65.4A. This large current necessitates the use of multiple paralleled devices, which aligns well with the inherent switch count increase and switch current-sharing of adding fractional-turns and/or additional phases. Because of the high switch count,  $Q_g V_g f_s$  gate drive losses, where  $Q_g$  is the required gate charge and  $V_q$  is the applied gate voltage, can be important. Thus, the key figure of merit for rectifier switch selection is  $R_{on} * Q_{a}$ .  $C_{oss}$  is of less concern owing to the high currents on the secondary [29]. Furthermore, it is important to note that the gate charge listed in a data sheet is usually provided under hard-switching. The gate charge required with ZVS is typically lower than this value as switch dynamics can cause the Miller charge region to be avoided [30]. In this work, the 25V IQE006NE2LM5 switch is selected owing to its competitive  $Q_g * R_{on}$  figure of merit and its very low on-resistance of approximately  $0.85 \text{m}\Omega$  at 5V,  $100^{\circ}\text{C}$ . This switch also has two

<sup>&</sup>lt;sup>9</sup>In this arrangement, the rectifiers are connected in parallel on their dc bus. The connecting vias carry dc current which can be easily designed for low loss while carrying high current.

<sup>&</sup>lt;sup>10</sup>Another potential advantage is that the unused layer in an SPP stack-up can be used to wind an auxiliary turn to provide hotel power to primary and/or secondary-side auxiliary electronics.



**Fig. 7:** Detailed SPHTV configuration. The secondaries are drawn as complete turns around the core as this is the geometry used for estimating copper loss.

available footprints which provides an additional advantage for termination design as discussed in Section IV.

### E. Transformer Optimization

The transformer is designed by selecting the core dimensions that result in the lowest overall loss in a specified volume, and this process is discussed in detail in [17]. In that study, the SPHTV is compared to a single-phase, splitphase, three-phase, and single-phase VIRT configuration, and the SPHTV is found to yield the lowest loss in a given volume for the 12V, 1kW application explored in this work. For completeness, this comparison is provided for the SPP configuration in this work in Appendix A. A summary of the SPHTV design procedure is provided in this section.

The dimensions b and w in Fig. 7, along with the length of the core, a, can be used to compute core volume, dc winding resistance, and overall box volume. The box volume includes the extent of the windings outside of the core. Namely,  $w_{tot} = 4w + 3b$ ,  $l = a + 2w_{winding} + 2s_{ct}$ ,  $h = h_w + b$ , and box volume  $= (w_{tot})(l)(h)$ . Note that  $w_{winding} = w - 2s_{ct}$ where  $s_{ct}$  is the core-to-trace spacing. The window height  $h_w$ is selected such that

$$h_w - h_{PCB} = w/4 \tag{4}$$

where  $h_{PCB}$  is the height of the PCB. This constraint ensures that the distance from the gap to the nearest conductor is w/4, which mitigates the loss impact of fringing fields from the gap [31]. Additionally, as discussed in Section IV, it is important for good terminations to constrain the search space such that

$$w \ge 2w_s,\tag{5}$$

where  $w_s$  is the width of a rectifier switch.

The dimensions a, b, w parameterize the core and can be used to determine core loss and copper loss as described below.

1) Core Loss: At resonance, the voltage on the core is a square wave, and core loss can be estimated via the improved General Steinmetz Equation (iGSE) [32]

$$P_{core} = k_{iGSE} \left(\frac{2V_o}{A_c}\right)^{\beta} \left(2f_s\right)^{(\alpha-\beta)} V_c \tag{6}$$

where  $V_o$  is the output voltage,  $A_c$  is the cross-sectional area of the center posts (a \* b) in m<sup>3</sup>,  $f_s$  is in Hz,  $V_c$  is the core volume in m<sup>3</sup>, and  $k_{iGSE} = 3.25 \times 10^{-6}$ ,  $\alpha = 2.15$ , and  $\beta = 3.0$  are the core Steinmetz parameters estimated from our own measured data.

2) Copper Loss: The mean path length (MPL) of the windings is MPL = 2(a + b + 2w). The resistance for each secondary winding is

$$R_{sec} = F_{R,sec} \cdot \rho \frac{MPL}{w_{winding} t_{cu,sec}} \tag{7}$$

where  $\rho$  is the resistivity of copper at 100°C,  $2.28 \times 10^{-8}$  $\Omega \cdot m$ ,  $t_{cu,sec}$  is the copper thickness of the secondary layer (3oz, 0.107mm), and  $F_{R,sec}$  is the ac resistance factor for the secondary layer as computed from Dowell's equation [23]. Note that the secondary resistance is computed as if it was wound as a full turn, reflecting the fact that the transformer current must flow in a closed loop. The net primary winding resistance is

$$R_{prim} = \rho \cdot \frac{8MPL}{w_{winding} - s_{tt}} \left( \frac{F_{R,prim,inner}}{t_{cu,prim,inner}} + \frac{F_{R,prim,outer}}{t_{cu,prim,outer}} \right)$$
(8)

where  $s_{tt}$  is the trace-to-trace spacing requirement of the PCB manufacturer (assumed to be 10 mils).  $t_{cu,prim,inner}$  and  $t_{cu,prim,outer}$  are the copper thickness of the inner and outer primary layers, 2oz (0.0711mm) and 3oz (0.107mm), respectively. Similarly,  $F_{R,prim,inner}$  and  $F_{R,prim,outer}$  are the ac resistance factors for the inner and outer primary layers, respectively, as computed via Dowell's equation.

As mentioned in Section III-A, a 3/2/3 oz copper distribution is used owing to the relatively high ac resistance factor of the inner primary layer if a 3/3/3oz distribution is used. The resistance factors are  $F_{R,sec} = 1.3$ ,  $F_{R,prim,inner} = 1.6$ ,  $F_{R,prim,outer} = 1.3$ .

3) Optimal Geometry: The winding resistances and core loss are parameterized by the dimensions a, b, and w. An optimal geometry is determined by specifying a desired box volume and searching through dimensions a and w until the values that minimize the sum of copper loss and core loss are determined. This can be done using the *fmincon* function in MATLAB, for example.

# F. LLC DCX Design

The leakage inductance of the transformer can be estimated from the selected minimum-loss geometry. Owing to the simple planar stack-up,  $L_{lk}$  (ref. Fig 5) can be estimated via the approach in [23] (assuming the leakage field is primarily stored in the space between the PCB layers),

$$L_{lk} \approx \frac{2\mu_o N_p^2}{(w)(MPL)} \left(s_{SP} + \frac{s_{PP}}{4}\right) \tag{9}$$



Fig. 8: ANSYS Icepak thermal simulation of the transformer.

where  $s_{SP}$  is the spacing between the secondary and primary layer and  $s_{PP}$  is the spacing between the two primary layers.

With this leakage estimate, the design of the LLC DCX can be completed in a conventional manner by setting this value equal to the resonant inductance. An overview of LLC design can be found in [25]. The design should be simulated (LTSPICE was used in this design) including the chargeequivalent  $C_{oss}$  of the inverter and rectifier switches, and ZVS operation of these devices should be confirmed. The output capacitance  $C_o$  should also be set to ensure acceptable ripple (e.g.  $100\mu$ F to achieve 1% peak-to-peak ripple in this design). Once  $C_r$  and  $L_m$  have been selected to achieve the required gain near 1MHz and ZVS operation, the value of the secondary and primary currents can be compared to the original estimates in (2) and (3). If there is a discrepancy, the minimum-loss geometry should be recomputed and the design should be iterated until there is good agreement between the designed and simulated currents. The design can also be iterated for different switch combinations, if desired. If transformer loss is unacceptable, a new transformer implementation or stack-up should be used, or the allowed volume should be increased.

# G. Thermal Analysis

The design procedure requires the selection of a desired volume, and is iterated based on a certain loss being achieved. While the loss may initially be selected based on a desired efficiency, it is ultimately thermal considerations that will determine if this efficiency is acceptable in the desired volume. This is best assessed experimentally, but Finite Element Analysis (FEA) simulations can be a useful guard against a thermally inviable prototype. Fig. 8 shows the result of a 3D FEA ANSYS Icepak thermal simulation of the transformer and rectifiers using their estimated losses. The windings are implemented as unconnected loops of copper each having an equal part of the primary or secondary winding losses, core loss is distributed according to the volume of the posts and endplates, switches are modeled by their datasheet thermal resistances and are placed in their approximate location near the core window, and the FR4 dielectric material of the PCB is included between winding layers. An air flow of 4m/s is used and the simulation shows an acceptable peak temperature of 92.4°C for an ambient temperature of 20°C.

# H. Summary of Design

An experimental prototype is developed based on the design procedure described above, with a targeted box volume of 12.5cm<sup>3</sup>. A summary of this prototype is provided in Table I. There are a few deviations from the procedure related to practical implementation details:

1) Window height: The window height,  $h_w$ , is larger than the requirement in (4) of 3.56mm. Due to its relatively long lead time, the core was commissioned before the PCB was manufactured. A margin on the window height was included to allow for flexibility in the PCB height delivered by the manufacturer.

2) Transformer box volume: The box volume is larger than the target box volume of  $12.5 \text{ cm}^3$ . This is partly attributable to the fact than the PCB must have cut-outs which are larger than the core. Here, the cutout dimensions are  $a_{co}=16.64\text{mm}$ ,  $b_{co}=5.7\text{mm}$ , and  $w_{co}=7\text{mm}$ . Furthermore, the overall length of the transformer is longer than the expected  $2w_{co} + a_{co}$  because of the additional primary winding section that must be used to connect the two sets of four primary turns in series, as discussed in Section IV-C. This adds an additional 2.86mm of length in the prototype.

3) Output capacitance: The output capacitance is larger than the  $100\mu$ F that is required to achieve 1% peak-to-peak ripple. This was increased simply to take advantage of the available space for these capacitors, as discussed in Section IV.

4) Gap lengths:  $g_2$  is approximately  $2.5g_1$ , rather than  $2g_1$ . In practice the reluctance of each path includes contributions from the finite permeability core, and the core paths associated with  $g_1$  are longer than those associated with  $g_2$ . The larger length of  $g_2$  counteracts the impact of this reluctance increase.

#### **IV. LAYOUT CONSIDERATIONS**

There are two critical considerations in the secondaryside layout. First, the connecting electronics should be symmetrically distributed about the center of the core. This is straightforward to enforce in a planar transformer, as all component positions are well-defined on the PCB. Second, the connecting components should be laid out to mitigate potential termination loss mechanisms. Terminations can be a dominant source of loss in a high-current, high-frequency planar magnetic component [4]. These losses are greatly mitigated in this design by avoiding an interleaved stack-up, removing the requirement for long, high-current vias and minimizing the excursion of the windings away from the core. However, good termination design practices are useful for informing the layout of the high-current secondary-side. The general principle is to arrange the secondary-side components such that they allow ac current to flow in a manner similar to how it would flow if the secondary was a closed conductive loop around the core, as illustrated in Fig. 9.

#### A. Rectifier Switch Placement

The design constraint on terminations in (5) allows for direct connection of the drain and source pads of the FETs that terminate each half-turn, as illustrated in Fig. 9. This

TABLE I:	Summary	of	Experimental	Prototype
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Component	Value
Planar Transformer	
Stack-up	Four layers; $L1/L2/L3/L4 = 3/2/2/3$ oz.
Winding arrangement	S/_/P/P (second layer unused)
$N_p$	Four turns; two turns each on L3 and L4, connected in series
Secondary winding	Four half-turns on L1
Layer spacing (approx.	L1-L2: 0.22mm; L2-L3: 1mm;
from manufacturer)	L3-L4: 0.22mm
Board height $(h_{PCB})$	1.68 mm
Core material	Hitachi Metals ML91S
Core-to-trace spacing	0.508mm
Trace-to-trace spacing	0.254mm
Core dimensions	<i>a</i> =16.13mm; <i>b</i> =5.16mm;
	$w$ =7.53mm; $h_w$ =4mm
Core height	9.23 mm
Transformer box	$14.2 \text{ cm}^3$
volume	
Inverter	
Inverter switches	GS66516T
Gate drivers	SI8271
Isolated power	ADUM5010
Rectifier	
Rectifier switches	IQE006NE2LM5 and
	IQE006NE2LM5CG
Gate drivers	LM5113QDPRRQ1
Output capacitors	$C_o \approx 144 \mu \mathrm{F}; 40 \mathrm{x}$
	C2012X7S1E106K125AC; 5
	pcs. per half-bridge. $10\mu$ F
	nominal, de-rated to $\approx 3.0 \mu F$
	ea. at 12 vdc, 100 C [55]
Reconcert connector	47.22pE: 1x
Resonant capacitor	47.22 Hr, 1X $47$ n E/630 V/1812/COG $\pm$
	0.22nF/2kV/C0G
Resonant inductor	520 nH: derived from
	transformer leakage
Magnetizing inductor	15.3 $\mu$ H: $q_1 = 0.127$ mm.
	$g_2=0.318$ mm
Other	
Controller	TMS320F28379D
Cooling	Nidec FAN-0100L4, 40mm
	Axial Fan, 40x40x28mm,
	8500RPM



**Fig. 9:** Illustration of secondary termination design on Layer 1. Layer 3 is also shown to indicate the orientation and direction of current flow of the primary winding in the same region of the PCB. (1) The source and drain pads of the connecting rectifiers directly interface with the half-turn, minimizing excursion loss. (2) The output capacitors are arranged to allow ac current to flow in a direction that is anti-parallel to current in the primary. (3) An additional conductor is required to connect the two primary turn sets in series, slightly increasing the overall length and box volume of the transformer.

minimizes excursion loss. The design takes advantage of the dual offering of the IQE006NE2LM5 switch, which has a conventional PQFN3.3x3.3 footprint and a "center gate" (IQE006NE2LM5CG) variant. Using both of these footprints allows the half-turn to terminate directly into the FET without interference from the routing of the gate drive signal.

# B. Output Capacitor Placement

The minimum output capacitance to achieve the desired ripple is  $100\mu$ F, which can be implemented as  $12.5\mu$ F local to each half-bridge as indicated in Fig. 4. The C2012X7S1E106K125AC capacitor is selected as it has a very high  $3.7\mu$ F capacitance at 12V,  $100^{\circ}$ C in a relatively small 0805 package [33]. For good alignment with the direction of current flow on the primary windings, the capacitors are laid out as illustrated in Fig. 9. There is room to place 5 of these capacitors, utilizing the full extent of the overlap with the primary.

The switching loop of each half-bridge is completed by connecting the source of the low-side switch and the output capacitor bank using a ground plane on layer 2, as indicated in Fig. 9. Because the space between layers 1 and 2 is relatively short, the vias that connect them have low resistance and therefore low loss. Blind vias are placed to match the extent of the primary windings in order to take advantage of the full conduction capability of the secondary.

# C. Primary Connection

The formulation for minimum-loss transformer geometry in [17] does not account for the detail of how the sets of primary turns are connected. In practice, an additional length of conductor is required to connect these turns in series, as illustrated in Fig. 9. This slightly increases the overall box volume of the transformer as discussed in Section III-H.

# D. dc Output Connections

The VIRT architecture distributes the connecting rectifiers around the magnetic core. The ac current loops are confined by the secondary-side layout described above, but the dc bus must be distributed. This is the case with any technique that parallels many rectifiers, including the MT [6] and the QTT [13]. In many designs, the converter is simply treated as having multiple output ports which are connected in parallel externally. In this design, for ease of testing, the dc bus is distributed on the PCB to connect to a single dc output terminal block as discussed in Section V.

#### V. EXPERIMENTAL RESULTS

In this section, experimental results are presented, and the SPHTV is compared to best-in-class transformer alternatives for this application in the literature. The core pieces are shown in Fig. 10a, and are mounted to the board using the acrylic fixture shown in Fig. 10b, as discussed in Section V-D. The core is mounted with the endplate on top of the secondary windings and the gap facing the primary windings. The top and bottom of the PCB are shown in Figs. 10c and 10d, respectively. Details of the PCB winding structure and arrangement are provided in Figs. 11a and 11b for the primary and secondary, respectively.

### A. Leakage and Magnetizing Inductance Measurement

The leakage and magnetizing inductance of the SPHTV can be measured in a conventional manner. In this design of an LLC DCX at resonance, the lumped model of Fig. 5 and the knowledge that  $L_{lk} \ll L_M$  allow these parameters to be reasonably estimated with only two measurements: (1) opencircuit the secondary and measure primary-referred inductance  $(\approx L_M + L_{lk})$ , and (2) short-circuit the secondary and measure primary-referred inductance  $(\approx L_{lk})$ . These tests are done in a similar manner as for a conventional two winding transformer. For example, the short-circuit secondary test is performed by connecting the half-turns on each side using a length of copper wire.

#### B. Efficiency and Loss Breakdown

The measured efficiency of the converter is shown in Fig. 12. The curve including hotel power accounts for the power loss associated with the gate drivers and isolated power supplies, measured to be 2.7W. The curve including hoteland fan power also adds the 1.44W power draw of the fan used for cooling. Cooling is usually determined at the system level and is typically not included in efficiency reporting. It is included here to highlight that a relatively small fan can sufficiently cool the prototype in its miniaturized form factor without a significant loss penalty.

A thermal image of the secondary at full-load is provided in Fig. 13, showing a maximum steady-state temperature of approximately 95°C. The temperature gradients match well with the thermal simulation results in Fig. 8. The hot-spot is on the A2 and C2 rectifiers due to these switches having their convective cooling disturbed by the presence of the transformer core and due to them being centrally located. Furthermore, as discussed in Section V-D, an acrylic mount is used for the core, part of which can be seen in the thermal image. This mount may also be disrupting cooling of the A2/C2 rectifiers. Finally, it is noted that the low emissivity of the copper pads between A1/B2 and C1/D2 causes two false cool spots to be measured; the thermal gradient in these regions is smooth, as on the other side of the transformer.

At full load, the power stage loss is 29.9W, and the estimated distribution of these losses is shown in Fig. 14. The transformer is copper loss dominated, and an SPPS build would improve this, approximately halving secondary loss and reducing primary loss by one-third, without strongly affecting volume since the window height is oversized as discussed in Section III-H. Nevertheless, the SPP build achieves high performance and allows for a simpler prototype as addressed in Section II-B. There is approximately 4W of loss marked "other" which is not accounted for by the modeling, likely attributable to a combination of: some degree of secondary loss increase related to terminations, uncertainty in the onresistance of the inverter GaNFETs, and body diode conduction in the rectifiers due to mismatch in their ZVS transitions as discussed below. However, the design procedure is confirmed to yield a high performing prototype and its loss is wellmatched to expectation.

# C. Operating Waveforms

Fig. 15 shows example operating waveforms at full load. The switching frequency is 967kHz and inverter ZVS is achieved. Four drain-source voltages are shown corresponding to A2 low, B1 high, C2 low, and D1 high. These are operated with the same fixed commanded on-time, but experience slightly different ZVS transitions, suggesting differences in the local decoupling paths between the switches and the output capacitors. These different uncontrolled transition times cause slight body diode conduction, but high performance is still obtained. The output voltage ripple is approximately 100mV peak-to-peak, less than the 1% design objective.

## D. Additional Implementation Details

The experimental prototype was designed to demonstrate the miniaturization potential of a SPHTV in a high output current 380/12V 1kW application. The transformer itself is well miniaturized. However, conveniences in this first prototype were included to assist with testing and evaluation, preventing the demonstration of a miniaturized overall package. These include:

1) Multiple secondary gate drivers: Each half-bridge was given its own gate driver for maximum flexibility in evaluating the SPHTV prototype. This flexibility was not needed as each half-bridge is operated with the same gating. Thus, secondary gate driver count can be greatly reduced in a future miniaturized prototype.



**Fig. 10:** Experimental prototype of the LLC DCX with a SPHTV. (a) Individual core pieces. (b) Core pieces arranged with acrylic mount. (c) PCB top. (d) PCB bottom. The red outline marks the footprint of the transformer used in assessing its box volume.



**Fig. 11:** Winding arrangements in the experimental prototype. The cutout-to-trace spacing is 20 mils, and the trace-to-trace spacing is 10 mils. (a) Primary. (b) Secondary.



**Fig. 12:** Measured prototype efficiency. Maximum powerstage efficiency is 97.7% and full-load efficiency is 97.1%. The hotel- and fan power are 2.7W and 1.44W, respectively.

2) A single dc output terminal: As discussed in Section IV-D, a single dc output terminal block is used instead of the distributed dc output that is used in many other designs featuring distributed rectifiers (e.g. [6], [13]). This requires the dc output bus to be wrapped around the transformer and gate drivers as shown in Fig. 10c. If the output bus is externally connected, these wrapping connections are not necessary. Similarly, room was included for dc bus bars in case they were needed for carrying dc current or assisting with cooling. These were also not used, but their fixed lengths required additional



**Fig. 13:** Thermal image of secondary-side under full-load (obtained after 15 minutes of continuous operation, 22°C room temperature). The fan is located to the right of the PCB.



**Fig. 14:** Estimated loss breakdown at full load, not including hotel power (2.7W) and fan power (1.44W).

length to be included on the PCB between the transformer and the dc output terminal. All of these elements can be removed if the dc bus is paralleled externally.

*3) Isolated supplies on the primary-side:* Two isolated supplies are used on the primary-side for experimental convenience. These account for approximately 0.45W of the hotel power.

4) Space for inverter heat sink: The primary layout in Fig. 10d is widely spaced to allow for the installation of a heat sink which was not required. Thus, the footprint of the primary layout can be dramatically reduced, as in other high performing designs featuring GaN inverter switches [6], [13].

5) Use of an acrylic core mount: In practice, the desired gap lengths would be made permanent during the process of mounting the core to the board. It was not desired to do this for the laboratory prototype. However, to ensure consistency in the gap lengths as the core is installed and removed during testing, the core was mounted using an acrylic fixture as shown in Fig. 10b.



**Fig. 15:** Experimental operating waveforms at full load. The drain-to-source voltage of rectifiers D1 High, C2 Low, A2 Low, and B1 High are shown. A2L and C2L are identical while B1H and D1H experience slightly different dead-time turn-off transitions.

# E. Transformer Performance Comparison

In Table II, the SPHTV is compared to two best-in-class transformers built for the same 380V-12V, 1kW LLC DCX specification. One uses a four-element MT [6], and the other uses a QTT [13]. The volume comparison is restricted to the box volume of the transformer including rectifier connections (outlined in Fig. 10c), which are the dominant contributors to volume. The proposed SPHTV achieves both higher efficiency and lower volume than these best-in-class solutions, clearly demonstrating its miniaturization benefit.

For additional context, Table III provides a comprehensive comparison to other planar transformer designs for 380-12V conversion at different power levels. The volume comparison is again restricted to the box volume of the transformer including

	This work	MT [6]	QTT [13]
Rectifier	Full-bridge	Center	-tapped
structure			
Num. rect.	16	16	8
switches			
<b>Rectifier devices</b>	IQE006NE2LM5	BSZ019N03LS	BSC010N04LS
<b>Inverter devices</b>	GS66516Tx2	GS66508Px2	GS66516Tx2
Stack-up	S/_/P/P	S/P/P/S	S/G/P/P/G/S <sup>a</sup>
Peak power	97.7%	-	97.0%
stage efficiency			
Peak efficiency	97.3%	97.1%	-
including hotel			
power			
Full load loss	29.9	34.4	41
(power stage			
only) [W]			
Transformer loss	10.8	16.3	13.2
at full load [W]			
Transformer	1536	2200	2500
footprint [mm <sup>2</sup> ]			
Transformer	65.1	45.5	40
areal density			
[W/cm <sup>2</sup> ]			
Height [mm]	9.23	7.3	8.9
Transformer box	14.2	16.1	22.3
volume [cm <sup>3</sup> ]			
Transformer	70.4	62.1	44.8
power density			
[W/cm <sup>3</sup> ]			

**TABLE II:** Comparison between this work and best-in-class380-12V, 1kW converters in the literature.

<sup>a</sup> 'G' is a secondary layer tied directly to secondary ground

rectifier connections. It is important to note that at different power levels (i.e. different output current levels), the best transformer technique to use will change based on the design trade-offs. In particular, lower power levels will have lower copper loss for the same core loss. However, this comparison provides context on the kinds of techniques, efficiencies, and power densities that have been reported at these different power levels. The efficiency and density of the present work also compares well to these designs.

Of note is that the height of the transformer in this work is significantly larger than many of the other designs. In particular, a similar areal power density is achieved compared to the two designs having higher power density, the 800W matrix transformer in [34] and the 1800W cellular transformer in [5], but volumetric power density is lower due to the larger height. This height is currently oversized as described in Section V-D, and can likely be further reduced by exploring widening the end plates as is done in [6] and [15]. As compared to the design based on the physical 'fractional turn' concept proposed in [15], the SPHTV design proposed here has a much higher full-load efficiency and a much lower fullload loss percentage of the transformer, perhaps due to the improved current carrying ability of the SPHTV and a full accounting of the closed path of current.

## VI. CONCLUSION

This work demonstrates the miniaturization benefit of a SPHTV in a 380-12V, 1kW data center server power supply application. The SPHTV combines the "linear" trade-off of core- and copper loss associated with adding multiple phases to a transformer, as in the matrix transformer technique, with the "exponential" trade-off associated with employing fractional turns using the VIRT technique. An intuitive description of these techniques is provided to make clear the capabilities and distinctions of exploring this and higher-order fractional-turn concepts and/or merging them with multi-phase transformer constructions. An SPHTV model is developed from first principles modeling of the physical structure and is shown to be schematically equivalent to a transformer having a turns ratio of  $N_p$  : 1/4 connected to a full-bridge rectifier, where  $N_p$  is the number of turns wound around each center-post. A detailed design procedure is presented, which comprehensively defines the design decisions made in this work and provides guidance to designers interested in building these kinds of planar transformers. The procedure includes: an assessment of the factors involved in down-selecting into a particular planar structure, full details on transformer loss optimization, and critical considerations of the physical layout. An experimental prototype is developed having a 97.7% peak efficiency and 97.1% full-load efficiency, and its performance matches well with both the estimated loss components and a thermal simulation of the system. The transformer has a volume that is 12%-36% lower than the best-in-class alternatives in the literature at the same voltage conversion and power levels, while also having higher efficiency, and has competitive performance when comparing more generally to converters in this space at different power levels. Thus, this paper both describes in detail how the SPHTV technique can be employed for transformer miniaturization and demonstrates that it is an effective means to achieve miniaturization in low output voltage, high output current designs.

# APPENDIX A

DETAILS OF TRANSFORMER COMPARISON

In this appendix, four planar SPP transformer configurations are compared for the 380-12V, 1kW application considered in this work. The comparison is done using the procedure described in [17]. The configurations that are compared are: single-phase (1P, 16 primary turns), split-phase (SP, 16 primary turns), single-phase half-turn VIRT (1PHTV, 8 primary turns), and split-phase half-turn VIRT (SPHTV, 8 primary turns). Three-phase configurations are investigated in [17] and are determined to be noncompetitive.

The primary turns are distributed evenly on the two primary layers. The 1P single-turn secondary is implemented using a complete turn on the secondary layer. The 1P transformer configuration is shown in Fig. 16, and it is identical in structure to the 1PHTV configuration. The SPHTV configuration is shown in Fig. 7 and it is identical in structure to the SP configuration. Note that the VIRT secondaries are assumed to comprise a single complete loop, reflecting the fact that current in the secondary must flow in a closed loop.

	This Work	'Fractional' Secondary [15]	Matrix [34]	Half-turn [11]	Half-turn [12]	Cellular [5]
Power [W]	1000	80	0	750	600	1800
Rectifier structure	Full-bridge		Center-	tapped		Center-tapped, cellular
Num. rect. switches	16	8	8	8	8	16
Rectifier devices	IQE006NE2LM5	BSC0500NSI	BSC0500NSI	BSC011N03LSI	BSC011N03LSI	BSZ0501NSI
Inverter devices	GS66516Tx2	GSS66508Tx2	PGA26E08x2	C3M0120090Jx2	GS66516Tx2	BSZ040N06LS5x16
Winding stack-up	S/_/P/P	_ a	S/Sh/P/P/Sh/S <sup>b</sup>	S/P/P/S	S/S/P/P	S/P/S/S/P/S
Peak eff. [%]	97.7	96.5	97.7	97.0	98.0	98.3
Full load efficiency [%]	97.1	94.4	97.4	96.1	97.2	97.0
Transformer full-load loss percentage	1.08%	1.63%	_ a	_a	_a	1.60%
Estimated transformer areal density [W/cm <sup>2</sup> ]	65.1	51.3	63.1	45.0	34.3	60.8
Height [mm]	9.23	7.0	6.9	10	7.6	7.5
Estimated transformer power density [W/cm <sup>3</sup> ]	70.4	73.3	92.0	45.0	45.1	81.1

TABLE III: Comparison between this work and other 380-12V converters rated for different power levels.

<sup>a</sup> Not reported.

<sup>b</sup> 'Sh' is a shield layer.



**Fig. 16:** Transformer configuration of the 1P. The 1PHTV has an identical structure.

Consider the single-phase transformer in Fig. 16. The copper and core loss of this transformer inherently trade off against each other as the dimensional parameters are changed. For example, to reduce core loss, a larger cross-sectional area can be used by increasing the dimension *a*. However, this results in a longer winding length, increasing copper loss. In general, a core can be optimized for a given application by designing its dimensional parameters such that the sum of core and copper loss is minimized.

Another means of trading-off core loss and copper loss is to add extra phases or employ fractional turns. For the same core dimensions being used, the trade-off between core loss and copper loss is linear if phases are added, and exponential if the degree of fractional turn is increased, as summarized in Fig. 3. This intuitive understanding of the change in these loss components helps a designer to decide which of these transformer configurations to consider in a given application. However, once a new configuration is selected, the dimensions of the core should be re-designed to find the new minimum loss geometry.

The comparison methodology used in this work is to select a box volume and determine which of these transformer configurations yields the lowest loss in that volume. A box volume limit (the product of  $w_{tot}$ , l, and h in Fig. 16) of 12.5 cubic cm is selected, representing a significant miniaturization over recently reported transformer volumes for 1kW data



Fig. 17: Results of transformer comparison in Appendix A.  $V_{tot} = 12.5 \text{ cm}^2$ .

center power supplies (e.g. [6], [35]).

The core loss for each transformer configuration can be computed as

$$P_{core} = k_{iGSE} \left(\frac{xV_o}{A_c}\right)^{\beta} \left(2f_s\right)^{(\alpha-\beta)} V_c.$$
(10)

This uses the same variable definitions as in Eqn. (6) but with the additional variable x. This variable accounts for the increased voltages that are inserted by the VIRT configurations. In the 1P and 2P configurations, x = 1. For the 1PHTV and SPHTV, x = 2.

The copper loss for each configuration can also be computed in a manner identical to the description in Section III-E. The same LLC parameters are assumed in each design. The current in the secondary winding is obtained from simulation of the 1P LLC DCX in Fig. 1 and scaled according to the transformer configuration: halved for the 1PHTV and SP, and quartered for the SPHTV. The current in the primary is the same in each configuration since it is assumed that the phases are series-connected in the SP and SPHTV configurations. The core loss and copper loss are thus parameterized by the core dimensions, and the dimensions that result in the lowest loss for a given volume are determined using the *fmincon* function in MATLAB.

The results of this comparison are shown in Fig. 17, and the computed minimum loss dimensions are provided in Table IV. The SPHTV is estimated to have the lowest loss and for this reason it is explored in this work. Note that the transformer dimensions used in the experimental study are slightly different from the values in Table IV as discussed in Section III-H. Namely, after specifying a fixed height of 4mm for the window, the updated minimum loss geometry is a=16.13mm, b=5.16mm, w=7.53mm. This also increases the estimated loss. Cutouts are accommodated by adding 0.5mm to the a and b dimensions, and subtracting 0.5mm from the w dimension. Ultimately, a very high performing prototype is obtained. It is expected, however, that improved performance is achievable if the transformer is built according to the dimensions in Table IV.

**TABLE IV:** Minimum loss geometries for the comparison in Appendix A. Dimensions in mm.

	a	b	W	$h_w$
1P	5.31	6.28	12.70	4.80
SP	4.53	7.36	8.38	3.72
1PHTV	12.62	5.37	12.08	4.64
SPHTV	14.4	5.29	7.99	3.62

90.0



**Fig. 18:** Simulated B-field magnitude showing balanced flux distribution.

# APPENDIX B FINITE ELEMENT ANALYSIS SIMULATION RESULTS

For completeness, 3D ANSYS Maxwell simulation results of the designed transformer are provided in this appendix. Fig. 18 shows the magnitude of the flux density along the center of the core for a 192V, 1MHz sinusoidal voltage excitation on the primary. The flux is well distributed among the four legs. Fig. 19 shows the current density under a short-circuit excitation test. The magnitude of the current density in the outer primary layer, inner primary layer, and secondary layer is shown in Figs. 19a, 19b and 19c, respectively. There is some current crowding owing to the use of rectangular windings, and the distribution of current in the two secondary loops is similar, as expected.

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**Fig. 19:** Simulated current density (showing magnitude). (a) Primary outer layer. (b) Primary inner layer. (c) Secondary.

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