A.J. Hanson and D.J. Perreault, "A High-Frequency Power Factor Correction Stage with Low Output Voltage," IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, No. 3, pp. 2143-2155, March 2020.

A High-Frequency Power Factor Correction Stage with Low Output Voltage

Alex J. Hanson, David J. Perreault
Massachusetts Institute of Technology
77 Massachusetts Avenue, Cambridge, MA 02139, USA
Email: ajhanson@mit.edu, djperrea@mit.edu

***Abstract*—Single-phase power factor correction (PFC) stages would ideally have three features – operation over the entire line cycle, soft switching at high frequency for all powers and voltages, and a reasonably low output voltage. These features permit high power factor, high combination of density and efficiency, and reduced stress on subsequent stages. Most PFC stages, including the most commonly used, achieve only a subset of these features. Here we present control innovations to allow a PFC stage to operate from universal input (90–265 $\mathrm{V_{ac}}$) over the entire line cycle with zero-voltage switching (ZVS) with a reduced output voltage. These features are verified with a prototype with very high power factor (>0.99), high efficiency (98 %), and high density (80 $\mathrm{W/in^3}$). The PFC can provide an output of 200 $\mathrm{V_{dc}}$ from the entire universal input voltage range which greatly reduces the conversion stress required from subsequent stages. The proposed PFC control consists of a blended feedforward/feedback method that provides additional advantages like guaranteed soft switching, the ability to correct for input capacitance, and the ability to interface with a high-ripple output bus. Therefore, the proposed PFC provides advantages in efficiency and density both for the PFC stage and the overall system.**

I. Introduction

Electrical loads process real power by drawing current at the same frequency as (and in phase with) the source voltage. Other frequency components of the input current result in reactive power and deliver no net energy to the load; these currents are nevertheless physically real and may dissipate energy in any source impedance (e.g. resistance in mains distribution lines and transformers). Currents at harmonic frequencies of the grid voltage are therefore regulated according to international standards (e.g. IEC/EN 61000-3-2) and power conversion stages which draw compliant currents by design are called Power Factor Correction (PFC) converters [2]–[4]. Power factor correction stages often make up a significant fraction of the overall power converter volume and, in multi-stage architectures, often impose onerous requirements on subsequent stages. Improvements in PFC stages can therefore have multi-faceted impacts.

Financial support was provided by Fairchild Semiconductor. This work was also supported in part by the National Science Foundation under Grant 1609240 and by the Cooperative Agreement between the Masdar Institute of Science and Technology (Masdar Institute), Abu Dhabi, UAE and the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA - Reference 02/MI/MIT/CP/11/07633/GEN/G/00.

This work is an extension of the conference paper: A. J. Hanson and D. J. Perreault, "A high frequency power factor correction converter with soft switching," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2027-2034. [1]. The journal version extends [1] with low-output-voltage operation and an improved prototype.

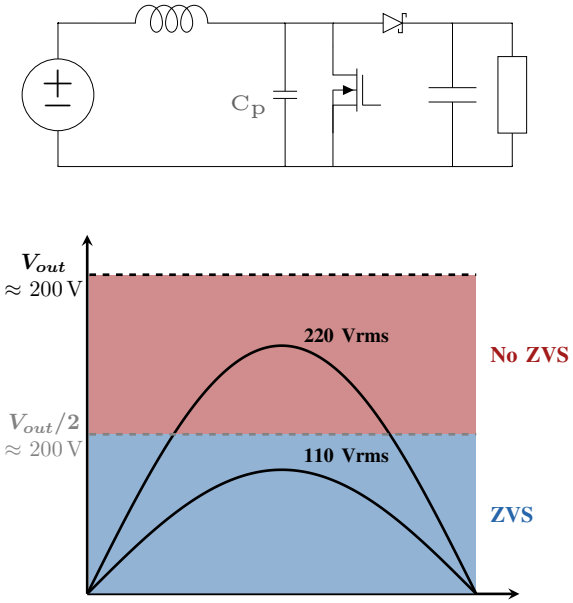

Fig. 1. The typical boost PFC fails to achieve ZVS for large portions of the line cycle with high rms input voltages, limiting its operating frequency, efficiency, and power density.

To illustrate the challenge, consider the boost converter PFC as part of a two-stage architecture – arguably the most common combination in use. The boost PFC operates from universal input 85–265 Vrms and outputs a dc bus around 400 V. Operated near boundary conduction mode, the boost converter may allow a resonant transition to reduce its switch node voltage prior to turn-on. This process results in true ZVS for $V_{in} < V_{out}/2$ and "valley-switching" otherwise with $v_{min} = 2V_{in} - V_{out}$. For much of a ~220 Vrms line cycle, the switch still turns on with hundreds of volts across it and the corresponding switching loss makes high frequency operation untenable. This choice of topology and control is thus limited to low-frequency operation with bulky magnetics and EMI filter components. Its necessarily high output voltage also increases the conversion stress on subsequent stages which, for computing and many other applications, must ultimately present much lower voltages to the load.

From this example, we suggest three desirable design features in a PFC stage:

1) operation over the entire line cycle for high power factor
2) high-frequency operation with soft switching for high

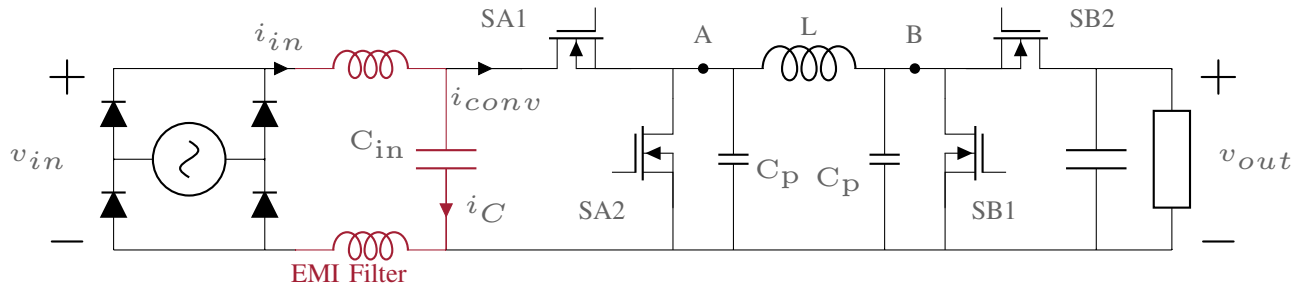

Fig. 2. The proposed PFC control applies to the four-switch buck-boost topology with four (or two) active switches and achieves ZVS across the line cycle, high-frequency operation, synchronous rectification, and a reduced output voltage which greatly alleviates the conversion burden of subsequent stages.

efficiency and density

3) lower output voltage to reduce the conversion burden on subsequent stages

Using this framework, we may categorize a variety of potential PFC solutions. Boost-type PFCs can operate near zero-crossings but generate a high output voltage. Buck-type PFCs make the opposite tradeoff. In both of these cases, the common implementations of each type cannot achieve soft switching without major performance concessions, and still do not achieve all of the goals stated above.

It is clear that only a buck-boost type PFC can operate over the whole line cycle with a low output voltage. The primary challenge with this type of PFC is maintaining soft switching over the entire line cycle as the typical modes of operation all lose soft switching for some voltage ratios. Here we present a control approach for the topology in Fig. 2 which achieves ZVS over the entire voltage range while maintaining low rms current and a low output voltage (e.g. near $200\,\mathrm{V}$ instead of near $400\,\mathrm{V}$, even for the higher $\sim 220\,\mathrm{V_{rms}}$ line). In addition, we present control techniques to achieve power factor correction, power regulation, and precise high-frequency timing. The proposed control has additional benefits, like the ability to account for input capacitance that can cause zero-crossing distortion and reduced power factor and the ability to interface with large buffer voltage swings.

II. Existing Technology

The boost PFC is likely the most common solution in use due to its ability to operate over the entire line cycle, including very low input voltages. In addition, now-popular bridgeless solutions are almost always boost-type due to the rectifying orientation of switches. Controlling the boost converter can also be very straightforward: operation in boundary conduction mode with constant on-time across the line cycle automatically achieves power factor correction. At sufficiently low switching frequency, boost converters of this type may also take advantage of valley switching without substantialy impacting power factor. However, as discussed, such a mode only obtains ZVS for $V_{in} < V_{out}/2$ which prohibits high-frequency operation.

Advanced control and/or additional hardware are sometimes used to achieve soft switching with increased complexity. Some approaches add additional lossy circuitry or only partly achieve soft switching [5], [6]. Other approaches achieve ZVS using complex switching networks [7], [8], or stacked architectures [9], [10].

One technique that merits further discussion is continuous conduction mode with ripple ratio larger than unity, sometimes called triangular conduction mode (TCM) [11]–[13]. This control, made possible by the use of all active switches, permits the inductor current to become negative before switching off the rectifying devices. This negative inductor current can aid in achieving ZVS even when $V_{in} > V_{out}/2$. If frequency is not adapted, then the ripple is the same at light load as at heavy load and the resulting high rms current causes low efficiency. Frequency can be adapted so that the negative inductor current is kept as small as possible to maintain ZVS. This approach does require large frequency ranges and complex control, but is effective at maintaining low rms current.

All of the boost techniques above must still produce an output voltage larger than the peak input voltage, placing additional conversion burden on the second stage.

Buck converters are sometimes used (see examples in Section VI). However, these cannot be operated over the entire line cycle, precluding their use in applications demanding high power factor.

The four-switch buck-boost topology (as in Fig. 2). has been used for power factor correction to achieve high power factor and low output voltage. With two synchronous active switches (SA1 and SB1), this topology can operate in boundary conduction mode to achieve power factor correction. Through valley switching, it may achieve ZVS for $V_{in} < V_{out}$; using TCM, it may achieve ZVS over a broader range (with the same disadvantage of light-load inefficiency or wide operating frequency). No matter what choice of control, operation as an indirect converter in this way requires high rms switch and inductor currents (as in a flyback converter), precluding its use at even moderate power levels.

This topology may also be operated as a cascaded buck and boost converter, with only one mode operated at a time. Operated in "boost mode" (with SA1/SA2 held on/off respectively), it achieves ZVS for $0 < V_{in} < V_{out}/2$. In "buck mode" (SB1/SB2 held off/on respectively), it achieves ZVS for $V_{out} < V_{in} < 2V_{out}$. Using these two direct delivery modes, the converter cannot achieve ZVS for $V_{out}/2 < V_{in} < V_{out}$ (see Fig. 3). When in this voltage range, TCM control in boost or indirect buck-boost mode could be used to achieve ZVS, with the same disadvantages as above. While these techniques

are possible, we are unaware of a published implementation that achieves ZVS over the entire line cycle, low output voltage, and high power factor.

Creative techniques have been developed to create seamless control of such a converter, reduce switch stresses, and achieve other advantages [14]–[17]. These approaches do not solve the problem of achieving ZVS and hence have severe limitations on operating frequency.

III. Proposed Operation

The proposed control allows the four-switch buck-boost topology to operate in the aforementioned "boost mode" (for $0 < V_{in} < V_{out}/2$), "buck mode" (for $V_{out} < V_{in} < 2V_{out}$), and a proposed modified boost mode (for $V_{out}/2 < V_{in} < V_{out}$), as demonstrated in Fig. 4.

Low Voltage / Boost Mode: The converter may be operated as a conventional boost converter by ensuring that switches SA1/SA2 are kept on/off respectively for the entire switching cycle. This mode has an energy storage phase (SB1 on), a direct delivery phase (SB2 on), and a resonant phase to achieve ZVS (SB1 and SB2 off). The LC resonant phase begins with zero initial current, a dc offset voltage V_{in}, and an initial capacitor voltage V_{out}; as such, v_B will ring down to zero as long as $V_{in} < V_{out}/2$. Switch SB1 is turned on in response to the zero voltage condition (see Sec. IV and Fig. 5) which may occur before the inductor current returns to zero; as such, the current at turn-on i_0 may be somewhat negative.

High Voltage / Buck Mode: The converter may also be operated as a conventional buck converter by ensuring that switches SB1/SB2 are kept off/on respectively for the entire switching cycle. This mode (see Fig. 4) is directly analogous to the boost mode. It has a direct delivery phase (SA1 on), an indirect delivery phase (SA2 on), and a resonant phase to achieve ZVS (SA1 and SA2 off). The LC resonant phase begins with zero initial current, a dc offset voltage V_{out}, and an initial capacitor voltage of 0; as such, v_A will ring up to V_{in} as long as $V_{in} < 2V_{out}$. Switch SA1 is turned on in response to the zero voltage condition (see Sec. IV) which may occur before the inductor current returns to zero; as such, the current at turn-on may be somewhat negative.

Medium Voltage / Modified Boost Mode: A modified boost mode, proposed in our associated conference paper [1] and expanded upon here, achieves ZVS for any $V_{in} < V_{out}$. The progression of switching states includes an energy storage phase (SA1 and SB1 on), a direct delivery phase (SA1 and SB2 on), an indirect delivery phase (SA2 and SB2 on), and a resonant phase (all switches off).[1] During the resonant phase, switch SA1 turns on when node A reaches V_{in}, while switch SB1 turns on Δt later when node B reaches zero; this does not significantly affect the understanding of the switching states, but must be accounted for in control.

The advantage of this mode lies in its "CLC" resonant phase, unlike the "LC" resonant phase of the boost mode. In

[1]Some work has used related kinds of modes that modulate both half bridges asynchronously [14], [18]–[21], usually for improved control in transitioning from pure boost to pure buck modes. To the authors' knowledge, none take advantage of both the reduced inductor current ripple (compared to the typical buck-boost mode) and ZVS.

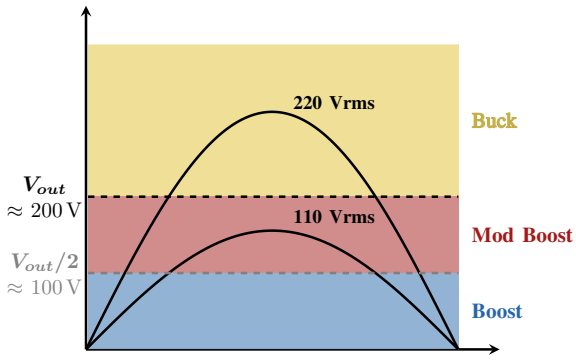

Fig. 3. The proposed converter may operate with a reduced output voltage (∼200 V) by engaging the typical boost, modified boost, and buck operating modes. As long as $V_{out} < 2V_{pk}$, the appropriate use of these modes universally allows ZVS and therefore high-frequency operation. The converter may also operate with the conventional ∼400 V output by using the boost mode for $V_{in} < V_{out}/2$ and the modified boost mode for $V_{out}/2 < V_{in} < V_{out}$.

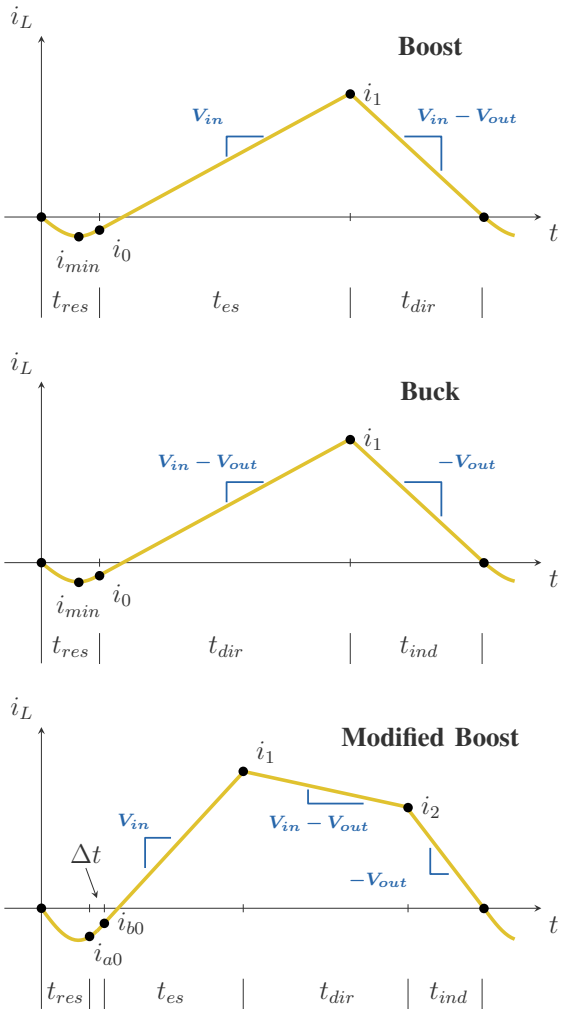

Fig. 4. The boost, buck, and proposed modified boost modes illustrated through the inductor current waveform. Each waveform is broken into phases labeled: energy storage (no connection to the output), direct delivery (connection to input and output), indirect delivery (no connection to the input), and resonant. By taking advantage of both direct and indirect (discharge) forms of energy transfer, the modified boost mode sets up initial conditions at the beginning of its resonant period which guarantee ZVS for any $V_{in} < V_{out}$.

the CLC resonant phase, v_A begins at zero, v_B begins at V_{out}, and there is no voltage offset from the input voltage source. This scenario is guaranteed to return v_B to zero and v_A to (at least) V_{in} for any $V_{in} < V_{out}$, including the desired range $V_{out}/2 < V_{in} < V_{out}$.

The progression of switching states may be understood as that of a boost converter with an indirect delivery phase added to the end, thereby creating the necessary conditions in the resonant period to achieve ZVS. The progression may alternatively be understood as that of the conventional indirect buck-boost mode (i.e. with a triangular inductor current waveform) with a direct delivery phase added in the middle, thereby reducing the rms current required for the same power.

The analysis so far has neglected the resonant commutation times at the end of the energy storage phases of every mode and the direct delivery phase of the modified boost mode. The resonance at the end of the energy storage phase can typically be neglected as the inductor current is usually large enough to effect voltage commutation very quickly on switching node B. The commutation at the end of the direct delivery phase in the modified boost mode can likewise be neglected if the inductor current at that moment (i_2 in Fig. 4) is sufficiently large, but minimizing rms current requires reducing i_2 as much as possible. There is a minimum value of i_2 that will properly commute node SA1 turning off to SA2 turning on, i.e. the inductor energy $\frac{1}{2}Li_2^2$ must be sufficient to discharge the parasitic capacitance C_p at node A. The minimum value for i_2 is therefore

$$i_{2,min} = \sqrt{\frac{C_p}{L} V_{in}(2V_{out} - V_{in})} \quad . \tag{1}$$

To the extent that this condition is violated, v_B may not ring all the way down to zero volts in the final resonant transition. Maintaining i_2 above its minimum value is an important constraint on control. In this work, we maintain i_2 somewhat above $i_{2,min}$ so that the assumptions in Fig. 4 are sufficiently true to justify the control calculations in Appendix A.

In all of the above operating modes, it is important to note that the inductor current may be inferred from on-times without measuring switching-frequency current. Indeed, in the modified boost mode example, t_{res}, Δt, i_{a0}, and i_{b0} may be computed from voltage measurements and circuit parameters alone. Switch on-times can be analytically related to t_{es}, i_1, t_{dir}, i_2, and t_{ind}. A similar logic applies to the boost and buck modes. This observation means that any desired features of the inductor current waveform (esp. the average input current and i_2) may simply be computed and executed without current measurement or feedback. This is an important advantage where complex control is required (as in PFCs) while maintaining ZVS at high frequency. The only additional requirement is a control circuit that can (1) respond to ZVS detection by turning a switch on with sufficiently low delay and (2) hold the switch on for a programmable duration. Such a circuit is described in Sec. IV.

IV. Control

The control of the proposed converter is different from many converters. A dedicated high-speed control circuit, like that shown in Fig. 5, is used for each controlled switch. A given switch is turned on when its corresponding ZVS Detector senses low voltage across the switch. The switch is then kept on for a certain on-time by way of its corresponding Ramp Timer, whose time-out is dictated by a dc or slowly-varying control voltage. After the switch turns off, the cycle repeats as long as ZVS is eventually achieved again (the assumptions that "guarantee" ZVS operation of the converter are violated at very light load, for example, where converter currents generally are not sufficient to commutate switch-node capacitances. Here it may be necessary to introduce additional control as is commonly done to improve efficiency at very light loads). These "self-oscillations" can be started by disabling the control circuit(s) and providing manual pulse(s) to the required switches, and then re-enabling the control circuit.

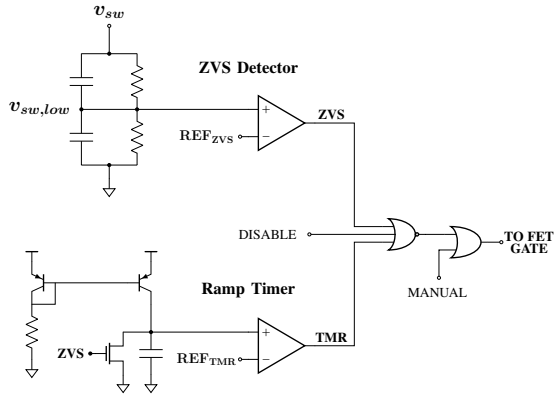

Fig. 5. Auxiliary comparator-based control circuit used for each active switch in the proposed topology, allowing for turn-on in response to zero-voltage conditions on v_{sw} (= v_a for input-side switches or v_b for output-side swithces) and a programmable on-time. Minor variations to this circuit may be required as discussed in Section V.

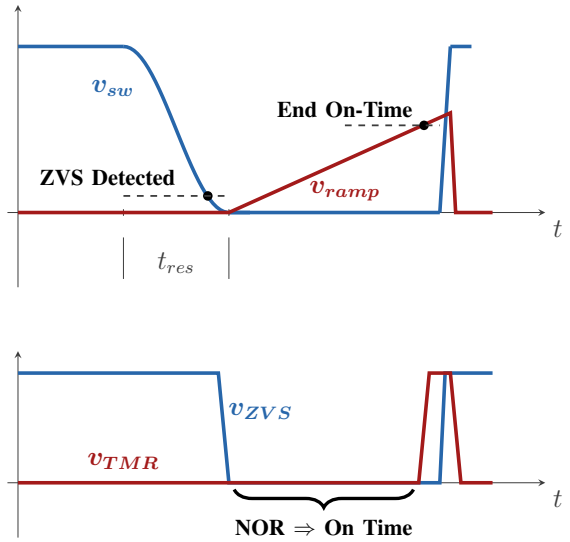

Fig. 6. Illustration of the waveforms in the auxiliary comparator-based control circuit. Detection of ZVS turns on the switch and begins the ramp timer. The ramp timer's completion turns the switch off. Current in the circuit causes v_{sw} to rise, thus resetting the ZVS detector and consequently the ramp voltage. The procedure begins again when ZVS is next detected (ZVS is guaranteed by the proposed modes of operation).

The switch turn-on and turn-off actions are thus, in a sense, passive. No input from a central controller is required, except to select the dc or slowly-varying ZVS trigger voltage $\mathrm{REF}_{\mathrm{ZVS}}$ and on-time control voltage $\mathrm{REF}_{\mathrm{TMR}}$. The turn-on and turn-off events for a switch are asynchronous from the central controller clock, and indeed even from the events of the other switches. Therefore, the proposed converter control should not be understood as direct pulse-width-modulation or frequency control, though pulse widths and frequencies will both vary. The most apt description would be "on-time control," which, in this case, simply means that the on-times are the only control variables, and the off-times and the timings of the turn-on/turn-off events are not directly commanded.

We now turn to the proposed converter in particular, with the goals of maximizing efficiency and granting the designer arbitrary control of the average input current waveform (including high power factor/low THD waveforms). The approach modulates on-times across the line cycle to control the input current shape; this is done in a feedforward manner using only input/output voltage measurements and pre-programmed circuit parameters. Thus, the designer need not include input current measurement nor design a feedback loop for this purpose. Though feedforward control in general is rightly avoided for its inaccuracy under uncertain parameters, inaccurate measurements, and incomplete models, we will show that feedforward control may be sufficiently reliable for purposes of power factor correction.[2]

There are only two control variables, $t_{a1,on}$ and $t_{b1,on}$. Switch SA2 is always operated as a rectifying device, so its timing is fixed as that of an uncontrolled diode (though synchronous rectification may be achieved). Likewise switch SB2 is operated as a rectifying device in the boost and modified boost modes and is always kept on in the buck mode, so its timing is fixed as well.

Converter Example: To proceed with an example, consider the modified boost mode. With two control variables ($t_{a1,on}$, $t_{b1,on}$), we may select two features of the inductor current waveform to target. We choose to target the average (over a switching cycle) input current I_{in} and the corner current i_2. We wish to maintain the corner current i_2 at its minimum allowable value, minimizing rms currents while maintaining ZVS. We target the average input current for power factor correction, though other waveforms may be synthesized when advantageous [22].

To meet these targets, we need a mathematical model relating switch on-times to I_{in} and i_2. The analysis is simply explained, though the actual computations are messy and left to the Appendix. We quote only the driving logic and the final results here. To maintain precision, we use capital symbols to denote values that are constant or averages across a switching cycle; we use lower-case symbols to denote values that change within a switching cycle or that only have meaning within a switching cycle. We also introduce the notation $X = V_{in}/V_{out}$, as this ratio appears frequently. Finally, because we use V_{in} for the local input voltage (averaged over a switching cycle), we instead use V_{rms} to refer to the rms input voltage (taken over the line cycle). The peak of the input voltage waveform is then $\sqrt{2}V_{rms}$.

The logic for input current control is as follows. Because the converter always returns to the same state each switching cycle (at $t = 0$ in Fig. 4), the switch times and the entire switching cycle are analytically related through circuit parameters and measured input/output voltages. Thus, we are able to use feedforward to select appropriate switch on-times.

As an example, consider the modified boost mode. We begin with a desired average input current I_{in} (determined by the position in the line cycle and also the output voltage feedback controller) and then account for the current into any EMI filter capacitors C_{in} to obtain a required average converter input current I_{conv}:

$$I_{conv} = I_{in} - C_{in}\omega_{line}\sqrt{2V_{rms}^2 - V_{in}^2} \tag{2}$$

With a required I_{conv} and a desired i_2, the required i_1 may be computed:

$$i_1 = I_{conv} + \sqrt{I_{conv}^2 + i_2^2 X - 2I_{conv}i_2X^2 + 2I_{conv}i_2DX(1-X)} \tag{3}$$

where $X = V_{in}/V_{out}$, $D = t_{res2}V_{out}/Li_2$ and $t_{res2} = \frac{1}{2}\frac{2\pi}{\omega_2} = \pi\sqrt{LC_p/2}$. From there, the required times $t_{a1,on} = \Delta t + t_{es} + t_{dir}$ and $t_{b1,on} = t_{es}$ can be backed out and then commanded:

$$t_{b1,on} = L\frac{i_1}{V_{in}} + L\frac{V_{out}\sqrt{\frac{C_p}{L}}\,(1-X)}{V_{in}} \tag{4}$$

$$t_{a1,on} = t_{b1,on} + L\frac{i_1 - i_2}{V_{out} - V_{in}} + \frac{2\sqrt{2LC}\,(1-X)}{\sqrt{X - X^2} + \sqrt{2}\,(1-X)} \tag{5}$$

While the equations for this feedforward approach appear complicated on paper, the approach is simple to implement in hardware. A microcontroller or ASIC has pre-programmed values for circuit parameters, measures the input/output voltages, performs the necessary calculations, and commands the switch on-times by way of the control voltages $\mathrm{REF}_{\mathrm{TMRa1,b1}}$. The actual turn-on and turn-off events are executed with the dedicated high-speed circuitry and need not be commanded in synchrony with a digital clock. Finally, we emphasize once again that no current measurement is required, neither high-frequency inductor current nor low-frequency input current.

Although the discussion above treats the proposed modified boost mode, similar logic applies to the boost and buck modes. Detailed calculations for all modes appear in the Appendix.

The feedforward equations also allow us to calculate switching frequencies at the design stage, with results in Fig. 7 (for a given power, rms input voltage, and instantaneous input voltage, the equations in the Appendix are used to calculate all of the time periods within a switching cycle, which are

[2]In addition to the feedforwad "inner loop" controlling the input current *shape* over the line cycle, a traditional feedback "outer loop" (slower than the line cycle) controls the output voltage by way of the *magnitude* of the input current waveform. There is nothing unique about this feedback loop, and it is mentioned only for completeness.

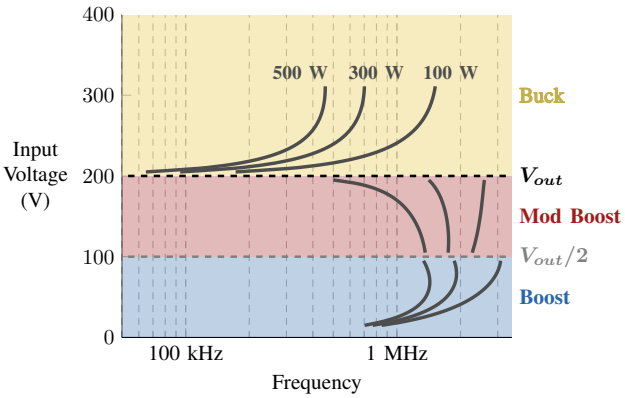

Fig. 7. Instantaneous switching frequency on the rising half of the input voltage half-sine for $V_{rms} = 220\,\text{V}$, $C_{in} = 4.5\,\mu\text{F}$, $L = 13.5\,\mu\text{H}$, $f_{line} = 50\,\text{Hz}$, and $i_2 = 2.1\,\text{A}$. The asymptote at $V_{in} = V_{out}$ is easily avoided with a brief transition period as is commonly done in cascaded buck-boost converters.

then summed to give the total period). The frequency varies across the line cycle and across power, though such variations are expected in most converters that achieve ZVS like BCM or resonant converters. Finally, we note that there is an asymptote at $V_{in} = V_{out}$, at which point the buck and modified boost modes have zero inductor current slope in their direct delivery phases. This is easily avoided with a brief transition period (from, say, $V_{in} = 190$–$210\,\text{V}$) during which the modified boost mode is used with the timing calculated at the lower voltage limit and held fixed. Similar approaches are commonly used to transition between boost and buck modes in conventional buck-boost converters. We used it in the prototype below, and the results confirm minimal distortion and impact on efficiency.[3]

Control Advantages: This type of control has several advantages. First, it is capable of accommodating high-frequency, but varying, switching patterns. Second, this control approach can naturally account for input capacitance, which has drawn significant attention as a source of input current distortion that can be difficult to manage [23]–[30]. Third, because the proposed control is based on generalized equations, it can enable conditions that would be considered non-idealities in other converters. As an example, consider that the output voltage for a PFC is usually considered fixed for control which requires very large buffer capacitances. Research has shown that using large voltage swings with smaller capacitances can shrink buffer volume substantially (e.g. with active buffers). The proposed control can accommodate large buffer voltage swings since it can monitor the output voltage and still compute correct on-times to achieve ZVS, low rms inductor current, and power factor correction.

V. Prototype

We implemented the proposed technique to validate its advantages and feasibility with the specifications in Table I.

[3]When $V_{in} > V_{out}$, the modified boost mode will lose ZVS slightly, but this will not significantly affect the efficiency and a sufficiently high V_{ZVS} threshold will still detect the valley.

For the power stage (Table II), we used Panasonic GaN FETs for their good figure of merit ($R_{on} \times C_{oss}$), availability of low-resistance parts, and modestly superior dynamic R_{on} [31]. The devices' C_{oss} alone constitute C_p and, though non-linear, are approximated as $125\,\text{pF}$ for feedforward control. Though four GaN HEMTs are used which may be cost-prohibitive in some applications today, it is expected that the cost of GaN will continue to decline as the technology matures. Though it is difficult to estimate achievable capability using different technology, we point the reader to [1] for an implementation with diodes instead of synchronous rectifiers which several advantages shown here but still achieve good efficiency.

The choice of inductor value is highly multi-variate, depending on the desired frequency range, power range, and efficiency (smaller inductor values cause resonant phases, which deliver no power, to occupy a greater fraction of a switching cycle). Here we used a custom core with a single-layer winding, distributed gaps, and field-shaping to ensure high conduction area. The core material was Fair-Rite 67 which has exceptional high-frequency performance [32]. The design of the inductor is covered fully in [33].

The input bridge is composed of active silicon devices with isolated opto-drivers (though low-loss diodes would also work). Since these devices operate at the low grid frequency, high-capacitance devices and low-speed drivers may be used.

The control stage (Table III) requires high-speed comparators, ideally with adjustable hysteresis. The various logic gates are chosen to minimize delay. The microcontroller (PIC32MZ) is overpowered for this application and is chosen for prototyping convenience only. Indeed, the microcontroller and most of the circuitry in Fig. 5 could be integrated for high volume production, which would avoid the high cost of discrete components with unnecessarily wide capabilities.

One control circuit is used for each active device. Circuits for low-side devices (SA2 and SB1) are arranged as in Fig. 5. Circuits for high-side devices (SA1 and SB2) are themselves ground-referenced, but the polarity of the ZVS timer inputs are reversed such that the detector responds to the ring-up of the switch-node voltage. For switch SA1, it is necessary to modulate REF_{ZVS} as V_{in} varies to appropriately sense ZVS across SA1.

Control circuits are used for the rectifying devices SA2 and SB2 to achieve synchronous rectification. On-times for these devices can be calculated and commanded in the same way as SA1 and SB1 (see the Appendix). The designer may freely set substantially shorter on-times for the rectifying devices than is actually required in the circuit; the devices' body-diode-like behavior will continue to rectify in exchange for somewhat higher loss. Nevertheless, it should be noted that the proposed control is quite robust to small over-estimations in rectifier on-times. Since all devices turn on in response to zero-voltage conditions, there is no risk of shoot-through or other catastrophic errors. Rectifier on-times that are slightly longer than required for pure rectifying behavior simply add energy to the resonant reset phase with very little impact on overall circuit operation.

The Panasonic devices require a fairly complex gate drive scheme due to their diode-like input impedance. We follow

TABLE I
PROTOTYPE SPECIFICATIONS

Specification	Value
Input Voltage	Universal (85–265 $\mathrm{V_{rms}}$)
Output Voltage	400 V, 200 V, 100 V
Power	660 W for 220 $\mathrm{V_{rms}}$
Dimensions	$3.23 \times 2.56 \times 1.00$ inches
Volume	$8.23\,\mathrm{in}^3$
Power Density	$80\,\mathrm{W/in}^3$

TABLE II
POWER STAGE IMPLEMENTATION

Component	Part/Value
SA1,SA2,SB1,SB2	PGA26E07BA (70 mΩ,125 pF C_{oss})
Capacitor C_{out}	450QXW220MEFC18X50 (220 µF)
Inductor L	13.5 µH
Core Material	Fair-Rite 67
Inductor Turns	13 @ 20 AWG
Inductor Size	⌀1 in, height 1 in
Inductor Design	$Q = 620$ at 3 MHz [34]
Input Bridge Devices	STL36N55M5
Input Bridge Drivers	VOM1271

TABLE III
CONTROL IMPLEMENTATION

Component	Part/Value
Step-down (high-Z)	100 kΩ and 10 pF
Step-down (low-Z)	976 Ω and 1000 pF
Comparators	ADCMP601
Hysteresis Resistors	150 kΩ
Current Mirror BJTs	2SA1873
Current Mirror Resistor	5.6 kΩ
Ramp Reset FET	SN74LVC1G06
NOR Gate	SN74LVC1G27
OR Gate	SN74LVC1G32
Microcontroller	PIC32MZ0512EFE064
High-Side Supply Isolator	RP-0505S
High-Side Signal Isolator	SI8410

TABLE IV
GATE DRIVE IMPLEMENTATION

Component	Part/Value
Gate Driver	LM5114
$R_{through}$	68 Ω
R_{up}	4.7 Ω
R_{down}	4.7 Ω
C_{drive}	2 nF
R_{bias}	10 kΩ
Supply Isolator	RP-0505S
Signal Isolator	SI8610

the schematic in [35], replicated in Fig. 8, with values in Table IV. These values are chosen for multi-MHz operation, giving sharp rise/fall times and substantial continuous gate current to minimize $R_{ds,on}$.

The entire circuit is shown in Fig. 9. The converter measures $3.23\,\mathrm{in}$ x $2.56\,\mathrm{in}$ x $1.00\,\mathrm{in} = 8.27\,\mathrm{in}^3$.

VI. EXPERIMENTAL PERFORMANCE

We operated the prototype across its rated voltage and power range using electronic sources and loads. For demonstration, experimental operating waveforms (across a switching period) are shown for the modified boost mode in Fig. 10 and for the buck mode in Fig. 11 (boost mode is commonly used and has analogous waveforms to buck mode, and hence is not shown).

Performance data is summarized in Fig. 12. For high-voltage operation ($220\,\mathrm{V_{rms}}$), the conventional output voltage

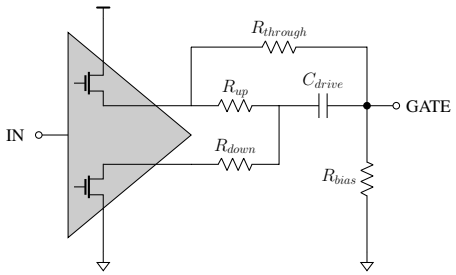

Fig. 8. The gate drive scheme recommended for Panasonic GaN FETs, which have diode-like gate behavior, as explained in the application note [35]. Our component values are listed in Table IV.

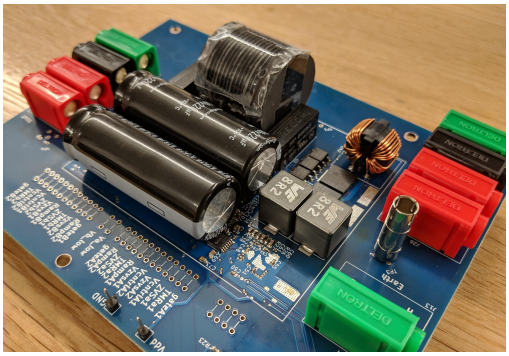

Fig. 9. Photograph of the prototype PFC stage showing input EMI filter magnetics and bridge devices, main power stage inductor, and buffer capacitors. The PFC stage as implemented has a volume of $8.27\,\mathrm{in}^3$ and a power density of $80\,\mathrm{W/in}^3$.

(~400 V) is demonstrated with the system operating in the boost and modified boost modes only. A lower output voltage is also chosen (200 V) to demonstrate operation with boost, modified boost, and buck modes. Operation with $V_{out} = 200\,\mathrm{V}$ shows superior efficiency across the power range, due to the high efficiency of the buck mode when $V_{in} \approx V_{out}$ and the lower average conversion ratio. Efficiencies in this mode reach 98 %, which are competitive for this power range (see Table V and Fig. 15). The lower output voltage will also benefit the efficiency and power density of any subsequent isolation and transformation stage delivering power to a low voltage.

At low voltage input ($110\,\mathrm{V_{rms}}$), we tested with output voltages of 400 V (only boost mode), 200 V (boost and modified boost modes), and 100 V (all three modes). Again, operation with $V_{out} = 400\,\mathrm{V}$ results in lower efficiency, while the lower output voltages give different results at heavy and light loads. The superior performance for $V_{out} = 100\,\mathrm{V}$ at light load is attributable to the same low conversion ratios and efficient buck operation. However, at heavy load, the low output voltage implies substantially larger currents which degrade the efficiency through conduction losses. This tradeoff may disappear, however, in a converter designed exclusively for operation with low output voltages, where high FOM/low-voltage switches can be used for SB1 and SB2 (the flexibility of this prototype required the use of high-voltages switches).

Regardless of the efficiency impact on the PFC stage, it should be remembered that the use of reduced output voltages provides a great relief of the conversion burden of subsequent

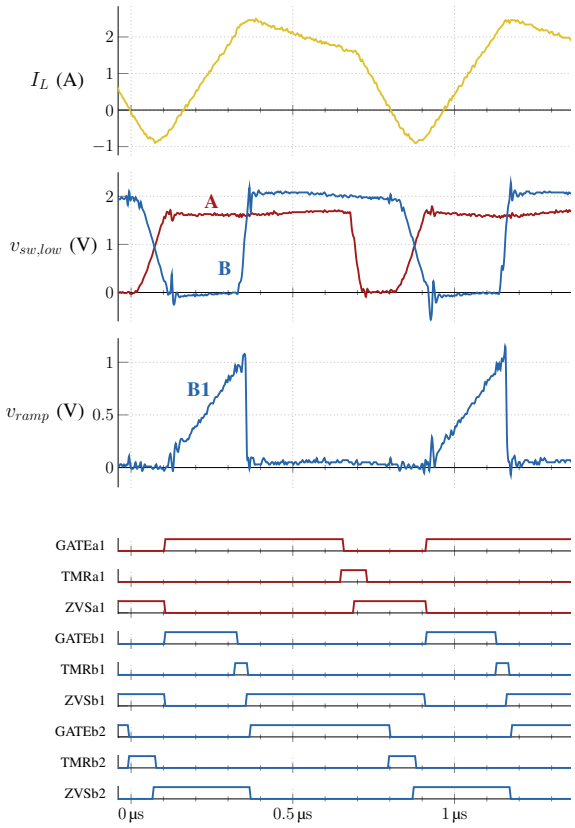

Fig. 10. Experimental operating waveforms in the proposed modified boost mode, demonstrating the inductor current, switch node voltages and the timing ramp for switch B1 (there are corresponding ramps for every switch), along with the relevant experimental digital signals.

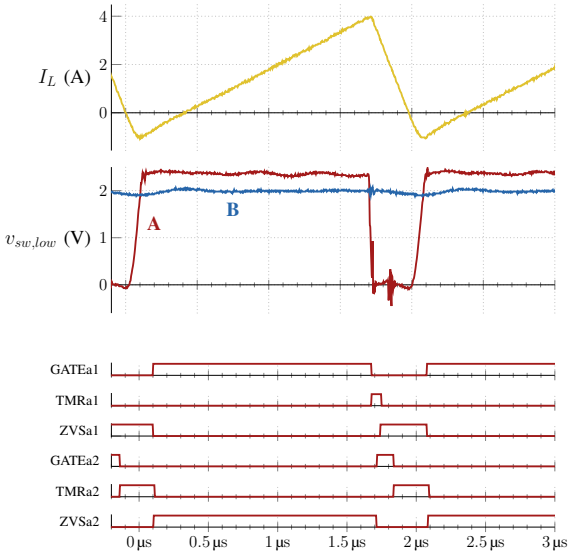

Fig. 11. Experimental operating waveforms in the buck mode, demonstrating the inductor current and switch node voltage, along with the relevant experimental digital signals.

stages. High conversion burdens on dc-dc stages can be very detrimental to their efficiency, and researchers have gone to great lengths to achieve such conversion ratios as efficiently as possible (e.g. [36]). The proposed converter thus exhibits improved PFC efficiency with a reduced output voltage, while providing another efficiency benefit to subsequent stages.

Fig. 12 also shows power factor and THD data, which demonstrate that the proposed control can achieve very high quality waveforms. More germane to the actual input current regulations is the harmonic content, as shown in Fig 13. Every regulated harmonic magnitude (rms) is normalized to its allowed value, and the converter is within the regulations for both high and low output voltages. An experimental waveform across a line cycle is also provided in Fig. 14.

The prototype performance is compared to other recent designs (most of which use GaN or SiC) in Table V and Fig. 15. While the prototype was not optimized for power density, it nonetheless achieves a highly competitive combination of power density and efficiency[4], especially for prototypes of a similar power range. It should be noted that the proposed technique has additional potential. For example, if a design commits to a low-voltage output bus, smaller buffer capacitors than the ones in the prototype could be used. Designs that permit a wider bus voltage swing (enabled by the proposed technique) could further reduce the buffer size. A reduced-voltage bus would also permit the use of lower-voltage switches for SB1/SB2, which would improve efficiency. Finally, as has been mentioned, the use of a reduced-voltage bus would provide benefits to subsequent stages (as compared to boost-type designs), a relevant system-level benefit not captured in Table V and Fig. 15.

[4]Our calculations of efficiency neglect control power, which amounts to approximately 0.5 W in our case, because (a) it is a negligible value for all but the lowest power levels, and (b) because a commercialized version of the prototype would be able to achieve even lower control powers than that. We quote the authors' efficiencies in Fig. 15, for most of which the inclusion/exclusion of control power is also negligible for the same reasons.

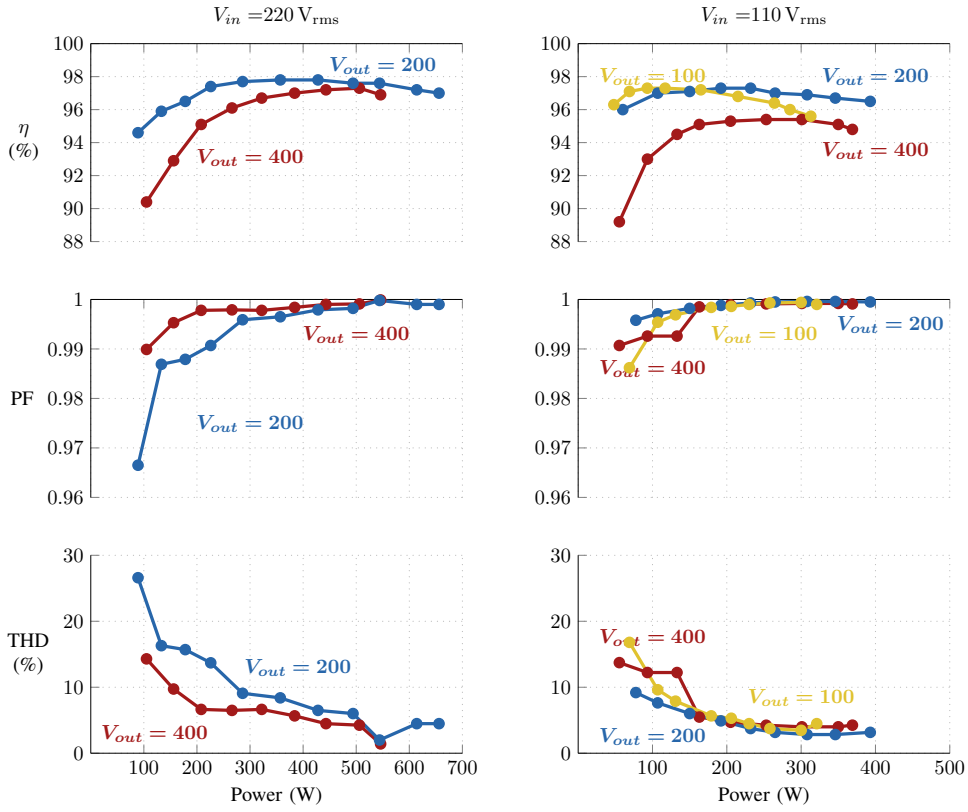

Fig. 12. Experimental efficiencies, power factors, and harmonic distortion for the prototype converter. Data is shown for high and low rms voltages as well as several output voltages. The use of lower output voltages has a positive impact on efficiency while maintaining good power factor and THD.

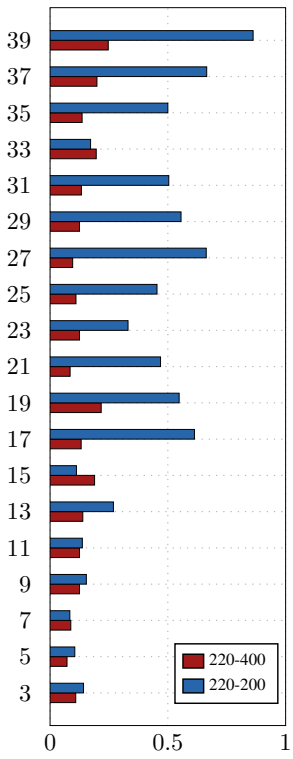

Fig. 13. Harmonic content of the prototype converter normalized to EN61000-3-2 Class D specifications at full power for both output voltages, showing that the prototype as implemented is within regulatory limits.

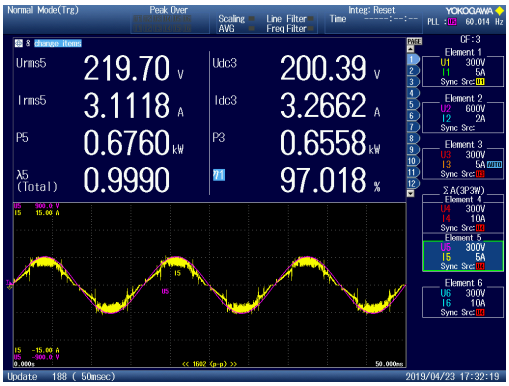

Fig. 14. An example experimental result at full power and low-voltage output, demonstrating the quality of the input waveform, power factor, and efficiency.

VII. Conclusion

Due to their wide required operating voltages and powers, power factor correction stages often make compromises between goals of full-cycle current draw (for high power factor), soft switching, and providing low output voltage for subsequent stages. Here, we proposed a PFC stage that uses a boost mode, a buck mode, and a proposed modified boost mode to achieve all three of the above goals for universal input voltage and a substantial power range. We provided mathematical analysis as well as an implementation approach including control circuits and computations. We demonstrated the capabilities of the proposed stage with a 660 W prototype

TABLE V
COMPARISON OF RECENTLY-PUBLISHED PFC'S THAT INCLUDE VOLUME AND EFFICIENCY

Ref	Year	Type	f_{sw} (kHz)	Power (W)	Volume (in^3)	Density (W/in^3)	Efficiency (%)	Includes EMI Filter?	Technology
[37]	2014	Boost	300	200	10.6	19	94.6	No	Si
[38]	2014	Boost	60	2000	17.5	114	98.6	No	Si
[39]	2014	Boost	130	1000	8.3	120	97.4	Yes	unknown
[40]	2016	Boost	250	3000	70.2	43	97.8	Yes	Si
[41]	2016	Buck	350	6600	55.5	*119	98.5	No	SiC
[42]	2017	Boost	140	3300	49.6	67	97.1	Yes	SiC
[43]	2017	Boost	200	1300	65.5	20	97.6	No	GaN
[44]	2017	Buck-Boost	500	150	2.0	*75	97.0	Yes	GaN
[45]	2018	Boost	140	600	17.2	*35	98.0	Yes	GaN
[46]	2018	Buck	2000	250	5.4	46	97.8	Yes	GaN
[47]	2019	Buck	80	216	5.3	41	94.5	No	GaN
[48]	2019	Boost	1000	3200	25.6	125	99.0	Yes	GaN
[49]	2019	Boost	140	3300	90	36.5	97.8	Yes	Si
[50]	2019	Buck	50	48	1.2	40	96.1	Yes	GaN
[51]	2019	Boost	2000	150	2.0	*76	98.4	Yes	GaN
Proposed	2019	Buck-Boost	2000	660	8.2	80	98.0	Yes	GaN

*Volume inferred from other data or provided photograph

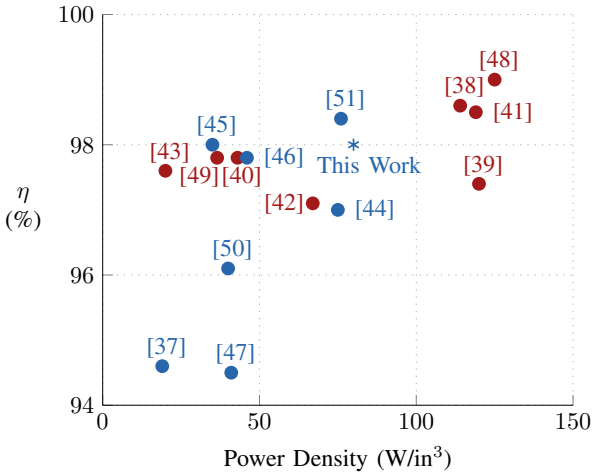

Fig. 15. Comparison of efficiency and power density in recently-published PFCs, divided between lower power (<1000 W, blue) and higher power (>1000 W, red) prototypes. The proposed converter prototype is competitive in general, and especially so when compared to prototypes in the same power range. The comparison across power speaks to the power level of the prototype, not the appropriateness of a given technique to a given power level.

that achieved $80\,\mathrm{W/in^3}$ power density at a peak efficiency of $98\,\%$, with very high power factor (above 0.99 for most operating conditions).

While the proposed PFC stage alone provides competitive efficiencies and densities, we note that its full potential will be most apparent in a full system which will benefit greatly from a reduced conversion burden.

ACKNOWLEDGMENT

We would like to thank L. Balogh of Texas Instruments for his expertise on industry practices and priorities.

APPENDIX A
CONVERTER ANALYSIS FOR FEEDFORWARD CONTROL

One critical feature of the proposed converter is that the inductor current always returns to zero ($t = 0$ in Fig. 4). From this point, based on constant circuit parameters and the instantaneous input and output voltages, the entire circuit behavior is predictable. Without sensing the inductor current or the input current, the switch on-times can be computed to produce a desired inductor current waveform with a specified average input current for power factor correction. This feed-forward approach avoids the need for current sensing altogether. On-times can easily be computed with standard CMOS control with sufficient bandwidth to achieve power factor correction (indeed, in our prototype, we compute and command new on-times at approximately $32\,\mu\mathrm{s}$ increments, or 260 updates per half-cycle).

The remainder of this section outlines how to model the converter for this purpose. The end goal of the model is to compute the required switch on-times as functions of *only* constant circuit parameters and measureables the controller will already have (instantaneous input and output voltage). The results will be t_{on} for each switch as functions of

- the values of the inductor L, parasitic capacitors C_p, and input capacitor C_{in},
- the measured input voltage V_{in}, output voltage V_{out}, line frequency ω_{line} and line rms voltage V_{rms}, and
- the desired values of i_2 (for the modified boost mode) and I_{in} (I_{in} is determined by the position in the line cycle and an output power parameter that is set by slow output voltage feedback).

We remind the reader that capital symbols denote constants or averages across a switching cycle and lower-case symbols denote truly instantaneous values or those that only have meaning within a switching cycle. For compact notation, we also use $X = V_{in}/V_{out}$, $\omega_1 = 1/\sqrt{LC_p}$ for the LC resonant frequency involving only one half-bridge capacitance, and $\omega_2 = 1/\sqrt{LC_p/2}$ for the CLC resonant frequency involving both half-bridge capacitances.

A. Determining I_{conv}

While it is desirable to control the net input current I_{in}, we recognize that the input current I_{in} is not equal to the

converter input current I_{conv}. Rather, it is the sum of I_{conv} and current into any input capacitance I_C. For simplicity, we model the input capacitance as a lumped linear sum of any EMI filter capacitor values. Using this simplified model, we compute the required I_{conv} in terms of the desired I_{in} and the I_C drawn by the input capacitance.

$$\begin{aligned} I_{conv} &= I_{in} - I_C \\ &= I_{in} - C_{in}\frac{dV_c}{dt} \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\cos(\omega_{line}t) \end{aligned} \tag{6}$$

We can replace $\omega_{line}t = \sin^{-1}\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)$ to get I_{conv} in terms of instantaneous measurables instead,

$$\begin{aligned} I_{conv} &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\sqrt{1-\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)^2} \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2V_{rms}^2 - V_{in}^2} \end{aligned} \tag{7}$$

Given I_{conv}, we can now model the converter operating in boost mode, modified boost mode, and buck modes and determine the on-times necessary to achieve I_{conv} at the maximum efficiency.

B. Low Voltage Mode

We analyze the low-voltage mode in accordance with Fig. 4, assuming that i_1 is sufficient to charge C_p in negligible time after SB1 turns off. In this mode, we wish to relate the average input current I_{in} (through I_{conv}) to the on-time of SB1. To do this, we first compute the current at turn-on i_0 and the most negative inductor current during resonance i_{min}. During resonance:

$$v_B = (V_{out} - V_{in})\cos(\omega_1 t) + V_{in} \tag{8}$$

$$i_L = i_{C_p} = C_p\frac{dv_B}{dt} = -C_p(V_{out} - V_{in})\omega_1\sin(\omega_1 t) \tag{9}$$

The minimum inductor current is easily computed,

$$i_{min} = -C_p\omega_1(V_{out} - V_{in}) \tag{10}$$

The current at turn-on is related to the time t_0 from the beginning of resonance until the time that node B reaches zero volts and SB1 turns on, $t_0 = \frac{1}{\omega_1}\cos^{-1}\left(\frac{-V_{in}}{V_{out}-V_{in}}\right)$.

$$\begin{aligned} i_0 &= -C_p\omega_1(V_{out} - V_{in})\sin\left(\cos^{-1}\left(\frac{-V_{in}}{V_{out}-V_{in}}\right)\right) \\ &= -C_p\omega_1 V_{out}\sqrt{1-2X} \end{aligned} \tag{11}$$

By making a piecewise-linear approximation for the inductor current, we compute the average converter input current as:

$$I_{conv} \approx \frac{i_1 + i_{min}}{2} = \frac{1}{2}\left(i_0 + \frac{V_{in}t_{b1,on}}{L} + i_{min}\right) \tag{12}$$

Plugging in for I_{conv}, i_0, and i_{min} and rearranging, we get

$$\begin{aligned} t_{b1,on} = \quad & 2\frac{L}{V_{in}}I_{in} \\ & + \sqrt{LC_p}\frac{1}{X}\left(1 - X + \sqrt{1-2X}\right) \\ & \mp 2LC_{in}\omega_{line}\sqrt{2\left(\frac{V_{rms}}{V_{in}}\right)^2 - 1} \end{aligned} \tag{13}$$

where the $\mp$ depends on whether the input voltage is rising $(-)$ or falling $(+)$. Note that this expression has an intuitive interpretation: the first term is equivalent to the popular constant-on-time control used in true Boundary Conduction Mode; the second term corrects for the resonant transition time (significant at high frequency); the third term accounts for the effect of input capacitance (which is not easily done for many types of PFC control).

Equation (13) is also a good platform to discuss sensitivities to parameter variation. Since the values of C_p and C_{in} each enter into correction terms, variations of their values (due to tolerance, temperature, etc.) are expected to have relatively small impact on the final result. The majority term is the first term with a lienar dependence on L – therefore, the sensitivity to the value of L is most critical. Fortunately, gapped inductors can be routinely manufactured with tolerances of a few percent or less. This general understanding of parameter sensitivity applies to the remaining calculations as well.

If synchronous rectification is desired, the on-time for switch SB2 can be calculated as

$$t_{b2,on} = \frac{L}{V_{in} - V_{out}}\left(\frac{t_{b1,on}V_{in}}{L} + i_0\right) \quad . \tag{14}$$

C. Buck Mode

The calculation for the buck mode is similar to that of the low-voltage boost mode. We first compute the current at turn-on i_0 (this time for SA1) and the most negative inductor current during resonance i_{min}. During resonance:

$$v_a = -V_{out}\cos(\omega_1 t) + V_{out} \tag{15}$$

$$i_L = i_{C_p} = C_p\frac{dv_a}{dt} = -C_pV_{out}\omega_1\sin(\omega_1 t) \tag{16}$$

The minimum inductor current is easily computed,

$$i_{min} = -C_p\omega_1 V_{out} \tag{17}$$

The time from the beginning of resonance until SA1 turns on $(t_0 = \frac{1}{\omega_1}\cos^{-1}(1-X))$ is used to compute the current at that moment:

$$\begin{aligned} i_0 &= -C_p\omega_1 V_{out}\sin\left(\cos^{-1}(1-X)\right) \\ &= -C_p\omega_1 V_{out}\sqrt{X(2-X)} \end{aligned} \tag{18}$$

By making a piecewise-linear approximation for the inductor current, we compute the average converter input current as:

$$I_{conv} \approx \frac{i_1 + i_{min}}{2} = \frac{1}{2}\left(i_0 + \frac{(V_{in} - V_{out})t_{a1,on}}{L} + i_{min}\right)$$

Plugging in for I_{conv}, i_0, and i_{min} and rearranging significantly, we arrive at

$$\begin{aligned} t_{a1,on} = \quad & 2\frac{L}{V_{out}(X-1)}I_{in} \\ & + \sqrt{LC_p}\frac{1}{X-1}\left(1+\sqrt{X(2-X)}\right) \\ & \mp \frac{2LC_{in}\omega_{line}}{V_{out}(X-1)}\sqrt{2\left(\frac{V_{rms}}{V_{in}}\right)^2-1} \end{aligned} \tag{19}$$

where the terms (albeit not as clean) are interpreted in a similar way to the boost mode.

If synchronous rectification is desired, the on-time for switch SA2 can be calculated as

$$t_{a2,on} = \frac{L}{V_{out}}\left(\frac{t_{a1,on}(V_{in}-V_{out})}{L}+i_0\right) \quad . \tag{20}$$

D. Modified Boost Mode

The model for the high voltage mode proceeds in a similar fashion. We take the input capacitance into account in the same way. We need only compute the relationship between the switch on-times and our design targets, I_{conv} and i_2 (Fig. 4). The average input current during the HV mode is given by:

$$\begin{aligned} I_{conv} &= \frac{1}{T}\left[\frac{1}{2}i_1 t_{es} + \frac{1}{2}(i_1+i_2)t_{dir}\right] \\ &= \frac{1}{2}\frac{\frac{i_1^2}{V_{in}} - \frac{i_2^2}{V_{out}-V_{in}} + \frac{i_1^2}{V_{out}-V_{in}}}{\frac{i_1}{V_{in}} + \frac{i_1-i_2}{V_{out}-V_{in}} + \frac{i_2}{V_{out}} + \frac{t_{res2}}{L}} \\ &= \frac{i_2}{2}\frac{(i_1/i_2)^2 - X}{i_1/i_2 - (X)^2 + DX(1-X)} \end{aligned} \tag{21}$$

where $D = t_{res2}V_{out}/Li_2$ and $t_{res2} = \frac{1}{2}\frac{2\pi}{\omega_2} = \pi\sqrt{LC_p/2}$, recalling that $\omega_2 = 1/\sqrt{LC_p/2}$ because there are two parasitic capacitors in series in the CLC case. The above equation reduces to a quadratic in i_1/i_2 which is easily solved,

$$\begin{aligned} i_1 = & I_{conv} + \\ & \sqrt{I_{conv}^2 + i_2^2 X - 2I_{conv}i_2X^2 + 2I_{conv}i_2DX(1-X)} \end{aligned} \tag{22}$$

Having set i_2 to maximize efficiency and i_1 to achieve the correct average converter input current, we only need to specify the on-times of the switches. To do this, we must understand when the switches turn on (equivalently, when the switch voltages reach zero). Switch SA1 will turn on first, with the inductor current equal to i_{a0} after a time t_{res}

$$t_{res} = \frac{1}{\omega_2}\cos^{-1}(1-2X) \tag{23}$$

$$\begin{aligned} i_{a0} &= -\frac{1}{2}CV_{out}\omega_2 \sin\left(\cos^{-1}(1-2X)\right) \\ &= -C_p\omega_2\sqrt{V_{out}V_{in}-V_{in}^2} \end{aligned} \tag{24}$$

Once SA1 turns on, the equivalent circuit changes from an undriven CLC to an LC resonant circuit with a low impedance input V_{in}. Taking t_{res} as an initial condition, we may use an energy argument to calculate i_{b0}:

$$\frac{1}{2}C_p\left[V_{in}-(V_{out}-V_{in})\right]^2 + \frac{1}{2}Li_{a0}^2 = \frac{1}{2}C_pV_{in}^2 + \frac{1}{2}Li_{b0}^2 \tag{25}$$

$$\begin{aligned} i_{b0} &= \sqrt{\frac{C_p}{L}(V_{in}-V_{out}+V_{in})^2 - \frac{C_p}{L}V_{in}^2 + i_{a0}^2} \\ &= \sqrt{\frac{C_p}{L}}V_{out}(1-X) \end{aligned} \tag{26}$$

Finally, we may estimate $\Delta t = t_{b0} - t_{a0}$ by assuming the parasitic capacitance is discharged by an average current $\frac{1}{2}(i_{a0}+i_{b0})$ from its initial voltage $V_{out}-V_{in}$ to zero.

$$\begin{aligned} \Delta t &= (V_{out}-V_{in})C_p/\left(\frac{i_{a0}+i_{b0}}{2}\right) \\ &= \frac{2\sqrt{2LC_p}(1-X)}{\sqrt{X-(X)^2}+\sqrt{2}(1-X)} \end{aligned} \tag{27}$$

Now, the on-time for SB1 is simply based on a linear inductor current ramp from i_{b0} to i_1,

$$t_{b1,on} = L\frac{i_1}{V_{in}} + L\frac{V_{out}\sqrt{\frac{C_p}{L}}(1-X)}{V_{in}} \tag{28}$$

And finally, the on-time for SA1 is simply equal to the on-time for SB1, plus the direct delivery time, plus Δt.

$$\begin{aligned} t_{a1,on} = & t_{b1,on} + L\frac{i_1-i_2}{V_{out}-V_{in}} \\ & + \frac{2\sqrt{2LC_p}(1-X)}{\sqrt{X-(X)^2}+\sqrt{2}(1-X)} \end{aligned} \tag{29}$$

If synchronous rectification is desired, the on-time for switch SA2 can be calculated as

$$t_{a2,on} = \frac{i_2 L}{V_{out}} \tag{30}$$

and the on-time for switch SB2 can be calculated as

$$t_{b2,on} = t_{a1,on} - t_{b1,on} + t_{a2,on} \quad . \tag{31}$$

REFERENCES

[1] A. J. Hanson and D. J. Perreault, "A high frequency power factor correction converter with soft switching," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2027–2034.

[2] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor-corrected converter topologies," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 23–35, Feb 2005.

[3] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749–755, May 2003.

[4] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[5] "High performance power factor preregulator," Texas Instruments, 2005. [Online]. Available: http://www.ti.com/lit/ds/symlink/uc2855a.pdf

[6] "Natural interleaved dual-phase transition-mode pfc controller," Texas Instruments, 2008. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc28060.pdf

[7] M. Scherbaum, M. Reddig, R. Kennel, and M. Schlenk, "An Isolated, bridgeless, quasi-resonant ZVS-switching, buck-boost single-stage AC-DC converter with power factor correction (PFC)," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 74–81.

[8] Z. Liu, X. Huang, M. Mu, Y. Yang, F. C. Lee, and Q. Li, "Design and evaluation of GaN-based dual-phase interleaved MHz critical mode PFC converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 611–616.

[9] S. Lim, D. M. Otten, and D. J. Perreault, "New AC-DC Power Factor Correction Architecture Suitable for High-Frequency Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2937–2949, April 2016.

[10] M. Chen, K. Afridi, S. Chakraborty, and D. Perreault, "MultiTrack Power Conversion Architecture," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[11] O. Knecht, D. Bortis, and J. W. Kolar, "ZVS Modulation Scheme for Reduced Complexity Clamp-Switch TCM DC-DC Boost Converter," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[12] M. Marvi and A. Fotowat-Ahmady, "A Fully ZVS Critical Conduction Mode Boost PFC," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1958–1965, April 2012.

[13] B. Su, J. Zhang, and Z. Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 427–435, Feb 2011.

[14] U. Anwar, D. Maksimovic, and K. Afridi, "A Simple Control Architecture for Four-Switch Buck-Boost Converter Based Power Factor Correction Rectifier," in *2017 IEEE Control and Modeling of Power Electronics (COMPEL) Workshop*, July 2017, pp. 1–6.

[15] M. O. Badawy, Y. Sozer, and J. A. De Abreu-Garcia, "A novel control for a cascaded buck–boost pfc converter operating in discontinuous capacitor voltage mode," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4198–4210, July 2016.

[16] R. Lin and R. Wang, "Non-inverting buck-boost power-factor-correction converter with wide input-voltage-range applications," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Nov 2010, pp. 599–604.

[17] Jingquan Chen, D. Maksimovic, and R. W. Erickson, "Analysis and design of a low-stress buck-boost converter in universal-input pfc applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 320–329, March 2006.

[18] P. Huang, W. Wu, H. Ho, and K. Chen, "Hybrid buck–boost feedforward and reduced average inductor current techniques in fast line transient and high-efficiency buck–boost converter," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 719–730, March 2010.

[19] Z. Zhou, H. Li, and X. Wu, "A constant frequency zvs control system for the four-switch buck–boost dc–dc converter with reduced inductor current," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 5996–6003, July 2019.

[20] A. Murthy and M. Badaway, "State Space Averaging Model of a Dual Stage Converter in Discontinuous Conduction Mode," in *2017 IEEE Control and Modeling of Power Electronics (COMPEL) Workshop*, July 2017.

[21] M. C. Ghanem, K. Al-Haddad, and G. Roy, "A new single phase buck-boost converter with unity power factor," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, Oct 1993, pp. 785–792 vol.2.

[22] A. J. Hanson, A. F. Martin, and D. J. Perreault, "Energy and size reduction of grid-interfaced energy buffers through line waveform control," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[23] J. Kim and G. Moon, "Minimizing effect of input filter capacitor in a digital boundary conduction mode power factor corrector based on time-domain analysis," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3827–3836, May 2016.

[24] M. Kim, O. A. Montes, S. Son, Y. Choi, and M. Kim, "Power factor improvement of flyback pfc converter operating at the light load," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 3019–3023.

[25] Y. Zhou, X. Ren, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Variable on-time (vot) control with phase leading input current (plic) compensation for 400hz crm boost pfc converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 2097–2102.

[26] O. A. Montes, S. Son, J. Kim, J. S. Lee, and M. Kim, "Duty-ratio feedforward controller design to minimize the capacitor effect of the flyback inverter under the light-load condition," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 979–10 989, Dec 2018.

[27] X. Ren, Z. Guo, Y. Wu, Z. Zhang, and Q. Chen, "Adaptive lut-based variable on-time control for crm boost pfc converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8123–8136, Sep. 2018.

[28] O. A. Montes, S. Son, J. Kim, and M. Kim, "Capacitor current compensation scheme for flyback based photovoltaic ac module," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 1896–1901.

[29] R. T. Ryan, J. G. Hayes, R. J. Morrison, and D. N. Hogan, "Improved zero-crossing distortion of a boundary-conduction-mode boost converter with digital average-current-mode control," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 1846–1853.

[30] M. Park, C. Yeon, J. Baek, Y. Jeong, G. Moon, and J. Park, "An improved current compensation method for high pf and low thd in digital boost power factor corrector," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, June 2017, pp. 1065–1070.

[31] B. J. Galapon, A. J. Hanson, and D. J. Perreault, "Measuring dynamic on resistance in gan transistors at mhz frequencies," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2018, pp. 1–8.

[32] A. J. Hanson, J. A. Belk, S. Lim, C. R. Sullivan, and D. J. Perreault, "Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7909–7925, Nov 2016.

[33] R. S. Yang, A. J. Hanson, B. A. Reese, C. R. Sullivan, and D. J. Perreault, "A low-loss inductor structure and design guidelines for high-frequency applications," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[34] R. S. Yang, A. J. Hanson, C. R. Sullivan, and D. J. Perreault, "A low-loss inductor structure and design guidelines for high-frequency applications," in *IEEE Applied Power Electronics Converence (APEC)*, 2018.

[35] "Gan-tr application note (pga26e19ba)," Panasonic, 10 2010. [Online]. Available: https://industrial.panasonic.com/content/data/SC/ds/ds8/c2/APN_PGA26E19BA_EN.pdf

[36] M. K. Ranjram, I. Moon, and D. J. Perreault, "Variable-inverter-rectifier-transformer: A hybrid electronic and magnetic structure enabling adjustable high step-down conversion ratios," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6509–6525, Aug 2018.

[37] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (tcm) single-phase pfc rectifier," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 873–882, Feb 2014.

[38] Y. Kim, W. Sung, and B. Lee, "Comparative performance analysis of high density and efficiency pfc topologies," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2666–2679, June 2014.

[39] C. Deng, M. Chen, P. Chen, C. Hu, W. Zhang, and D. Xu, "A pfc converter with novel integration of both the emi filter and boost inductor," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4485–4489, Sep. 2014.

[40] M. Ibrahim, L. Gonnet, P. Lefranc, D. Frey, J. Ferrieux, and S. Am, "Effectiveness of pareto-front analysis applied to the design of a single-phase pfc rectifier," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2700–2705.

[41] Z. Liu, B. Li, F. C. Lee, and Q. Li, "Design of crm ac/dc converter for very high-frequency high-density wbg-based 6.6kw bidirectional on-board battery charger," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–8.

[42] J. Le Leslé, R. Caillaud, F. Morel, N. Degrenne, C. Buttay, R. Mrad, C. Vollaire, and S. Mollov, "Multi-objective optimisation of a bidirectional single-phase grid connected ac/dc converter (pfc) with two different modulation principles," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 5298–5305.

[43] I. Moon, C. F. Haken, E. K. Saathoff, E. Bian, Y. Lei, S. Qin, D. Chou, S. Sedig, W. H. Chung, and R. C. N. Pilawa-Podgurski, "Design and implementation of a 1.3 kw, 7-level flying capacitor multilevel ac-dc converter with power factor correction," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 67–73.

[44] M. Khatua, D. Shahzad, S. Pervaiz, and K. K. Afridi, "A high-power-density electrolytic-free offline led driver utilizing a merged energy buffer architecture," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 768–773.

[45] S. Pervaiz, A. Kumar, and K. K. Afridi, "Gan-based high-power-density electrolytic-free universal input led driver," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3890–3901, July 2018.

[46] J. A. Santiago-Gonzalez, D. M. Otten, S. Lim, K. K. Afridi, and D. J. Perreault, "Single phase universal input pfc converter operating at hf," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 2062–2069.

[47] E. Candan, A. Stillwell, N. C. Brooks, R. A. Abramson, J. Strydom, and R. C. N. Pilawa-Podgurski, "A 6-level flying capacitor multi-level converter for single phase buck-type power factor correction," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019, pp. 1180–1187.

[48] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive zvs control with improved zvs time margin and limited variable frequency range for a 99efficient, 130-w/in3 mhz gan totem-pole pfc rectifier," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 7079–7091, July 2019.

[49] H. Xu, D. Chen, F. Xue, and X. Li, "Optimal design method of interleaved boost pfc for improving efficiency from switching frequency, boost inductor, and output voltage," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6088–6107, July 2019.

[50] W. Qi, S. Li, H. Yuan, S. C. Tan, and R. Hui, "High-power-density single-phase three-level flying-capacitor buck pfc rectifier," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[51] M. Chen, S. Chakraborty, and D. J. Perreault, "Multitrack power factor correction architecture," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2454–2466, March 2019.

[52] Z. Liao, N. C. Brooks, Z. Ye, and R. C. N. Pilawa-Podgurski, "A high power density power factor correction converter with a multilevel boost front-end and a series-stacked energy decoupling buffer," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 7229–7235.