A High-Frequency Power Factor Correction Stage with Low Output Voltage

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Abstract—Single-phase power factor correction (PFC) stages would ideally have three features – operation over the entire line cycle, soft switching at high frequency for all powers and voltages, and a reasonably low output voltage. These features permit high power factor, high combination of density and efficiency, and reduced stress on subsequent stages. Most PFC stages, including the most commonly used, achieve only a subset of these features. Here we present control innovations to allow a PFC stage to operate from universal input (90–265 V) over the entire line cycle with zero-voltage switching (ZVS) with a reduced output voltage. These features are verified with a prototype with very high power factor (>0.99), high efficiency (98%), and high density (80 W/in³). The PFC can provide an output of 200 Vdc from the entire universal input voltage range which greatly reduces the conversion stress required from subsequent stages. The proposed PFC control consists of a blended feedforward/feedback method that provides additional advantages like guaranteed soft switching, the ability to correct for input capacitance, and the ability to interface with a high-ripple output bus. Therefore, the proposed PFC provides advantages in efficiency and density both for the PFC stage and the overall system.

I. INTRODUCTION

Electrical loads process real power by drawing current at the same frequency as (and in phase with) the source voltage. Other frequency components of the input current result in reactive power and deliver no net energy to the load; these currents are nevertheless physically real and may dissipate energy in any source impedance (e.g. resistance in mains distribution lines and transformers). Currents at harmonic frequencies of the grid voltage are therefore regulated according to international standards (e.g. IEC/EN 61000-3-2) and power conversion stages which draw compliant currents by design are called Power Factor Correction (PFC) converters [2]–[4]. Power factor correction stages often make up a significant fraction of the overall power converter volume and, in multi-stage architectures, often impose onerous requirements on subsequent stages. Improvements in PFC stages can therefore have multi-faceted impacts.

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Fig. 1. The typical boost PFC fails to achieve ZVS for large portions of the line cycle with high rms input voltages, limiting its operating frequency, efficiency, and power density.

To illustrate the challenge, consider the boost converter PFC as part of a two-stage architecture – arguably the most common combination in use. The boost PFC operates from universal input 85–265 Vrms and outputs a dc bus around 400 V. Operated near boundary conduction mode, the boost converter may allow a resonant transition to reduce its switch node voltage prior to turn-on. This process results in true ZVS for \( V_{in} < V_{out}/2 \) and "valley-switching" otherwise with \( V_{min} = 2V_{in} - V_{out} \). For much of a \( \sim 220 \text{ Vrms} \) line cycle, the switch still turns on with hundreds of volts across it and the corresponding switching loss makes high frequency operation untenable. This choice of topology and control is thus limited to low-frequency operation with bulky magnetics and EMI filter components. Its necessarily high output voltage also increases the conversion stress on subsequent stages which, for computing and many other applications, must ultimately present much lower voltages to the load.

From this example, we suggest three desirable design features in a PFC stage:

1) operation over the entire line cycle for high power factor
2) high-frequency operation with soft switching for high
efficiency and density
3) lower output voltage to reduce the conversion burden on subsequent stages

Using this framework, we may categorize a variety of potential PFC solutions. Boost-type PFCs can operate near zero-crossings but generate a high output voltage. Buck-type PFCs make the opposite tradeoff. In both of these cases, the common implementations of each type cannot achieve soft switching without major performance concessions, and still do not achieve all of the goals stated above.

It is clear that only a buck-boost type PFC can operate over the whole line cycle with a low output voltage. The primary challenge with this type of PFC is maintaining soft switching over the entire line cycle as the typical modes of operation all lose soft switching for some voltage ratios. Here we present a control approach for the topology in Fig. 2 which achieves ZVS over the entire voltage range while maintaining low rms current and a low output voltage (e.g., near 200 V instead of near 400 V, even for the higher ∼220 V rms line). In addition, we present control techniques to achieve power factor correction, power regulation, and precise high-frequency timing. The proposed control has additional benefits, like the ability to account for input capacitance that can cause zero-crossing distortion and reduced power factor and the ability to interface with large buffer voltage swings.

II. EXISTING TECHNOLOGY

The boost PFC is likely the most common solution in use due to its ability to operate over the entire line cycle, including very low input voltages. In addition, now-popular bridgeless solutions are almost always boost-type due to the rectifying orientation of switches. Controlling the boost converter can also be very straightforward: operation in boundary conduction mode with constant on-time across the line cycle automatically achieves power factor correction. At sufficiently low switching frequency, boost converters of this type may also take advantage of valley switching without substantially impacting power factor. However, as discussed, such a mode only obtains ZVS for \( V_{in} < V_{out}/2 \) which prohibits high-frequency operation.

Advanced control and/or additional hardware are sometimes used to achieve soft switching with increased complexity. Some approaches add additional lossy circuitry or only partly achieve soft switching [5], [6]. Other approaches achieve ZVS using complex switching networks [7], [8], or stacked architectures [9], [10].

One technique that merits further discussion is continuous conduction mode with ripple ratio larger than unity, sometimes called triangular conduction mode (TCM) [11]–[13]. This control, made possible by the use of all active switches, permits the inductor current to become negative before switching off the rectifying devices. This negative inductor current can aid in achieving ZVS even when \( V_{in} > V_{out}/2 \). If frequency is not adapted, then the ripple is the same at light load as at heavy load and the resulting high rms current causes low efficiency. Frequency can be adapted so that the negative inductor current is kept as small as possible to maintain ZVS. This approach does require large frequency ranges and complex control, but is effective at maintaining low rms current.

All of the boost techniques above must still produce an output voltage larger than the peak input voltage, placing additional conversion burden on the second stage.

Buck converters are sometimes used (see examples in Section VI). However, these cannot be operated over the entire line cycle, precluding their use in applications demanding high power factor.

The four-switch buck-boost topology (as in Fig. 2), has been used for power factor correction to achieve high power factor and low output voltage. With two synchronous active switches (SA1 and SB1), this topology can operate in boundary conduction mode to achieve power factor correction. Through valley switching, it may achieve ZVS for \( V_{in} < V_{out} \); using TCM, it may achieve ZVS over a broader range (with the same disadvantage of light-load inefficiency or wide operating frequency). No matter what choice of control, operation as an indirect converter in this way requires high rms switch and inductor currents (as in a flyback converter), precluding its use at even moderate power levels.

This topology may also be operated as a cascaded buck and boost converter, with only one mode operated at a time. Operated in “boost mode” (with SA1/SA2 held on/off respectively), it achieves ZVS for \( 0 < V_{in} < V_{out}/2 \). In “buck mode” (SB1/SB2 held off/on respectively), it achieves ZVS for \( V_{out} < V_{in} < 2V_{out} \). Using these two direct delivery modes, the converter cannot achieve ZVS for \( V_{out}/2 < V_{in} < V_{out} \) (see Fig. 3). When in this voltage range, TCM control in boost or indirect buck-boost mode could be used to achieve ZVS, with the same disadvantages as above. While these techniques
are possible, we are unaware of a published implementation that achieves ZVS over the entire line cycle, low output voltage, and high power factor.

Creative techniques have been developed to create seamless control of such a converter, reduce switch stresses, and achieve other advantages [14]–[17]. These approaches do not solve the problem of achieving ZVS and hence have severe limitations on operating frequency.

III. PROPOSED OPERATION

The proposed control allows the four-switch buck-boost topology to operate in the aforementioned “boost mode” (for \(0 < V_{in} < V_{out}/2\)), “buck mode” (for \(V_{out} < V_{in} < 2V_{out}\)), and a proposed modified boost mode (for \(V_{out}/2 < V_{in} < V_{out}\)), as demonstrated in Fig. 4.

Low Voltage / Boost Mode: The converter may be operated as a conventional boost converter by ensuring that switches SA1/SA2 are kept on/off respectively for the entire switching cycle. This mode has an energy storage phase (SB1 on), a direct delivery phase (SB2 on), and a resonant phase to achieve ZVS (SB1 and SB2 off). The LC resonant phase begins with zero initial current, a dc offset voltage \(V_{in}\), and an initial capacitor voltage \(V_{out}\); as such, \(v_A\) will ring down to zero as long as \(V_{in} < V_{out}/2\). Switch SB1 is turned on in response to the zero voltage condition (see Sec. IV and Fig. 5) which may occur before the inductor current returns to zero; as such, the current at turn-on \(i_0\) may be somewhat negative.

High Voltage / Buck Mode: The converter may also be operated as a conventional buck converter by ensuring that switches SB1/SB2 are kept off/on respectively for the entire switching cycle. This mode (see Fig. 4) is directly analogous to the boost mode. It has a direct delivery phase (SA1 on), an indirect delivery phase (SA2 on), and a resonant phase to achieve ZVS (SA1 and SA2 off). The LC resonant phase begins with zero initial current, a dc offset voltage \(V_{out}\), and an initial capacitor voltage of 0; as such, \(v_A\) will ring up to \(V_{in}\) as long as \(V_{in} < 2V_{out}\). Switch SA1 is turned on in response to the zero voltage condition (see Sec. IV) which may occur before the inductor current returns to zero; as such, the current at turn-on may be somewhat negative.

Medium Voltage / Modified Boost Mode: A modified boost mode, proposed in our associated conference paper [1] and expanded upon here, achieves ZVS for any \(V_{in} < V_{out}\). The progression of switching states includes an energy storage phase (SA1 and SB1 on), a direct delivery phase (SA1 and SB2 on), an indirect delivery phase (SA2 and SB2 on), and a resonant phase (all switches off).\(^1\) During the resonant phase, switch SA1 turns on when node A reaches \(V_{in}\), while switch SB1 turns on \(\Delta t\) later when node B reaches zero; this does not significantly affect the understanding of the switching states, but must be accounted for in control.

The advantage of this mode lies in its “CLC” resonant phase, unlike the “LC” resonant phase of the boost mode. In

\(^1\)Some work has used related kinds of modes that modulate both half bridges asynchronously [14], [18]–[21], usually for improved control in transitioning from pure boost to pure buck modes. To the authors’ knowledge, none take advantage of both the reduced inductor current ripple (compared to the typical buck-boost mode) and ZVS.
the CLC resonant phase, \( v_A \) begins at zero, \( v_B \) begins at \( V_{out} \), and there is no voltage offset from the input voltage source. This scenario is guaranteed to return \( v_B \) to zero and \( v_A \) to (at least) \( V_{in} \) for any \( V_{in} < V_{out} \), including the desired range \( V_{out}/2 < V_{in} < V_{out} \).

The progression of switching states may be understood as that of a boost converter with an indirect delivery phase added to the end, thereby creating the necessary conditions in the resonant period to achieve ZVS. The progression may alternatively be understood as that of the conventional indirect buck-boost mode (i.e., with a triangular inductor current waveform) with a direct delivery phase added in the middle, thereby reducing the rms current required for the same power.

The analysis so far has neglected the resonant commutation times at the end of the energy storage phases of every mode and the direct delivery phase of the modified boost mode. The resonance at the end of the energy storage phase can typically be neglected as the inductor current is usually large enough to effect voltage commutation very quickly on switching node B. The commutation at the end of the direct delivery phase in the modified boost mode can likewise be neglected if the inductor current at that moment (\( i_2 \) in Fig. 4) is sufficiently large, but minimizing rms current requires reducing \( i_2 \) as much as possible. There is a minimum value of \( i_2 \) that will properly commute node SA1 turning off to SA2 turning on, i.e., the inductor energy \( \frac{1}{2}L i_2^2 \) must be sufficient to discharge the parasitic capacitance \( C_p \) at node A. The minimum value for \( i_2 \) is therefore

\[
i_{2,\text{min}} = \sqrt{\frac{C_p V_{in}(2V_{out} - V_{in})}{L}}.
\]

To the extent that this condition is violated, \( v_B \) may not ring all the way down to zero volts in the final resonant transition. Maintaining \( i_2 \) above its minimum value is an important constraint on control. In this work, we maintain \( i_2 \) somewhat above \( i_{2,\text{min}} \) so that the assumptions in Fig. 4 are sufficiently true to justify the control calculations in Appendix A.

In all of the above operating modes, it is important to note that the inductor current may be inferred from on-times without measuring switching-frequency current. Indeed, in the modified boost mode example, \( t_{res}, \Delta t, i_{a0}, \) and \( i_{b0} \) may be computed from voltage measurements and circuit parameters alone. Switch on-times can be analytically related to \( t_{es}, i_1, t_{dir}, i_2, \) and \( t_{ind} \). A similar logic applies to the boost and buck modes. This observation means that any desired features of the inductor current waveform (esp. the average input current and \( i_2 \)) may simply be computed and executed without current measurement or feedback. This is an important advantage where complex control is required (as in PFCs) while maintaining ZVS at high frequency. The only additional requirement is a control circuit that can (1) respond to ZVS detection by turning a switch on with sufficiently low delay and (2) hold the switch on for a programmable duration. Such a circuit is described in Sec. IV.

IV. CONTROL

The control of the proposed converter is different from many converters. A dedicated high-speed control circuit, like that shown in Fig. 5, is used for each controlled switch. A given switch is turned on when its corresponding ZVS Detector senses low voltage across the switch. The switch is then kept on for a certain on-time by way of its corresponding Ramp Timer, whose time-out is dictated by a dc or slowly-varying control voltage. After the switch turns off, the cycle repeats as long as ZVS is eventually achieved again (the assumptions that “guarantee” ZVS operation of the converter are violated at very light load, for example, where converter currents generally are not sufficient to commutate switch-node capacitances. Here it may be necessary to introduce additional control as is commonly done to improve efficiency at very light loads). These “self-oscillations” can be started by disabling the control circuit(s) and providing manual pulse(s) to the required switches, and then re-enabling the control circuit.
The switch turn-on and turn-off actions are thus, in a sense, passive. No input from a central controller is required, except to select the dc or slowly-varying ZVS trigger voltage \( \text{REF}_{\text{ZVS}} \) and on-time control voltage \( \text{REF}_{\text{TMR}} \). The turn-on and turn-off events for a switch are asynchronous from the central controller clock, and indeed even from the events of the other switches. Therefore, the proposed converter control should not be understood as direct pulse-width-modulation or frequency control, though pulse widths and frequencies will both vary. The most apt description would be “on-time control,” which, in this case, simply means that the on-times are the only control variables, and the off-times and the timings of the turn-on/turn-off events are not directly commanded.

We now turn to the proposed converter in particular, with the goals of maximizing efficiency and granting the designer arbitrary control of the average input current waveform (including high power factor/low THD waveforms). The approach modulates on-times across the line cycle to control the input current shape; this is done in a feedforward manner using only input/output voltage measurements and pre-programmed circuit parameters. Thus, the designer need not include input current measurement nor design a feedback loop for this purpose. Though feedback control in general is rightly avoided for its inaccuracy under uncertain parameters, inaccurate measurements, and incomplete models, we will show that feedforward control may be sufficiently reliable for purposes of power factor correction.\(^2\)

There are only two control variables, \( t_{a1,\text{on}} \) and \( t_{b1,\text{on}} \). Switch SA2 is always operated as a rectifying device, so its timing is fixed as that of an uncontrolled diode (though synchronous rectification may be achieved). Likewise switch SB2 is operated as a rectifying device in the boost and modified boost modes and is always kept on in the buck mode, so its timing is fixed as well.

**Converter Example:** To proceed with an example, consider the modified boost mode. With two control variables \( (t_{a1,\text{on}}, t_{b1,\text{on}}) \), we may select two features of the inductor current waveform to target. We choose to target the average (over a switching cycle) input current \( I_{\text{in}} \) and the corner current \( i_2 \). We wish to maintain the corner current \( i_2 \) at its minimum allowable value, minimizing rms currents while maintaining ZVS. We target the average input current for power factor correction, though other waveforms may be synthesized when advantageous [22].

To meet these targets, we need a mathematical model relating switch on-times to \( I_{\text{in}} \) and \( i_2 \). The analysis is simply explained, though the actual computations are messy and left to the Appendix. We quote only the driving logic and the final results here. To maintain precision, we use capital symbols to denote values that are constant or averages across a switching cycle; we use lower-case symbols to denote values that change within a switching cycle or that only have meaning within a switching cycle. We also introduce the notation

\[
X = \frac{V_{\text{in}}}{V_{\text{out}}},
\]

as this ratio appears frequently. Finally, because we use \( V_{\text{in}} \) for the local input voltage (averaged over a switching cycle), we instead use \( V_{\text{rms}} \) to refer to the rms input voltage (taken over the line cycle). The peak of the input voltage waveform is then \( \sqrt{2}V_{\text{rms}} \).

The logic for input current control is as follows. Because the converter always returns to the same state each switching cycle (at \( t = 0 \) in Fig. 4), the switch times and the entire switching cycle are analytically related through circuit parameters and measured input/output voltages. Thus, we are able to use feedforward to select appropriate switch on-times.

As an example, consider the modified boost mode. We begin with a desired average input current \( I_{\text{in}} \) (determined by the position in the line cycle and also the output voltage feedback controller) and then account for the current into any EMI filter capacitors \( C_{\text{in}} \) to obtain a required average converter input current \( I_{\text{conv}} \):

\[
I_{\text{conv}} = I_{\text{in}} - C_{\text{in}}\omega_{\text{line}}\sqrt{2V_{\text{rms}}^2 - V_{\text{in}}^2}\tag{2}
\]

With a required \( I_{\text{conv}} \) and a desired \( i_2 \), the required \( i_1 \) may be computed:

\[
n_{i_1} = I_{\text{conv}} + \sqrt{I_{\text{conv}}^2 + i_2^2 - 2I_{\text{conv}}i_2X^2 + 2I_{\text{conv}}i_2DX(1 - X)}\tag{3}
\]

where \( X = \frac{V_{\text{in}}}{V_{\text{out}}} \), \( D = t_{\text{res2}}V_{\text{out}}/L_{i_2} \) and \( t_{\text{res2}} = \frac{1}{2}\frac{\pi}{\omega_{\text{ZVS}}} = \frac{\pi}{\sqrt{L_{\text{conv}}C_{\text{in}}}^2}. \) From there, the required times \( t_{a1,\text{on}} = \Delta t + t_{\text{es}} + t_{\text{dir}} \) and \( t_{b1,\text{on}} = t_{\text{es}} \) can be backed out and then commanded:

\[
t_{b1,\text{on}} = L \frac{i_1}{V_{\text{in}}} + V_{\text{out}}\sqrt{\frac{C_{\text{conv}}}{L_{\text{conv}}}(1 - X)}\tag{4}
\]

\[
t_{a1,\text{on}} = t_{b1,\text{on}} + L \frac{i_1 - i_2}{V_{\text{out}} - V_{\text{in}}}
+ \frac{2\sqrt{2L_{\text{conv}}C_{\text{conv}}}(1 - X)}{X - X^2 + \sqrt{2}(1 - X)}\tag{5}
\]

While the equations for this feedforward approach appear complicated on paper, the approach is simple to implement in hardware. A microcontroller or ASIC has pre-programmed values for circuit parameters, measures the input/output voltages, performs the necessary calculations, and commands the switch on-times by way of the control voltages \( \text{REF}_{\text{TMRa1.b1}} \). The actual turn-on and turn-off events are executed with the dedicated high-speed circuitry and need not be commanded in synchrony with a digital clock. Finally, we emphasize once again that no current measurement is required, neither high-frequency inductor current nor low-frequency input current.

Although the discussion above treats the proposed modified boost mode, similar logic applies to the boost and buck modes. Detailed calculations for all modes appear in the Appendix.

The feedforward equations also allow us to calculate switching frequencies at the design stage, with results in Fig. 7 (for a given power, rms input voltage, and instantaneous input voltage, the equations in the Appendix are used to calculate all of the time periods within a switching cycle, which are

\(^2\)In addition to the feedforward “inner loop” controlling the input current shape over the line cycle, a traditional feedback “outer loop” (slower than the line cycle) controls the output voltage by way of the magnitude of the input current waveform. There is nothing unique about this feedback loop, and it is mentioned only for completeness.
then summed to give the total period). The frequency varies across the line cycle and across power, though such variations are expected in most converters that achieve ZVS like BCM or resonant converters. Finally, we note that there is an asymptote at $V_{in} = V_{out}$, at which point the buck and modified boost modes have zero inductor current slope in their direct delivery phases. This is easily avoided with a brief transition period (from, say, $V_{in} = 190–210$ V) during which the modified boost mode is used with the timing calculated at the lower voltage limit and held fixed. Similar approaches are commonly used to transition between boost and buck modes in conventional buck-boost converters. We used it in the prototype below, and the results confirm minimal distortion and impact on efficiency.3

**Control Advantages:** This type of control has several advantages. First, it is capable of accommodating high-frequency, but varying, switching patterns. Second, this control approach can naturally account for input capacitance, which has drawn significant attention as a source of input current distortion that can be difficult to manage [23]–[30]. Third, because the proposed control is based on generalized equations, it can enable conditions that would be considered non-idealities in other converters. As an example, consider that the output voltage for a PFC is usually considered fixed for control which requires very large buffer capacitances. Research has shown that using large voltage swings with smaller capacitances can shrink buffer volume substantially (e.g. with active buffers). The proposed control can accommodate large buffer voltage swings since it can monitor the output voltage and still compute correct on-times to achieve ZVS, low rms inductor current, and power factor correction.

**V. Prototype**

We implemented the proposed technique to validate its advantages and feasibility with the specifications in Table I.

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3When $V_{in} > V_{out}$, the modified boost mode will lose ZVS slightly, but this will not significantly affect the efficiency and a sufficiently high $V_{ZVS}$ threshold will still detect the valley.
TABLE I

PROTOTYPE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Input Voltage</td>
<td>Universal (85–265 V\text{rms})</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>400 V, 200 V, 100 V</td>
</tr>
<tr>
<td>Power</td>
<td>660 W for 220 V\text{rms}</td>
</tr>
<tr>
<td>Dimensions</td>
<td>3.23 \times 2.56 \times 1.00 inches</td>
</tr>
<tr>
<td>Volume</td>
<td>8.23 \text{in}^3</td>
</tr>
<tr>
<td>Power Density</td>
<td>80 W/\text{in}^3</td>
</tr>
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TABLE II

POWER STAGE IMPLEMENTATION

<table>
<thead>
<tr>
<th>Component, Part/Value</th>
<th>SA1, SA2, SB1, SB2</th>
<th>PGA26E07BA (70 m\Omega, 125 pF, C\text{oss}=1800 pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor C\text{out}</td>
<td>450QW220MEFC18X50 (220 \mu F)</td>
<td></td>
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<tr>
<td>Inductor L</td>
<td>13.5 \mu H</td>
<td></td>
</tr>
<tr>
<td>Core Material</td>
<td>Fair-Rite 67</td>
<td></td>
</tr>
<tr>
<td>Inductor Turns</td>
<td>13 @ 20 AWG</td>
<td></td>
</tr>
<tr>
<td>Inductor Size</td>
<td>\text{\varphi}1 in, height 1 in</td>
<td></td>
</tr>
<tr>
<td>Inductor Design</td>
<td>Q = 620 at 3 MHz [34]</td>
<td></td>
</tr>
<tr>
<td>Input Bridge Devices</td>
<td>STL36N55MS</td>
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</tr>
<tr>
<td>Input Bridge Drivers</td>
<td>VOM1271</td>
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</tr>
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TABLE III

CONTROL IMPLEMENTATION

<table>
<thead>
<tr>
<th>Component, Part/Value</th>
<th>Step-down (high-Z)</th>
<th>100 k\Omega and 10 pF</th>
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<tr>
<td>Component, Part/Value</td>
<td>Step-down (low-Z)</td>
<td>976 \Omega and 1000 pF</td>
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<tr>
<td>Component, Part/Value</td>
<td>Comparators</td>
<td>ADCMP601</td>
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<tr>
<td>Component, Part/Value</td>
<td>Hysteresis Resistors</td>
<td>150 k\Omega</td>
</tr>
<tr>
<td>Component, Part/Value</td>
<td>Current Mirror BJTs</td>
<td>2SA1873</td>
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<tr>
<td>Component, Part/Value</td>
<td>Current Mirror Resistor</td>
<td>5.6 k\Omega</td>
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<tr>
<td>Component, Part/Value</td>
<td>Ramp Reset FET</td>
<td>SN74LV1G06</td>
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<tr>
<td>Component, Part/Value</td>
<td>NOR Gate</td>
<td>SN74LVC1G27</td>
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<td>Component, Part/Value</td>
<td>OR Gate</td>
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<tr>
<td>Component, Part/Value</td>
<td>Microcontroller</td>
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<tr>
<td>Component, Part/Value</td>
<td>High-Side Supply Isolator</td>
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<tr>
<td>Component, Part/Value</td>
<td>High-Side Signal Isolator</td>
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TABLE IV

GATE DRIVE IMPLEMENTATION

<table>
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<tr>
<th>Component, Part/Value</th>
<th>Gate Driver</th>
<th>LM5114</th>
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<tbody>
<tr>
<td>Component, Part/Value</td>
<td>R\text{thru}</td>
<td>68 \Omega</td>
</tr>
<tr>
<td>Component, Part/Value</td>
<td>R\text{up}</td>
<td>4.7 \Omega</td>
</tr>
<tr>
<td>Component, Part/Value</td>
<td>R\text{down}</td>
<td>4.7 \Omega</td>
</tr>
<tr>
<td>Component, Part/Value</td>
<td>C\text{drive}</td>
<td>2 nF</td>
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<tr>
<td>Component, Part/Value</td>
<td>R\text{bias}</td>
<td>10 k\Omega</td>
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<tr>
<td>Component, Part/Value</td>
<td>Supply Isolator</td>
<td>RP-0505S</td>
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<tr>
<td>Component, Part/Value</td>
<td>Signal Isolator</td>
<td>SI8410</td>
</tr>
</tbody>
</table>

the schematic in [35], replicated in Fig. 8, with values in Table IV. These values are chosen for multi-MHz operation, giving sharp rise/fall times and substantial continuous gate current to minimize \(R_{\text{ds,on}}\).

The entire circuit is shown in Fig. 9. The converter measures 3.23 in \times 2.56 in \times 1.00 in = 8.27 in\(^3\).

VI. EXPERIMENTAL PERFORMANCE

We operated the prototype across its rated voltage and power range using electronic sources and loads. For demonstration, experimental operating waveforms (across a switching period) are shown for the modified boost mode in Fig. 10 and for the buck mode in Fig. 11 (boost mode is commonly used and has analogous waveforms to buck mode, and hence is not shown).

Performance data is summarized in Fig. 12. For high-voltage operation (220 V\text{rms}), the conventional output voltage (\sim 400 V) is demonstrated with the system operating in the boost and modified boost modes only. A lower output voltage is also chosen (200 V) to demonstrate operation with boost, modified boost, and buck modes. Operation with \(V_{\text{out}} = 200 V\) shows superior efficiency across the power range, due to the high efficiency of the buck mode when \(V_{\text{in}} \approx V_{\text{out}}\) and the lower average conversion ratio. Efficiencies in this mode reach 98% which are competitive for this power range (see Table V and Fig. 15). The lower output voltage will also benefit the efficiency and power density of any subsequent isolation and transformation stage delivering power to a low voltage.

At low voltage input (110 V\text{rms}), we tested with output voltages of 400 V (only boost mode), 200 V (boost and modified boost modes), and 100 V (all three modes). Again, operation with \(V_{\text{out}} = 400 V\) results in lower efficiency, while the lower output voltages give different results at heavy and light loads. The superior performance for \(V_{\text{out}} = 100 V\) at light load is attributable to the same low conversion ratios and efficient buck operation. However, at heavy load, the low output voltage implies substantially larger currents which degrade the efficiency through conduction losses. This tradeoff may disappear, however, in a converter designed exclusively for operation with low output voltages, where high FOM/low-voltage switches can be used for SB1 and SB2 (the flexibility of this prototype required the use of high-voltages switches).

Regardless of the efficiency impact on the PFC stage, it should be remembered that the use of reduced output voltages provides a great relief of the conversion burden of subsequent
stages. High conversion burdens on dc-dc stages can be very detrimental to their efficiency, and researchers have gone to great lengths to achieve such conversion ratios as efficiently as possible (e.g. [36]). The proposed converter thus exhibits improved PFC efficiency with a reduced output voltage, while providing another efficiency benefit to subsequent stages.

Fig. 12 also shows power factor and THD data, which demonstrate that the proposed control can achieve very high quality waveforms. More germane to the actual input current regulations is the harmonic content, as shown in Fig 13. Every regulated harmonic magnitude (rms) is normalized to its allowed value, and the converter is within the regulations for both high and low output voltages. An experimental waveform across a line cycle is also provided in Fig. 14.

The prototype performance is compared to other recent designs (most of which use GaN or SiC) in Table V and Fig. 15. While the prototype was not optimized for power density, it nonetheless achieves a highly competitive combination of power density and efficiency4, especially for prototypes of a similar power range. It should be noted that the proposed technique has additional potential. For example, if a design commits to a low-voltage output bus, smaller buffer capacitors than the ones in the prototype could be used. Designs that permit a wider bus voltage swing (enabled by the proposed technique) could further reduce the buffer size. A reduced-voltage bus would also permit the use of lower-voltage switches for SB1/SB2, which would improve efficiency. Finally, as has been mentioned, the use of a reduced-voltage bus would provide benefits to subsequent stages (as compared to boost-type designs), a relevant system-level benefit not captured in Table V and Fig. 15.

4Our calculations of efficiency neglect control power, which amounts to approximately 0.5 W in our case, because (a) it is a negligible value for all but the lowest power levels, and (b) because a commercialized version of the prototype would be able to achieve even lower control powers than that. We quote the authors’ efficiencies in Fig. 15, for most of which the inclusion/exclusion of control power is also negligible for the same reasons.
Fig. 12. Experimental efficiencies, power factors, and harmonic distortion for the prototype converter. Data is shown for high and low rms voltages as well as several output voltages. The use of lower output voltages has a positive impact on efficiency while maintaining good power factor and THD.

Fig. 13. Harmonic content of the prototype converter normalized to EN61000-3-2 Class D specifications at full power for both output voltages, showing that the prototype as implemented is within regulatory limits.

Fig. 14. An example experimental result at full power and low-voltage output, demonstrating the quality of the input waveform, power factor, and efficiency.

VII. CONCLUSION

Due to their wide required operating voltages and powers, power factor correction stages often make compromises between goals of full-cycle current draw (for high power factor), soft switching, and providing low output voltage for subsequent stages. Here, we proposed a PFC stage that uses a boost mode, a buck mode, and a proposed modified boost mode to achieve all three of the above goals for universal input voltage and a substantial power range. We provided mathematical analysis as well as an implementation approach including control circuits and computations. We demonstrated the capabilities of the proposed stage with a 660 W prototype.
#### Table V
Comparing recently-published PFC’s that include volume and efficiency

<table>
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<tr>
<th>Ref</th>
<th>Year</th>
<th>Type</th>
<th>$f_{sw}$ (kHz)</th>
<th>Power (W)</th>
<th>Volume (in³)</th>
<th>Density (W/in³)</th>
<th>Efficiency (%)</th>
<th>Includes EMI Filter?</th>
<th>Technology</th>
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<tr>
<td>[37]</td>
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<td>Proposed</td>
<td>330</td>
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<td>19</td>
<td>94.6</td>
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<td>Boost</td>
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<tr>
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<td>2000</td>
<td>660</td>
<td>8.2</td>
<td>80</td>
<td>98.0</td>
<td>Yes</td>
<td>GaN</td>
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</table>

*Volume inferred from other data or provided photograph

Fig. 15. Comparison of efficiency and power density in recently-published PFCs, divided between lower power (<1000 W, blue) and higher power (>1000 W, red) prototypes. The proposed converter prototype is competitive in general, and especially so when compared to prototypes in the same power range. The comparison across power speaks to the power level of the prototype, not the appropriateness of a given technique to a given power level.

While the proposed PFC stage alone provides competitive efficiencies and densities, we note that its full potential will be most apparent in a full system which will benefit greatly from a reduced conversion burden.

**Acknowledgment**

We would like to thank L. Balogh of Texas Instruments for his expertise on industry practices and priorities.

**Appendix A**

**Converter Analysis for Feedforward Control**

One critical feature of the proposed converter is that the inductor current always returns to zero ($t = 0$ in Fig. 4). From this point, based on constant circuit parameters and the instantaneous input and output voltages, the entire circuit behavior is predictable. Without sensing the inductor current or the input current, the switch on-times can be computed to produce a desired inductor current waveform with a specified average input current for power factor correction. This feed-forward approach avoids the need for current sensing altogether. On-times can easily be computed with standard CMOS control with sufficient bandwidth to achieve power factor correction (indeed, in our prototype, we compute and command new on-times at approximately 32 µs increments, or 260 updates per half-cycle).

The remainder of this section outlines how to model the converter for this purpose. The end goal of the model is to compute the required switch on-times as functions of only constant circuit parameters and measureables the controller will already have (instantaneous input and output voltage). The results will be $t_{on}$ for each switch as functions of

- the values of the inductor $L$, parasitic capacitors $C_p$, and input capacitor $C_{in}$,
- the measured input voltage $V_{in}$, output voltage $V_{out}$, line frequency $\omega_{line}$ and line rms voltage $V_{rms}$, and
- the desired values of $I_2$ (for the modified boost mode) and $I_{in}$ ($I_{in}$ is determined by the position in the line cycle and an output power parameter that is set by slow output voltage feedback).

We remind the reader that capital symbols denote constants or averages across a switching cycle and lower-case symbols denote truly instantaneous values or those that only have meaning within a switching cycle. For compact notation, we also use $X = V_{in}/V_{out}$, $\omega_1 = 1/\sqrt{LC_p}$ for the LC resonant frequency involving only one half-bridge capacitance, and $\omega_2 = 1/\sqrt{LC_p}/2$ for the CLC resonant frequency involving both half-bridge capacitances.

**A. Determining $I_{conv}$**

While it is desirable to control the net input current $I_{in}$, we recognize that the input current $I_{in}$ is not equal to the
The current at turn-on is related to the time \( t \) for current, we compute the average converter input current beginning of resonance until the time that node B reaches resonance:

\[
\begin{align*}
I_{\text{conv}} &= I_{\text{in}} - I_C \\
&= I_{\text{in}} - C_{\text{in}} \frac{dV_L}{dt} \\
&= I_{\text{in}} - C_{\text{in}} \omega_{\text{line}} \sqrt{2V_{\text{rms}}} \cos(\omega_{\text{line}} t) 
\end{align*}
\]  

(6)

We can replace \( \omega_{\text{line}} t = \sin^{-1} \left( \frac{V_{\text{in}}}{\sqrt{2V_{\text{rms}}}} \right) \) to get \( I_{\text{conv}} \) in terms of instantaneous measurables instead,

\[
\begin{align*}
I_{\text{conv}} &= I_{\text{in}} - C_{\text{in}} \omega_{\text{line}} \sqrt{2V_{\text{rms}}} \sqrt{1 - \left( \frac{V_{\text{in}}}{\sqrt{2V_{\text{rms}}}} \right)^2} \\
&= I_{\text{in}} - C_{\text{in}} \omega_{\text{line}} \sqrt{2V_{\text{rms}}^2 - V_{\text{in}}^2} 
\end{align*}
\]  

(7)

Given \( I_{\text{conv}} \), we can now model the converter operating in boost mode, modified boost mode, and buck modes and determine the on-times necessary to achieve \( I_{\text{conv}} \) at the maximum efficiency.

### B. Low Voltage Mode

We analyze the low-voltage mode in accordance with Fig. 4, assuming that \( i_1 \) is sufficient to charge \( C_p \) in negligible time after SB1 turns off. In this mode, we wish to relate the average input current \( I_{\text{in}} \) (through \( I_{\text{conv}} \)) to the on-time of SB1. To do this, we first compute the current at turn-on \( i_0 \) and the most negative inductor current during resonance \( i_{\text{min}} \). During resonance:

\[
v_B = (V_{\text{out}} - V_{\text{in}}) \cos(\omega_1 t) + V_{\text{in}}
\]  

(8)

\[
i_L = i_{C_p} = C_p \frac{dv_B}{dt} = -C_p(V_{\text{out}} - V_{\text{in}}) \omega_1 \sin(\omega_1 t)
\]  

(9)

The minimum inductor current is easily computed,

\[
i_{\text{min}} = -C_p \omega_1 (V_{\text{out}} - V_{\text{in}})
\]  

(10)

The current at turn-on is related to the time \( t_0 \) from the beginning of resonance until the time that node B reaches zero volts and SB1 turns on, \( t_0 = \frac{1}{\omega_1} \cos^{-1} \left( \frac{-V_{\text{in}}}{V_{\text{out}} - V_{\text{in}}} \right) \).

\[
i_0 = -C_p \omega_1 (V_{\text{out}} - V_{\text{in}}) \sin \left( \cos^{-1} \left( \frac{-V_{\text{in}}}{V_{\text{out}} - V_{\text{in}}} \right) \right)
\]  

\[
= -C_p \omega_1 V_{\text{out}} \sqrt{1 - 2X}
\]  

(11)

By making a piecewise-linear approximation for the inductor current, we compute the average converter input current as:

\[
I_{\text{conv}} \approx \frac{i_0 + i_{\text{min}}}{2} = \frac{1}{2} \left( i_0 + \frac{V_{\text{in}} t_{b,1,\text{on}}}{L} + i_{\text{min}} \right)
\]  

(12)

Plugging in for \( I_{\text{conv}} \), \( i_0 \), and \( i_{\text{min}} \) and rearranging, we get

\[
t_{b,1,\text{on}} = \frac{2L}{V_{\text{in}}} I_{\text{in}} + \sqrt{LC_p \frac{1}{X} \left( 1 - X + \sqrt{1 - 2X} \right)}
\]  

\[
+ 2LC_i \omega_{\text{line}} \sqrt{2 \left( \frac{V_{\text{rms}}}{V_{\text{in}}} \right)^2 - 1}
\]  

(13)

where the \( \mp \) depends on whether the input voltage is rising (−) or falling (+). Note that this expression has an intuitive interpretation: the first term is equivalent to the popular constant-on-time control used in true Boundary Conduction Mode; the second term corrects for the resonant transition time (significant at high frequency); the third term accounts for the effect of input capacitance (which is not easily done for many types of PFC control).

Equation (13) is also a good platform to discuss sensitivities to parameter variation. Since the values of \( C_p \) and \( C_{\text{in}} \) each enter into correction terms, variations of their values (due to tolerance, temperature, etc.) are expected to have relatively small impact on the final result. The majority term is the first term with a linear dependence on \( L \) – therefore, the sensitivity to the value of \( L \) is most critical. Fortunately, gapped inductors can be routinely manufactured with tolerances of a few percent or less. This general understanding of parameter sensitivity applies to the remaining calculations as well.

If synchronous rectification is desired, the on-time for switch SB2 can be calculated as

\[
t_{b,2,\text{on}} = \frac{L}{V_{\text{in}} - V_{\text{out}}} \left( \frac{t_{b,1,\text{on}} V_{\text{in}}}{L} + i_0 \right)
\]  

(14)

### C. Buck Mode

The calculation for the buck mode is similar to that of the low-voltage boost mode. We first compute the current at turn-on \( i_0 \) (this time for SA1) and the most negative inductor current during resonance \( i_{\text{min}} \). During resonance:

\[
v_a = -V_{\text{out}} \cos(\omega_1 t) + V_{\text{out}}
\]  

(15)

\[
i_L = i_{C_p} = C_p \frac{dv_a}{dt} = -C_p V_{\text{out}} \omega_1 \sin(\omega_1 t)
\]  

(16)

The minimum inductor current is easily computed,

\[
i_{\text{min}} = -C_p \omega_1 V_{\text{out}}
\]  

(17)

The time from the beginning of resonance until SA1 turns on \( (t_0 = \frac{1}{\omega_1} \cos^{-1} (1 - X)) \) is used to compute the current at that moment:

\[
i_0 = -C_p \omega_1 V_{\text{out}} \sin \left( \cos^{-1} (1 - X) \right)
\]  

\[
= -C_p \omega_1 V_{\text{out}} \sqrt{X(2 - X)}
\]  

(18)

By making a piecewise-linear approximation for the inductor current, we compute the average converter input current as:

\[
I_{\text{conv}} \approx \frac{i_0 + i_{\text{min}}}{2} = \frac{1}{2} \left( i_0 + \frac{(V_{\text{in}} - V_{\text{out}}) t_{a,1,\text{on}}}{L} + i_{\text{min}} \right)
\]
Plugging in for $I_{\text{conv}}$, $i_0$, and $i_{\text{min}}$ and rearranging significantly, we arrive at

$$t_{a1,\text{on}} = \frac{L}{V_{\text{out}}(X - 1)} I_{\text{in}}$$

$$+ \frac{\sqrt{LC_p}}{X - 1} \left( 1 + \sqrt{X(2 - X)} \right)$$

$$+ \frac{2LC_{i\text{n}} \omega_{\text{line}}}{V_{\text{out}}(X - 1)} \sqrt{\frac{2}{V_{\text{rms}}}} \left( \frac{V_{\text{rms}}}{V_{\text{in}}} \right)^2 - 1 \quad (19)$$

where the terms (albeit not as clean) are interpreted in a similar way to the boost mode.

If synchronous rectification is desired, the on-time for switch SA2 can be calculated as

$$t_{a2,\text{on}} = \frac{L}{V_{\text{out}}} \left( \frac{t_{a1,\text{on}}(V_{\text{in}} - V_{\text{out}})}{L} + i_0 \right) \quad \cdot (20)$$

### D. Modified Boost Mode

The model for the high voltage mode proceeds in a similar fashion. We take the input capacitance into account in the same way. We need only compute the relationship between the switch on-times and our design targets, $I_{\text{conv}}$ and $i_2$ (Fig. 4). The average input current during the HV mode is given by:

$$I_{\text{conv}} = \frac{1}{T} \left[ \frac{1}{2} t_{\text{res}} + \frac{1}{2} (i_1 + i_2) t_{\text{dir}} \right]$$

$$= \frac{1}{2} \frac{V_{\text{in}}^2 - V_{\text{out}}^2 V_{\text{in}} + V_{\text{conv}}^2 - V_{\text{conv}} V_{\text{in}}}{i_1 + i_2}$$

$$= \frac{i_2}{2} \frac{1}{i_1 / i_2} \left( \frac{i_1 / i_2}{2} - X \right) + DX (1 - X) \quad (21)$$

where $D = t_{\text{res}} V_{\text{out}} / L_i$ and $t_{\text{res}} = \frac{1}{2 \omega_2} = \pi \sqrt{LC_2 / 2}$, recalling that $\omega_2 = 1 / \sqrt{LC_2 / 2}$ because there are two parasitic capacitors in series in the CLC case. The above equation reduces to a quadratic in $i_1 / i_2$ which is easily solved,

$$i_1 = I_{\text{conv}}$$

$$+ \sqrt{I_{\text{conv}}^2 + \frac{X^2}{2} - 2 I_{\text{conv}} i_2 X^2 + 2 I_{\text{conv}} i_2 DX (1 - X)} \quad (22)$$

Having set $i_2$ to maximize efficiency and $i_1$ to achieve the correct average converter input current, we only need to specify the on-times of the switches. To do this, we must understand when the switches turn on (equivalently, when the switch voltages reach zero). Switch SA1 will turn on first, with the inductor current equal to $i_0$ after a time $t_{\text{res}}$

$$t_{\text{res}} = \frac{1}{\omega_2} \cos^{-1} (1 - 2X) \quad (23)$$

$$i_0 = -\frac{1}{2} CV_{\text{out}} \omega_2 \sin \left( \cos^{-1} (1 - 2X) \right)$$

$$= -C_p \omega_2 \sqrt{V_{\text{out}} V_{\text{in}} - V_{\text{in}}^2} \quad (24)$$

Once SA1 turns on, the equivalent circuit changes from an undriven CLC to an LC resonant circuit with a low impedance input $V_{\text{in}}$. Taking $t_{\text{res}}$ as an initial condition, we may use an energy argument to calculate $i_0$:

$$\frac{1}{2} C_p \left[ V_{\text{in}} - (V_{\text{out}} - V_{\text{in}})^2 \right] + \frac{1}{2} L_i^2 i_0^2 = \frac{1}{2} C_p V_{\text{in}}^2 + \frac{1}{2} L_i^2 i_0^2 \quad (25)$$

$$i_0 = \sqrt{\frac{C_p}{L} (V_{\text{in}} - V_{\text{out}} + V_{\text{in}})^2 - \frac{C_p V_{\text{rms}}^2}{V_{\text{in}}^2} + i_0^2} \quad (26)$$

Finally, we may estimate $\Delta t = t_{\text{b0}} - t_{\text{a0}}$ by assuming the parasitic capacitance is discharged by an average current $\frac{1}{2} (i_{00} + i_{00})$ from its initial voltage $V_{\text{out}} - V_{\text{in}}$ to zero.

$$\Delta t = \frac{(V_{\text{out}} - V_{\text{in}}) C_p / (i_{00} + i_{00})}{2}$$

$$= \frac{2 \sqrt{2LC_p} (1 - X)}{\sqrt{X - (X)^2 + \sqrt{2} (1 - X)}} \quad (27)$$

Now, the on-time for SB1 is simply based on a linear inductor current ramp from $i_{00}$ to $i_1$,

$$t_{b1,\text{on}} = \frac{i_1 L}{V_{\text{in}}} + L \sqrt{\frac{C_p}{L} (1 - X)} \quad (28)$$

And finally, the on-time for SA1 is simply equal to the on-time for SB1, plus the direct delivery time, plus $\Delta t$.

$$t_{a1,\text{on}} = t_{b1,\text{on}} + L \frac{i_1 - i_2}{V_{\text{out}} - V_{\text{in}}}$$

$$+ \frac{2 \sqrt{2LC_p} (1 - X)}{\sqrt{X - (X)^2 + \sqrt{2} (1 - X)}} \quad (29)$$

If synchronous rectification is desired, the on-time for switch SA2 can be calculated as

$$t_{a2,\text{on}} = \frac{i_2 L}{V_{\text{out}}} \quad (30)$$

and the on-time for switch SB2 can be calculated as

$$t_{b2,\text{on}} = t_{a1,\text{on}} - t_{b1,\text{on}} + t_{a2,\text{on}} \quad . (31)$$

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