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A Two-Stage Universal Input Charger With Wide Output Voltage Range

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ABSTRACT This article presents the design of a two-stage 50 W portable charger architecture with universal ac input and 5 V/25 W, 9 V/45 W, 12 V/50 W output. A 98.5% efficient valley-switched boost converter operating at 0.5–2 MHz enables a 59% reduction in buffer capacitor volume compared to an example electrolytic capacitor while a stacked-bridge LLC converter with a Variable-Inverter-Rectifier-Transformer (VIRT) offers greater than 96% efficiency across the wide output voltage range. The design demonstrates the potential and trade-offs of a two-stage architecture at this operating power and illustrates the benefits of the utilized power stage topologies in achieving both small size and high efficiency over wide input- and output voltage ranges.

INDEX TERMS Two-stage charger, valley-switched boost converter, LLC converter, Variable-Inverter-Rectifier-Transformer, fractional turns, wide output voltage range.

I. INTRODUCTION

While miniaturization is highly desirable for ac/dc chargers, it is difficult to achieve due to the dual requirements of reducing volume and increasing efficiency [1]. Passive components in particular present a critical bottleneck towards miniaturization as advancements in passive components have lagged active devices. Magnetic passives suffer from poor scaling laws for miniaturization [2] and energy buffer capacitors must accommodate stubborn second-line-harmonic buffering requirements.

Most portable chargers rated below 75 W utilize the architecture shown in Fig. 1.¹ At their input they accept a "universal" ac input range (e.g. 90–265 Vac) and on their output they provide a fixed or variable dc bus voltage, typically between 5 V and 20 V. Within the charger, a full-bridge rectifier feeds a capacitive energy buffer in order to establish an internal dc bus which has an undesirable but unavoidable second-line-harmonic voltage ripple. This bus then connects to an isolated



FIGURE 1. Conventional architecture for portable chargers.

dc/dc converter which is responsible for providing a large voltage step down and regulating the output voltage while also establishing isolation to satisfy safety requirements. Finally, input EMI filtering is required to satisfy EN55022 Class B requirements. In this architecture, the capacitive energy buffer, the transformer in the isolated dc/dc converter stage, and the EMI filter typically comprise the dominant contributions to passive component volume and overall system volume.

The minimization of these three passive component blocks is governed by distinct design considerations. The size of the EMI filter can be reduced by increasing the switching frequency of the dc/dc converter, as this increases the

¹Note that converters rated below 75 W are not subject to EN61000-3-2 line current "power factor correction" (PFC) regulations.



required filter corner frequency and therefore enables smaller filter inductance and capacitance values. An extreme example of this miniaturization can be seen in [3] for a PFC converter design operating between 5-10 MHz. The transformer's size and efficiency may also be improved by operating at higher frequencies, up to the performance limits of available core materials and winding technologies [4]. Additionally, because the transformer is employed as part of a dc/dc converter, the properties of that converter can be leveraged to better utilize the transformer and improve performance. For example, the recently-proposed Variable-Inverter-Rectifier-Transformer (VIRT) structure enables transformers with effective fractional-turn secondaries while also providing voltage gain reconfiguration to accommodate a wide output voltage range; these properties can be especially valuable in portable charger designs [5], [6]. On the other hand, the size of the capacitive energy buffer is dictated by the maximum voltage ripple that the dc/dc converter stage can tolerate and cannot be reduced by operating the dc/dc converter at higher frequency.

An electrolytic capacitor is typically used to implement the energy buffer. The volume of the capacitor is related to the peak energy it stores, namely

$$E_{pk} = \frac{1}{2}CV_{ac,\max}^2,\tag{1}$$

where *C* is the capacitance and $V_{ac,max}$ is the peak value (maximum) of the ac input voltage (380 V for 265 Vac input). Thus, the buffer size can be reduced by using a lower capacitance value. However, the capacitance is limited by the voltage range requirements of the dc/dc converter stage. This can be seen by evaluating the energy storage swing in the capacitor,

$$E_{stored} = \frac{1}{2} C \left(V_{bus, \max}^2 - V_{bus, \min}^2 \right), \qquad (2)$$

where $V_{bus,max}$ and $V_{bus,min}$ are the maximum and minimum voltages across the capacitor, respectively. E_{stored} is dictated by the operating power and line frequency and $V_{bus,max}$ is set by the input ac voltage, leaving only $V_{bus,min}$ to be reduced in order to reduce C. Note that with a conventional passive front end, the capacitance must be sized for the worst-case energy storage condition where $V_{bus,max}$ is smallest, corresponding to the lowest applied ac input voltage (90 Vac for universal input).

The key constraint at the heart of sizing the energy buffer is that the capacitance is selected to satisfy ripple requirements when the input voltage is lowest, but it must be physically sized for the voltage rating when the input voltage is highest. This motivates the concept of an "active buffer" in which an additional conversion stage is interfaced to the capacitor in order to better utilize its energy storage capability [7]–[9]. This idea has primarily been investigated in designs which must satisfy power factor correction (PFC) regulations (e.g. >75 W portable chargers). For example, in the commonly employed two-stage architecture shown in Fig. 2, the front-end converter (typically a boost converter) is used to achieve the requisite



FIGURE 2. Two-stage architecture for portable chargers.

line-current shaping but also enables regulation of the dc bus voltage, improving the energy storage capability of the bus capacitor by making $V_{bus,max}$ in (2) independent of the input ac voltage.² In higher power designs (typically greater than 100 W) this idea is further extended by including dedicated circuitry for processing second-harmonic power in order to reduce the energy storage requirement of the bus capacitor in (2) [7], [8], [10].

The use of a two-stage architecture in sub-75 W portable chargers is less common as these designs have typically emphasized cost-minimization which has historically been associated with component count minimization.³ However, the miniaturization benefit of two-stage conversion in this application has been considered in the literature as early as the late-1990s [11]. In this early study, the authors note that a boost PFC front-end is advantageous for the miniaturization of a 70 W/19 V notebook charger contingent on the ability to implement a highly efficient dc/dc converter, which they demonstrate is possible using either a half-bridge LLC or an asymmetric half-bridge back-end operated at 100-250 kHz. Further research over the last decade has explored the boost PFC front-end and half-bridge LLC back-end combination in the 100 kHz regime for a 60 W notebook charger [12]-[14] with increasing power density over [11] attributable to technological improvement of the active and passive components. More recently, [15] proposes a 65 W/20 V charger using a two-stage architecture in which a merged rectifier and boost topology is employed as the front-end with an active clamp flyback back-end, and buffer size reduction is achieved both by increasing the minimum dc bus voltage and by the controlled injection of harmonic currents. These studies demonstrate the potential promise of two-stage conversion in miniaturizing chargers below 75 W, even using PFC designs operating at relatively modest frequencies. In this work we consider the degree of miniaturization available for the front end using an optimized design that leverages the latest components and materials and operates under soft switching at increased frequencies. In particular, we explore the use of a 0.5-2 MHz valley-switched boost converter front-end in the architecture of Fig. 2. The miniaturization potential of this active buffer is enabled by the availability of high energy density high-voltage ceramic capacitors [16] and a recently

²In the case of the boost front-end, $V_{bus,max}$ is typically set equal to $V_{ac,max}$, 380 V.

³Further, the establishment of a common architecture for a given application, such as the standard electrolytic buffer capacitor and flyback implementation of Fig. 1, itself drives a reduction in cost as these "standardized" components enjoy the benefits of economies of scale.

proposed optimization approach for the valley-switched boost converter [17] which takes advantage of the performance benefits of high frequency operation enabled by Gallium Nitride (GaN) devices and modern magnetic materials.

While earlier studies on two-stage conversion focus on applications with a fixed output voltage requirement, there is growing interest in chargers that are capable of delivering a configurable output voltage. In this paper, we consider a charger design with a configurable output of 5 V/25 W, 9 V/45 W, and 12 V/50 W. This wide output voltage range motivates the use of a Variable-Inverter-Rectifier-Transformer (VIRT) in concert with a stacked-bridge LLC converter, as explored in [5], as the back-end stage.

This study expands on our preliminary conference publication in [18] by elaborating on the line-frequency operation of the boost converter, including a refinement of the preliminary operation which enables an increase in system efficiency by approximately 0.5%. We include previously unreported lineto-output operating waveforms, and present an experimental comparison of the volume and loss trade-off between an active front-end buffer and a passive buffer, verifying the miniaturization benefit of the proposed approach.

We emphasize that although the VIRT stacked-bridge LLC converter [5] and valley-switched boost converter [17] represent topologies that have been defined in the literature, this study is distinct in its exploration of the net miniaturization benefit that is achievable when using these converters in a twostage charger. Section II elucidates the design considerations involved in selecting the minimum and maximum bus voltage value, and Section III explores the trade-off between an active buffer and a passive buffer. These discussions then frame a quantitative analysis in Section IV of the trade-off between buffer capacitor volume reduction and second-stage efficiency associated with selection of the minimum bus voltage. Section V provides detail on the design of the two stages once the bus voltage profile has been selected. Finally, Section VI presents experimental results of the prototype two-stage conversion architecture.

II. IMPACT OF BUS VOLTAGE ON BACK-END STAGE

Selection of the bus voltage represents a key design parameter in the proposed two-stage design as it affects the performance and operation of both of the stages, and also contextualizes the trade-off between an active and passive buffer. In this section, we elucidate the impact of the bus voltage profile on the backend stage.

A. ISOLATED DC/DC CONVERTER ARCHITECTURE

Given the wide output voltage range of 5 V, 9 V, and 12 V and relatively high operating currents of 5 A, 5 A, and 4.17 A, respectively, the stacked-bridge LLC+VIRT converter [5] is an attractive candidate for this application. The circuit schematic is shown in Fig. 3. The operating principles of the VIRT architecture are explained in detail in [5] and an overview of this converter is provided in Appendix A; here we instead focus on its salient design features. The voltage gain of the



FIGURE 3. Stacked-bridge LLC+VIRT converter implementing the isolated dc/dc converter stage in Figs. 1 and 2.

stacked-bridge LLC+VIRT converter is

$$\frac{V_o}{V_{bus}} = M_{g,LLC} M_{inv} \frac{N_s}{N_p} \tag{3}$$

where $M_{g,LLC}$ represents the voltage gain of the LLC resonant tank, which is variable and controlled by the switching frequency of the inverter, M_{inv} is the gain of the inverter topology, and N_s/N_p represents the effective transformer turns ratio which is set by the VIRT operating mode,

$$\frac{N_s}{N_p} = \begin{cases} \frac{1}{2N_p}, & \text{FB/FB mode} \\ \frac{2}{3N_p}, & \text{FB/HB mode} \\ \frac{1}{N_p}, & \text{HB/HB (or FB/0) mode} \\ \frac{2}{N_p}, & \text{HB/0 mode.} \end{cases}$$
(4)

 M_{inv} is a controllable quantity due to the stacked-bridge topology and the ability to operate in "variable frequency multiplier" (VFX) mode [19]:

$$M_{inv} = \begin{cases} 1/2, & \text{Inverter Mode 1} \\ 1/4, & \text{Inverter Mode 2 (VFX).} \end{cases}$$
(5)

This converter topology offers a high degree of flexibility in accommodating input- and output voltage variations. In particular, assignment of the VIRT operating modes in (4) and the number of primary turns N_p are used to accommodate the output voltage range, as discussed in Section IV, while M_{inv} and $M_{g,LLC}$ accommodate input voltage variations and are therefore critical to consider in selecting the bus voltage.

B. DC/DC INVERTER DESIGN

Considering the maximum ac input voltage of 265 Vac, a natural maximum value of V_{bus} is 380 V. While the boost front-end in principle enables larger $V_{bus,max}$, increasing this value aggravates the step-down burden of the dc/dc stage and compromises its performance.

The proposed stacked-bridge inverter offers two key advantages over the half-bridge inverter topology typically employed in LLC designs [20]. First, the voltage-quartering gain in (5) can be beneficial for reducing the step-down burden of the LLC transformer. Second, while the stacked-bridge inverter requires twice the number of switches and the addition of a voltage balancing circuit (ref. Fig. 3), each of the switches has half the voltage rating of the switches in the half-bridge



inverter. This is highly beneficial in this design as it enables the use of 350 V rated GaN devices instead of 600/650 V rated devices, which currently represent the next available voltage class of this technology. In particular, we employ 350 V EPC2050 devices which have an $R_{on} * C_{oss}$ figure-of-merit that outclasses any available 600/650 V devices at the time of writing.⁴ Further, these devices have a footprint of 4 mm² such that four of them together have a lower area footprint than a single 600/650 V device of interest (e.g. 33 mm² for a GS66504B device or 64 mm² for a PGA26E07BA device). This reduction in packaged device area is partly driven by the difference in creepage distances and resulting packaging for these different voltage ratings. Thus, the ability to employ these lower voltage devices strongly mitigates the drawback of the increased switch count of the stacked-bridge inverter and the topology is well-suited for miniaturization in this application.

It is sensible to operate the inverter in Mode 2 (frequency multiplier mode, with small gain) when V_{bus} is at its maximum in order to minimize the step-down burden of the dc/dc stage. However, the question of when to operate in Mode 1, or if to operate in this mode at all, depends on further design considerations which we address in Section III.

C. LLC CONVERTER GAIN VARIATION

When operating at the resonant frequency defined by L_r and C_r in the LLC converter, $M_{g,LLC} = 1$ in (3). This is typically the most efficient operating point of this topology [20]. Although $M_{g,LLC}$ may be greater than or less than unity depending on operation below or above the resonant frequency, respectively, we focus on operation at or below resonance as is conventionally done to ensure Zero Voltage Switching (ZVS) of the inverter switches [20]. In this case, we assign the maximum bus voltage $V_{bus,max} = 380$ V to the resonant frequency and primarily use the increase in gain below the resonant frequency to accommodate decreases in the input voltage. Thus, the required LLC converter gain variation, and in particular the maximum gain $M_{g,LLC,max}$, is defined by the minimum energy buffer voltage, $V_{bus,min}$.

While the selection of $V_{bus,max}$ is naturally dictated by the maximum input voltage requirement, selecting $V_{bus,min}$ represents the key design trade-off of this two-stage architecture. As $V_{bus,min}$ is decreased, the gain burden of the LLC converter is increased, which tends to reduce the efficiency of the dc/dc converter stage as discussed in Section IV-A. However, this also reduces the required buffer capacitance for the same energy storage capability as described in (2), which can help to minimize the volume of the buffer capacitor. For discussion

purposes, we initially restrict the LLC gain to be less than or equal to two. This constraint is revisited in Section IV.

III. ENERGY BUFFER CAPACITANCE REDUCTION WITH ACTIVE VS. PASSIVE BUFFER

Based on the inverter gain profile in (5) and an example maximum LLC gain of two, the allowed bus voltage range is 190–380 V (operating the inverter in Mode 2) or 95–190 V (operating in Mode 1). With these operating limits in mind, we may now evaluate the benefit of an active buffer in this application.

First, we consider the design of the energy buffer if only a passive rectifier front end and bulk electrolytic capacitor are used. In this case, with no boost capability, sizing of the energy buffer capacitor is dictated by the minimum input voltage of 90 Vac (127 V_{pk}); we operate the inverter in Mode 1 and a 100 μ F buffer capacitor⁵ is required to keep the bus voltage above 95 V under a constant 50 W power draw. A good 400 V/100 μ F candidate is EPCOS-TDK B43501A9107M000, which has a listed volume of 11.4 cm³ and equivalent series resistance (ESR) of 0.63 Ω [21] corresponding to approximately 0.46 W of loss at 50 W.

An alternative to using an electrolytic capacitor is to use a bank of ceramic capacitors. Ceramic capacitors generally have much lower ESR but suffer from a capacitance that is highly dependent on the applied voltage. For example, the 400 V/2.2 µF EPCOS-TDK C5750X6S2W225K250KA has been identified as having excellent energy density [16], but has a capacitance derating to approximately 0.44 μ F at 400 V. ESR data for ceramic capacitors is typically provided for frequencies above 1 kHz, since they have not conventionally been designed or marketed with low-frequency energy buffering in mind. By extrapolating manufacturer-provided data for ESR, we estimate an ESR of 2.6Ω per capacitor. Considering a capacitance derating to 1.1 μ F at a dc bias of 120 V, 91 pieces of the ceramic capacitor are required, yielding a total (displacement) volume of 6.5 cm³ and a negligible net ESR of 28.6 m Ω at 100 Hz.⁶ This makes the ceramic buffer solution attractive for miniaturization compared to an electrolytic buffer, but it leverages a very high number of ceramic capacitors which may be prohibitive from a cost and/or manufacturing perspective.

An active front-end boost converter enables a greatly reduced buffer capacitance value and can help make the use of high energy density ceramic capacitors more viable. This is because it enables energy to be buffered at high voltage even for low ac voltage conditions, and permits energy to be drawn from the line over a more desirable fraction of the line cycle. The selected front-end valley-switched boost converter and its gating logic are shown in Fig. 4. The converter is topologically simple, requiring only one low-side switch, and a recently

⁴While figure-of-merits can be ill-defined when comparing across different inverter structures, the $R_{on} * C_{oss}$ metric is well defined when comparing the half-bridge to the stacked-bridge. The same switches used in the stacked-bridge as in the half-bridge will have $2R_{on}$ in the conduction path, but will have half the effective C_{oss} at the terminals of the inverter. If switches with $R_{on}/2$ and $2C_{oss}$ are used in the stacked-bridge and switches with R_{on} and C_{oss} are used in the half-bridge, the two inverters exhibit the same effective on-resistance and effective capacitance at the terminals of the inverter.

⁵In this study, capacitor sizing is determined via a MATLAB/Simulink simulation of a diode bridge rectifier interfaced to a buffer capacitor in parallel with a constant power load.

⁶Laboratory measurements confirm that this ceramic capacitor bank has negligible loss compared to the electrolytic capacitor alternative.



FIGURE 4. Valley-switched boost converter, including control logic used to implement valley switching [17].

proposed optimization approach offers a means to achieve high efficiencies in volume-constrained designs operating at MHz frequencies [17]. An overview of the operation of this converter is provided in Appendix A.

For the valley-switched boost converter to operate efficiently it must achieve ZVS which is theoretically possible only when its output voltage is at least twice the input voltage. It is important here to note that the universal input ac connection does not represent a continuously serviceable range and is instead split into a set of "low-range" voltages (90-132 Vac) and "high-range" voltages (198-265 Vac) associated with Japanese/American and European voltage ranges, respectively. The maximum low-range voltage of 132 Vac corresponds to 187 V peak, which is slightly less than half of the selected maximum bus voltage of 380 V. Thus, by choosing to boost to 380 V we can in principle operate the converter with ZVS over the entire low-range. On the other hand, we cannot achieve ZVS for all of the high-range voltages. Instead, we bypass the converter in this regime and rely on passive buffering.⁷ As discussed in Section IV, this allows one to operate the inverter exclusively in Mode 2 and utilize a 17 μ F buffer capacitor, corresponding to 26 pieces of C5750X6S2W225K250KA accounting for voltage de-rating at 250 V, the minimum required to keep the bus voltage above 190 V under a constant 50 W power draw. Note that the buffer capacitance requirement is reduced by approximately 5.9 times compared to the case without boost capability owing to the energy buffering occurring at much higher voltages and the larger spread between the minimum and maximum voltage (i.e. 190–280 V bus voltage ripple in this case versus 95–127 V worst-case ripple with no boost capability).

While this design leverages the inherent partition between "low-range" (nominally 100–120 Vac) and "highrange" (nominally 220–240 Vac) grid voltages in order to optimally select the bus capacitor, operation under atypical "brownout" voltages between 132–198 Vac is still possible. However, because these represent voltages that are only seen in either grid brownout conditions, or in poorly-regulated and/or lossy microgrids, operation in this regime is not a priority for design. Instead, operation in this brownout voltage regime is achieved by reducing power throughput. This is discussed in more detail in Section V-D.

IV. TRADE-OFF BETWEEN ACTIVE ENERGY BUFFER VOLUME AND BACK-END PERFORMANCE

Thus far we have assumed a maximum LLC gain $(M_{g,LLC,max})$ of two in order to assess the potential benefit of an active buffer in this application. In this section, we consider the impact of different values of $M_{g,LLC,max}$ on the capacitor buffer volume and second-stage efficiency, and present a simple quantitative framework in which to consider this trade-off.

A. LLC EFFICIENCY IMPACT

In general, LLC design is an iterative process that involves choosing the inductance ratio $L_n = L_r/L_m$, where L_r and L_m are the resonant and effective magnetizing inductance, respectively, and choosing the effective quality factor $Q_e = 2\pi f_r L_r/R_e$, where f_r is the resonant frequency and R_e is the effective load resistance mapped to the primary [5], [20]. The LLC is capable of servicing a wide gain range, but by focusing on the resonant operating point of the LLC converter we can glean useful insight into the efficiency impact of the choice of $M_{g,LLC,max}$. Further, since this point typically represents the most efficient operating regime of the LLC converter [20], it is a useful representation of overall performance.

At the resonant frequency of the LLC converter, a square wave voltage is imposed on the magnetizing inductance such that the resulting magnetizing current waveform is triangular with a peak value of

$$i_{pk} = \frac{V_o}{R_e} \frac{\pi}{2} \frac{N_p}{N_s} \frac{1}{L_n Q_e}.$$
(6)

The maximum gain of a given LLC design is associated with the boundary between the capacitive and inductive mode in below-resonance operation [22]. This constrains the design according to

$$L_n Q_e \approx \sqrt{\frac{1 + L_n \left(1 - M_{g,LLC,\max}^{-2}\right)}{M_{g,LLC,\max}^2 - 1}}.$$
 (7)

⁷In principle, one can enter a partial boosting mode in this regime such that the converter provides boost capability up to 190 V at the input, and then enters a bypass mode above this voltage. This can further reduce the buffer capacitance at the cost of increased operational complexity.

$ \begin{bmatrix} M_{g,LLC,} \\ max \end{bmatrix} $	Relative LLC i_{pk}^2	$V_{bus,min}$	C [µF]	Num. pcs.	Capacitor vol. [cm ³]
1.25	1.0	304	-	-	-
1.5	1.7	253	60	100	7.1
1.75	2.4	217	25	39	2.8
2.0	3.1	190	17	26	1.9
2.25	4.0	170	14	21	1.5

TABLE 1. Example Influence of $M_{g,LLC,max}$ on LLC Loss and Buffer Size Using C5750X6S2W225K250KA Capacitors, Assuming $L_n = 5$ and an Input Voltage of $198V_{ac}$ With the Front-End Boost Converter Bypassed

Eqns. (6) and (7) show that the peak magnetizing current is reduced when the L_nQ_e product is increased, and this is associated with minimizing $M_{g,LLC,max}$. The peak value of the magnetizing current is important for achieving ZVS of the inverter switches, but otherwise represents an unavoidable component of circulating current which increases loss in the LLC converter. Thus, in principle, the lower the maximum gain requirement of the LLC, the more efficiently it can be operated.⁸ The squared value of the peak current in (6) is representative of the loss impact of this circulating current, and relative values of i_{pk}^2 for different values of $M_{g,LLC,max}$ are enumerated in Table 1. This table is generated for an example value of $L_n = 5$, which is a typical starting point in LLC designs [20], and a similar trend exists for other values of L_n according to (7).

B. CAPACITOR BUFFER SIZING

For the example range of $M_{g,LLC,\max}$ in Table 1 we can determine the buffer capacitance that is required to satisfy the associated minimum bus voltage requirement and compute the required number of C5750X6S2W225K250KA pieces considering appropriate voltage derating. The results of this analysis are shown in Table 1. Note that there is no capacitance entry for the $M_{g,LLC,\max} = 1.25$ case since the associated minimum bus voltage cannot be accommodated when the input voltage is 198 Vac.

C. SELECTING V_{bus,min}

Our aim is to utilize the boost converter to reduce overall converter volume. Table 1 shows that increasing $M_{g,LLC,max}$ from 1.5 to 1.75 yields a substantial capacitor volume savings of 4.3 cm³ for a relative circulating current loss penalty increase of 41%. Moving from a maximum gain of 1.75 to 2.0 yields a further volume reduction of 0.9 cm³ while incurring an additional loss penalty increase of 30%. A further increase to 2.25 maximum gain yields only an additional 0.4 cm³ volume reduction at the cost of an additional 29% relative loss penalty increase. We see that there are diminishing returns on overall volume reduction for increasing the maximum LLC gain, and a maximum gain of around two is a good trade-off in

TABLE 2.	Nominal Mode Voltages As	ssociated With Each	VIRT Mode for
Varying N	P		

	N_p	FB/FB	FB/HB	HB/HB
ĺ	8	6.0	8.0	11.9
	10	4.8	6.3	9.5

this example between LLC performance and capacitor volume reduction. Thus, based on this analysis we select $V_{bus,min} = 190V$, $M_{g,LLC,max} = 2$, and $C_{bus} = 17 \ \mu F$.

V. DESIGN OF THE TWO CONVERSION STAGES

With the bus voltage profile defined, we can complete the design of the two stages of the converter.

A. VIRT MODE ASSIGNMENT AND NUMBER OF PRIMARY TURNS

As discussed previously, we operate the LLC inverter in Mode 2 and associate the LLC resonance with $V_{bus,max} = 380V$. Using (3) we can enumerate the output voltage associated with each VIRT mode at resonance as we vary the number of primary turns N_p . We refer to these as the "nominal" mode voltages and they, in principle, represent the most efficient operating voltage in each VIRT mode. The nominal voltage of each VIRT mode for different values of N_p are shown in Table 2, where we omit HB/0 mode due to the 4x gain variation offered by this mode having limited value in this application [5].

Achieving high efficiency in both the 9 V/45 W and 12 V/50 W cases is important to minimize the total loss of the converter. The efficiency of the 5 V/25 W case is of less concern (e.g. 3 W of loss corresponds to 94.3% efficiency at 50 W, 93.8% efficiency at 45 W, and 89.3% efficiency at 25 W). From this perspective, $N_p = 8$ appears to be an attractive choice, as it places 9 V and 12 V near the nominal voltage of the FB/HB mode and HB/HB modes, respectively. However, this places the 5 V operating point well above FB/FB resonance. Although the efficiency in this mode is not of primary concern, designing the LLC to achieve attenuation to 5 V in this case compromises the achievable efficiency in the other two modes, as part of the available design freedom is lost to meeting this attenuation constraint rather than prioritizing performance in the higher power modes. On the other hand, $N_p = 10$ comfortably sets 5 V in FB/FB mode, and 9 V and 12 V in HB/HB mode, with only approximately 5% attenuation required in HB/HB mode to achieve 9 V operation. This relatively low attenuation is typically achievable with slightly-above-resonance operation in many LLC designs without requiring special consideration.

B. LLC CONVERTER AND TRANSFORMER DESIGN

The required gain curve can be implemented by many pairs of Q_e and L_n , and the choice of these parameters is typically

⁸Note that ZVS can be achieved for a given value of $M_{g,LLC,\max}$ through selection of the values of L_n , Q_e , and f_r .



Two half-turn windings each of 8 paralleled 450/48 Litz

FIGURE 5. Winding arrangement of EQ20/EQ20 back-to-back Hitachi Metals ML91S core halves (spacing of 0.1 mm in each leg) used in the prototype. The primary winding comprises 10 turns of 450/48 Litz wire, while the two half-turn secondaries each comprise 8 paralleled 450/48 Litz wire segments.

an iterative process associated with meeting the gain requirements within a desired frequency window while also achieving realizable passive component values. From a miniaturization perspective, it is desirable for the resonant inductance to be entirely sourced from the leakage inductance of the transformer, as this eliminates the need for an additional external inductor. To achieve this, we employ a relatively high-leakage non-interleaved design in which the primary and secondary windings straddle opposite ends of the core window as indicated in Fig. 5 and discussed in [23]. Further, we utilize 450/48 Litz wire on the primary and secondary in order to mitigate the ac resistance detriment of the non-interleaved configuration. A resonant frequency of around 1 MHz is selected in order to aid future EMI filter miniaturization efforts while also enabling the use of high-performance-factor ML91S core material. A back-to-back EQ20 core configuration is selected to minimize transformer loss within a reasonable volume (approximately one-third of the overall converter volume) while also enabling a core window arrangement that is beneficial for achieving the desired leakage inductance value and providing primary-to-secondary isolation.

Under these constraints, a high-performance design has L_r equal to the leakage of the transformer, places the resonant frequency at or near 1 MHz, and operates with the largest possible $L_n Q_e$ product to minimize circulating currents while also achieving ZVS of the inverter switches and meeting the required gain profile. The resulting design is shown in Table 3 and the components used in the prototype are listed in Table 4. The control approach for the LLC converter is described in Appendix B.

C. VALLEY-SWITCHED BOOST CONVERTER DESIGN

The front-end boost converter is optimized according to the approach detailed in [17]. The resulting converter operates

TABLE 3. LLC Parameters

Parameter	Value	
Resonant frequency	1.13 MHz	
Operating frequency range (trans-	0.5 - 1.3 MHz	
former drive frequency)		
Inverter operating mode	Fixed Mode 2 (freq.	
	multiplier mode)	
Number of primary turns (N_p)	10	
VIRT Mode Assignments: 5: 9:	FB/FB;	
12V	НВ/НВ; НВ/НВ	
Resonant capacitance (C_r)	4.88 nF	
Resonant inductance (L_r)	4.1 μH	
Magnetizing inductance (L_M)	30.5 µH	

TABLE 4. Components Used in Prototype

Component	Value
Second-stage Inverter	
GaN FETs	350V EPC2050
Gate drivers	LMG1210
Signal isolators	Si8620
Balancer diodes	MMBD3004BRM
Balancer capacitors	1uF/450V/1812
VIRT Rectifiers	
MOSFETs	30V TPN2R703NL
Gate drivers	LM5113
Blocking capacitors	3x 4.7uF/25V/0805 per rectifier
Decoupling capacitors	2x 4.7uF/25V/0805 per half-bridge
Output capacitors	8x 10uF/25V/1210
LLC	
Resonant capacitor	3300pF/1kV/C0G/1210 +
	1000pF/2kV/C0G/1812 +
	470pF/2kV/C0G/1812 +
	100pF/2kV/C0G/1206
Resonant inductor	4.1 μ H derived from transformer
VIRT Transformer	
Core	EQ20+EQ20/ML91-S, 0.1 mm gap on all legs
Primary windings	Ten turns of $450/48$ Litz wire wound in three layers $(4/4/2)$.
Secondary windings	Two half-turn secondaries each com- prising 8 paralleled 450/48 Litz wire segments.
Front-End Boost Conve	erter
S_1	GS66504B
D_1	C3D1P7060Q
Input and output de-	ea. 1x C5750X6S2W225K250KA
coupling capacitors	
Boost inductor	41.4 μ H, RM6/3F46, 21 turns 450/48 AWG Litz wire
Buffer capacitors	$24x C5750X6S2W225K250KA (\approx 16$
	μ F effective)
Current ramp	$I_{ramp} = 3.8$ mA (BCV62B current mirror); $C_{ramp} = 1.8$ nF; $S_{ramp} = $ SSMK329R
Comparators	LTC1720
SR latch	SN74LVC1G02
Gate driver	SN74LVC1G08
Line Rectifier	
Rectifier	Z4DGP406L



TABLE 5. Front-End Operating Scheme

Low-range voltages (90-132 V _{ac})	Atypical "brownout" voltages (132-198 V _{ac})	High-range voltages (198-265 V_{ac})	
• Boost converter active, seg- mented operation	• Boost converter bypassed	• Boost converter bypassed	
• Regulated line current similar to unity power factor	• Unregulated line current pulses	• Unregulated line current pulses	
• Draws current when V_{in} greater	• Draws current when V_{in} greater	• Draws current when V_{in} greater	
than desired value	than bus voltage	than bus voltage	
• Deliver rated power	• Deliver reduced power	• Deliver rated power	

between 0.5–2 MHz and the prototype parameters are listed in Table 4.

A valuable degree of freedom enabled by the boost frontend is the ability to shape the line current. In conventional PFC designs, this functionality is used to satisfy EN61000-3-2 harmonic regulations. However, in this application no such regulations exist. Earlier two-stage designs for sub-75 W chargers have typically operated the front-end with a power factor of one as they have focused on adapting existing PFC converters, and their established controllers, into their designs [11]–[14]. On the other hand, in [15] the line-current shaping ability is used to draw higher-order harmonic currents in order to reduce the volume of the buffer capacitor. In this work, however, the buffer capacitor size is set by the passive buffering requirements in high-range operation and this kind of harmonic injection has limited use. Instead, the line current draw is set to maximize the performance of the boost front-end.

First, we note that high efficiency boost operation to 380 V cannot be maintained over the entire input line cycle due to large losses associated with the large conversion ratio required when the input voltage is low. Thus, we apply segmented operation of the boost converter in which the bus voltage is regulated only when the instantaneous input voltage is above a desired value (\approx 50 V) and we otherwise run the converter with a constant boost ratio. The proposed segmented operation is conveniently implemented by setting the on-time reference command (v_{on} in Fig. 4) equal to V_{CC} , resulting in constant on-time operation set by the slope of the ramp in Fig. 4. A summary of the operating scheme of the front-end converter is provided in Table 5 and example waveforms of the line current draw in the low-range and high-range/brownout regimes are shown in Fig. 6.

As illustrated in Fig. 6(a), when the converter is active we draw line current similar to a power factor of one (this is seen experimentally to maximize converter efficiency). Specifically, we regulate a half-wave sinusoidal shape which is truncated by the segmentation described above. The amplitude of this current shape is scaled to regulate the average voltage of the bus to the desired value in a manner similar to the operation of conventional power factor correction converters [24], with the modification that this current draw is automatically cut-off by the segmented operation described above. The controller samples the output voltage every 0.2 ms and the current amplitude scaler is updated every 40 ms based



FIGURE 6. Illustrative line voltage and current waveforms at 50 W. (a) 110 V_{ac} (front-end active). The shaded areas indicate segments where the converter is bypassed in order to avoid lossy regimes of high conversion ratio operation. (b) 240 V_{ac} (front-end bypassed).

on the average output voltage measured in that interval. Note that the input current of the valley-switched boost converter can be computed from the measured input and output voltage, avoiding the need for explicit input current measurement [24].

In high-range (198–265 Vac) and brownout (132–198 Vac) operation, the line current draw is as illustrated in Fig. 6(b).

The boost converter front-end is bypassed and these waveforms are typical of passive rectification with a buffer capacitor: unregulated triangular line current pulses are drawn from the grid when the grid voltage is larger than the bus voltage.

We emphasize that since the application under consideration is not subject to line current harmonic regulations, any desired current waveform can be drawn when the boost converter is active, and this choice can be made to maximize performance. For example, in our preliminary conference publication of [18], line current was controlled in an attempt to minimize bus voltage variation. This was done by updating the boost converter's on-time reference after each sample of the output voltage (every 0.2 ms) in order to steer the output voltage to being instantaneously equal to the desired value, rather than controlling its average value. The result of this operation is a highly distorted line current draw and a bus voltage which is constant over more of the line cycle. This exploratory implementation was rooted in the idea that it may be favourable to keep the second-stage in its highest possible efficiency regime for as much of the line cycle as possible. Further experimentation revealed that the proposed pseudo half-wave sinusoidal draw results in lower overall loss, attributable to more favourable transient boosting conditions and more consistent power throughput over a line cycle. Transitioning from the preliminary line current draw scheme of [18] to that of Fig. 6 a reduced worst case loss by 0.25 W (a 0.5% efficiency improvement).⁹

As a result of this segmented operation, bus voltage ripple will exist even in low-range conditions when the boost converter is active. However, the resulting ripple is well above the minimum bus voltage requirement owing to buffering at voltages near 380 V, and sizing of the capacitor for passive buffering in the worst-case high-range operation.

D. OPERATION IN BROWNOUT CONDITIONS (132–198 VAC)

The specified brownout range is associated with a reduction in voltage when operating in the high-range regime, thus the boost converter remains bypassed. These atypical brownout voltages can be accomodated by reducing power throughput. This has two key consequences: first, as output power is reduced, the LLC quality factor is reduced which increases the maximum achievable gain [20]. Second, the ripple on the bus voltage is reduced due to lower power draw on the bus capacitor when it is disconnected from the grid. Together, these allow the requisite higher gains to be achieved, and operation in this regime is confirmed experimentally in Section VI.

VI. EXPERIMENTAL EVALUATION

The back- and front-end stages of the protoype converter are shown in Figs. 7 and 8, respectively, and the component volumes are listed in Table 6. The net (displacement) volume of the back-end stage, including VIRT transformer, rectifiers,



FIGURE 7. Back-end stacked-bridge LLC+VIRT prototype with a United States dime for scale. The power stage schematic is shown in Fig. 3 and the component values are shown in Table 4. (a) Top. (b) Bottom.



FIGURE 8. Front-end valley-switched boost converter prototype with a United States dime for scale. The power stage schematic is shown in Fig. 4 and the component values are listed in Table 4.

output capacitors, LLC resonant capacitors, and the stackedbridge inverter (including gate-drive circuitry and decoupling capacitors) and balancer is 10 cm³.

Note that we omit the volume of logic and control circuitry in this metric as these represent circuit components that can be miniaturized by other established means, such as implementation in an integrated circuit. Further, similar to prior investigations into two-stage chargers [11], [15], an EMI filter is not considered in this experimental evaluation. We note

⁹Introducing higher order harmonics into this current draw worsened overall efficiency.



TABLE 6. Prototype Component Displacement Volumes

Component	Volume [cm ³]
Isolated dc/dc Stage	
Transformer	5.3
VIRT circuitry and output capacitors	2.5
Stacked-bridge inverter circuitry and by-	2.1
pass capacitors	
LLC resonant capacitors	0.1
Total	10
Front-end Stage	
Power stage components	0.97
Boost inductor	2.3
Buffer capacitors	1.7
Gate driver	0.05
Total	5.02
Line Rectifier	•
Line Rectifier	0.26

only that this filter can be implemented by well-established means [25] and that the relatively high operating frequencies of the converters in this design aid in miniaturization of the EMI filter. However, for this reason and because the prototype itself is not optimally packaged, we avoid quoting a system power density directly. Instead, we present the stages in terms of their component displacement volumes in order to provide insight into the achievable power density of this architecture.

A. EFFICIENCY

The measured ac/dc power-stage efficiency¹⁰ of the prototype (including the loss of the line rectifier) at rated power is shown in Fig. 9(a). These results are obtained under closed-loop control with the front-end (line-interface) stage either bypassed or operated by adjusting the on-time of the boost converter switch in order to regulate the bus voltage while also drawing a line current similar to a power factor of one as discussed in Section V-C, and the back-end (dc/dc stage) adjusting its operating frequency in order to regulate the output voltage to the desired value as discussed in Appendix B. The individual power-stage efficiencies of the front-end and back-end are shown in Figs. 9(b) and 9(c), respectively. The high-range efficiencies in Fig. 9(a) are higher than the low-range efficiencies because the boost converter is bypassed (i.e. switch S_1 in Fig. 4 is held off) and the input current yields lower line rectifier loss at higher input voltages. The limiting condition in terms of overall converter loss is 90 Vac, 12 V/50 W in which 3.1 W loss is generated. If rectifier losses are omitted, the worst-case loss is in the 132 Vac, 12 V/50 W case. This is expected from the drop-off in the front-end efficiency above 145 V in Fig. 9(b). We note that this drop in efficiency does not impact sub-100 Vac operation since the input voltage remains less than 142 V in this regime, and that above this regime the boost converter only partially operates at these less



FIGURE 9. Experimentally measured power-stage efficiencies. (a) ac/dc conversion efficiency. (b) Front-end valley-switched boost converter efficiency at 50 W. (c) Back-end isolated dc/dc converter stage efficiency.

¹⁰Measurements were obtained with a Yokogawa WT1800 power analyzer.



FIGURE 10. Power envelope and ac/dc conversion efficiency under brownout (132–198 Vac) conditions. The percent deviation from nominal 220 Vac is indicated.

efficient operating points. We also note that although there is a drop-off in 5 V/25 W efficiency at 132 Vac in Fig. 9(a), the associated loss of 2.75 W is well below the limiting case of 3.1 W in the 90 Vac 12 V/50 W operating mode, affirming the relative unimportance of this lower power condition on overall converter loss.

The back-end efficiency in Fig. 9(c) is reduced for bus voltages near 190 V, which is expected since here we must operate the LLC well below its resonance, near its maximum gain. We note, however, that the back-end operates in this lower voltage regime only when the front-end boost converter is bypassed. On the other hand, when the boost converter is active, the bus voltage is kept high and the back-end stage is operated with higher efficiency. Thus, these stages operate in a synergistic manner: when the boost converter is active we incur increased loss in the front-end but decreased loss in the back-end; when the boost converter is bypassed, we incur increased loss in the back-end but decreased loss in the front-end. The peak in the 9 V/45 W efficiency around 340 V is associated with the transition from maximally efficient resonant operation to above-resonant operation around that voltage (recall that slightly above-resonant operation is required due to the choice of $N_p = 10$ as discussed in Section V-A).

In the brownout regime (132–198 Vac), the converter is operated with the reduced power profile shown in Fig. 10; also shown is the associated ac/dc conversion efficiency. Efficiency is reduced at lower input voltages due to operation of the LLC converter in its highest gain regime, and the increasing importance of core loss which is maintained under the reduction in power since the voltage level applied to the transformer is constant. The loss associated with worst-case brownout operation is well below the limiting loss in 12 V/50 W operation.

Fig. 11 shows the bus voltage, output voltage, ac line voltage (V_{ac}) and ac line current (I_{ac}) for 90 Vac input, 12 V/50 W output. The boost converter is active in this regime and



FIGURE 11. Low-frequency waveforms for 90 Vac/50 Hz input and 12 V/50 W output: V_{bus} (pink), V_o (green), V_{line} (blue), and I_{line} (cyan). Note that V_{bus} and V_o share the same reference position on the scope, as do V_{line} and I_{line} .



FIGURE 12. Low-frequency waveforms for 198 Vac/50 Hz input and 12 V/50 W output: V_{bus} (pink), V_o (green), I_{line} (cyan), and V_{line} (blue). Note that V_{line} and I_{line} share the same reference position on the scope.

controls for an approximately sinusoidal input current as desired. The bus voltage is regulated to an average of approximately 360 V, with a peak of 380 V and a minimum of 340 V. This keeps the back-end stage well within its high efficiency operating regime (ref. Fig. 9(c)). The output voltage exhibits a low frequency +/-0.25 V ripple around 12 V attributable to the control of the back-end stage as discussed in Appendix B.

Fig. 12 shows the low-frequency waveforms for 198 Vac/50 Hz input and 12 V/50 W output. The boost converter is bypassed and the commonly observed input current associated with a purely passive buffer can be seen. The minimum bus voltage is 190 V with a 16 μ F effective buffer capacitance (accounting for voltage de-rating), sufficient to maintain the bus above this minimum desired voltage. The output voltage again exhibits low frequency ripple, favouring a voltage closer to 11.75 V when the bus voltage is decreasing. However, the output now also has a 0.3 V transient excursion associated with the input current spike and corresponding high-slew charging of the buffer capacitance.



FIGURE 13. Low-frequency waveforms for 90 Vac/50 Hz input and 12 V/50 W output with a 400 V/100 μ F passive buffer: V_{bus} (pink), V_o (green), I_{line} (cyan), and V_{line} (blue). Note that V_{line} and I_{line} share the same reference position on the scope.

B. COMPARISON TO A PASSIVE BUFFER

Section III we noted that a 400 V/100 μ F In B43501A9107M000 electrolytic capacitor could satisfy the bus voltage requirements in the 90 Vac/12 V/50 W case in lieu of an active buffer. Fig. 13 shows the key low-frequency waveforms when operating with this passive buffer in this regime. The corresponding ac/dc conversion efficiency is measured to be 94.1%, representing a 0.3% efficiency improvement over the active buffer case. Although the passive buffer in this case does not incur the loss of the boost converter, the electrolytic capacitor introduces additional loss and the much lower bus voltage keeps the back-end stage in its less efficient operating regime.¹¹ Thus, by employing an active buffer in this application we incur marginal additional loss (an increase in loss of approximately 165 mW or 5.3% over the passive buffer in this limiting case, corresponding to a decrease in efficiency of 0.3%) but are able to reduce overall buffer volume by approximately 59% corresponding to an overall reduction in converter component volume of approximately 32%. This can be an attractive trade-off for miniaturization in portable charger designs.

C. COMPONENT VOLUME AND EFFICIENCY COMPARISON

The converter in this paper is a high output current charger with rated conditions of 12 V/4.17 A, 9 V/5 A, and 5 V/5 A. This is distinct from many charger designs in the literature which accommodate either a single output voltage (e.g. 20 V/45W [26], 20 V/65W [27]) or a wide output voltage of 5 V/3 A, 9 V/3 A, 15/3 A, and 20 V/3A [28], [29]. It is difficult to directly compare chargers in these distinct applications owing to the differences in design that can be leveraged within these specifications. For example, a fixed output voltage design need not worry about accommodating voltage variability, and a 3 A 5-20 V charger has a limiting loss case at 20 V/65 W which can be prioritized for design similar to the manner in which 9 V/45 W and 12 V/50 W operation is prioritized in the proposed design over the 5 V/25 W case. However, the relative component volumes and efficiencies of these different chargers can provide a baseline context for the state-of-the-art in terms of charger miniaturization, and we provide this comparison in Table 7. The proposed converter has relatively high complexity but achieves a high degree of miniaturization, and is presently useful in designs where the volumetric benefit is worth this trade-off.

VII. CONCLUSION

This paper presents a two-stage 50 W charger architecture with a valley-switched boost converter on the front-end and a stacked-bridge LLC+VIRT converter on the back-end. Twostage architectures at this power level are shown to be both viable and advantageous from a component size perspective, owing to the ability to design high-performance miniaturized front-end converters, even in applications with variable voltage and load conditions. The design considerations involved in selecting the bus voltage profile are presented, and a quantitative framework for understanding the trade-off between capacitor buffer volume and second-stage efficiency is discussed. Experimental results demonstrate the efficiency and volume trade-off of the two-stage architecture. Compared to an example low-loss electrolytic capacitor, the active buffer enables a 59% reduction in energy buffer volume corresponding to a 32% reduction in converter component volume at the expense of a 5.3% increase in loss (0.3% reduction in efficiency).

APPENDIX A OVERVIEW OF THE FRONT- AND BACK-END STAGES

This paper focuses on the trade-offs and potential of the proposed two-stage architecture and uses conversion stages which have been explored in detail in the literature [5], [17], [24]. For convenience, this appendix provides an overview of the operation of the front- and back-end stages.

A. FRONT-END STAGE

Example operating waveforms of the valley-switched boost converter obtained for $V_{in} = 70V$ and $V_{out} = 360V$ are shown in Fig. 14. In Stage 1, switch S_1 is on and the inductor current ramps linearly as in a conventional boost converter. This stage remains active until a desired turn-on time is reached, as dictated by the reference value v_{on} in Fig. 4. At this point, S_1 turns off and D_1 turns on, and the inductor current begins to ramp down linearly. When the current reaches zero, Stage 3 is entered in which the device capacitances of D_1 and S_1 resonate with L_1 . If there is sufficient energy in the inductor, v_{sw} will reach zero. At this point, S_1 is turned on with zero volts across it and the cycle repeats. Note that the switching logic in Fig. 4 will maintain the switching sequence automatically. When the sensed switch voltage, $v_{sw,sense}$, is lower than the desired turn-on voltage, v_{ref} , S_1 is turned on.

¹¹Note that the sub-130 V bus voltage ripple in Fig. 13 maps to sub-260 V in the efficiency plot of Fig. 9(c) owing to the use of Mode 1 operation of the inverter in the dc/dc stage instead of Mode 2.

	This Work	[26]	[27]	[28]	[29]
	5W/25W/	201//4511		5V/15W;	5V/15W;
Potod Voltago/Powor	$5\sqrt{25}$		20V/45W 20	20W/65W	9V/27W;
Kateu voltage/10wei	9 V / 45 W,	20 143 1	20 105 1	20V/05W 15V/45W;	15V/45W;
	12 1/30 W			20V/65W	[28][29] $1/15W;$ $5V/15W;$ $1/27W;$ $9V/27W;$ $V/45W;$ $15V/45W;$ $V/65W$ $20V/65W$ $14-0.49$ $0.1-0.22$ Y Y $ac: 93.5\%$ $90Vac: 93\%$ $ac: 94.5\%$ $240Vac: 94.5\%$ 7.8 8.4 10.9 19 18.7 27.4
freq. [MHz]	0.5-2	1	0.9-1.2	0.14-0.49	0.1-0.22
EMI Filter?	N	N	Y	Y	Y
Efficiency at	90Vac: 93.8%	90Vac: 93.1%	90Vac: 92.8%	90Vac: 93.5%	90Vac: 93%
Max Power	240Vac: 95.7%	240Vac: 94.5%	240Vac: 93%	240Vac: 94.5%	240Vac: 94.5%
Buffer Vol. [cm ³]	5.0	6.5	6.5	7.8	8.4
Approx. dc/dc Vol. [cm ³]	10	10	10.5	10.9	19
Buffer plus dc/dc Vol. [cm ³]	15.0	16.5	17.0	18.7	27.4

TABLE 7. Charger Design Comparison



FIGURE 14. Example operating waveforms of the valley-switched boost converter used in the front-end of the proposed two-stage architecture: V_{bus} (pink), V_{in} (blue), i_L (cyan), and v_{sw} (green) (ref. Fig. 4). Note that V_{in} and V_{bus} share the same reference position on the scope. The switching frequency is approximately 580 kHz.

The sensed input- and output voltages are used to compute the input current [24] and the on-time of the switch is set by v_{on} which is controlled in order to regulate the desired input current shape and average output voltage.

In principle, ZVS is achievable when $V_o > 2V_{in}$. However, the non-linear nature of the device capacitances can compromise this relationship. For example, Fig. 15 shows operating waveforms for $V_{in} = 170$ V and $V_{out} = 370$ V. We see that v_{sw} does not reach zero in Stage 3 and instead resonates down to some minimum. Note that the switching logic will not complete Stage 3 until v_{sw} is less than the reference value v_{ref} in Fig. 4. In this example, the controller sets v_{ref} such that Stage 3 ends when v_{sw} is approximately 40 V. Note also that the switching frequency is increased in this lower-gain case compared to Fig. 14.

B. BACK-END STAGE

Example operating waveforms for the LLC+VIRT converter obtained for 12 V/50 W operation with $V_{bus} = 380$ V are



FIGURE 15. Example operating waveforms of the valley-switched boost converter used in the front-end of the proposed two-stage architecture: V_{bus} (pink), V_{in} (blue), i_L (cyan), and v_{sw} (green) (ref. Fig. 4). Note that V_{in} and V_{bus} share the same reference position on the scope. The switching frequency is approximately 1.5 MHz.



FIGURE 16. Example operating waveforms of the LLC+VIRT converter used in the back-end of the proposed two-stage architecture: V_{bus} (blue), V_{inv} (pink), i_{Lr} (cyan), and v_{A1} (black) (ref. Fig. 3). Note that V_{bus} and V_{inv} share the same reference position on the scope. The switching frequency is approximately 800 kHz. Stages 1-3 are labeled.

shown in Fig. 16. The waveforms are typical of LLC operation below resonance.

For 12 V output, the VIRT operates in HB/HB mode in which the half-bridge cells A2 and B2 are bypassed by keeping their low-side switches on and cells A1 and B1 are operated identically (the full-bridge cells "A" and "B" in the schematic of Fig. 3 can be thought of as operating as conventional half-bridge cells). Further, the inductances L_A and L_B effectively operate as a single magnetizing inductance L_M .

At the start of Stage 1, the inverter voltage has just switched to its maximum value, $V_{bus}/2$, and the tank current i_{L_r} begins to increase as C_r and L_r resonate. The high-side switches of A1 and B1 are turned on and current is delivered to the output. When the current through the rectifiers reaches zero, Stage 2 is entered in which the high-side switches of A1 and B1 are turned off and the tank resonance changes as L_M now participates in the resonance. Note that this current does not participate in energy transfer to the output and represents part of the circulating current in the LLC. Stage 2 ends when the inverter is switched. At this point, the circulating current discharges the inverter device capacitances until they reach zero volts, at which point the low-side switches of A1 and B1 are turned on. The half-cycle then repeats in a similar manner except that there is no energy delivered to the output. Note that although V_{inv} switches between $V_{bus}/2$ and 0V, C_r blocks the dc component of this voltage and an effective ac inverter voltage of $\pm V_{bus}/4$ is applied to the tank (this is the voltage quartering gain associated with Mode 2 inverter operation).

The gain of the LLC converter is adjusted by changing the frequency of the inverter voltage. When the operating frequency is equal to the resonant frequency, f_r , set by L_r and C_r , the voltage gain is unity. As the operating frequency is reduced below f_r , the voltage gain increases. This is the case until the frequency is reduced so that it is near the resonant frequency, f_p , set by L_M and C_r , at which point the LLC experiences its maximum gain. ZVS of the inverter switches requires that the frequency of operation be kept higher than f_p . On the other hand, if the operating frequency is increased above f_r , the voltage gain is reduced below unity. In this regime, the rectifiers continue to conduct current when the inverter changes voltage, and less of the energy available in the inductors is available to achieve ZVS of the inverter switches.

The voltage balancer circuit in Fig. 3 is a safeguard against the possibility for voltage imbalance in the stacked input capacitors owing to component or operational mismatch. The balancer capacitors, inverter switches, and diodes form a switched-capacitor network that equalizes the stacked capacitor voltages by moving charge from the higher voltage capacitor to the lower voltage one during each switching cycle. In steady-state, the balancer capacitors and stackedbridge voltages will have a value of $V_{in}/2$. This network processes a relatively small amount of energy in steady-state as it shuffles an incremental amount of charge to ensure that the stacked-capacitors remain equal in value, with the exact energy processed depending on the degree of mismatch between the capacitors.

APPENDIX B LLC CONTROL SCHEME

The LLC is controlled via a hill climbing algorithm which increases or decreases the period by up to 0.5% every 20 μ s in order to regulate the output voltage to the desired value. In

order to avoid oscillations around this value owing to imperfect output voltage sensing, the controller allows for a voltage error of +/-0.2 V in the 5 V and 9 V cases and +/-0.25 V in the 12 V case, representing errors of 4%, 2.2% and 2.1%, respectively. This algorithm is selected for its simplicity and we note that another suitable controller could be implemented as desired.

An additional benefit of the hill climbing algorithm is that it provides a simple framework to actively tune the synchronous rectifiers (SRs) of the back-end stage. These SRs are implemented via MOSFETs which are controlled to mimic diodes, and a loss penalty is incurred for turning off the SRs too early.¹² A conventional approach to this problem, and the one taken in this work, is to program the on-times of the SRs in a look-up table associated with the frequency of operation¹³ [30]. This is straightforward to implement as part of the hill climber.

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¹²In LLC converters, the *turn-on* of the SRs is in phase with the inverter voltage, which is commanded by the governing controller [30]. Thus, the timing of this event is known and special consideration is not required to ensure correct SR turn-on.

¹³An alternative approach to this problem is to use dedicated integrated circuits (ICs) which locally sense the MOSFET voltage to determine turn-on time. However, these ICs are not available for LLCs with MHz switching frequencies at the time of writing.

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