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Light Load Efficiency Improvements in Dual Active Bridge Converters via Dead time Control

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***Abstract*—Many converters suffer from poor efficiency at light loads even though much of their lifetime is spent at lightly loaded conditions. During normal operation, the dual active bridge (DAB) family of converters loses soft switching at low power levels, leading to poor light-load efficiency. In this paper a control approach for DAB converter is investigated that enhances their light-load efficiency via dead time control. A model is developed that captures the relationship between output power and dead time, and is used to formulate a control approach for light-load operation. Experimental results from a prototype converter validate the proposed approach.**

Keywords—power converter, dual active bridge, dead time control, zero voltage switching.

I. Introduction

Modern power converters often have to operate over a wide load range. In many applications, such as computer power supplies, the converter spends a significant part of its lifetime operating at relatively low power levels. Therefore, it is important to improve light load efficiency of power converters to achieve improved overall energy efficiency.

The dual active bridge (DAB) converter, for example, typically suffers from significantly reduced efficiency at light loads. Shown in Fig. 1, the DAB consists of a transformer and two controllable FET bridges [1]. Typically, output regulation is obtained by controlling the phase shift between the inverter and rectifier bridges [1-4]. Under normal (high load) operation this converter can achieve zero voltage switching (ZVS); however, ZVS is only maintained when there is enough energy stored in the leakage inductance to charge and discharge the switch parasitic capacitance during dead time. As output power decreases the DAB loses ZVS, unless one "sloshes" additional power back and forth across the transformer to preserve ZVS [2,5]. The ZVS range (without "power sloshing") can be extended by increasing the transformer magnetizing current, but this is accomplished at the cost of full power efficiency.

Various techniques exist that manipulate dead time of dc-dc converters with the goal of increasing efficiency [4-10]. Some of them require additional components for sensing [6,8] or for energy "sloshing" [2,5]. Additional components adds to the complexity, cost and volume of the converter. Others utilize adaptive techniques where the dead time is adjusted as another variable in the circuit is used to control power delivery (usually phase shift or duty cycle) [7,9].

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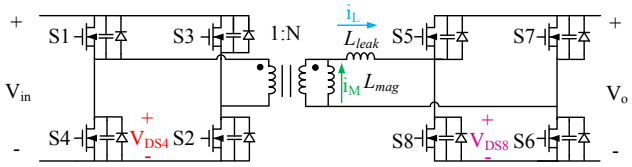

Fig.1. DAB converter schematic. All inductances are referred to the secondary. The FET parasitic capacitances and body diodes are explicitly shown. The colored variables (FET voltages and inductor currents) match the colors of their waveforms in Fig 2.

This paper explores the use of dead time control to improve efficiency in the DAB at light loads, instead of conventional phase shift control. This approach does not sacrifice high load efficiency and requires no hardware changes to the power stage. We show that dead time control can maintain high efficiency even at <10% of output power. While this approach has been proposed before [4], it has only been explored empirically, and a proper model of the output modulation due to variations in dead time (with fixed phase shift) has not been previously developed. Here, we present a general model that can be used for prediction of dead time control characteristics in the DAB and design and control of DAB converters using this approach. We validate the proposed model and control approach with SPICE simulations and with experimental results.

II. Modeling and Control of the DAB Circuit

Fig. 1 shows a typical DAB converter. The load is modeled as a voltage source because it is assumed the converter will operate in closed loop with the output voltage changing only on a time scale that is slow compared to the switching period. By operating the two full bridges in "square-wave" mode and modulating the phase shift ϕ between them, one can control output power. The DAB output power as a function of phase shift can be modeled as [1]:

$$P_O = \frac{N * V_{in} * V_O}{\omega * L_{leak}} * \phi * \left(1 - \frac{abs(\phi)}{\pi}\right) \qquad (1)$$

where ϕ is the phase shift in radians, N is the 1:N turns ratio of the transformer, V_{in} is the input voltage, V_O is the output voltage, ω is the switching frequency in radians/second and L_{leak} is the inductance of the DAB converter including the transformer equivalent leakage inductance referred to the secondary. If there is enough current in the DAB inductor to charge and discharge the switch capacitances, ZVS can be achieved. The minimum current needed is a function of the input and output voltages, switch capacitance and leakage inductance [1]. If the output power is low enough

where the switch current is less than a certain minimum current, the converter will lose ZVS. However, if dead time within the full bridges were increased to give time to discharge the switch capacitances, then ZVS could be recovered. Modulating dead time will also affect output power; thus, it is necessary to understand the effect of dead time both on ZVS and output power control.

One goal of this paper is to find the relationship between the output power and switch dead time in the DAB converter for a fixed phase shift value. As illustrated in Fig. 2, with appropriate (and large) dead times, ZVS operation can be maintained under light-load conditions. Based on this relation, dead time control can be used to modulate output power during light load operation while maintaining high efficiency. As will be seen, the relationship between dead time and output power is complicated, so accurate modeling is valuable in selecting a control law.

The following analysis assumes the circuit is lossless, all leakage is referred to the secondary, the switches have linear capacitance, the transformer magnetizing inductance value is much bigger than the total DAB leakage inductance and $V_{in} * N = V_O$ so that the DAB inductance current is constant outside of the phase shift and dead time periods. Also this analysis assumes that in light load the dead time period of the converter will correspond to a longer duration than the phase shift delay.

The switching cycle of the DAB converter in high dead time operation (light load) can be divided into 8 modes; only 4 will be discussed as the other 4 are symmetric. The relevant modes are shown in detail in Fig. 2. In mode 1 (on-time mode), the switches S1, S2, S5 and S6 are on such that the source delivers direct energy to the load. The voltage across all the FETs is constant, as is the current through the DAB leakage inductance L_{leak}. However the current through the magnetizing inductance L_{mag} is rising linearly. The simplified circuit referred to the transformer secondary is shown in Fig. 3a.

Mode 2 (1st phase shift mode), starts when the inverter side switches S1 and S2 turn off and the source is disconnected from the circuit. The inverting bridge switch capacitances and the leakage and magnetizing inductances form a resonant circuit, shown in Fig. 3b. Here the inverter side capacitances of switches S3 and S4, which sum to a value C_i, start discharging from an initial voltage V_{in} as the transformer and DAB inductances resonate with them. Expressions for the leakage current, magnetizing current and switch capacitances voltages are derived for all 4 modes and are shown in the Appendix. Mode 2 leakage current is equation (A.1), magnetizing current is (A.2) and switch capacitance voltage is (A.3). Mode 2 lasts for the phase shift time set by the controller.

Mode 3 (dead time mode) starts when the rectifying bridge switches S5 and S6 turn off and the load is also disconnected from the circuit. The net inverter capacitance C_i, rectifier capacitance C_o, leakage inductance and magnetizing inductance form a resonant circuit (shown in Fig. 3c) that has two resonant frequencies: one "fast" resonance between the capacitors and the leakage inductance and another "slow" resonance between the

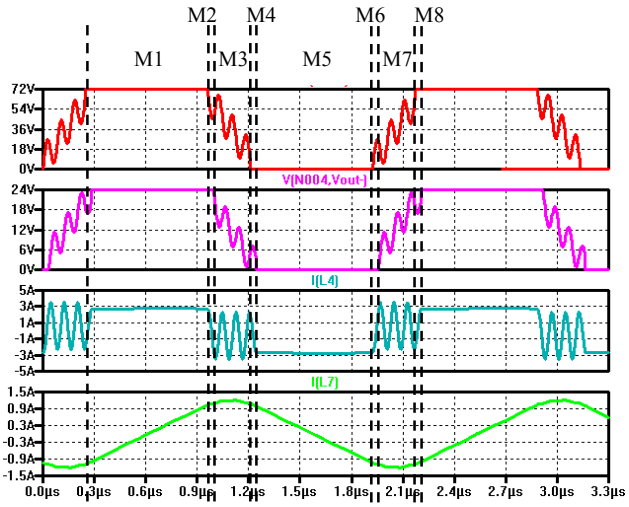

Fig. 2. SPICE simulation time domain waveforms of the DAB converter operating with high dead time. From the top: inverter FET S4 voltage, rectifier FET S8 voltage, leakage current referred to secondary, and magnetizing current referred to secondary. All 8 modes are shown.

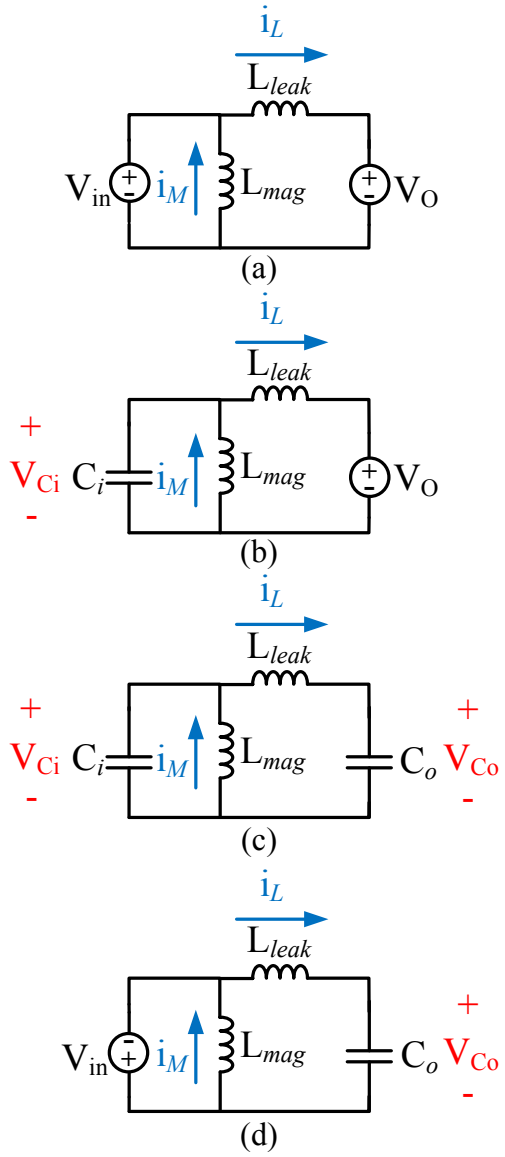

Fig. 3. Simplified, equivalent resonant circuits for, top to bottom: (a) mode 1, (b) mode 2, (c) mode 3 and (d) mode 4.

capacitors and the magnetizing inductance. The "fast" resonant frequency can be approximated as:

$$f_{leak,m3} = \frac{1}{2\pi\sqrt{L_{leak} * \left(\frac{C_i * C_O}{C_i + C_O}\right)}} \quad (2)$$

where C_i is the equivalent inverter capacitance referred to the secondary and C_o is the equivalent rectifier capacitance. The "slow" resonant frequency can be approximated as:

$$f_{mag,m3} = \frac{1}{2\pi\sqrt{L_{mag} * (C_i + C_O)}} \quad (3)$$

The magnetizing current can be considered nearly constant during this mode and helps ring down the switch capacitance voltage for ZVS turn on of the incoming switches if given enough time, as can be seen in Fig 2. The equations for this mode are: leakage current (A.5), magnetizing current (A.6), inverter capacitance voltage (A.7) and rectifier capacitance voltage (A.8). Mode 3 lasts for the switch dead time minus the phase shift time.

Mode 4 (2nd phase shift) starts when the inverter side switches S3 and S4 turn on and connect the source in the opposite polarity than in Mode 1. A new resonant circuit is formed between the leakage and magnetizing inductances and the rectifier capacitance, shown in Fig. 3d. The equations for this mode are: leakage current (A.10), magnetizing current (A.11) and rectifier capacitance voltage (A.12). This mode lasts for the phase shift time value set in the controller.

The load current is the same as the leakage inductance current during modes 1 and 5 (on-time modes) and approximately zero for all other times. During dead time periods, no current flows to the output. The output power can be approximated by finding the average current delivered to the load:

$$I_{O,avg} = \frac{\left(\frac{1}{f_s} - 2 * \left(t_{ps} + t_{dt}\right)\right)}{\frac{1}{f_s}} * I_{L,SS} \quad (4)$$

$$P_{O,avg} = V_O * I_{O,avg} \quad (5)$$

where f_s is the converter switching frequency in hertz, t_{ps} is the phase shift time in seconds, t_{dt} is the switch dead time and $I_{L,SS}$ is the value of constant leakage inductor current in mode 1. By finding $I_{L,SS}$, one can use (4) and (5) to find the output power.

There are 4 unknowns in the equations describing the timings (found in the Appendix): the initial values of inductor currents and capacitor voltages at the start of mode 2 ($I_{L,SS}$, $I_{M,ini,2}$, $V_{ci,ini,2}$, and $V_{co,ini,3}$). The inverter and rectifier capacitor initial voltage values ($V_{ci,ini,2}$ and $V_{co,ini,3}$) are set by the input and output voltages, respectively. The magnetizing current at the beginning of mode 2 can be approximated by:

$$I_{M,ini,2} = \frac{V_{in} * N}{L_{mag}} * \left(\frac{1}{2 * f_s} - t_{dt} - t_{ps}\right) \quad (6)$$

This equation approximates the magnetizing current at the beginning of mode 2 as being half of the peak-to-peak swing in the current over the duration in which constant voltage is applied across it by the input voltage.

A final equation is needed to finally solve for $I_{L,SS}$. In periodic steady state, the current in the leakage inductor at the beginning of mode 2 has to be equal in magnitude but opposite in sign to the current at the end of mode 4. This can be seen in the 3rd pane in Fig. 2. In equation form:

$$I_{L,ini}(0) = I_{L,SS} = -I_{L,ini}\left(t_{dt} + t_{ps}\right) \quad (7).$$

Using these equations, one can develop a model of the circuit. An analytical solution for output power vs dead time is not possible, but a numerical solution can be useful. The numerical model is solved in a piece-wise fashion using the time duration of the different modes as intervals described by different sets of equations. Equations A.1, A.2 and A.3 are used to describe the circuit variables over a time t_{ps} (mode 2 duration). The final values of mode 2 are used as the initial values of mode 3, which has duration $t_{dt} - t_{ps}$ and uses equations A.5 through A.8. In turn the final values of mode 3 are used as the initial conditions of mode 4, which also has duration t_{ps} and uses equations A.10, A.11 and A.12. All initial conditions of mode 2 are known except for $I_{L,SS}$. This variable can be kept through the numerical solutions and at the end solved for using (7). The output power can be calculated using (4) and (5). A Matlab script was used here to readily evaluate all the computations. By arranging a sweep of dead time values t_{dt}, one can generate a plot such as the one on Fig. 4.

Using this model, the output power can be calculated as a function of dead time for a given DAB circuit with the following inputs: switch capacitances, leakage and magnetizing inductance, input and output voltages, switching frequency and phase shift time value.

Figure 4 shows a comparison of the model developed here to an LT SPICE simulation. The simulation and the model are in very good agreement.

In the following section, the numerical model is compared to experimental results.

III. Experimental Verification

The DAB converter used for experimental verification of the model is seen in Fig. 5. It is a two-input, single-output design that has been employed at the core of a high-power-density, high-frequency power factor correction converter [3]. Here we use the converter as a simple DAB converter. This converter's transformer has two primaries and one secondary, and the inverter on each primary is a half bridge inverter. Nevertheless, this converter can be reduced to the simplified circuits shown in Fig. 3 and thus can be described accurately with the model developed here. There are minor changes in how to calculate the net values of switch capacitance, net inductance referred to the secondary, etc. but the model is useful if the mode transitions happen as described above. For the circuit in Fig. 5, both input voltages are identical (the input ports are

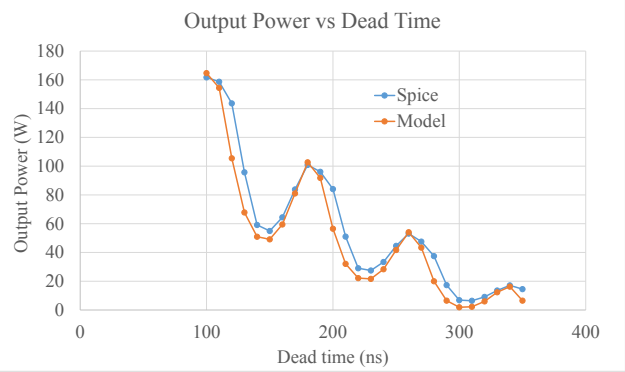

Fig. 4. Output power vs dead time plot. This plot compares the numerical model developed here to a SPICE simulation at the same operating points. Simulation parameters and operating point: 72 V input, 24 V output, N=1/3, fs=520 kHz, phase shift = 30 ns, L_{leak}= 82.07 nH, L_{mag}=8020.7 nH, rated power of 250 W, inverter total switch capacitance C_i=3735 pF, and rectifier total switch capacitance C_o=4100 pF (all capacitance and inductance values are referred to secondary). These capacitances are representative of using EPC2016C devices for the inverter and EPC2024 devices for the rectifier.

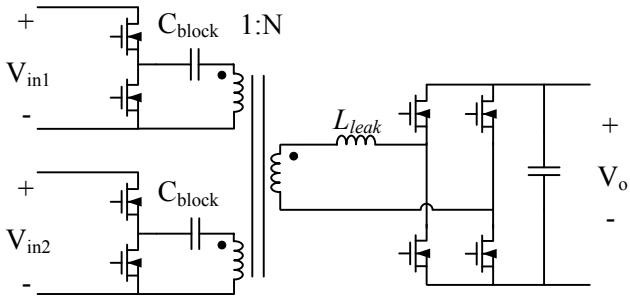

Fig. 5. DAB converter used for experimental verification of the model [3]. This converter has two primaries and a half bridge inverter on each primary. The components used can be found in Table 1.

Table 1. DAB converter part list. The schematic is found in Fig.5

Part	Description	Parameters
Inverter FETs	EPC2016C	Coss = ~220 pF
Rectifier FETs	2x EPC2024	Coss = ~2050 pF
Transformer	core: DMR51 2x E22; turns: 3 on primary, 2 on secondary; wire: 1000/48 Litz on each winding;	leakage inductance= ~50 nH, magnetizing inductance = ~8 uH, (all referred to secondary) 3:2 turns ratio
External leakage inductors on inverter side	core: 1 rod core 3061990871 from Fair-Rite split in two; turns: 5 wire: 1000/48 Litz	Primary external leakage 1 = ~280 nH Primary external leakage 2 = ~260 nH

connected in parallel in the experiments) and the blocking cap has negligible ripple on it (effectively acting as a dc

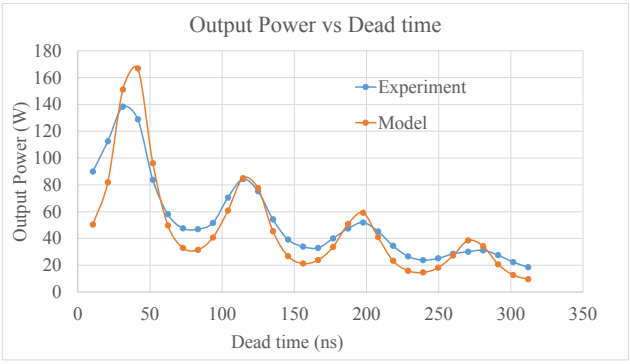

Fig. 6. Output power vs dead time plot. This plot compares the experimental results to the model. The switching frequency is 1 MHz, the phase shift is fixed at 10 ns, the input voltage is 72 V, output voltage is 24 V, and rated power of 250 W for both experiment and model. Additional circuit parameters (for model) and parts list (for experiment) are found in Table 1.

offset in the model which can be easily accounted for). The two primaries and the secondary are wound around the center leg, sharing the same flux. The two primaries can be effectively seen as two identical circuits in parallel when referred to the secondary.

The model can be easily adapted to this DAB variant with minor corrections. Table 1 shows the components list of the converter used to gather experimental data. The converter rated power is 250 W.

Figure 6 shows data that compares the model developed here to experimental results. In these experiments the converter is operated at a switching frequency of 1 MHz and at a phase shift of 10 ns. Contrary to "normal" DAB operation, phase shift is held constant and output power is modulated using dead time as described in the introduction.

IV. Improvements in Light Load Efficiency

Operating with high dead time significantly increases light load efficiency, as is shown experimentally in [4], and also applied in our earlier work [5]. Figure 7 shows experimental results of efficiency vs output power for our prototype DAB converter of Fig. 5 using phase shift control and dead time control. Our results show that by increasing dead time the FET capacitors are allowed to losslessly charge and discharge which mitigates switching loss, which is a main loss mechanism (along with transformer core loss) at light loads, while enabling power control. Figure 8 shows an experimental waveform of the drain voltage. Although it is not always possible to achieve true ZVS for a given output power, the turn-on voltage of the switch can be reduced significantly.

From Fig. 6 we can see that there are multiple dead times that can provide the same output power; from simulation and empirical results it was found that the most efficient dead time for a given output power is the highest dead time. A high dead time allows for maximum charge/discharge of the switch capacitance (reducing switching loss) and yields minimal volts-seconds applied to the transformer (reducing transformer core loss).

An efficient control algorithm is to use phase shift control with a small, fixed dead time down to some load

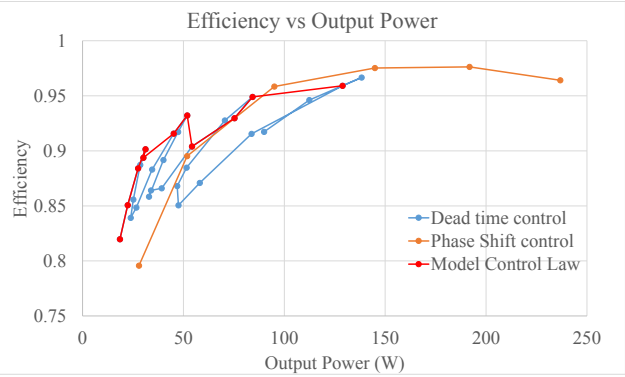

Fig. 7. Efficiency vs output power plot for different control methods; experimental data. This plot shows the efficiency of the converter when controlled by typical phase shift modulation (orange), by sweeping dead time up to about 30% of period (blue), and by following the dead times predicted by the model (red). It can be seen that one can smoothly control power with improved efficiency using the model-predicted controls. The operating conditions and circuit parameters are the same as in Fig 6.

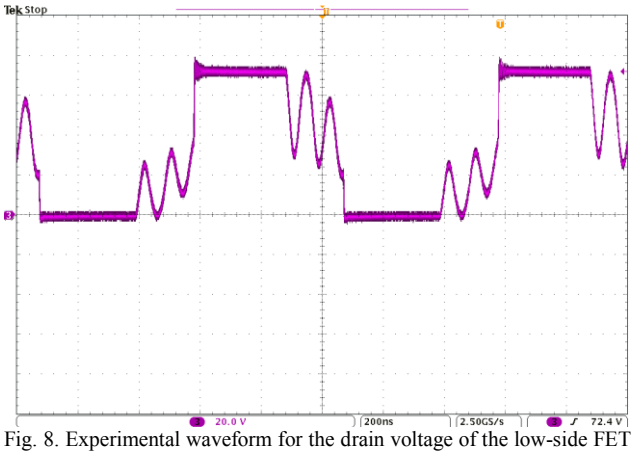

Fig. 8. Experimental waveform for the drain voltage of the low-side FET in the top inverter in Fig. 5. This particular operating point shows a reduction of 10 V in the turn-on voltage across the switch when compared to turning on at the bottom of the first "valley". Operating point: input voltage= 72 V, output voltage = 24 V, output power = 48 W, phase shift time = 10 ns, and dead time = 185 ns.

boundary (~40% in our example), and to modulate dead time at fixed phase shift time at lighter loads. The desired effect of the capacitors reaching ZVS or near ZVS occurs only when the dead time is bigger than the phase shift time. For the example converter used in these experiments, phase shift is fixed at 10 ns and dead time is modulated from 52 ns (~33% load) to 300 ns (~8% load).

An effective way to use dead time control is to program the controller to jump between dead time "sections" to maximize efficiency for a given power level. These operating "sections" of dead time are selected based on being the highest dead time for a given power level. The numerical model can be used to rapidly create an output power vs dead time curve (such as the one in Fig. 6) and graphically select the regions of dead time for efficient operation for a given power level. An example of the way to select the dead time regions of interest is shown in Fig. 9. Figure 7 also shows the efficiency vs output power curve for this converter if operated in the regions selected using this method. The efficiency is improved greatly compared to the standard phase shift control method. At around 25 W (10% load), efficiency is improved about ~9%. However there are a few areas where the model captures a suboptimal

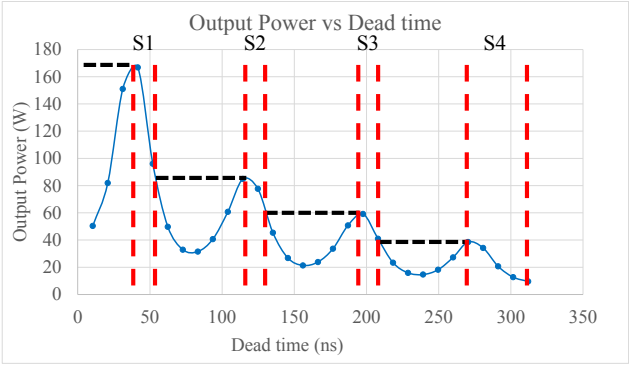

Fig. 9. Output power vs dead time plot created using the model (a repeat of the one shown in Fig. 6). Here the graphical method used to select the operating dead times sections is shown. The sections are divided into S1 to S4. These sections are selected based on the highest dead time for a given amount of output power. S1 can deliver between 165 W to 85 W using the dead times between 35 ns and 60 ns; S2 can deliver between 85 W to 60 W by modulating dead time between 110 ns and 130 ns, S3 can deliver between 60 W to 40 W by utilizing dead times between 190 ns and 210 ns; S4 can deliver between 40 W to ~10 W by using dead times between 270 ns to 310 ns. As seen on this plot, these sections are quasi-linear and can provide a reliable control handle.

operating point. This inaccuracies in the model are very likely due to non-linear capacitance of the FETs and magnetic component losses which are phenomena not captured in the model. The inaccuracies of the model can be corrected by using empirical data on a given converter. Nevertheless, this model is useful for predicting the behavior of the output power as dead time is modulated, and gives the designer the tools to rapidly determine how changing a parameter in the circuits affects said relation. Of note is that this algorithm increases light load efficiency without any increases in component count, circuit complexity, volume or cost.

V. Conclusion

In this work a numerical model is developed for the DAB converter that captures the relationship between dead time and output power. This enables a dead-time control scheme to be rapidly synthesized. It is further found that at light loads efficiency is improved if dead time is used as a control variable instead of phase shift for values of dead times much higher than the phase shift. A control algorithm is proposed that increases light load efficiency. The proposed approach is verified in simulation and experiment. The model matches SPICE simulations extremely well, and provides a good first-pass prediction for dead time control rules. Absolute accuracy is limited owing to device capacitance nonlinearity and other factors, suggesting that adjustment of the dead time control law rule based on experimental results is useful.

VI. Appendix

Here the set of equations that compose the numerical model are derived. The equations consists of the inductor currents and capacitor voltages in each of modes 2, 3 and 4. The complete circuit is solved numerically by matching the initial conditions of one mode to the final conditions of the previous one. The circuit analyzed for mode 2 operation

is shown in Fig. 3(b). The leakage inductor current, magnetizing inductor current and inverter capacitance voltage are:

$$I_{L,m2} = -\frac{V_O}{L_{leak}} * t \; + \; \frac{V_O}{L_{leak}} * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) * t \; + \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) * (\cos(\omega_{m2} * t) - 1) \; + \frac{1}{\omega_{m2} * L_{leak}} * \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * sin(\omega_{m2} * t) + I_{L,SS} \quad (\boldsymbol{A.1})$$

$$I_{M,m2} = \frac{V_O}{L_{mag}+L_{leak}} * t - \left(\frac{L_{leak}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) + \left(\frac{L_{leak}}{L_{mag}+L_{leak}}\right) * \left(I_{L,SS} + I_{M,ini,2}\right) * \cos(\omega_{m2} * t) + \frac{1}{\omega_{m2} * L_{mag}} * \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * sin(\omega_{m2} * t) + I_{M,ini,2} \quad (\boldsymbol{A.2})$$

$$V_{ci,m2} = V_{in} * N - V_{ci,ini,2} + V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right) + \left(V_{ci,ini,2} - V_O * \left(\frac{L_{mag}}{L_{mag}+L_{leak}}\right)\right) * cos(\omega_{m2} * t) - \left(\frac{L_{mag} * L_{leak}}{L_{mag}+L_{leak}}\right) * \omega_{m2} * \left(I_{L,SS} + I_{M,ini,2}\right) * sin(\omega_{m2} * t) \quad (\boldsymbol{A.3})$$

where L_{mag} is the magnetizing inductance, L_{leak} is the leakage inductance, $I_{L,SS}$ is the leakage current at the beginning this mode (initial value), $I_{M,ini,2}$ is the magnetizing current at the beginning of this mode (initial value), $V_{ci,ini,2}$ is the inverter capacitance voltage at the beginning of this mode (initial value), and ω_{m2} is the resonance frequency of the mode 2 circuit defined as:

$$\omega_{m2} = \frac{1}{\sqrt{C_i * \left(\frac{L_{mag} * L_{leak}}{L_{mag} + L_{leak}}\right)}} \quad (\boldsymbol{A.4})$$

where C_i is the inverter capacitance. The equations that describe mode 3 (with equivalent circuit shown in Fig. 3(c)) are:

$$I_{L,m3} = V_{dc,caps} * \left(\omega_{leak,m3} * C_i - \frac{1}{\omega_{leak,m3} * L_{mag}}\right) * sin(\omega_{leak,m3} * t) + \left(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{C_i} + \frac{I_{M,ini,3}}{C_i+C_o}\right) * \left(\frac{1}{(\omega_{leak,m3})^2 * L_{mag}} - C_i\right) * \cos(\omega_{leak,m3} * t) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * \left(\omega_{mag,m3} * C_i - \frac{1}{\omega_{mag,m3} * L_{mag}}\right) * sin(\omega_{mag,m3} * t) + \left(-L_{mag} * I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{(\omega_{leak,m3})^2 * C_i} - \frac{I_{M,ini,3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \left(\omega_{mag,m3}\right)^2 * C_i\right) * \cos(\omega_{mag,m3} * t) \quad (\boldsymbol{A.5})$$

$$I_{M,m3} = I_{M,ini,3} + \frac{V_{dc,caps}}{\omega_{leak,m3} * L_{mag}} * sin(\omega_{leak,m3} * t) + \left(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{(\omega_{leak,m3})^2 * C_i} + \frac{I_{M,ini,3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \frac{\cos(\omega_{leak,m3} * t)}{L_{mag}}\right) + \frac{(V_{ci,ini,3} - V_{dc,caps})}{\omega_{mag,m3} * L_{mag}} * sin(\omega_{mag,m3} * t) + \left(-L_{mag} * I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{(\omega_{leak,m3})^2 * C_i} - \frac{I_{M,ini,3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * \left(\frac{1}{L_{mag}} - \frac{cos(\omega_{mag,m3} * t)}{L_{mag}}\right) \quad (\boldsymbol{A.6})$$

$$V_{ci,m3} = V_{dc,caps} * \cos(\omega_{leak,m3} * t) + \left(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{\omega_{leak,m3} * C_i} + \frac{I_{M,ini,3}}{\omega_{leak,m3} * (C_i+C_o)}\right) * \sin(\omega_{leak,m3} * t) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * cos(\omega_{mag,m3} * t) + \left(-\omega_{mag,m3} * L_{mag} * I_{M,ini,3} + \frac{(I_{L,ini,3}+I_{M,ini,3}) * \omega_{mag,m3}}{(\omega_{leak,m3})^2 * C_i} - \frac{I_{M,ini,3} * \omega_{mag,m3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * sin(\omega_{mag,m3} * t) \quad (\boldsymbol{A.7})$$

$$V_{co,m3} = V_{dc,caps} * \cos(\omega_{leak,m3} * t) + \left(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{\omega_{leak,m3} * C_i} + \frac{I_{M,ini,3}}{\omega_{leak,m3} * (C_i+C_o)}\right) * \sin(\omega_{leak,m3} * t) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * cos(\omega_{mag,m3} * t) + \left(-\omega_{mag,m3} * L_{mag} * I_{M,ini,3} + \frac{(I_{L,ini,3}+I_{M,ini,3}) * \omega_{mag,m3}}{(\omega_{leak,m3})^2 * C_i} - \frac{I_{M,ini,3} * \omega_{mag,m3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * sin(\omega_{mag,m3} * t) - L_{leak} * \left(V_{dc,caps} * \left(\left(\omega_{leak,m3}\right)^2 * C_i - \frac{1}{L_{mag}}\right) * \cos(\omega_{leak,m3} * t) - \left(\frac{-(I_{L,ini,3}+I_{M,ini,3})}{C_i} + \frac{I_{M,ini,3}}{C_i+C_o}\right) * \left(\frac{1}{\omega_{leak,m3} * L_{mag}} - \omega_{leak,m3} * C_i\right) * \sin(\omega_{leak,m3} * t) + \left(V_{ci,ini,3} - V_{dc,caps}\right) * \left(\left(\omega_{mag,m3}\right)^2 * C_i - \frac{1}{L_{mag}}\right) * cos(\omega_{mag,m3} * t) - \left(-L_{mag} * \; I_{M,ini,3} + \frac{I_{L,ini,3}+I_{M,ini,3}}{(\omega_{leak,m3})^2 * C_i} - \frac{I_{M,ini,3}}{(\omega_{leak,m3})^2 * (C_i+C_o)}\right) * \left(\frac{\omega_{mag,m3}}{L_{mag}} - \left(\omega_{mag,m3}\right)^3 * C_i\right) * \sin(\omega_{mag,m3} * t)\right) \quad (\boldsymbol{A.8})$$

where $I_{M,ini,3}$ is the magnetizing current at the beginning of this mode (initial value), $I_{L,ini}$ is the leakage current at the beginning of this mode (initial value), $V_{ci,ini,3}$ is the inverter capacitance voltage at the beginning of this mode (initial value), C_o is the capacitance of the rectifier FETs, $\omega_{leak,m3}$ is the resonant frequency of the capacitors and leakage inductance in radians and it is defined in (2) in hertz, and $\omega_{mag,m3}$ is the resonant frequency of the capacitors and magnetizing inductance in radians and it is defined in (3) in hertz; finally $V_{dc,caps}$ is defined as:

$$V_{dc,caps} = \left(\frac{C_O}{C_i + C_O}\right) * \left(V_{ci,ini,3} - V_{co,ini,3}\right) \quad (\boldsymbol{A.9})$$

where $V_{co,ini,3}$ is the rectifier capacitance voltage at the beginning of this mode (initial value).

The equations that describe mode 4 (with equivalent circuit shown in Fig. 3(d)) are:

$$I_{L,m4} = -\omega_{m4} * C_O * \left(V_{in} * N + V_{Co,ini,4}\right) * \sin(\omega_{m4} * t) + \; I_{L,ini,4} * \cos(\omega_{m4} * t) \quad (\boldsymbol{A.10})$$

$$I_{M,m4} = -\frac{V_{in} * N}{L_{mag}} * t + I_{M,ini,4} \quad (\boldsymbol{A.11})$$

$$V_{co,m4} = \left(V_{in} * N + V_{Co,ini,4}\right) * \cos(\omega_{m4} * t) + L_{leak} * \omega_{m4} * I_{L,ini,4} * \sin(\omega_{m4} * t) - V_{in} * N \qquad (\boldsymbol{A.12})$$

where the "ini" values are the initial conditions of this mode, and ω_{m4} is defined as:

$$\omega_{m4} = \frac{1}{\sqrt{L_{leak} * (C_O)}} \qquad (\boldsymbol{A.13})$$

VII. REFERENCES

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