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Energy and Size Reduction of Grid-Interfaced Energy Buffers Through Line Waveform Control

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***Abstract*—Grid-interface converters with power factor correction (PFC) generally require large energy buffer capacitors to maintain a constant power output. These buffer capacitors can occupy 20-30 % of total system volume, and their size is unaffected by typical methods of miniaturizing power converters such as increasing efficiency or changing switching frequency. Here we investigate an approach in which harmonic current is intentionally drawn from the grid (within allowed regulations) to reduce the required energy storage. We show that this method can achieve up to a 62 % reduction in energy storage requirements under EN61000-3-2 Class D regulations, with continued benefit available at higher powers under Class A. This benefit can generally be achieved solely through controls without additional hardware and can be applied across PFC converter topologies. A valley-switched boost PFC converter is used to validate that harmonic injection achieves the calculated energy storage reduction with little impact on efficiency. It is also shown that the proposed approach provides the added benefit of compressing the PFC switching frequency range.**

I. Introduction

Grid-interface converters are often required to provide power factor correction (PFC) [1] wherein they draw current having strictly limited harmonic content and with a fundamental component in phase with the input voltage. The ideal unity power factor case (PF = 1) having perfectly sinusoidal currents in phase with the grid voltage leads to a pulsating power waveform ($\propto \sin^2$) with very large instantaneous variations about the constant power required by typical loads. The converter must buffer this twice-line-frequency power pulsation, and the resulting low frequency energy storage $E_{store} = P_o/\omega_{grid}$ is necessarily very large. This storage is typically achieved with electrolytic capacitors, which have low lifetime and can occupy over 50 % of PFC converter volume [2] (20-30 % of overall system volume).

Energy buffer capacitors are stubbornly immune to typical miniaturization approaches when $PF = 1$ because the energy storage requirement is fixed by factors outside of the circuit designer's control – the power rating of the converter and the frequency of the grid. In other words, the energy storage requirement is not a function of efficiency, topology, architecture, or switching frequency [3].

Some research has observed that the usable energy storage depends on both the buffer capacitance and its voltage swing

$$E_{store} = \frac{1}{2}CV_{peak}^2 - \frac{1}{2}CV_{trough}^2 = CV_{avg}\Delta V \qquad (1)$$

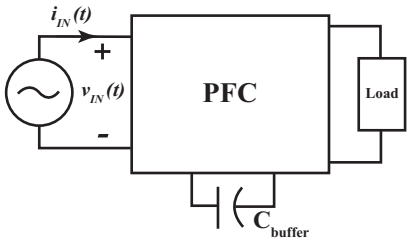

Fig. 1. Three-terminal representation for power converter with PFC, including input from grid source, dc output to load, and ac buffer capacitor.

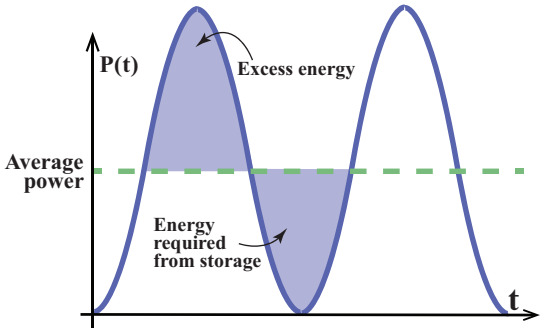

Fig. 2. When PF = 1, power oscillates $\propto \sin^2$; integrating over time relative to average (desired) power gives energy storage requirement over a line cycle, shown as shaded.

and have used high voltage swings to permit lower capacitance. Entire converters (sometimes called active buffers) have been designed to emulate a large capacitor while taking advantage of this observation [4]–[7]. These approaches have largely been successful, but suffer primarily from added component counts while still buffering the same amount of energy.

Here we investigate an alternative approach which fundamentally reduces the amount of twice-line-frequency energy that needs to be stored.[1] It accomplishes this by purposefully drawing small amounts of harmonic current, resulting in a more constant input power and therefore less required energy

[1] Some uninterruptible applications (e.g. servers) impose an additional hold-up time requirement wherein the converter must maintain its output power for some duration (e.g. one line cycle) in the event of a voltage interruption. This requirement may dwarf the twice-line-cycle energy buffering requirement and such converters may be unaffected by the proposed technique. Nevertheless, the proposed approach has broad applicability in charger, adapter, appliance, and motor drive applications which have no hold-up time requirement.

TABLE I
EN61000-3-2 CLASS D & CLASS A LIMITS ON ODD HARMONICS

n-th Harmonic	Class D Limit (mA/W)	Class A Absolute Maximum (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	$3.85/n$	0.21
$15 \leq n \leq 39$	$3.85/n$	$0.15 * 15/n$

storage. While operating within EN61000-3-2 line current regulations, this method can reduce energy storage requirements – and consequently energy buffer size – by up to 62 % (in Class D). This approach usually requires no additional hardware and can be applied to many existing PFC converters solely by a change in controls.

Energy storage reduction has been explored before, mainly in the context of LED drivers which fall under EN61000-3-2 Class C regulations [8]–[15], but this method has not thoroughly been explored in other classes which are sometimes thought to have substantially stricter regulations [16].[2] Here we show that this approach maintains substantial benefit for devices operated under Class D and Class A regulations, well into the kilowatt range.

In addition, the side effects introduced by this approach (e.g. loss, frequency variation, etc.) have not been explored previously but are investigated here. In particular, we investigate a valley-switched boost PFC both theoretically and with a hardware prototype. For this implementation, we find negligible variation in loss by introducing harmonic input current. We also find a beneficial compression in the operating frequency range (from 4:1 to 1.4:1 for a given average power), which alleviates some of the challenges with using high-efficiency, variable-frequency converters like the valley-switched boost, resonant converters, etc.

II. THE IDEAL CASE: NO BUFFER

If we first imagine our goal is to eliminate the need for an energy buffer entirely, in the absence of regulations or notions of power factor, then we would need to draw constant power from the grid, implying that:

$$i_{in,C=0}(t) = \frac{P_{out}}{V_{in}} \frac{1}{\sin(\omega t)}. \qquad (2)$$

where P_{out} is the dc output power of the PFC stage and V_{in} is the ac line voltage amplitude.

When drawing such a current, since there would be no instantaneous mismatch in power, the energy buffer size could be reduced by 100 % (i.e. no buffer). Undoubtedly, this is not a feasible current to draw, as it clearly violates harmonic limits (Table I) and requires infinite current at zero-crossings of the grid voltage, as illustrated in Fig. 3. Nevertheless, we can take inspiration from this approach and analyze the harmonic content of $i_{in,C=0}$ which is composed of an infinite, equally weighted sum of all odd harmonics of the fundamental line frequency.

$$\frac{1}{\sin(\omega t)} = 2\Big(\sin(\omega t) + \sin(3\omega t) + \sin(5\omega t) + ...\Big) \qquad (3)$$

One interpretation of (3) is that intentionally drawing harmonic currents can be used to reduce the energy buffer size. While we may not achieve a 100 % reduction in energy buffer size, we can draw a subset of current harmonics, with weights limited by regulations, and achieve some (indeed much) of the same benefit.

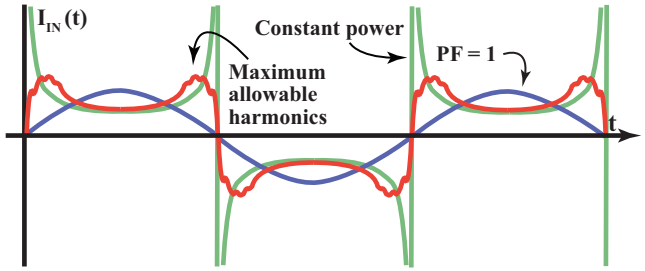

Fig. 3. Input current waveforms for PF = 1 (blue), zero-buffer solution (green), and maximum Class D harmonic current (red). The maximum harmonic current waveform closely approximates the zero-buffer current for a large portion of line cycle.

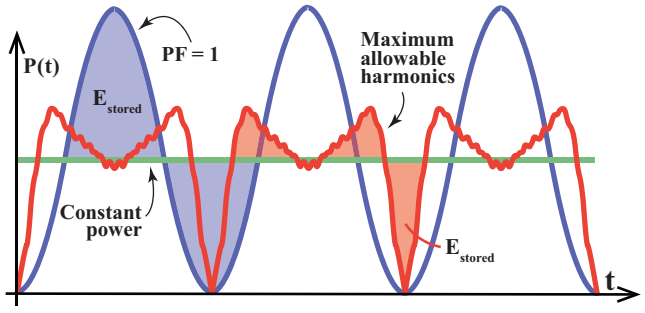

Fig. 4. The energy storage requirement when using maximum allowable Class D harmonics (shaded area,red) is significantly decreased from the energy storage required at PF = 1 (shaded area,blue).

III. OPERATING AT REGULATION LIMITS

To appreciate the limits that regulations impose on this approach, consider the EN61000-3-2 Class D requirements [20], which apply to devices in the 75-600 W power range, governing all odd harmonics to the 39th. These current limits are expressed in terms of device power ($\mathrm{mA_{rms}/W}$), with decreasing amplitudes for higher order harmonics (Table I). Beyond 600 W, most devices fall under the Class A regulation,

[2]Exceptions include [17], [18] which only consider Class D and [19] which considers all classes but with limited harmonic inclusion.

which imposes constant limits on all odd harmonic components, independent of device power.[3]

There are infinitely many ways to incorporate harmonic current across a many-dimensional space. To constrain the problem, we chose two approaches: first, by introducing all governed harmonics together in equal percentages p of their individual maximum allowable values; and second, by introducing each harmonic individually to its maximum before introducing the next. Both methods are investigated numerically.

The former method allows us to observe what happens in the most extreme case of utilizing the maximum of every regulated harmonic within the EN61000-3-2 regulations. Let the input current be

$$i_{in}(t) = I_1 \sin(\omega t) + I_3 \sin(3\omega t) + \ldots + I_{39} \sin(39\omega t) \quad (4)$$

where, in Class D, each coefficient is proportional to the regulated limit $I_{reg,n}$ (mA/W) and to the output power:

$$I_n = \sqrt{2}(I_{reg,n} \times p) P_{out}. \quad (5)$$

By increasing the percentage p of all harmonics, the energy storage requirement monotonically decreases (Fig. 5), yielding up to a 62 % decrease in the energy storage requirement at $p = 1$. This can be seen geometrically in Fig. 3, where the current approximates (2) and in Fig. 4 where the shaded energy storage area is clearly reduced.

While using the maximum allowable amount of of each harmonic current yields the largest drop in storage, it is an undeniably difficult function to generate reliably without violating regulations. Fortunately, as described below, it is still possible to benefit from the majority of these storage savings by only incorporating third and fifth harmonic terms.

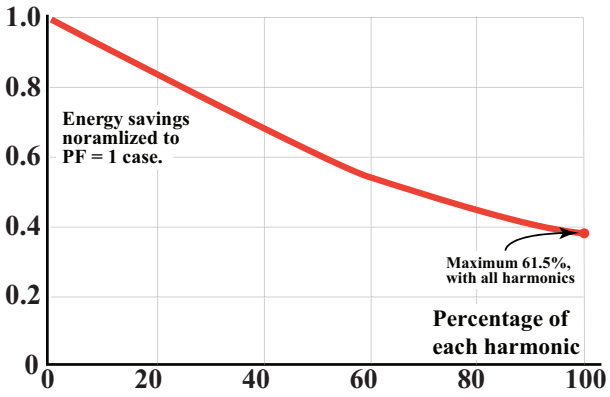

Fig. 5. Energy storage requirement as all harmonics are included at the same percentage p of their individual allowed maxima under Class D. By including all every available harmonic, the energy storage requirement can be reduced by nearly 62 %

[3]Class A also governs even harmonics, but systems with power electronic front ends typically have half-wave-symmetric input currents which have no even harmonics. Even harmonics are also not useful for energy storage reduction, and are not considered further.

IV. Incorporating Harmonics Sequentially

Instead of drawing all harmonics in equal proportion to their individual maxima, we can instead include one harmonic at a time. Let us start by drawing only third harmonic current,

$$i_{in}(t) = I_1 \sin(\omega t) + I_3 \sin(3\omega t). \quad (6)$$

as shown in Fig. 6 where I_3 is varied from 0-100 % of its allowed maximum value in class D.

With the inclusion of I_3, observe that the resulting input power begins to approximate the input power of Fig. 4, with reduced peak power and more constant power overall.[4]

By adding I_3 we observe a significant impact on energy storage (Fig. 7), even when operating well within the allowable Class D harmonic limits. Introducing the third harmonic component alone can yield up to a 44 % improvement in the storage requirement, which is two-thirds of the maximum possible reduction under Class D.

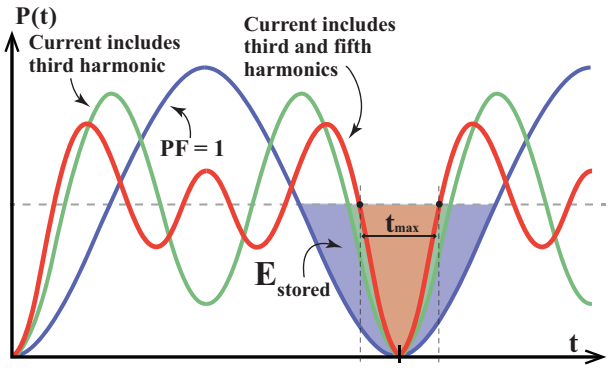

Fig. 6. Introducing the maximum allowed third harmonic reduces the central peak (blue) and divides it into smaller peaks (green); introducing fifth harmonic further corrects the extremities (red). Shaded regions correspond to time of maximum capacitor depletion (e.g. t_{max} of line cycle using fifth harmonic), and corresponds to required energy storage.

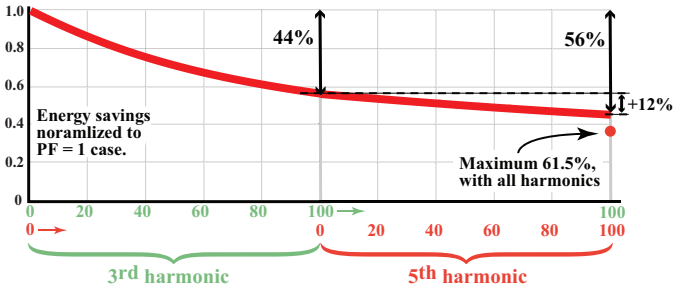

Fig. 7. Reduction in energy storage requirement by incorporating third harmonic current up to its regulation limit, then adding fifth harmonic up to its limit. These two harmonics contribute substantially towards the maximum achievable energy storage reduction.

[4]As we increase I_3 beyond 65 % of its maximum allowable value, the input power at high voltage falls below the constant desired output. This area should not be included in the integral to calculate energy storage requirements, as the minor ΔV associated with this time does not affect the overall peak-to-peak ripple voltage on the energy buffer capacitor.

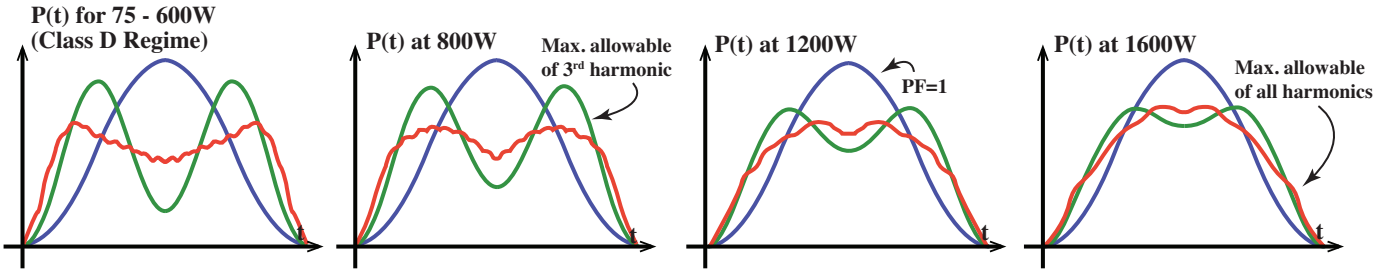

Fig. 8. Power waveforms when including all available harmonic currents are identical across the 75 W-600 W Class D range. Beyond 600 W (in Class A), the benefits brought by harmonic currents diminishes as their relative weight to the fundamental decreases. Still, this method yields up to a 35 % reduction in energy storage at 1600 W.

Once we have included 100 % of $I_{reg,3}$, we can further improve the result by incorporating incremental amounts of a new fifth harmonic term

$$i_{in}(t) = I_1 \sin(\omega t) + I_{3,max} \sin(3\omega t) + I_5 \sin(5\omega t). \quad (7)$$

The energy storage requirement continues to decrease (Fig. 7) although the additional energy savings are much less substantial. Maximizing the fifth harmonic contributes an additional 12 % reduction to the storage requirement, significantly less than the third harmonic. The same logic applies to each successive harmonic, each having less impact on overall energy storage due to the tighter limits on higher-order harmonic currents (e.g. introducing the maximum seventh harmonic contributes an additional 4 % reduction to the storage requirement).

V. Impact Across Power

The previous discussion was based on Class D requirements, which apply up for devices up to 600 W. Because Class D harmonic limits scale with power, the results are largely the same across the entire range.[5]

Beyond 600 W, devices are governed by Class A regulations, which define maximum permissible harmonic current values independent of power. As power is increased, the allowed harmonics become smaller relative to the fundamental and we observe (Fig. 9) that the power waveform with maximum harmonic content begins to recede toward the PF = 1 shape . This trend obviously decreases the available benefit from harmonic inclusion at higher powers, but the benefit is still substantial well into the kilowatt range. Indeed, at 1600 W, roughly half of the Class D energy storage reduction from harmonic inclusion is still available (≈ 35 % reduction).

VI. Impact on Losses

Although reducing energy buffer size can be an important gain for power density, the increased current drawn is not free and the side effects of using harmonic current have not been thoroughly explored in the literature. Since this approach can

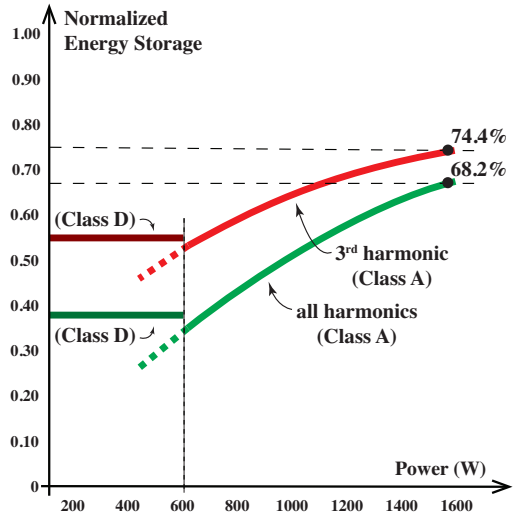

Fig. 9. Class D regulation limits do not seamlessly transition into their Class A maxima at 600 W, hence the discontinuity in achievable energy storage at this boundary. Almost two-thirds of the possible energy storage reduction across a wide range of power can be achieved through the 3rd harmonic alone.

be applied independent of the converter topology, one cannot quantify the exact impacts on system loss without considering detailed design, but we can attempt to model which converter components or stages will be affected and how.

Adding harmonic content increases the rms and average rectified current at the input. Resistive losses will grow $\propto i_{rms}^2$, while diode losses are approximately proportional to their average currents. Adding harmonics will increase both of these metrics without increasing output power, lowering efficiency.

Nevertheless, not all components are affected equally, or at all, and loss reductions may also accrue in some cases.[6] As an example, consider a two-stage architecture with an input diode bridge, dc-side EMI filter, boost PFC stage, energy buffer capacitor holding approximately constant voltage, and a subsequent isolated dc/dc step-down stage, as in Fig. 10.

By drawing additional harmonic current at the input, the diode bridge and EMI filter will see increased average and

[5]The results are identical for devices operating at or below 584W. At 584W, the higher-order 15th-39th harmonics reach the Class D absolute limits on maximum permissible harmonic current. This has negligible impact on the available energy storage savings, as high-order harmonics are already tightly regulated.

[6]For example, switching frequency range compression may be achieved which can be used to reduce skin/proximity effect losses, core losses, and frequency-dependent semiconductor losses like dynamic R_{on} and losses in C_{oss} capacitance [21]–[23].

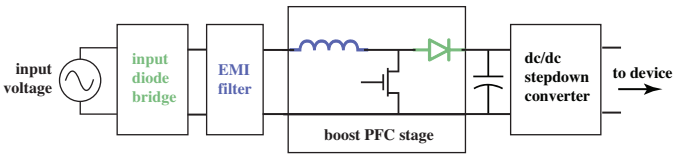

Fig. 10. The two-stage converter with boost PFC is a very popular grid-interface architecture. For this example, incorporating input current harmonics may negatively impact losses in the diode bridge, EMI filter, and boost inductor, should not affect the boost diode or dc/dc step-down converter, and may improve losses in the buffer capacitor and boost switch.

rms currents, increasing their loss. These losses extend to the boost inductor of the PFC, but not to all PFC stage components. Since the PFC output voltage is approximately constant in this example, the PCF output current tracks the power waveform in Fig. 4 which has the same average value regardless of harmonic content. Since $i_{D,ave} = i_{out,ave}$, it can be reasonably argued that the boost diode losses should be largely unaffected by drawing harmonic input current. Additionally, the output current actually has a lower rms value when the input harmonics are included and the boost switch conduction losses may even improve (although they remain also functions of duty cycle).

The energy buffer capacitor sees reduced rms currents and therefore reduced esr losses. Even if capacitance is reduced to maintain the same voltage ripple (and therefore esr is increased), the loss $P_{esr} = I_{C,rms}^2 R_{esr}$ is still reduced.

Finally, downstream elements (in this example, the dc/dc step-down stage) should be entirely unaffected by the inclusion of input harmonics. Thus, only "input facing" components see additional losses by introducing input harmonic content.

We can begin to model the increased losses in affected components by examining the mean-square and average rectified input currents when utilizing all harmonic currents together (Fig. 11), subject to Class D regulations. Logically, the largest mean-square and average rectified input currents correspond to the largest harmonic currents. The same pattern is observed when only the third harmonic is included (Fig. 12). While currents and associated losses do increase, they may be a small fraction of overall loss. In addition, because losses and energy storage do not vary linearly, effective compromises are available. For example, incorporating $40\,\%$ of the third harmonic alone grants nearly $30\,\%$ decrease in energy storage (in Class D) with a very small impact on the rms and average rectified input current metrics.

VII. Hardware Validation

Many PFC implementations can draw input currents with specified harmonics. Indeed, one benefit of this approach is its versatility across topologies without requiring additional hardware. Nevertheless, as a concrete example, we implemented a valley-switched boost PFC, with controls as described in [24] (Table II).

The converter was operated at constant power and adjustable harmonic content, with third and fifth harmonics included up to the same percentage p of their individual allowed Class D

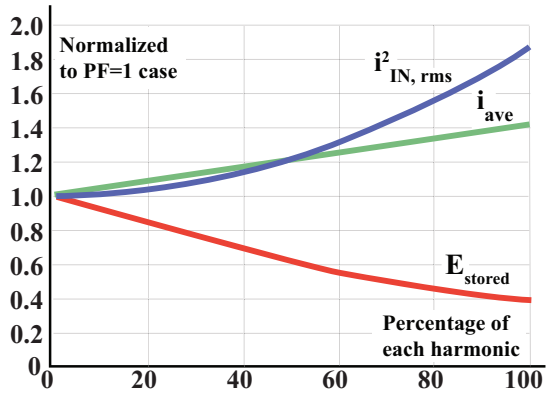

Fig. 11. Increases in $i_{in,ave}$ and $i_{in,rms}$ for a given energy storage reduction goal when using all allowable harmonic currents at equal percentages relative to their EN61000-3-2 limits.

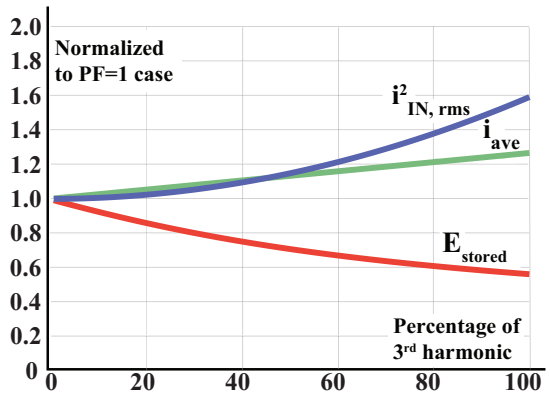

Fig. 12. Increases in $i_{in,ave}$ and $i_{in,rms}$ for a given energy storage reduction goal when using only allowable third harmonic.

TABLE II
Prototype Details for All Experiments

$V_{in,rms}$	220 V
$V_{out,ave}$	400 V
Power	250 W
Efficiency	96 % (see Fig. 17)
Boost Inductance	116 µH
Buffer Capacitors	10 µF × 10
Buffer Capacitor PN	Nichion UCY2H100MHD1TO
Boost Diode PN	C3D1P7060Q (SiC)
Boost FET PN	GS66506T (GaN)

maxima. Fig. 13 shows a series of oscilloscope captures for the specifications in Table II where p is increased and the peak-to-peak amplitude of the output voltage ripple decreases (recall from (1) that, for constant average bus voltage, energy storage is directly proportional to voltage ripple ΔV). The measured output voltage ripples are plotted Fig. 14, normalized to the ripple expected in PF = 1 conditions. The calculated reduction in energy storage is also plotted, and matches to within measurement precision.

The capacitor size is limited by the allowed output voltage

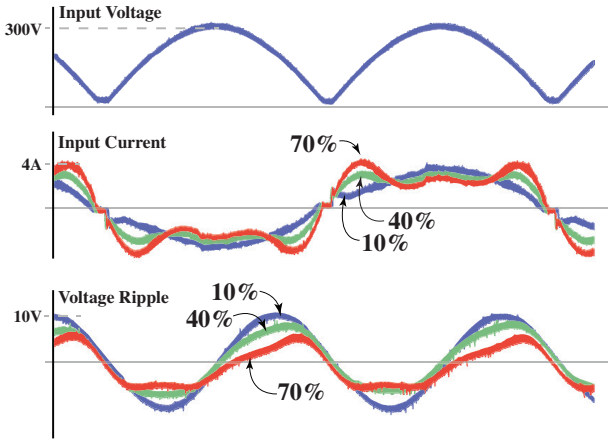

Fig. 13. Experimental input voltage, input current, and output voltage ripple for 10 % (blue), 40 % (yellow), and 70 % (purple) of the allowed 3rd and 5th harmonic. The output voltage ripple decreases for fixed capacitance, as expected; the original voltage ripple could be restored with less capacitance and improved power density.

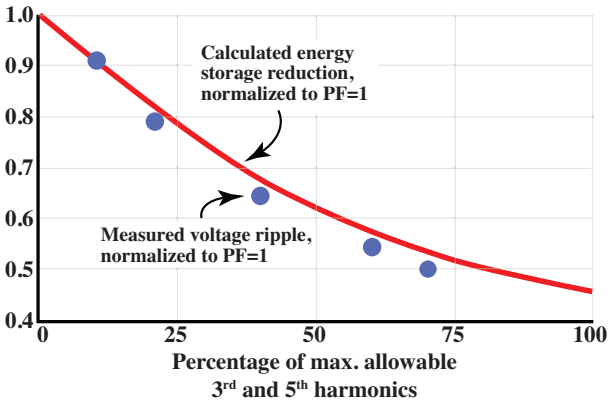

Fig. 14. Experimental output voltage ripple, normalized to the PF = 1 case, showing a close match to theory.

ripple, so any decrease in voltage ripple for a specific power can also be interpreted as an available reduction in bus capacitance. Therefore, with modest amounts of third and fifth harmonics alone, the bus capacitor can be reduced by upwards of 50 %. This is verified in Figs. 15-16, where the converter is operated with output capacitance $C = 100\,\mu\text{F}$ and low harmonic content, and also with $C/2 = 50\,\mu\text{F}$ output capacitance and high harmonic content. It can be seen that 1) the reduced voltage ripple from Fig. 14 can be translated into a capacitance reduction instead, and 2) that the impact on system volume is substantial (in this example, about a $1/3$ reduction in PFC volume).

We also measured system losses for varying amounts of harmonic currents,[7] plotted in Fig. 17. When introducing up to 70% of maximum allowable amounts of third and fifth harmonic currents, entire system losses across the input

[7]When measuring efficiency with input harmonics, it is important to remember that the real power into the system with no phase shift is $I_{1,rms} \times V_{rms}$, not $I_{rms} \times V_{rms}$.

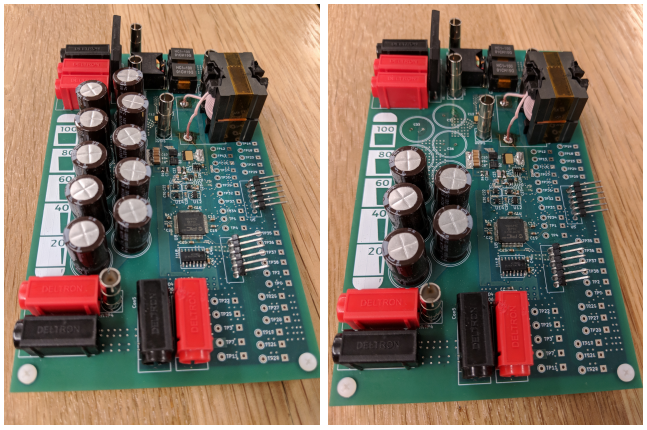

Fig. 15. Photograph of prototype PFC showing the available buffer size reduction when introducing 70 % of third and fifth harmonic Class D limits with constant output ripple. The capacitor reduction matches theory, and is a major improvement to the system power density.

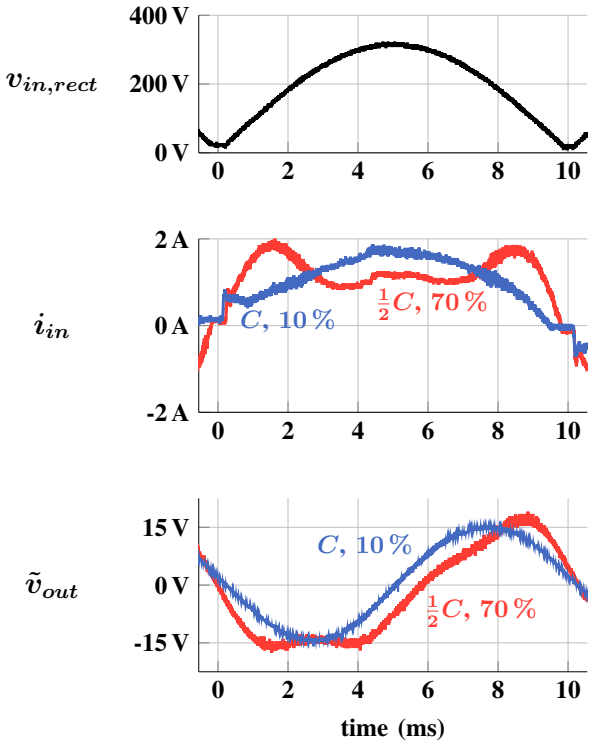

Fig. 16. Comparison of output voltage ripple when harmonics are included (10 % vs 70 % of the allowable third and fifth harmonics) and capacitance is reduced. The reduced voltage ripple of about 50 % in Fig. 14 is traded for 50 % less capacitance.

diode bridge, EMI filter, and PFC stage remained well within 10 % of the losses otherwise incurred by operating at perfect power factor. This is likely due to the converter being heavily dominated by losses in the boost diode which is not expected to change with harmonic inclusion. This is verified thermally in Fig. 18.

Additionally, incorporating harmonic content introduces new benefits to the converter's switching frequency. Fig. 19

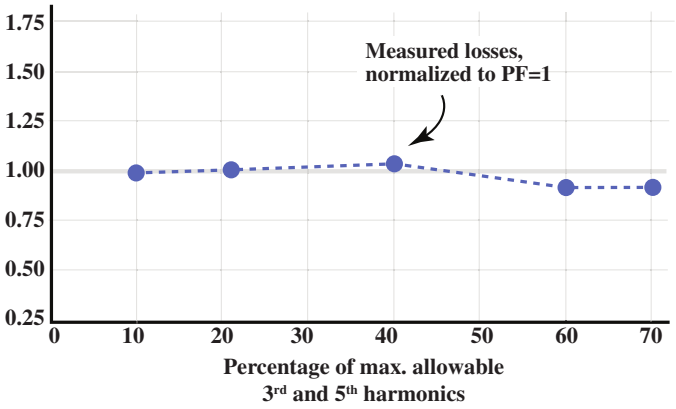

Fig. 17. Measured converter losses, normalized to the low-harmonic case (10 % harmonic usage, 96 % efficiency). In this prototype, which is dominated by diode losses, including significant harmonic content has negligible effect on efficiency.

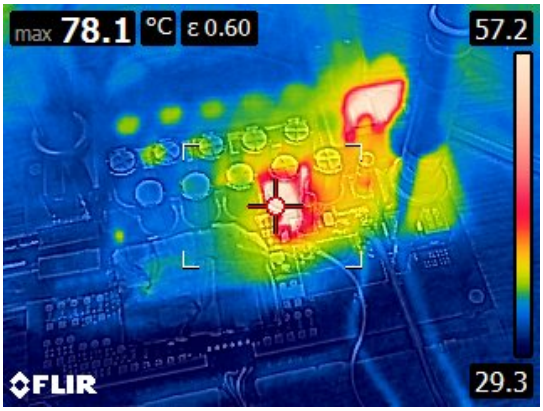

Fig. 18. Thermal capture of the converter operating with 70 % of allowable harmonics, showing that diode losses (which are harmonic-independent) dominate in this prototype. The hot spot in the center is the boost diode, and the hot spot in the upper right is the diode bridge.

shows the measured converter switching frequency, across the rising half of each line half-cycle for different amounts of harmonic input current. In sinusoidal current (PF $\approx$ 1) operation, the switching frequency of the example boost PFC varies from 200 kHz at high line to almost 800 kHz at low line. When harmonics are introduced, more current is drawn at low line which reduces the switching frequency (this will generally hold for most variable-frequency converters). Indeed, when the example converter operates with approximately 50 % of the third and fifth harmonics allowed in Class D, the switching frequency variation is reduced to 250 kHz to 300 kHz, or a ratio of 1.4:1. This compression has a variety of benefits, including for EMI filter and magnetic component design and for avoiding dynamic R_{on} and C_{oss} loss penalties. Indeed, by suppressing the highest operating frequencies, the inclusion of harmonics may improve the loss in the boost inductor, which may contribute to the flat loss characteristic in Fig. 17.

Overall, the prototype demonstrates many of the benefits (and costs) of purposefully drawing higher order harmonic currents discussed earlier. While drawing many harmonics

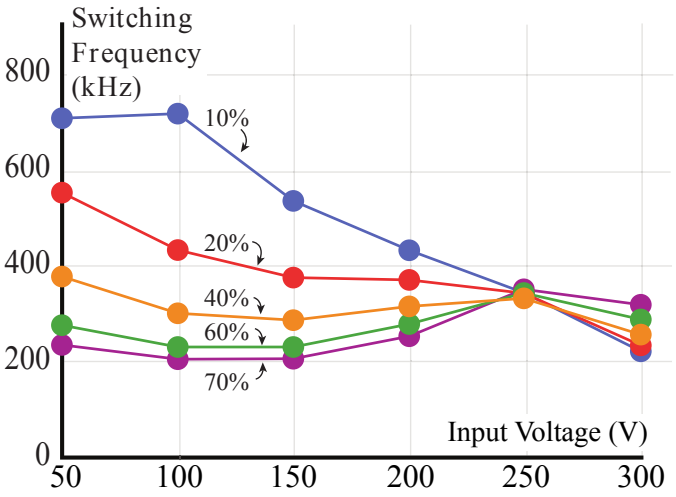

Fig. 19. Local operating frequency of the valley-switched boost PFC across the first half of the rectified input voltage half-cycle. The variable frequency introduced by the valley-switched boost is greatly mitigated with the inclusion of input harmonics, by drawing more current at low voltage.

offers the greatest volume reduction, by using only third and fifth harmonics one can achieve a substantial amount of that reduction while still operating well within harmonic limits. Variable frequencies may beneficially have their ranges compressed, and additional losses may be reasonable and/or partially compensated.

VIII. Conclusion

As increased efficiency and switching frequency improve the size of other components of ac/dc converters, energy buffers become more of a bottleneck to miniaturization. By intentionally drawing currents at harmonics of the grid voltage, designers can greatly reduce the energy that must be stored each cycle, and therefore significantly reduce the size of energy buffer capacitors. Energy buffer capacitors for Class D devices can be reduced by 62 %, with significant reductions for those of Class A devices even at kilowatt-rated powers. In most cases, this technique is available with a change of controls only, which is an important advantage over other techniques for cost-constrained applications. We presented a prototype which validates the results without incurring a significant efficiency penalty.

Looking forward, we note that there is nothing fundamentally incompatible between this approach and others that aim for high voltage ripple or use “active buffers” to reduce the buffer size (e.g. [4]–[7]). The benefits available from each approach are compoundable, such that a 50 % energy buffer reduction from each approach should reduce the buffer to 25 % of its original volume.

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