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Series diode balancing and diode evaluation for high-voltage high-frequency power converters

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***Abstract*—Miniaturization of high voltage power converters is severely limited by the availability of fast-switching, low-loss high-voltage diodes. This paper explores techniques for using discrete low-voltage diodes in series as one high voltage diode. We identify that when series connecting diodes, the parasitic capacitance from the physical diode interconnections to common can result in voltage and temperature imbalance among the diodes, along with increased loss. We quantify the imbalance and propose two related compensation techniques. To validate the approaches, a full-bridge rectifier is tested with each branch consisting of four 3.3 kV SiC diodes in series. Experimental results showcase the imbalance and demonstrate the effectiveness of the compensation techniques. Additionally, we characterize the performance of a range of diodes for use in high-frequency, high-voltage converters. The proposed technique and evaluation results will be valuable for the design of lightweight and miniaturized high voltage power converters.**

I. Introduction

Applications such as electro-aerodynamic propulsion, portable X-ray machines, small-scale electrostatic precipitators, and others have stimulated the need for lightweight and miniaturized high voltage power converters [1]–[8]. This motivates the increased switching frequencies to the high hundreds of kHz and MHz range. One of the bottlenecks to achieving high frequency while preserving high efficiency is the lack of low-loss high-voltage diodes capable of operation at high frequency [3], [9]. Si Schottky diodes are appealing in high frequency applications but they are mostly rated below $250\,\mathrm{V}$ [10]; commercially available Silicon Carbide (SiC) diodes exhibit low loss and can block up to $3.3\,\mathrm{kV}$; however, above $5\,\mathrm{kV}$, the only presently affordable and available diodes are Si high-voltage diodes [10].

To better explore the range of diodes that might be useful in such applications, we have tested a range of diodes (from $400\,\mathrm{V}$ to $15\,\mathrm{kV}$) in a full-bridge rectifier topology at $600\,\mathrm{kHz}$. Most of the tested Si high voltage diodes are not suitable for operation at or above $600\,\mathrm{kHz}$ at even a fraction of their rated outputs without heat sinks. Nonetheless, low voltage ultrafast diodes ($400\,\mathrm{V}$ to $800\,\mathrm{V}$) and SiC Schottky diodes ($650\,\mathrm{V}$ to $3.3\,\mathrm{kV}$) are promising candidates for building high-voltage, high-frequency systems. The evaluation methods and results will be explained in details in Section II.

One can use such high-frequency, low-loss low-voltage diodes in various ways to achieve a high-voltage output. One can (1): have multiple transformer windings that are separately rectified, with the rectified outputs stacked in series (e.g., [2], [6], [11]); (2): Use the diodes in voltage multiplying rectifier topologies (e.g., [3], [7], [12]–[14]); and/or (3): Series connect discrete low-voltage diodes to construct an approximate equivalent to a high-voltage diode (e.g., [15]).

Each method has limitations: the losses of a voltage multiplier increase drastically with the number of stages [13], [16]. The complexity (and often-times the loss) of a transformer increases with more secondaries as does its nonideality of operation, especially when high insulation levels are needed between outputs. Series connection of devices leads to questions about how the individual devices actually act, and the impact on their voltage sharing during the off-state and their losses owing to switching and conduction.

This paper explores design considerations in the use of series-connected low-voltage diodes as a single high voltage diode for high-frequency applications. We observe that there are off-state serious voltage and temperature imbalance issues that can arise when series-connecting such diodes. We present a theoretical model showing that significant voltage imbalance and loss differences can be caused by parasitic capacitances of the diode interconnection points to common.

The paper also describes two related compensation techniques to mitigate voltage imbalance and increased loss owing to these interconnect capacitances. The proposed compensation techniques function by adding external low-loss capacitors to restore voltage balance and reduce diode losses. We present analytical solutions as well as theoretical limitations of these compensation techniques. We present experimental results using four $3.3\,\mathrm{kV}$ diodes to form a high-voltage diode, showcasing the voltage/temperature imbalance issue as well as demonstrating the effectiveness of the compensation technique. The compensation capacitors can be further integrated into the PCB design, thus can enable the design of ultra-lightweight high voltage rectifiers.

Section II explains the diode evaluation tests and the results. Section III presents the theoretical model for series-connected discrete diodes and the voltage imbalance issue. Section IV explains the compensation techniques and their limitations. Section V presents the experimental results, both showcasing the imbalance issue as well as the effectiveness of one version of the proposed compensation techniques for improving system performance. Section VI concludes the paper.

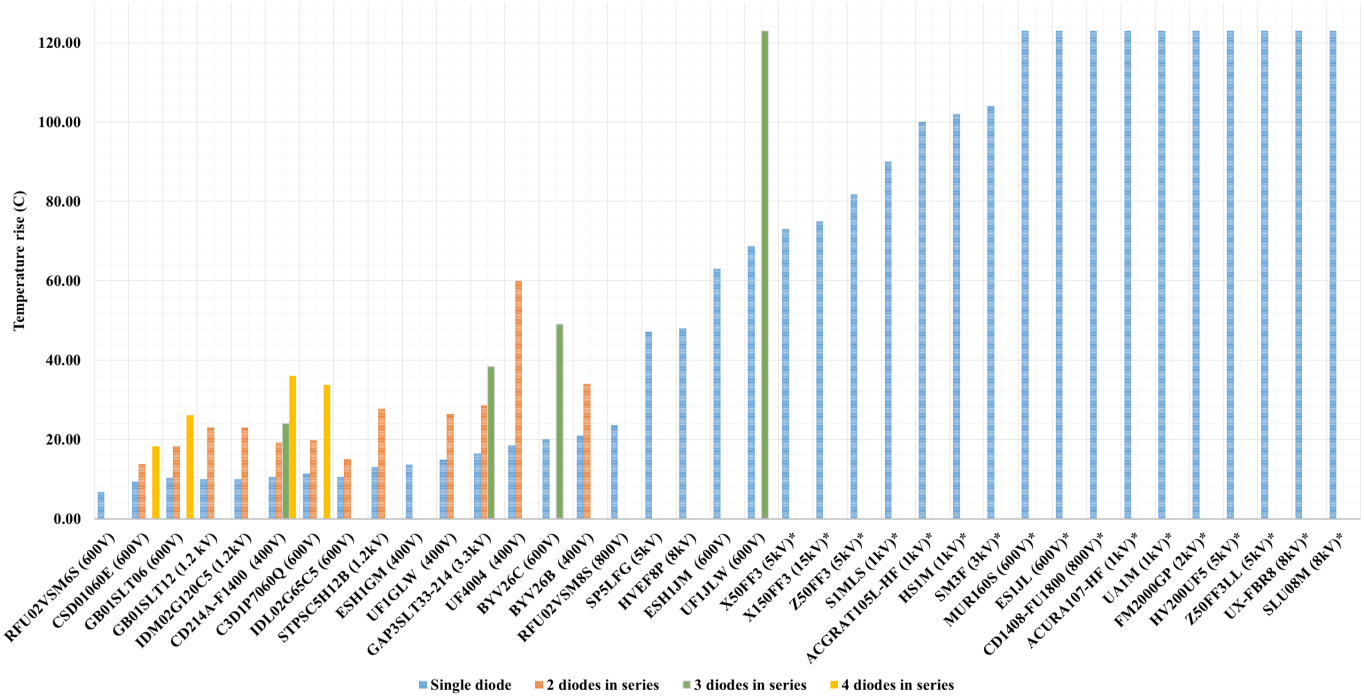


Figure 1: Temperature rise of each diode when rectifying a 600 kHz ac waveform in a full-bridge rectifier topology. Each leg of the rectifier can be a single diode, or a few diodes in series. Each leg blocks ∼50 % of its rated voltage and carries ∼10 % to 20 % of its rated current. Diodes with asterisk did not reach thermal equilibrium before the temperature became too high; all other diodes were tested for 10 min to reach the thermal equilibrium. The specifications of all diodes and the conditions of all tests are listed in Table. I in the Appendix. We group diodes with similar sizes together and use three PCBs to conduct the tests: RFU02VSM6S, RFU02VSM8S, ESH1GM and ESH1JM are grouped together; diodes blocking 5 kV to 15 kV are grouped together; all other diodes are grouped together. Within each group, the thermal path of the PCB layout is the same.

II. Evaluation of High Voltage Diodes

High-voltage Si diodes present higher losses compared with their low voltage counterparts. The conventional ways to boost the blocking voltage (e.g. multi-junction, single deep-diffused junction, or glass passivated) also raise the forward voltage of the diode, proportionally increasing the conduction losses. As the off-state voltage increases, the switching losses tend to increase rapidly. In addition, higher blocking voltage introduces larger leakage current [17], resulting in more severe heating thus even worse tolerance of losses [18].

SiC diodes have shown to have higher performance (e.g., shorter recovery times and lower reverse leakage currents) than Si diodes with comparable breakdown voltages [19], [20]. They have promise for replacing Si devices in the kV range.

In order to identify suitable diodes operating at high voltage and high frequency (>500 kHz), we have tested and compared 37 off-the-shelf diodes, including ultrafast recovery Si diodes, SiC Schottky diodes and Si high voltage diodes. The blocking voltages of these diodes range from 400 V to 15 kV, and their forward currents range from 30 mA to 5 A.

The evaluation process is as follow:

- AC tests: all diodes are tested in a full-bridge rectifier topology. Each leg of the rectifier can comprise a single diode or multiple diodes in series. We drive the rectifier with a resonant inverter and a transformer at 600 kHz, such that the rectified dc voltage is at roughly 50 % of the rated voltage of each leg and the rectified dc current is roughly 10 % to 20 % of the rated current of the diode. All tests are done with no cooling. We record the maximum temperature rise after the rectifier reaches thermal equilibrium. The specifications of all diodes and the conditions of all tests are listed in Table. I.
- DC tests: for diodes that perform well in the AC tests, we drive the same full-bridge rectifier with a dc source at various voltages and currents. We again record the maximum temperature rise in each test after the rectifier reaches thermal equilibrium. A mapping between maximum temperature rise and power loss can be generated based on these tests.
- Loss mapping: we map the temperature rise in an AC test with a specific loss by interpolating on the temperature to loss map from the DC tests.

Results in Fig. 1 reveal that several low voltage ultrafast diodes (400 V to 800 V) and SiC Schottky diodes (650 V to 3.3 kV) show significantly lower temperature rises compared with most Si high voltage diodes (3 kV to 15 kV). For diodes with a temperature rise lower than 50 °C, we characterize the losses using DC tests, as shown in Appendix A Fig. 13.

However, when connecting these diodes in series, Fig. 1 also suggests that the more diodes in series, the higher the temperature rises. This presents a challenge when using the low-voltage diodes in high voltage applications.

III. Challenges when series connecting diodes

Series connection of diodes to attain higher effective blocking voltages is well known, and issue of voltage imbalance

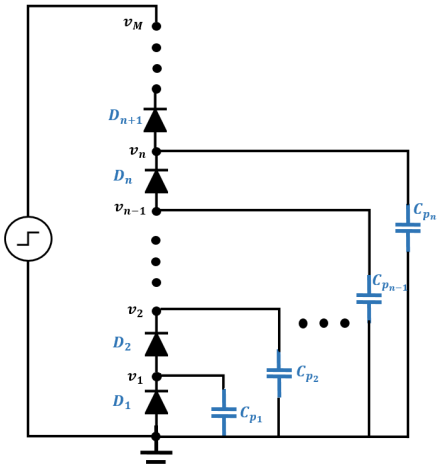


Figure 2: Circuit diagrams of connecting diodes in series (showing parasitic capacitances from each node to common)

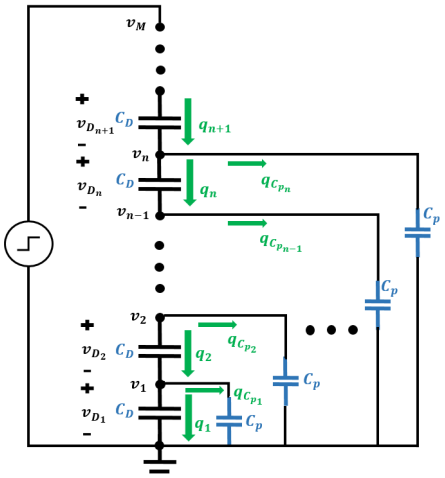


Figure 3: Simplified ac equivalent circuit model of Fig. 2

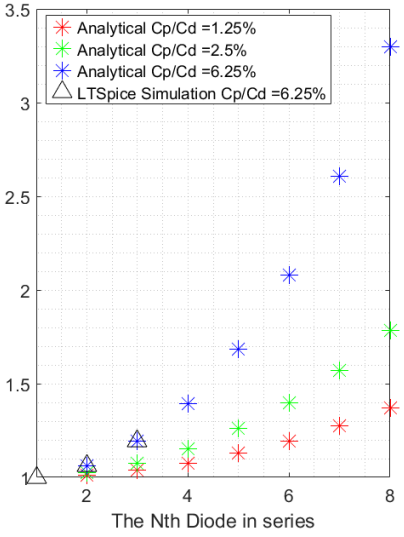


Figure 4: The voltage across the nth diode as a ratio of that of the 1st diode

due to the variation among diodes has been observed [21]. The common solution is to parallel balancing resistors with the diodes to ensure each diode reach the same dc state [21]. Here we identify that the parasitic capacitance to common at each connection node between the diodes also contributes to voltage imbalance and to increased loss.

A. Parasitic capacitance causing voltage imbalance

Figure 2 shows an equivalent circuit of one branch in a full-bridge rectifier. Each branch consists of M series-connected diodes $D_1, D_2, ..., D_M$. Each diode has its junction capacitance C_D and each node has parasitic capacitance to common $C_{p1}, C_{p2}, ..., C_{pM}$. These capacitances sink or source charge from each node. At high frequencies, the voltage distribution among diodes is mostly determined by the capacitances. As a first order analysis, we assume each diode has the same C_D and the parasitic capacitance from each node to ground has the same value C_P. Thus we simplify Fig. 2 to Fig. 3.

In the following analysis, we consider an incremental increase in the source voltage, this increment will inject an incremental amount of charge into the diode chain. To charge the voltage v_{D_1} at Node 1 from zero to v_1, the charge going through ground-connected capacitor C_D is $q_1 = v_1 C_D$, and the charge going through C_P is $q_{Cp1} = v_1 C_P$. Since both charges come from D_2, the charge going through the C_D of D_2 is $q_2 = q_1 + q_{Cp1} = v_1 C_D + v_1 C_P$. If we want $V_{D1} \approx v_{D2}$, we must make sure $q_2 \approx q_1$, thus $q_1 \gg q_{Cp1}$ (equivalently $C_D \gg C_p$).

To generalize, at Node N, $q_n = v_{Dn} C_D$ and $q_{Cpn} = v_n C_P$. If we want $v_{Dn+1} \approx v_{Dn} ... \approx v_{D1}$, in another word $v_n \approx n v_{D1}$, we must make sure $q_n \gg q_{Cpn}$, equivalently $C_D \gg nC_p$. Intuitively, the diode closest to the ac node needs to carry all the charge going down the diode chain and that going through all the parasitic capacitances. If all diodes are identical, then this diode passes more charge through its capacitance C_D than diodes below it, and thus needs to block higher voltage.

To provide approximate voltage balancing among the diodes, then, we require $C_D \gg nC_p$. This constraint becomes more limiting as: n increases, C_D decreases, and C_P increases. As shown in Appendix B, a closed form expression for the diode voltages in Fig. 3 in terms of the bottom diode voltage v_1 can be found as:

$$\frac{v_{Dn}}{v_{D1}} = \frac{1}{\sqrt{a(a+4)}} \left\{ \left(\frac{a+2+\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a+\sqrt{a(a+4)}}{2} \right) - \left(\frac{a+2-\sqrt{a(a+4)}}{2} \right)^n \left(\frac{a-\sqrt{a(a+4)}}{2} \right) \right\}$$

where $a = C_P/C_D$. We plot these voltages for different values of C_P/C_D in Fig. 4. It can be seen that the diode closes to the common potential blocks the lowest voltage, and as the number of series diodes increases, the off-state voltage imbalance increases; in addition, when C_P/C_D gets bigger, the voltage imbalance gets worse. The analytical solution is also validated by LTspice simulations.

The voltage imbalance suggests the switching loss among diode is also imbalanced: the diodes closer to the ac node must carry higher capacitive switching currents and thus exhibit higher loss. In stating this, we recognize that the currents carried through diode capacitances (and associated device voltage swings) induce significant loss in the diodes. These losses may be due to joule heating and/or may represent other loss phenomena, as observed with capacitance losses in other device types [22]–[24]. Based on this, if each diode has similar thermal path to ambient, then diodes closer to the ac node would show higher temperature rise. The experimental results in Section V demonstrate this predicted voltage and temperature imbalance.

IV. Compensation Techniques for Achieving Voltage Balance

When connecting diodes in series, the charge going through each diode is different due to the presence of parasitic ca-

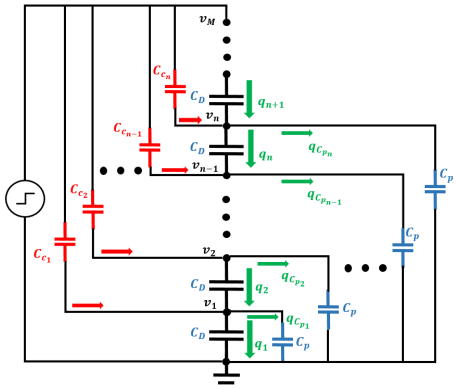


Figure 5: Independent compensation: adding compensation capacitors to each node

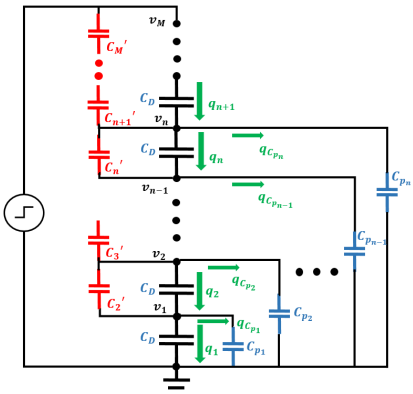


Figure 6: Coupled compensation: adding compensation capacitors across each diode

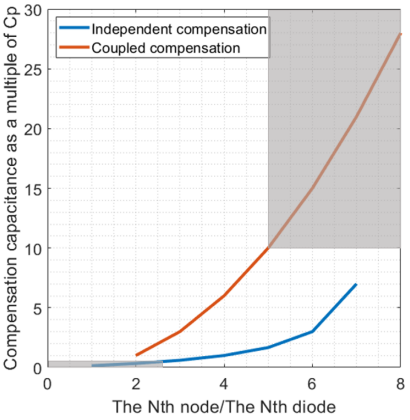


Figure 7: Compensation capacitance increases with the number of diodes in series (the capacitance should not be too small, as limited by the physically realizable capacitance; nor too big, as limited by the increased capacitor system losses offsetting the reduced diode losses. These limits are marked out by two grey areas conceptually)

pacitance at each connection node, and additional losses are introduced owing to the lossy nature of the device capacitances carrying the currents associated with the parasitics. We can redistribute the charge flows through the diodes and mitigate some of the associated voltage imbalances and losses by adding low-loss external capacitors. Two related compensation techniques are proposed in this section.

A. *Independent compensation*

Figure 5 illustrates the first compensation technique. Taking Node 1 as an example, C_P draws charge from the node. Instead of providing this charge from D_2, we can inject the charge directly to Node 1 through an additional capacitor C_{c_1} connected between Node 1 and the ac node. In this way, we guarantee $q_1 = q_2$ thus $v_{D1} = v_{D2}$. The amount of charge needs to be injected is $q_{Cp1} = v_1 C_P$. Since, after compensation, C_{c_1} blocks $(M-1)v_1$, where M is the number of series-connected diodes (assuming after adding the compensation, all diode voltages balance), the required capacitance of C_{c_1} is $\frac{1}{M-1}C_p$. Similarly for Node n, we can inject the charge directly from the ac node to the nth parasitic capacitance through C_{c_n}.

These additional compensation capacitors solely provide charge to the corresponding parasitic capacitance, and can be independently adjusted. Their values are calculated as below.

$$C_{c_1} = \frac{1}{M-1}C_p, C_{c_2} = \frac{2}{M-2}C_p, ...,$$
$$C_{c_n} = \frac{n}{M-n}C_p, ..., C_{c_M} = (M-1)C_p \quad (1)$$

The lower and the upper bound of the compensation capacitances are $\frac{1}{M-1}C_p$ and $(M-1)C_p$ respectively. As M increases, the lower bound decreases approximately inversely with the number of series-connected diodes and is eventually limited by the smallest physical capacitance that one can accurately implement; the upper bound increases approximately linearly with the number of series-connected diodes and is limited by the increased losses and the load regulation effect associated with the total capacitance between the ac node and common [25]. A benefit of this technique is that each compensation capacitance may be selected/adjusted based on the voltage distribution impact at a single node. At the same time, each of the compensation capacitances blocks different voltage making their implementation more cumbersome.

B. *Coupled compensation*

An alternative compensation approach is to add a low-loss capacitor across each diode to carry the charge for the parasitic capacitances. A benefit of this implementation is that each compensation capacitor blocks the same voltage; a disadvantage is that the charges going through them (and the capacitor values) are coupled. All the charges are carried by the top compensation capacitor, and they trickle down the chain to each parasitic capacitance.

The capacitance of each compensation capacitor is calculated and listed in (2). C'_n provides the sum of charges for $Q_{C_{p_1}}, Q_{C_{p_2}}, ..., Q_{C_{p_{n-1}}}$. Since $Q_{C_{p_i}} = iV_1C_P$, the sum of the charges is $V_1[C_P + 2C_P + ... + (n-1)C_P] = \frac{n(n-1)}{2}V_1C_P$. Thus $C'_n = \frac{n(n-1)}{2}C_P$.

$$C'_2 = C_p, C'_3 = 3C_p, ...,$$
$$C'_n = \frac{1}{2}n(n-1)C_p, ..., C'_M = \frac{1}{2}M(M-1)C_p \quad (2)$$

With coupled compensation, the required capacitance increase quadratically with the number of diodes in series.

C. *Comparison*

Figure 7 shows the compensation capacitances needed for each node or each diode in the two compensation implementations. One limiting factor in practical realizations is that a given compensation capacitance should not be too small nor too large, as illustrated qualitatively with the two grey areas in Fig. 7.

The total capacitive energy storage is identical in either implementation:

$$E_{independent} = \sum_{1}^{M} \frac{1}{2} C_{c_n} V_{C_{cn}}^2 = \frac{C_p V_1^2}{2} \sum_{1}^{M} n(M-n)$$

$$E_{coupled} = \sum_{1}^{M} \frac{1}{2} C'_n V_{C'_n}^2 = \frac{C_p V_1^2}{2} \sum_{1}^{M} \frac{n(n-1)}{2}$$

$$E_{independent} = E_{coupled} = \frac{C_p V_1^2}{2} \frac{M^3 - M}{6}$$

However, the facility with which such injection can be implemented with available components or PCB structures (in terms of capacitance values and voltages) will determine the best method to select in a given application. Often, however, the coupled compensation is easier to implement with discrete components or by PCB design.

V. Experimental Results

A. Setup and measurement techniques

The experimental setup is shown in Fig. 8. We connect four 3.3 kV GeneSiC diodes (GAP3SLT33-214) in series to form a single diode, then use this diode in each leg of a full-bridge rectifier. We drive the rectifier at 600 kHz using a resonant inverter and a transformer, outputting 3.6 kV and 20 mA at the output of the rectifier; the inverter and transformer are detailed in [3]. We measure the voltages at three nodes on one branch of the rectifier using three Teledyne LeCroy PPE4KV probes, as shown in Fig. 8. For sensing, we add a 0.5 pF NP0 capacitor at each node as a divider capacitor to reduce the effect of the probe capacitance on the voltage distribution. By subtracting the voltage readings from three probes, we obtain three voltages that are proportional to the off-state voltage of each diode. In terms of voltage balancing, we only care about the ratio of these three voltages instead of their absolute values.

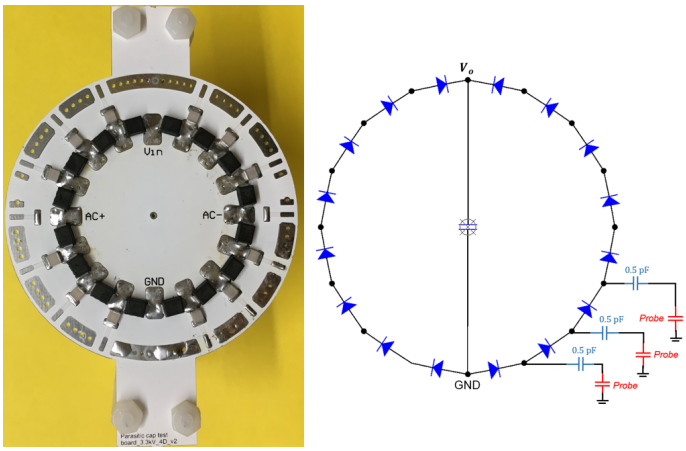


Figure 8: Full-bridge rectifier test board and capacitor divider used for voltage measurements

B. Implementation the compensation capacitance

Several CAD and FEA tools are used to simulate the parasitic capacitance of the PCB layout in Fig. 8. First, we export the PCB layout of the rectifier from Altium Designer [26] to a .STEP file; then we import the .STEP file to FreeCAD [27], use a plug-in script provided by Fast Field Solver [28] to process this geometry and save it as a net list file; lastly, we import the netlist file in the Fast Field Solver to solve for the capacitance between each two nodes in the geometry, as shown in Fig. 9.

We can simplify the capacitance matrix down to only the capacitances between each node and common (either GND or V_o), as shown in blue in Fig. 10. The detailed simplification process is explained in Appendix C. We choose to implement the coupled compensation because of the availability of discrete capacitors at the required voltage rating. Following the derivation in Section IV, we can calculate the required compensation capacitances, shown in red in Fig. 10.

In the experiments, we used Vishay Vitramon Quad HIFREQ series capacitors to obtain the closest discrete capacitances available: 0.5 pF (VJ1111D0R5VXRAJ), 1.5 pF (VJ1111D0R5VXRAJ and VJ1111D1R0BXRAJ) and 3 pF (VJ1111D1R0BXRAJ and VJ1111D2R0BXRAJ) respectively.

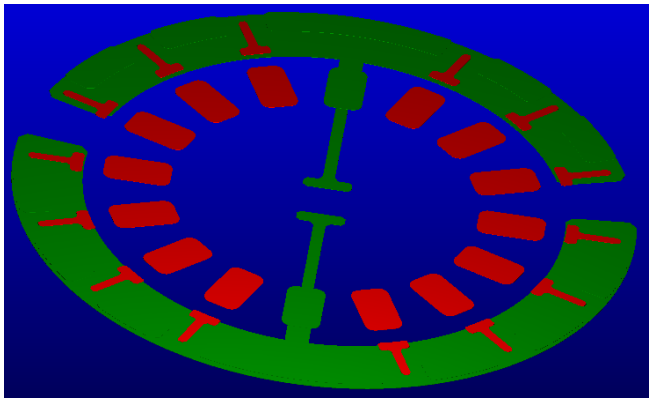


Figure 9: Fast Field Solver solves the capacitance between each node in this geometry. One can define a group of conductors (traces, pads, via, etc) as one node. In our geometry, ground node and V_o node are in green; rest of the nodes are in red. The square-shape pads are nodes connecting two diodes and the T-shape pads are nodes connecting to the measurement probe.

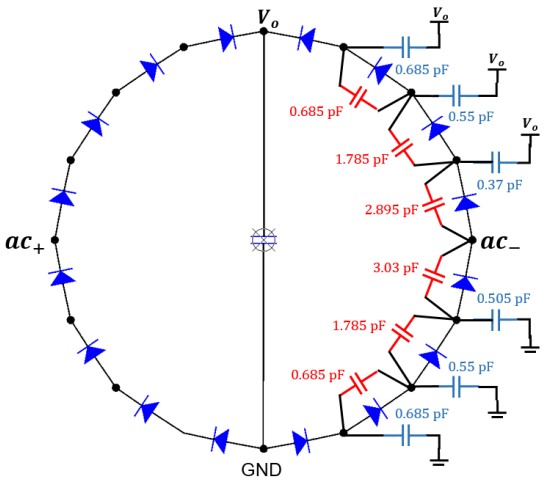
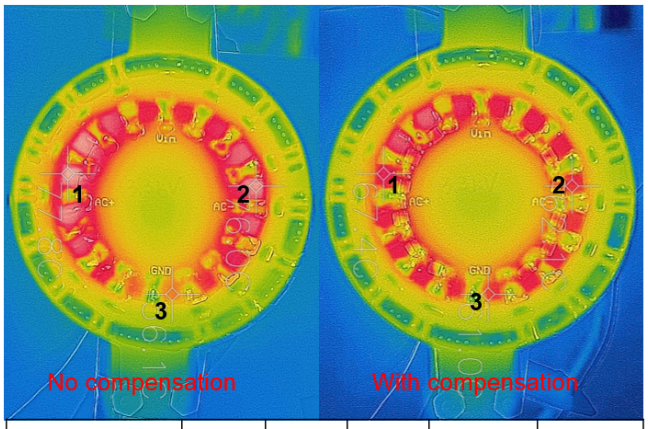


Figure 10: The estimated parasitic capacitance of each node to common and the required compensation capacitance across each diode. We implement these using the available capacitors with the closest capacitance values.

C. Experimental results

Figure 11 shows the temperature profiles of before and after compensation at three different locations in the rectifier (illustrated). The operating conditions for the rectifier are as follows: $f = 600\,\text{kHz}$, V_o =3.6 kV, I_o =20 mA (P_o =72 W). With compensation, the peak diode temperature drops by 10.4 degrees (peak temperature rise drops by approximately 20 %). The temperature differences among diodes drop from 20 °C to 7 °C and the average temperature of the diodes drops from 70 °C to 64 °C. Figure 12 compares the divided-down voltage waveform across three out of four diodes before and after compensation. (We did not measure the voltage at the ac-node to infer the voltage across the diode connected to the ac node. This was because adding a probe with capacitor divider to the ac node causes significant imbalance between the two ac nodes and significantly changes the charge distribution). With the measurements of the rest of the three diodes, each of the waveforms is proportional to the actual off-state voltage of an individual diode. With compensation, the discrepancies in the off-state voltages reduces. This further demonstrates the voltage imbalance issue and the effectiveness of the compensation technique.

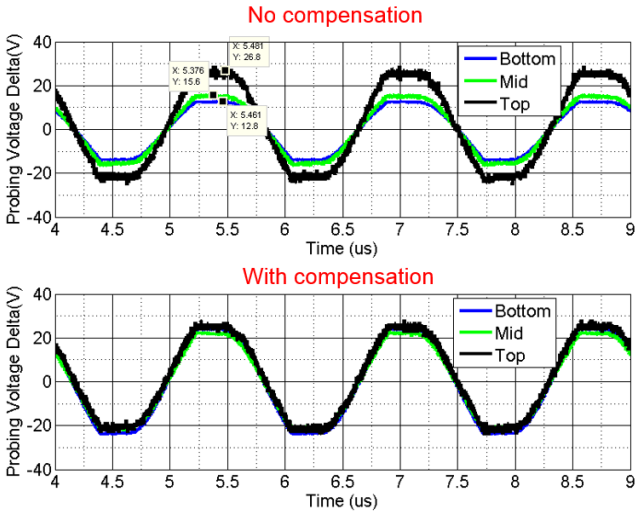


Conditions	Node 1 (C)	Node 2 (C)	Node 3 (C)	Average (C)	Maximum Delta (C)
No Compensation	77.8	76	56.1	~70	~20
W/Compensation	67.4	62.1	61	~64	~7

Figure 11: Temperature profile before/after compensation

VI. Conclusion

The paper explores compensation techniques for using discrete low-voltage diodes in series as one high voltage diode. Additionally, the performance of a range of diodes are characterized for use in high-voltage converters. We identify that when series connecting diodes, the parasitic capacitance of the physical connections to common can result in severe voltage and temperature imbalances, and corresponding increases in loss. We propose two related compensation techniques to mitigate this issue. We demonstrate the voltage imbalance issue and validate the compensation approach through experimental results. Both the proposed techniques and the diode evaluation results will be useful for miniaturization of high voltage converters.



	Voltage ratio (VD1:VD2:VD3)
No Compensation	1 : 1.22 : 2.09
With Compensation	1 : 1.09 : 1.22

Figure 12: Proxy (divided down) diode voltages before/after compensation. The full-bridge is operating at: $f = 600\,\text{kHz}$, V_o =3.6 kV, I_o =20 mA. We did not measure the voltage across the diode connected to the ac node because adding a probe with capacitor divider to the ac node causes severe imbalance between two ac nodes and largely change the charge distribution.

VII. Appendix

A. Diode specs and loss characterization

For diodes with a temperature rise lower than 50 °C in Fig. 1, we characterize their losses using DC tests and create a temperature-loss map. Then we estimate diode losses at different temperatures by interpolating this temperature-loss map. In Fig. 13, we show the temperature rise of the diodes when each rectifier leg is comprised of a single diode (same data as in Fig. 1), and the loss corresponding to this temperature rise. With the same temperature rise, some diodes exhibit lower losses compared with others. The specifications of these diodes are listed in Table. I.

B. Closed-form analytical solution of the diode voltages

We start with the charge equation at each node in Fig. 3.

$$q_{n+1} = q_n + C_P v_n, ..., q_2 = q_1 + C_P v_1, q_1 = C_D v_1$$

Then we substitute q_i in the function of q_{i+1}'s function,

$$\begin{aligned} q_{n+1} &= q_n + C_P v_n \\ &= q_{n-1} + C_P v_{n-1} + C_P v_n = ... \\ &= q_1 + C_P(v_n + v_{n-1} + ... + v_1) \end{aligned}$$

Combine with

$$q_{n+1} = C_D(v_{n+1} - v_n)$$

We can solve for v_{n+1}

$$v_{n+1} = v_n + v_1 + \frac{C_P}{C_D}\sum_1^n v_i$$

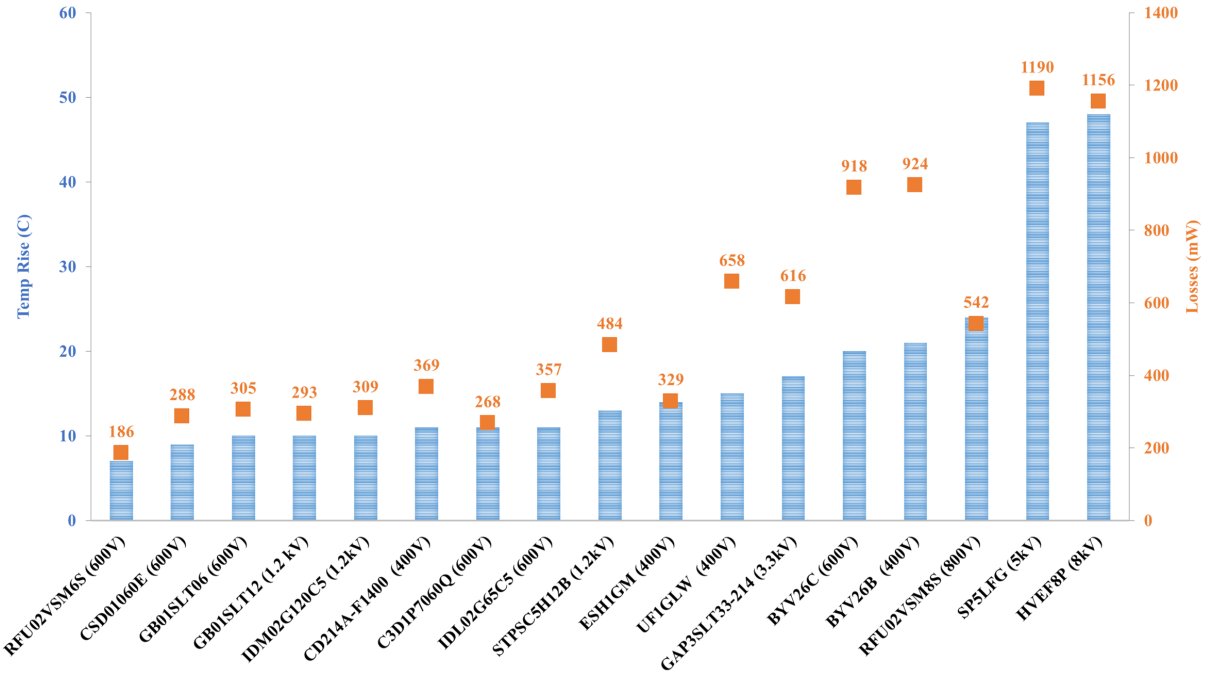


Figure 13: The temperature rise of lower-loss diodes when each rectifier leg is comprised of a single diode (same data as in Fig. 1), and the loss corresponding to this temperature rise. The losses were estimated using the DC tests described in Section II. The specifications of these diodes are listed in Table. I

Rearrange the equation, we find v_{n+1} is a function of v_n and v_{n-1},

$$\begin{aligned} v_{n+1} &= v_n + (-v_{n-1} + v_{n-1}) + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i + \frac{C_P}{C_D} v_n \\ &= v_n - v_{n-1} + (v_{n-1} + v_1 + \frac{C_P}{C_D}\sum_1^{n-1} v_i) + \frac{C_P}{C_D} v_n \\ &= v_n - v_{n-1} + v_n + \frac{C_P}{C_D} v_n = (\frac{C_P}{C_D} + 2)v_n - v_{n-1} \end{aligned}$$

We can find the closed-form solution of this series by solving the differential equation

$$x^2 = (\frac{C_P}{C_D} + 2)x - 1$$

Denote $a = \frac{C_P}{C_D}$, the roots to the equation $x^2 - (a+2)x + 1 = 0$ are

$$x_1 = \frac{a + 2 + \sqrt{a(a+4)}}{2}, x_2 = \frac{a + 2 - \sqrt{a(a+4)}}{2}$$

Thus v_n is in the format

$$v_n = c_1 x_1^n + c_2 x_2^n$$

Where c_1 and c_2 are constants.

The voltage drop across the nth diode is then

$$v_{Dn} = v_n - v_{n-1} = c_1 x_1^{n-1}(x_1 - 1) + c_2 x_2^{n-1}(x_2 - 1)$$

Considering the 1st diode (connect to common),

$$\begin{aligned} v_{D1} &= c_1(x_1 - 1) + c_2(x_2 - 1) \\ v_1 &= c_1 x_1 + c_2 x_2 \\ &\because v_{D1} = v_1 \\ &\therefore c_1 = -c_2 = \frac{v_1}{x_1 - x_2} \end{aligned}$$

Therefore

$$v_1 = \frac{v_1}{x_1 - x_2}(x_1^n + x_2^n)$$

Therefore the closed-form analytical solution for the voltage across each diode in Fig. 3 is

$$\begin{aligned} \frac{v_{Dn}}{v_{D1}} = \frac{1}{\sqrt{a(a+4)}} \Bigg\{ &\left(\frac{a + 2 + \sqrt{a(a+4)}}{2}\right)^n \left(\frac{a + \sqrt{a(a+4)}}{2}\right) \\ &- \left(\frac{a + 2 - \sqrt{a(a+4)}}{2}\right)^n \left(\frac{a - \sqrt{a(a+4)}}{2}\right) \Bigg\} \end{aligned}$$

Where

$$a = \frac{C_P}{C_D}$$

C. Simplify the capacitance matrix

The original capacitance matrix are shown in Fig. 14. We ignore the capacitance to ground from pads far away from the ground node (same for the V_o node). Since the capacitances between each two probe pads are very small (in green), we simplify Fig. 14 to Fig. 15. Then by combining the capacitance to common at each node, we can get Fig. 10.

Table I: Specifications of diodes under tests and conditions of tests in Fig. 1 and Fig. 13. The tests with asterisks did not reach thermal equilibrium and were cut off after 30 second to 90 second. The reverse recovery time marked by † are defined as "Switching Time" in the corresponding data sheets.

Manufacturer PN	Manufacturer	Type	Nominal Voltage (V)	Forward Current (mA)	Reverse Recovery (ns)	Capacitance at 1 V (pF)	Number of diodes in series	Test Voltage (V)	Test Current (mA)
RFU02VSM6S	ROHM Semiconductor	Si	600	200	35	3	1	301	39.9
CSD01060E	Wolfspeed	SiC Schottky	600	1000	∼0	80 (@0 V)	1	298	197.3
							2	598	200.3
							4	1200	187
GB01SLT06	GeneSiC Semiconductor	SiC Schottky	650	1000	20†	76	1	298	197.5
							2	599	199.1
							4	1190	186.3
GB01SLT12	GeneSiC Semiconductor	SiC Schottky	1200	1000	17†	69	1	599	198
							2	1190	200
IDM02G120C5	Infineon Technologies	SiC Schottky	1200	2000	∼0	182	1	599	198
							2	1200	186.7
CD214A-F1400	Bourns Inc.	SiC	400	1000	35	17	1	205	202.2
							2	401	202.6
							3	602	201.5
							4	804	200
C3D1P7060Q	Infineon Technologies	SiC Schottky	600	1700	∼0	63	1	301	198
							2	597	198.7
							4	1200	187
IDL02G65C5	Infineon Technologies	SiC Schottky	650	2000	∼0	70	1	300	199.5
							2	598	198.7
STPSC5H12B	STMicroelectronics	SiC Schottky	1200	5000	∼0	350	1	600	199.5
							2	1180	198
ESH1GM	Taiwan Semiconductor	Si	400	1000	25	3 (@4 V)	1	201	201
UF1GLW	Taiwan Semiconductor	Si	400	1000	20	25 (@4 V)	1	205	202.7
							2	400	202.2
GAP3SLT33	GeneSiC Semiconductor	SiC Schottky	3300	300	60†	42	1	1025	20
							2	2020	20
							4	3000	18.3
UF4004	ViSHAY Semiconductor	Si	400	1000	50	22	1	200	198
							2	399	201.6
BYV26C	ViSHAY Semiconductor	Si	600	1000	30	25	1	298	196
							3*	902*	208*
BYV26B	ViSHAY Semiconductor	Si	400	1000	30	25	1	203	199.8
							2	400	202.5
RFU02VSM8S	ROHM Semiconductor	Si	800	200	35	3	1	407	40
SP5LFG	Dean Technology	Si	5000	270	50	7.2 (@0 V)	1	2500	30
HVEF8P	Dean Technology	Si	8000	30	20	0.33(@0 V)	1	3700	2.76
ESH1JM	Taiwan Semiconductor	Si	600	1000	25	3 (@4 V)	1	301	200
UF1JLW	Taiwan Semiconductor	Si	600	1000	25	15 (@4 V)	1	299	201
							3*	900*	207*
X50FF3	Voltage Multiplier Inc	Si	5000	75	30	3	1*	2500*	17*
X150FF3	Voltage Multiplier Inc	Si	15000	25	30	1.2	1*	5000*	3.5*
Z50FF3	Voltage Multiplier Inc	Si	5000	180	30	16	1*	2500*	36*
S1MLS	Taiwan Semiconductor	Si	1000	1200	-	50	1*	500*	13*
ACGRAT105L-HF	Comchip Technology	Si	1000	1000	-	12	1*	500*	5.6*
HS1M	Taiwan Semiconductor	Si	1000	1000	75	18	1*	400*	160*
SM3F	Dean Technology	Si	3000	900	65	6 (@4 V)	1*	1500*	80*
MUR160S	Taiwan Semiconductor	Si	600	1000	50	50	1*	298*	207*
ES1JL	Taiwan Semiconductor	Si	600	1000	35	9.6	1*	299*	197*
CD1408-FU1800	Bourns Inc	Si	800	1000	35	16	1*	300*	150*
ACURA107-HF	Comchip Technology	Si	1000	1000	75	18	1*	400*	190*
UA1M	SMC Diode	Si	1000	1000	75	-	1*	400*	40*
FM2000GP	MCC	Si	2000	500	500	30 (@4 V)	1*	800*	70*
HV200UF5	Dean Technology	Si	5000	200	50	12 (@0 V)	1*	2500*	42*
Z50FF3LL	Voltage Multiplier Inc	Si	5000	400	30	18	1*	2500*	60*
UX-FBR8	Dean Technology	Si	8000	420	40	7.5 (@0 V)	1*	4000*	40*
SLU08M	Dean Technology	Si	8000	400	40	7.5 (@0 V)	1*	4000*	50*

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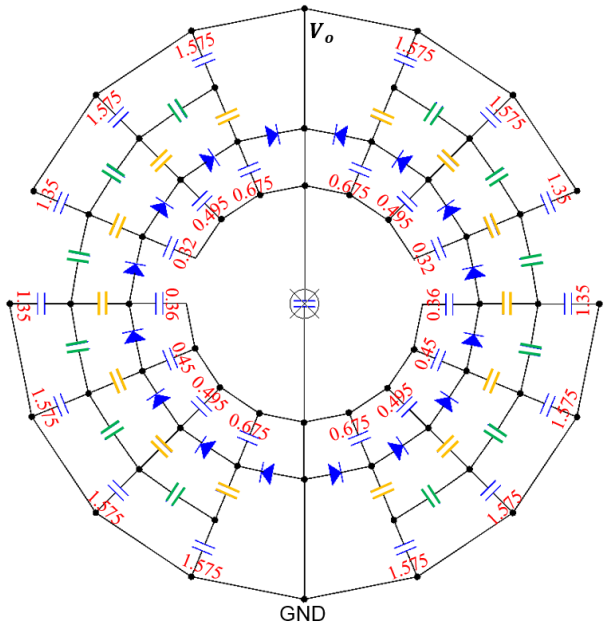

Figure 14: The simulated capacitance matrix of the PCB layout in Fig. 9. All capacitances to common (either GND or V_o) are marked in red and in pF. The capacitors in green are between each two probe pads, all the same at 0.002 pF; all capacitors in yellow are between each diode pad and the probe pad, all the same at 0.045 pF

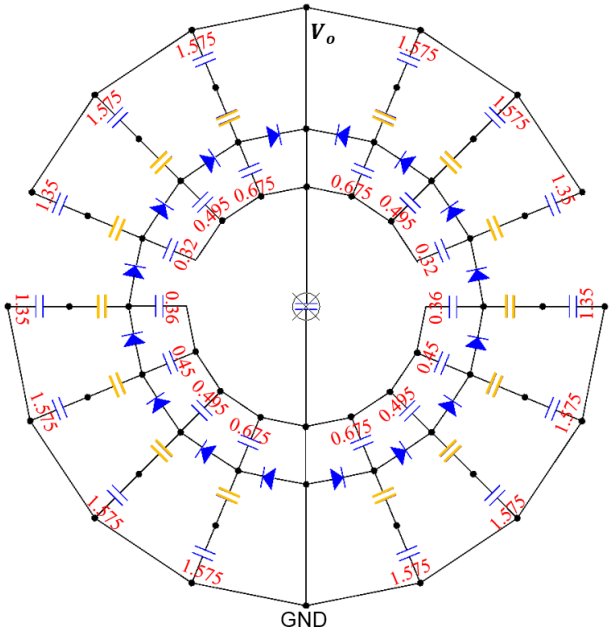

Figure 15: Simplify the capacitance matrix in Fig. 14

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