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(54) **HIGH-FREQUENCY, HIGH DENSITY POWER FACTOR CORRECTION CONVERSION FOR UNIVERSAL INPUT GRID INTERFACE**

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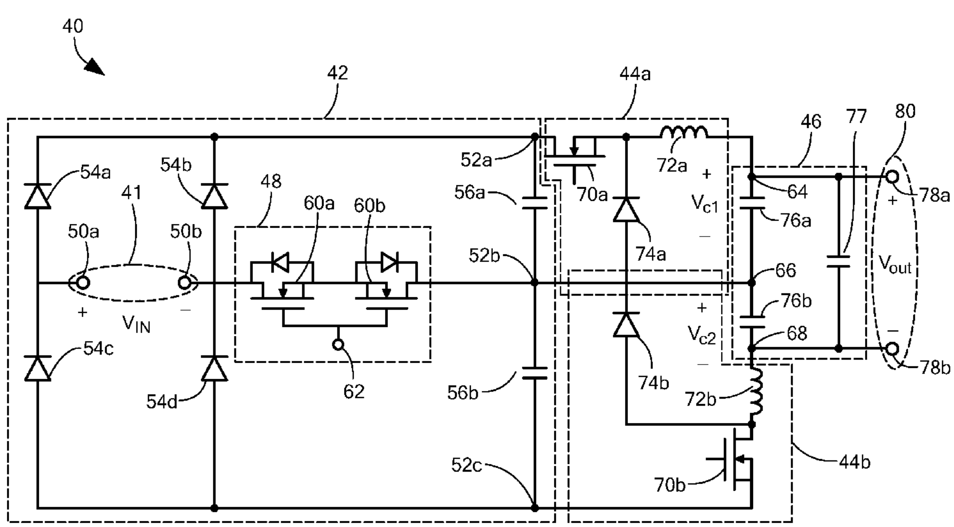
(57) **ABSTRACT**

A circuit includes a reconfigurable rectifier, a voltage balancer, and a pair of converters. The reconfigurable rectifier includes an ac input port and three output ports. In a first configuration, the reconfigurable rectifier can deliver power at a first output port and, in a second configuration, to at least a second output port. The voltage balancer includes first and second ports coupled to second and third output ports of the reconfigurable rectifier and is configured to balance received voltage at the first and second ports. The first converter has an input coupled to the first port of the voltage balancer and an output at which a first converted voltage signal is provided. The second converter has an input coupled to the second port of the voltage balancer and an output at which a second converted voltage signal is provided.

20 Claims, 14 Drawing Sheets



(58) **Field of Classification Search**
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See application file for complete search history.

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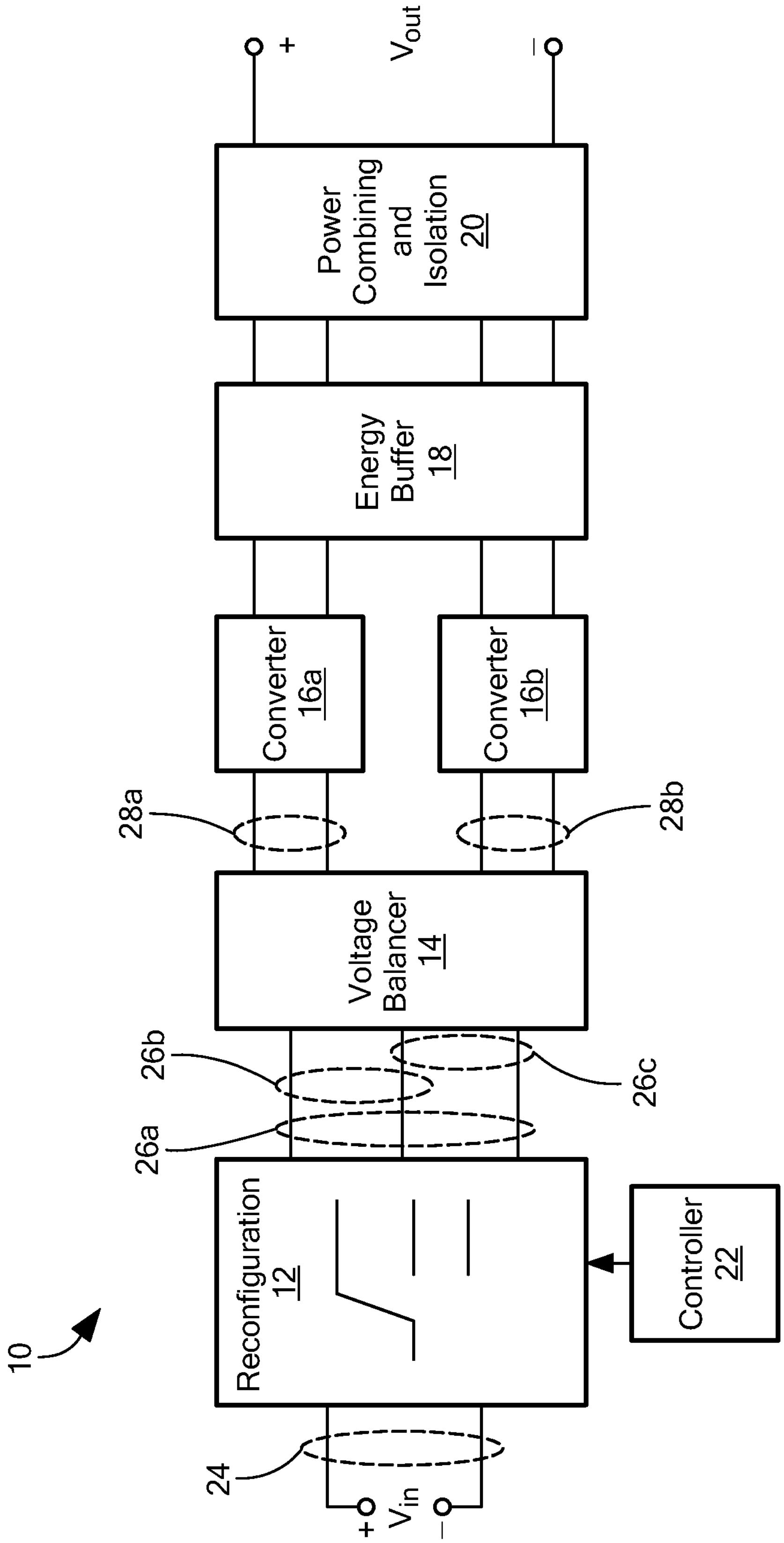
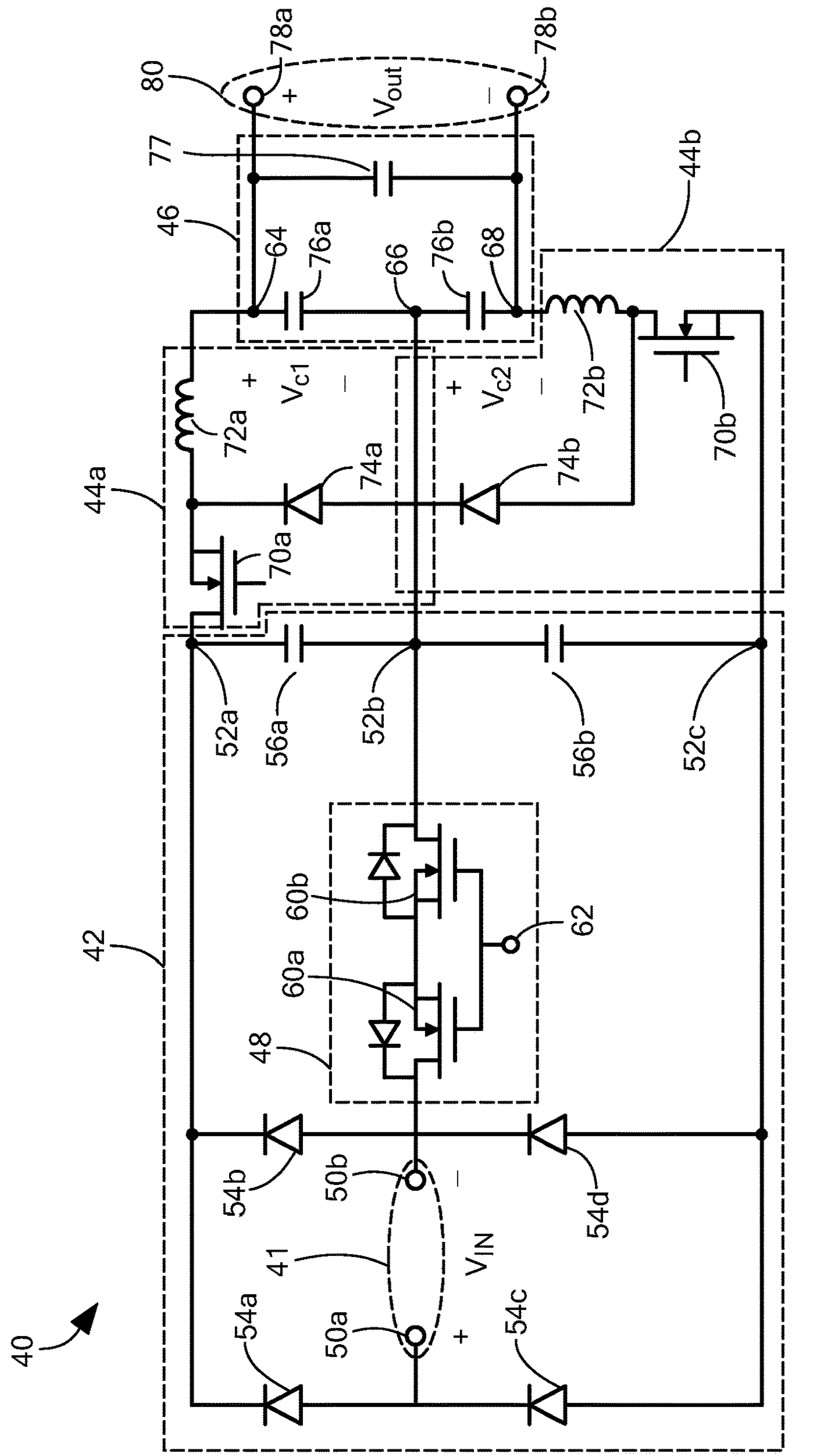

10
Reconfiguration
12
Controller
22
24
+ V_{in} –
26a
26b
26c
Voltage
Balancer
14
28a
28b
Converter
16a
Converter
16b
Energy
Buffer
18
Power
Combining
and
Isolation
20
+ V_{out} –

FIG. 1



40
41
42
44a
44b
46
48
50a
50b
52a
52b
52c
54a
54b
54c
54d
56a
56b
60a
60b
62
64
66
68
70a
70b
72a
72b
74a
74b
76a
76b
77
78a
78b
80
V_{IN}
V_{out}
V_{c1}
V_{c2}

FIG. 2

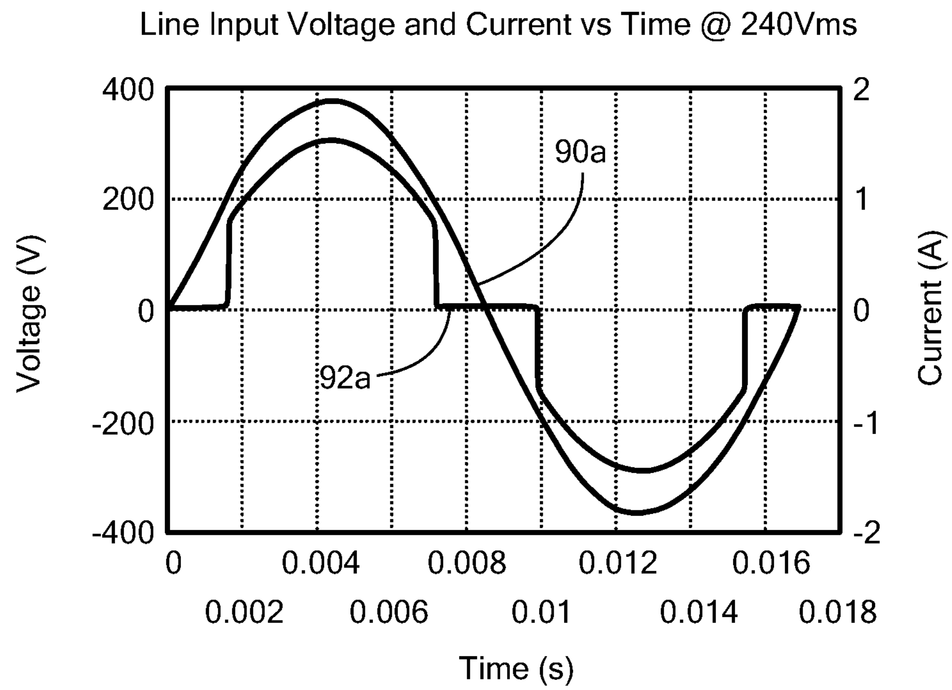

Line Input Voltage and Current vs Time @ 240Vms
400
200
0
-200
-400
2
1
0
-1
-2
Voltage (V)
Current (A)
90a
92a
0
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
Time (s)

FIG. 3A

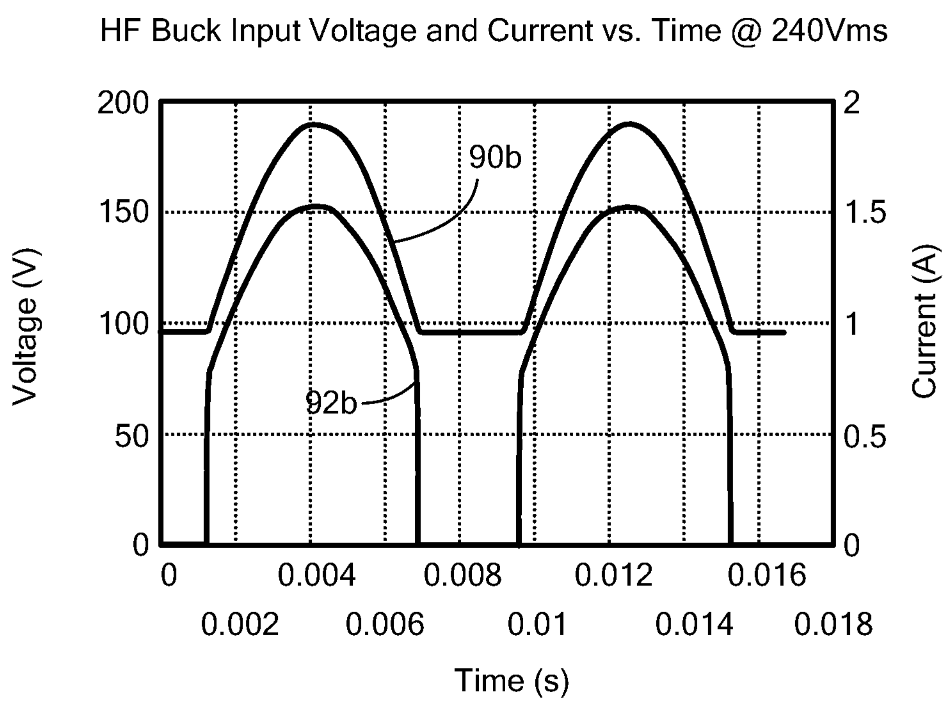

HF Buck Input Voltage and Current vs. Time @ 240Vms
200
150
100
50
0
2
1.5
1
0.5
0
Voltage (V)
Current (A)
90b
92b
0
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
Time (s)

FIG. 3B

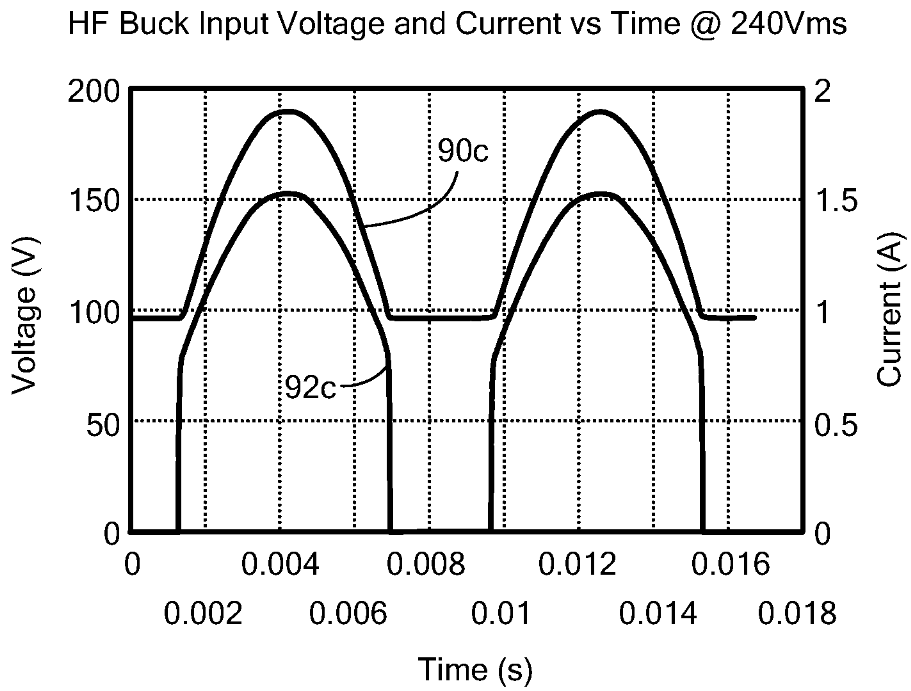

HF Buck Input Voltage and Current vs Time @ 240Vms
Voltage (V)
Current (A)
Time (s)
200
150
100
50
0
2
1.5
1
0.5
0
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
90c
92c

FIG. 3C

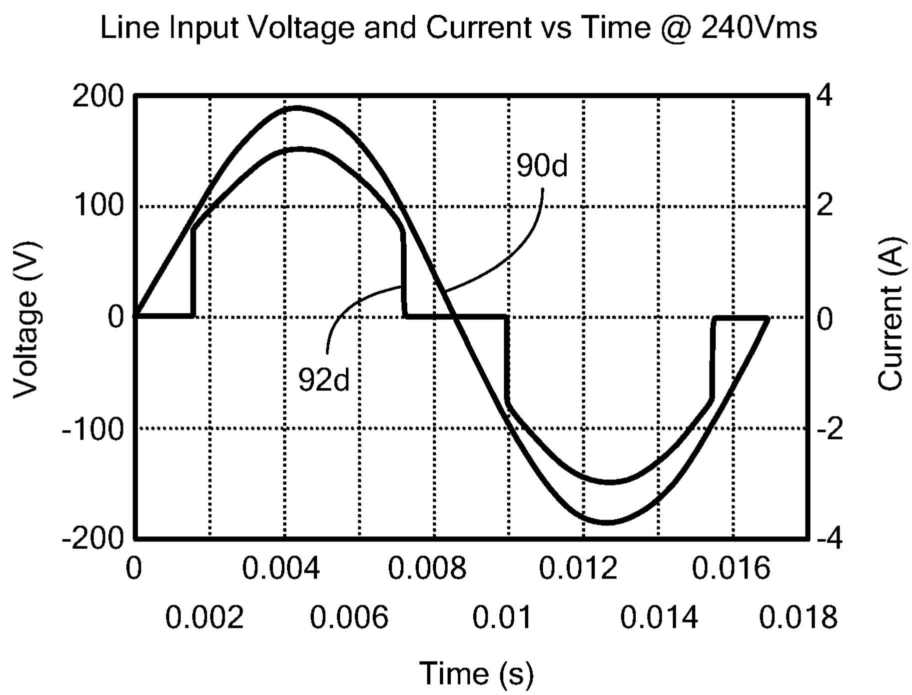

Line Input Voltage and Current vs Time @ 240Vms
Voltage (V)
Current (A)
Time (s)
200
100
0
-100
-200
4
2
0
-2
-4
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
90d
92d

FIG. 3D

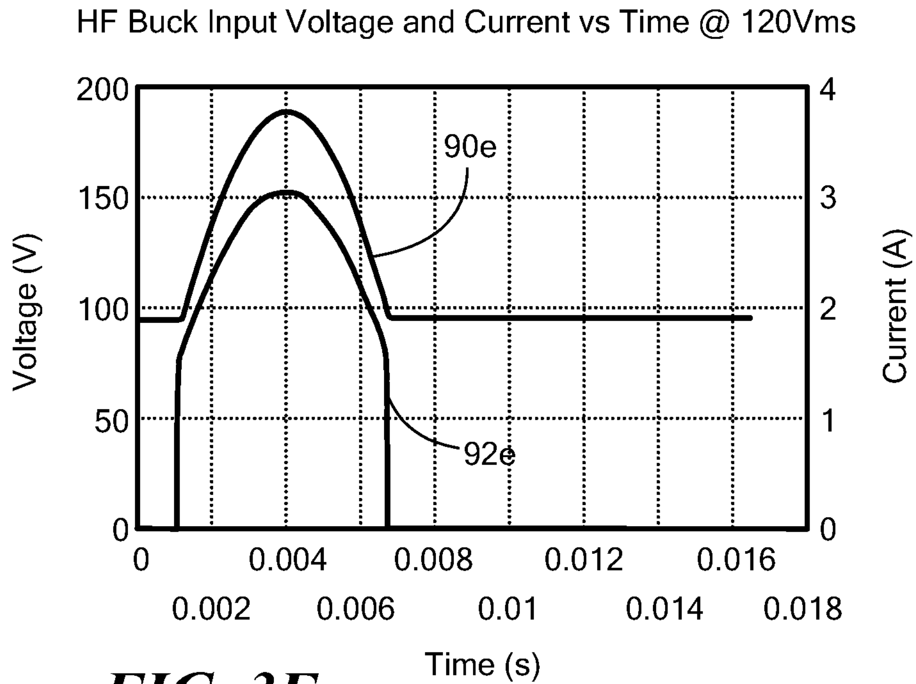

HF Buck Input Voltage and Current vs Time @ 120Vms
Voltage (V)
Current (A)
200
150
100
50
0
4
3
2
1
0
90e
92e
0
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
Time (s)

FIG. 3E

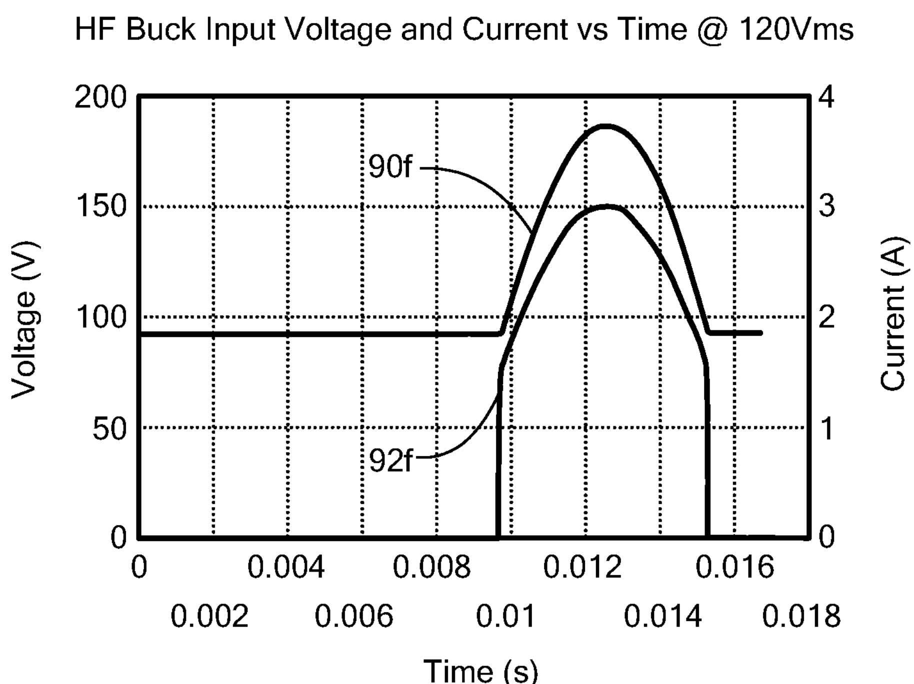
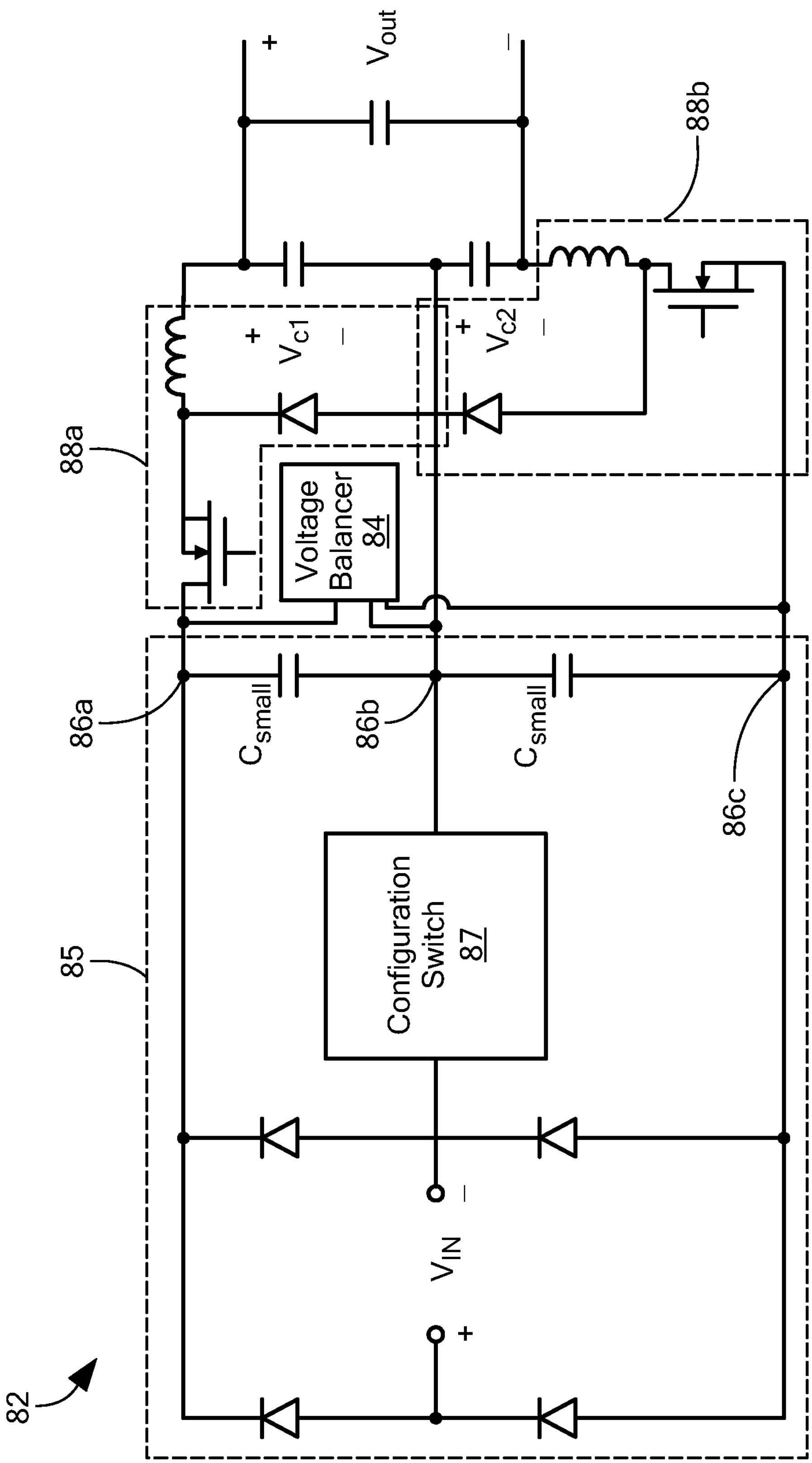

HF Buck Input Voltage and Current vs Time @ 120Vms
Voltage (V)
Current (A)
200
150
100
50
0
4
3
2
1
0
90f
92f
0
0.004
0.008
0.012
0.016
0.002
0.006
0.01
0.014
0.018
Time (s)

FIG. 3F



+
V_{out}
−
88b
88a
+
V_{c1}
−
+
V_{c2}
−
Voltage Balancer 84
86a
86b
86c
C_{small}
C_{small}
Configuration Switch 87
85
−
V_{IN}
+
82

FIG. 4

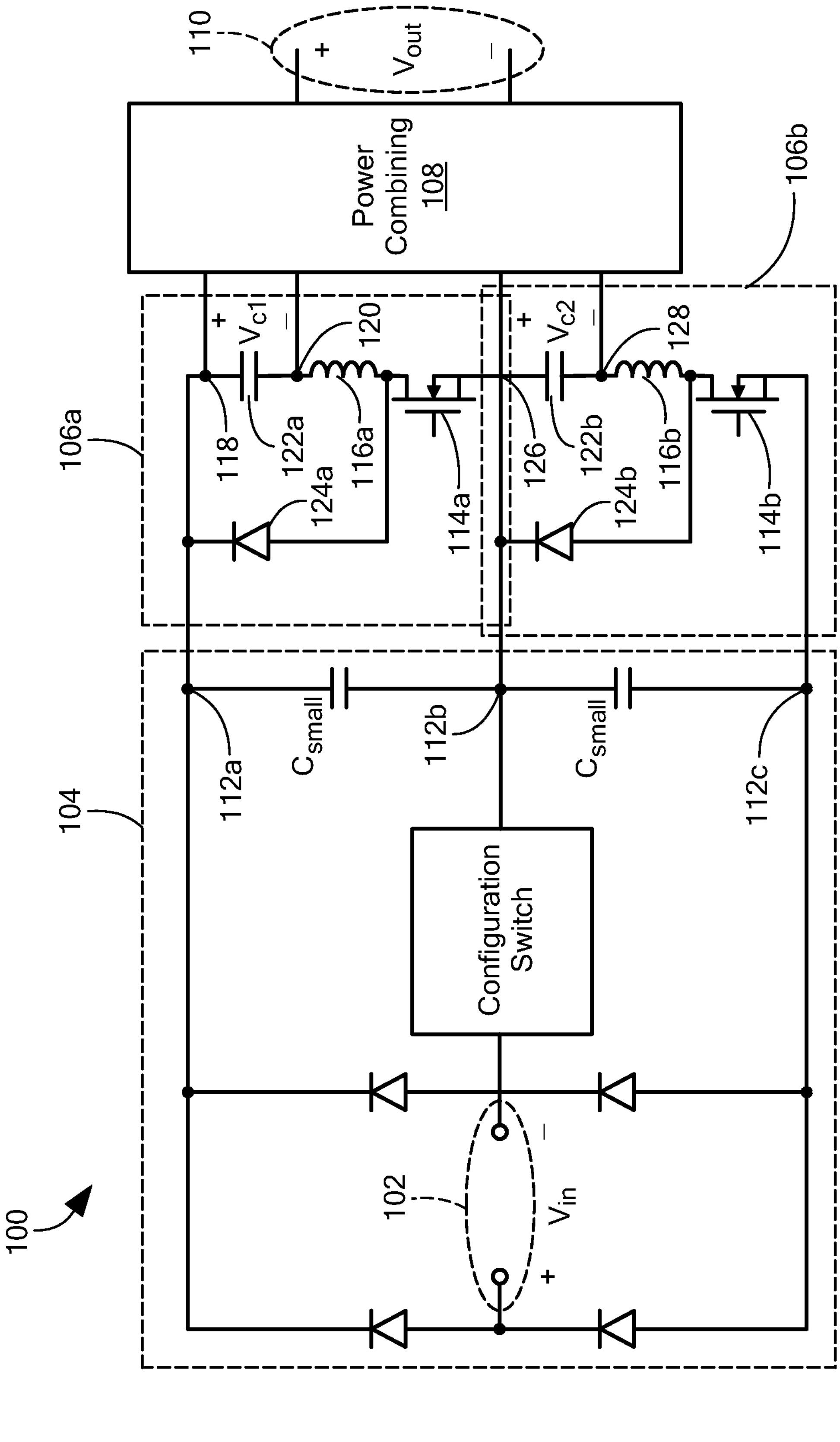
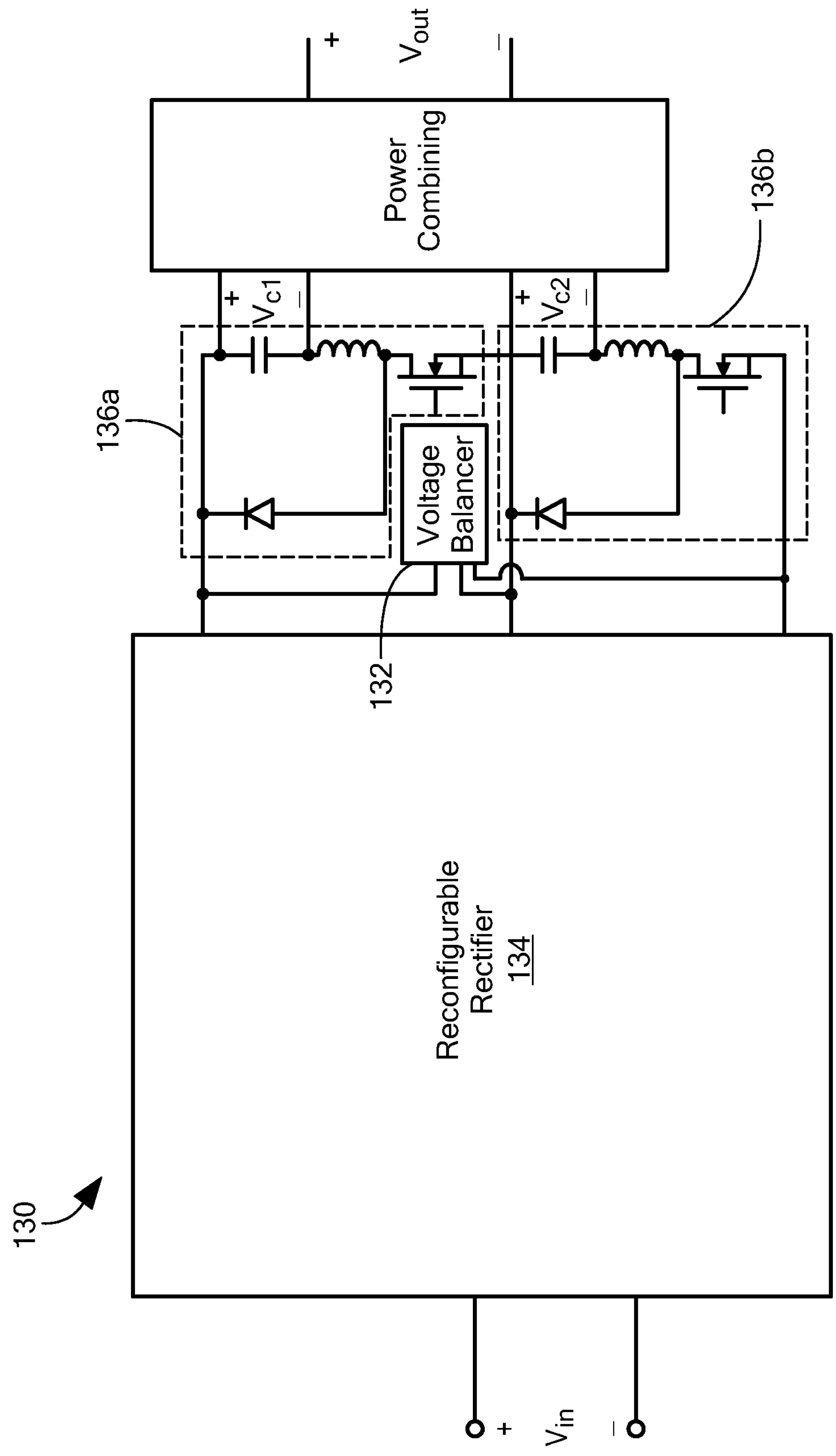

110
+
V_{out}
–
Power Combining 108
106b
106a
+
V_{c1}
–
120
+
V_{c2}
–
128
118
122a
116a
126
122b
116b
124a
114a
124b
114b
104
C_{small}
112a
112b
C_{small}
112c
Configuration Switch
100
102
–
V_{in}
+

FIG. 5



Vout
Power Combining
136b
Vc1
Vc2
136a
Voltage Balancer
132
Reconfigurable Rectifier
134
130
Vin

FIG. 6

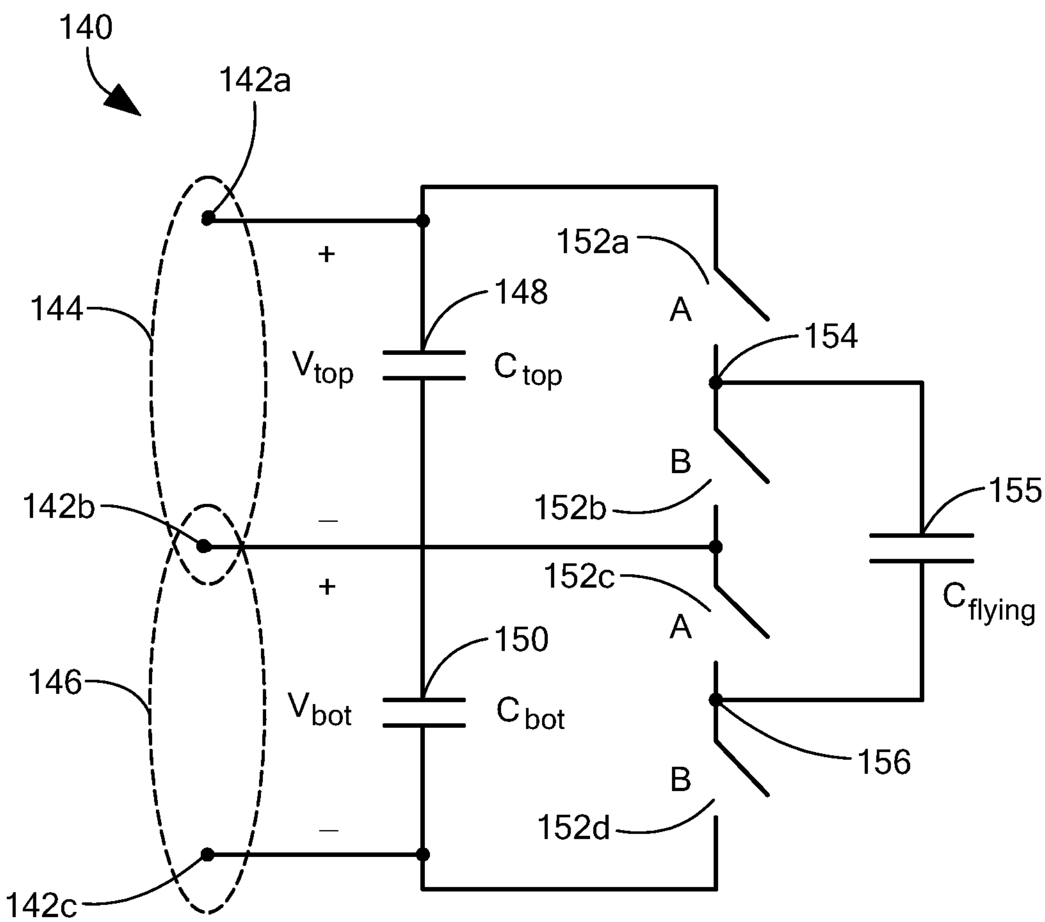

140
142a
144
142b
146
142c
+
–
+
–
148
Vtop
Ctop
150
Vbot
Cbot
152a
A
154
B
152b
152c
A
156
B
152d
155
Cflying

FIG. 7

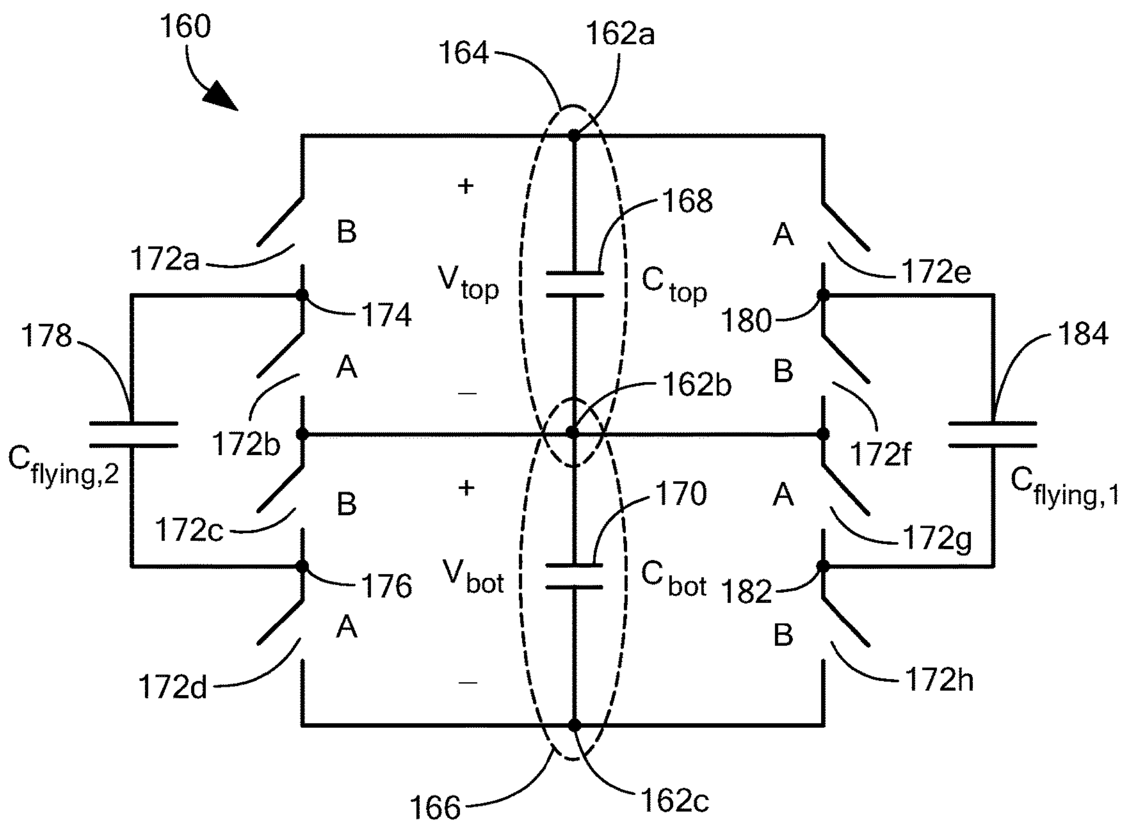

160
164
162a
+
168
B
A
172a
172e
V_{top}
C_{top}
174
180
178
184
A
B
–
162b
$C_{flying,2}$
172b
172f
$C_{flying,1}$
+
170
B
A
172c
172g
176
V_{bot}
C_{bot}
182
A
B
172d
172h
–
166
162c

FIG. 8

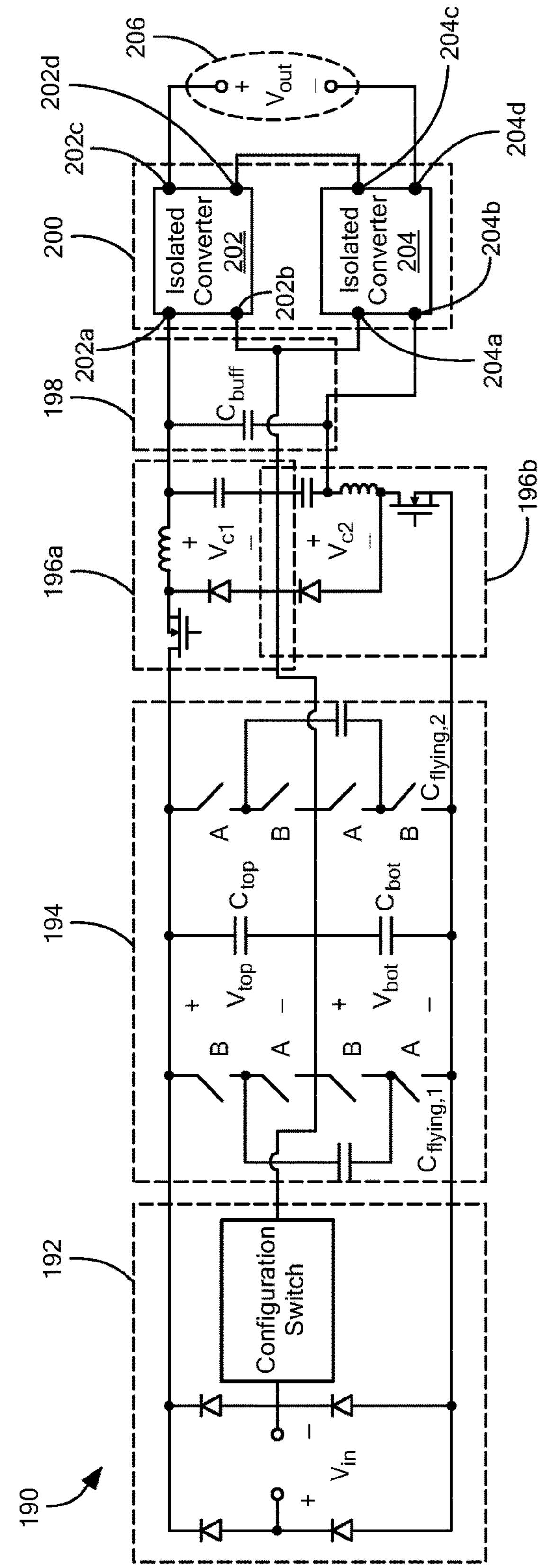

190
192
194
196a
196b
198
200
202a
202b
202c
202d
204a
204b
204c
204d
206
Configuration Switch
Vin
Ctop
Cbot
Vtop
Vbot
Cflying,1
Cflying,2
A
B
Vc1
Vc2
Cbuff
Isolated Converter 202
Isolated Converter 204
Vout

FIG. 9

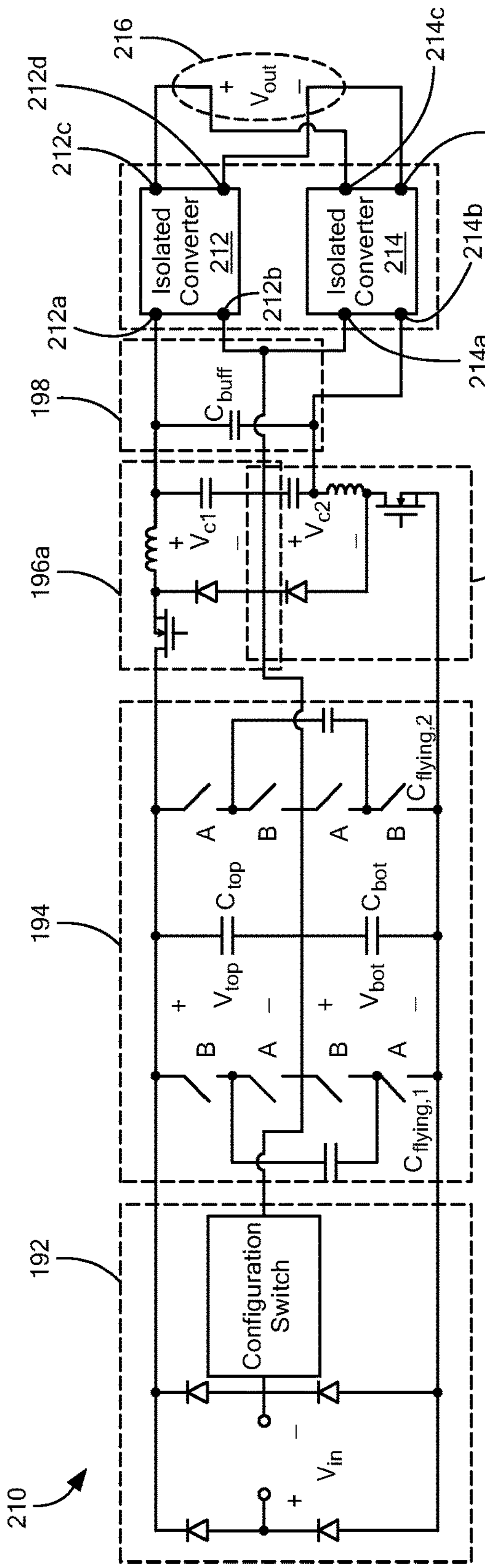

216
Vout
212d
214c
212c
214d
Isolated Converter 212
Isolated Converter 214
212a
212b
214b
214a
198
Cbuff
196a
Vc1
Vc2
196b
194
Cflying,2
Ctop
Cbot
Vtop
Vbot
Cflying,1
A
B
192
Configuration Switch
Vin
210

FIG. 10

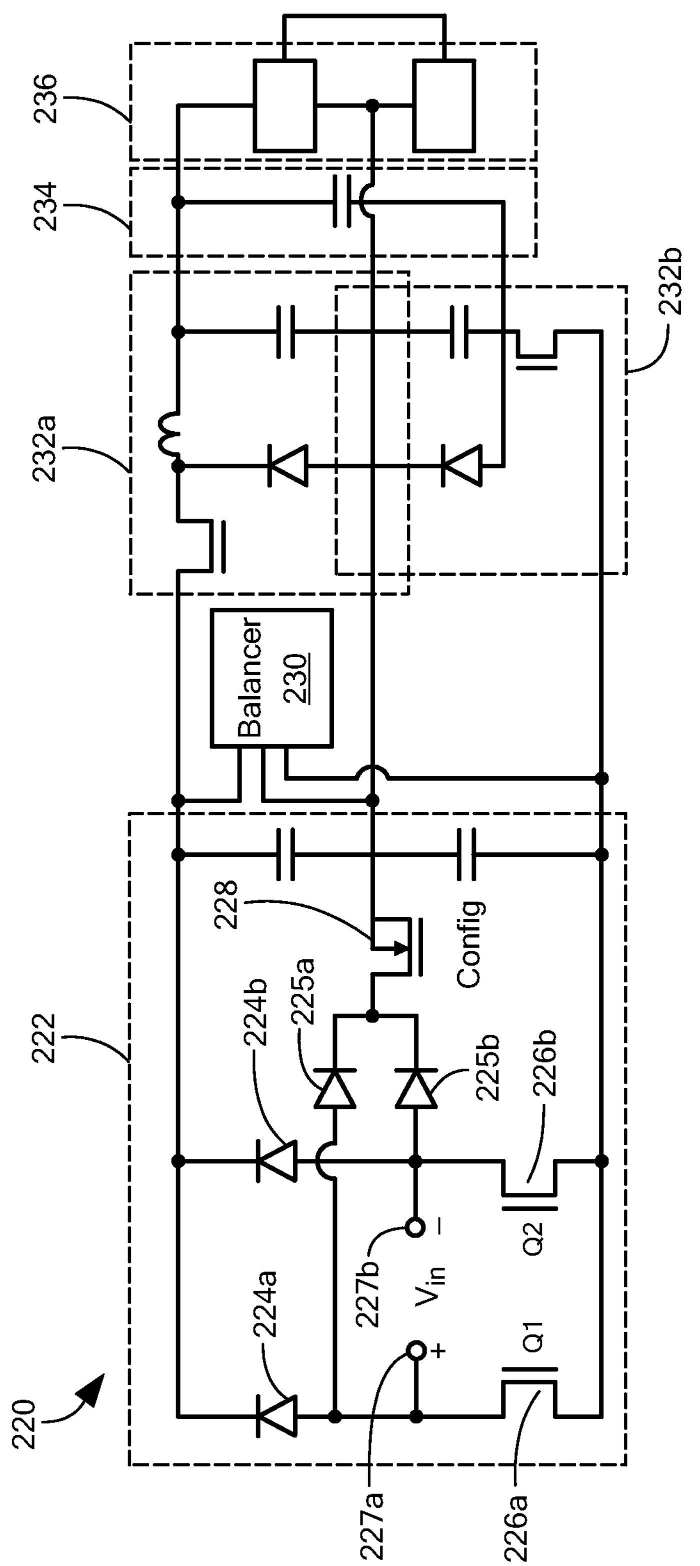

220
222
224a
224b
225a
225b
226a
226b
227a
227b
228
Q1
Q2
V_{in}
+
−
Config
Balancer
230
232a
232b
234
236

FIG. 11

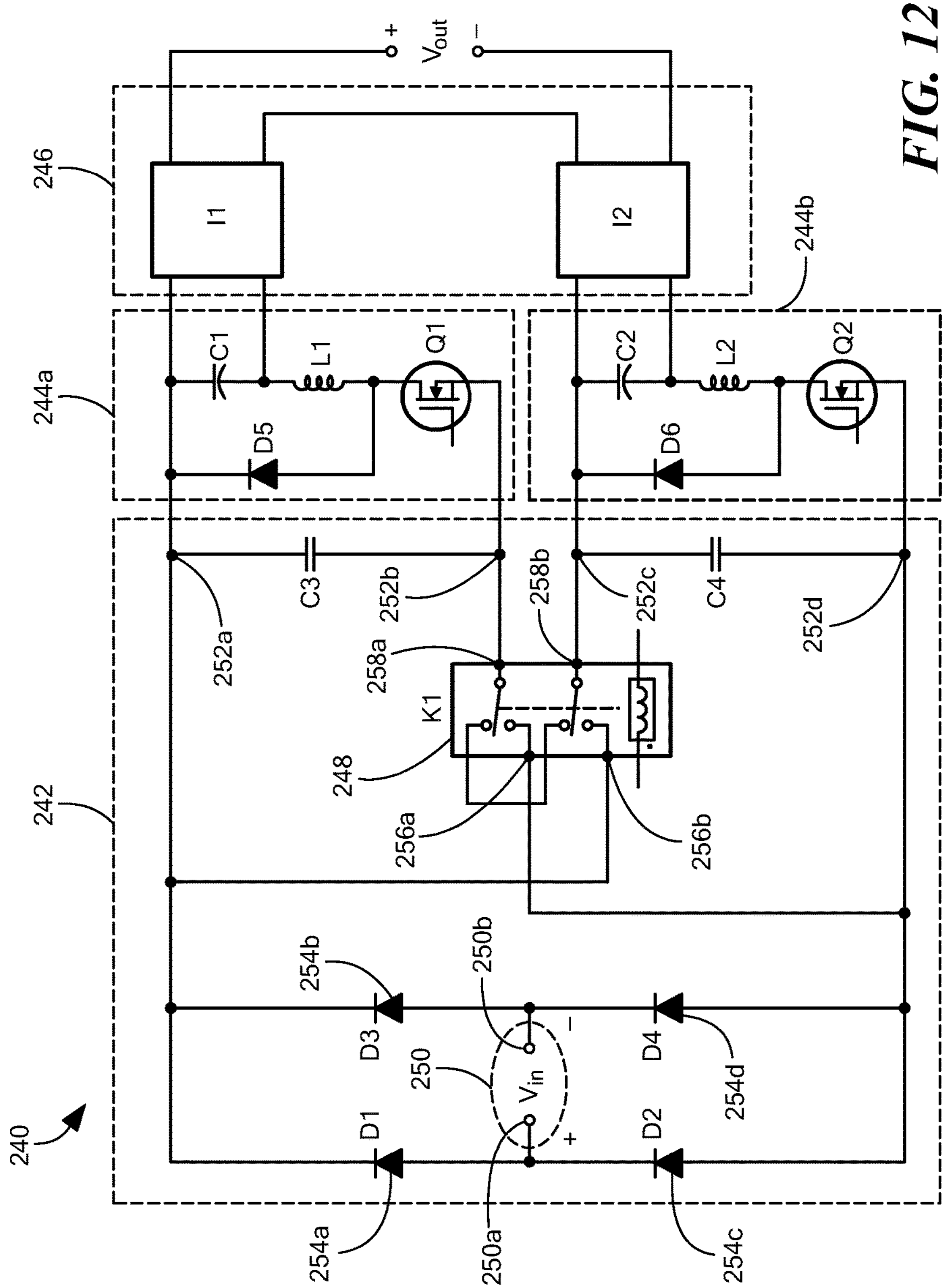

240
242
244a
244b
246
248
250
250a
250b
252a
252b
252c
252d
254a
254b
254c
254d
256a
256b
258a
258b
I1
I2
C1
C2
C3
C4
L1
L2
Q1
Q2
D1
D2
D3
D4
D5
D6
K1
V_{out}
V_{in}
+
−

FIG. 12

HIGH-FREQUENCY, HIGH DENSITY POWER FACTOR CORRECTION CONVERSION FOR UNIVERSAL INPUT GRID INTERFACE

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application No. 62/020,472 filed Jul. 3, 2014, which application is incorporated herein by reference in its entirety.

BACKGROUND

As is known in the art, power converters for supplying dc loads from a single-phase ac grid are used to power many electronic systems. Typical designs must operate on ac input voltage having a relatively wide range (e.g., 85-264 Vrms), and provide a (preferably regulated) dc output. Some applications require an isolated low-voltage dc output (e.g., 24 V). The efficiency of a power converter is also important for many applications (e.g., >95% for a non-isolated output or 90-95% for isolated conversion to low voltage), as is ac line power factor (e.g., >0.9 or >0.95).

Conventional power converters typically operate at relatively low switching frequencies (typically on the order of 200 kHz or below) with associated low power densities (~10 W/in^3 or below). Moreover, at such switching frequencies, the magnetic energy storage components and filters needed for power converters may be relatively large and expensive. Thus, the size and cost of conventional power converters is often dominated by the requirements of the necessary magnetic components.

SUMMARY

In accordance with the concepts described herein, it has been recognized that there is a need for new power electronics technologies that can meet the requirements of practical applications at far lower size and cost than is presently achievable. To achieve these goals, new circuit designs are disclosed herein. Such designs can operate at high frequencies and thus utilize passive energy storage components which are relatively small compared with the size of storage components used in conventional systems. This disclosure describes high-frequency power converter designs that may be well-suited to systems operating at relatively high power levels (e.g., >100 W) from ac universal input voltage. Circuits disclosed herein can provide one or more of the following advantages: low-voltage isolated outputs, high efficiency, and/or power factor while at the same time providing large reductions in the physical size of circuits.

According to one aspect of the disclosure, a circuit comprises a reconfigurable rectifier having an input port configured to receive an alternating current (ac) input signal and first, second, and third output ports, wherein in a first configuration the reconfigurable rectifier is configured to deliver power at the first output port and in a second configuration the reconfigurable rectifier is configured to deliver power to at least the second output port; a voltage balancer having first and second ports, with the first and second ports coupled to the second and third output ports of the reconfigurable rectifier and configured to balance the voltage at the first and second ports; a first converter having an input coupled to the first port of the voltage balancer and having an output at which a first converted voltage signal is provided; and a second converter having an input coupled to the second port of the voltage balancer and having an output at which a second converted voltage signal is provided.

In some embodiments of the circuit, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second output port, wherein the voltage balancer is configured to transfer power received from the second output port of the reconfigurable rectifier such that first and second converters may process substantially equal power levels. In other embodiments, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second and third output ports in alternating half ac cycles, wherein the voltage balancer is configured to transfer power received from the second and third output ports of the reconfigurable rectifier such that first and second converters may process substantially equal power levels.

In various embodiments, the circuit further comprises at least one configuration switch having a first state to place the reconfigurable rectifier in the first and a second state to place the reconfigurable rectifier in a second configuration. The circuit may include a controller, wherein in response to a value of the ac input signal, the controller places the configuration switch in the first or second state.

In certain embodiments of the circuit, the first and second converters are provided as buck converters. For example, the first converter may be a provided as a resonant-transition buck converter and the second converter may be provided as an inverted resonant-transition buck converter.

In some embodiments, the circuit further comprises an energy buffer network having an input coupled to the outputs of the first and second converters and at least one energy storage element (e.g., a capacitor), the energy buffer circuit network configured to provide buffering of twice-line-frequency energy. The outputs of the first and second converters can be connected such that the energy buffer circuit appears across the sum of the output voltages of the first and second converters. In certain embodiments, the energy buffer circuit network comprises three capacitors connected in a delta fashion.

BRIEF DESCRIPTION OF THE DRAWINGS

The concepts, structures, and techniques sought to be protected herein may be more fully understood from the following detailed description of the drawings, in which:

FIG. **1** is a block diagram of a power converter system architecture;

FIG. **2** is a schematic of an illustrative power converter;

FIGS. **3A-3F** are a series of plots of voltage vs. time illustrating the operation of a circuit that can be used as a power converter;

FIGS. **4-6** are a series of schematic diagrams showing additional circuits that may be used within a power converter;

FIGS. **7** and **8** are schematic diagrams showing circuits that may be used within a voltage balancer; and

FIGS. **9-12** are schematic diagrams showing additional circuits that may be used within a power converter.

The drawings are not necessarily to scale, or inclusive of all elements of a system, emphasis instead generally being placed upon illustrating the concepts, structures, and techniques sought to be protected herein.

DETAILED DESCRIPTION

Before proceeding with a description of the architecture, systems, circuits and techniques described herein, some introductory concepts are explained. If a power converter draws energy from wide-input-range ac signal and provides low-voltage output dc, the converter system can be viewed as having two functional aspects. The first is a so-called "Power Factor Correction" (PFC) function, which refers to the ability of the circuit to draw energy from the wide-range ac input at high power factor, buffer the required energy and provide it for use. The second is an isolation, transformation, and regulation function. This includes providing electrical isolation between an ac input and a dc output, transforming whatever (usually large, e.g. 400 V) voltage is obtained from PFC to the (usually low, e.g., 24 V) output voltage, and regulating the output voltage in the face of load variations. Such a converter may be implemented using a "two-stage" architecture having a PFC stage and an isolation stage, with an energy buffer provided between the two stages. Alternatively, the PFC and isolation stages may partially or fully merge these two functions (i.e. a single set of circuitry may perform both of these functions.

The concepts, systems, circuits and techniques disclosed herein can reduce the required size of a power converter through substantial (e.g., >10×) increases in switching frequency relative to existing power converters, while maintaining high efficiency. It should also be appreciated that circuits designed using the concepts disclosed herein can be used to operate at lower frequencies with very high efficiency. Frequency increases can particularly benefit the size of magnetic components (e.g., inductors and transformers) that contribute substantially to converter size.

Achieving miniaturization may require careful attention to loss and parasitic effects that traditionally limit operation. Described herein are concepts, circuit architectures and topologies that take such effects into consideration. For example, with PFC circuitry interfacing to a high-voltage grid, it has been recognized that significant operational advantages can be gained by addressing switching loss through zero-voltage switching (ZVS) or near-ZVS operation. Even with advanced device types, high-efficiency conversion at greatly increased frequencies (e.g., above 1 MHz) generally requires that the high-voltage switches be turned on at relatively low voltage (ideally "zero" voltage) so as to dissipate only a relatively small amount of the energy stored in the device capacitances. Thus, the present disclosure includes circuit designs that provide ZVS or near-ZVS operation.

In addition to the benefits of ZVS soft switching, it has been recognized that in accordance with the concepts described herein parasitic effects may place constraints on switching frequency. In particular it has been recognized that at increased operating frequencies, the capacitances of high-voltage devices may become a design constraint.

As will become apparent from the description provided herein, the disclosure addresses these constraints through multiple features. First, circuit topologies that naturally operate with relatively small inductances and large capacitances (e.g., with low characteristic impedance) are utilized. Such topologies enable use of higher operating frequencies than would otherwise be possible. This, in part, suggests topologies that limit device voltages to as low values as possible, thereby minimizing voltage and increasing current (reduced characteristic impedance, Z_0). This drive towards topologies with low voltage stress is further driven by semiconductor device considerations: the capacitances of high-voltage devices tend to be intrinsically worse than those of low-voltage devices for a given power handling capability, such that the devices in high-voltage-stress designs place greater capacitive constraints on frequency than devices in lower-voltage-stress designs. Thus, some implementations disclosed herein utilize semiconductor devices having relatively low capacitances for a given voltage and current carrying capability (including GaN and SiC devices, when sufficiently economical from a system perspective).

Various circuits described herein utilize resonant-transition buck converters topologies. Resonant-transition buck converters can operate with high current ripple in the inductor and minimum transistor voltage stress, yielding a high achievable switching frequency and small inductor size. Moreover, while such converters operate with ZVS or near-ZVS soft switching over a 2:1 input voltage range, they can maintains high efficiency (with loss of ZVS but still low-loss switching) over an input voltage range of approximately 3:1.

The disclosure includes architectures that are reconfigurable such that the operating range of the individual components can be reduced, enabling better selection of components and operating ranges; and a reduction in the voltages (and ideally, minimizing the voltages) applied to individual power stage elements, enabling increases in frequencies as described above.

Referring to FIG. **1**, a system architecture **10** can be used within a power conversion system to provide PFC functionality in addition to isolation, transformation, and regulation. The illustrative architecture **10** includes a reconfigurable rectifier **12**, a voltage balancer **14**, a plurality of converters (with two converters **16***a* and **16***b* being shown in this example), an energy buffer network **18**, a power combination and isolation network **20**, and a controller **22**. The various architecture elements **12**-**22** may be coupled as shown or in any other suitable arrangement.

Reconfigurable rectifier **12** is provided having an input port **24** configured to receive an ac input signal (herein denoted V_{in} and sometimes referred to as a "ac line voltage"), and having a plurality of output ports **26** (with three output ports **26***a*-**26***c* shown in this example). As used herein, the term "port" refers to a pair of terminals (e.g., positive and a negative voltage terminals). A given terminal may be shared among two or more ports. For example, the three output ports **26***a*-**26***c* may correspond to different combinations of only three distinct terminals, as shown.

The reconfigurable rectifier **12** receives an ac input signal at input port **24** and delivers power to one or more of the output ports **26** according to its instant configuration. For example, in some embodiments, the reconfigurable rectifier **12** supports two distinct configurations, wherein in a first configuration, the reconfigurable rectifier **12** delivers power continuously at a first output port **26***a* and, in a second configuration, the reconfigurable rectifier **12** delivers power to the second port **26***b* for a half line cycle, and to the third output port **26***c* for a different half line cycle. Various other configurations may be supported as discussed further below.

The reconfigurable rectifier **12** includes a switching element (referred to herein as a "configuration switch") having a first state to place the reconfigurable rectifier in a first configuration and a second state to place the reconfigurable rectifier in a second, different configuration. The configuration switch can be driven by a controller **22**, which may be implemented as an application specific integrated circuit (ASIC) or in any other suitable form.

In certain embodiments, the controller **22** is configured to receive at least a portion of the ac input signal (V_{in}) and in response thereto to set the state of reconfigurable rectifier **12** based upon characteristics of the ac signal (e.g. a voltage amplitude level, or "voltage level," associated the ac input signal). For example, the controller may place the reconfigurable rectifier **12** into a first configuration state if a peak ac line voltage exceeds a predetermined threshold value (e.g., 200V) and may place the reconfigurable rectifier **12** into a second configuration state otherwise (e.g. if the peak ac line voltage is below a predetermined threshold).

It will be appreciated the use of a reconfigurable rectifier **12** can reduce (and ideally, minimize) voltage stress and operating range within subsequent conversion elements, such as converters **16**.

The voltage balancer **14** is optional in some embodiments. Voltage balancer **14** includes an input coupled to the reconfigurable rectifier **12** and a plurality of outputs coupled to respective ones of the plurality of converters **16**. In the example shown, an input of the voltage balancer **14** is coupled to the three output ports **26***a*-**26***c* of reconfigurable rectifier **12**, and two voltage balancer outputs **28***a* and **28***b* are coupled to converters **16***a* and **16***b*, respectively. The voltage balancer **14** is configured to balance power received at the input across the first and second outputs. For example, if the reconfigurable rectifier **12** alternates between delivering power at its second and third output ports **26***b*, **26***c*, the voltage balancer may balance the received power to continuously deliver an even amount of power at both its output ports **28***a*, **28***b* (and thus to each of the converters **16***a*, **16***b*).

The converters **16***a*, **16***b* receive rectified signals from the voltage balancer **14** (or directly from the reconfigurable rectifier **12**) and provide (at outputs thereof), a desired output voltage (i.e. an output voltage signal having an output voltage level suitable for the needs of a particular application). As noted above, in some embodiments, the converters **16***a*, **16***b* are provided as resonant-transition buck converters. In certain embodiments, two converters **16***a*, **16***b* are provided in a so-called stacked arrangement, in which a first converter **16***a* is a provided as a resonant-transition buck converter and a second converter **16***b* is provided as an inverted resonant-transition buck converter. It should be appreciated that other topologies could be used for the converters **16***a*, **16***b*, such as boost or buck-boost topologies.

The energy buffer network **18** has an input coupled to the outputs of the converters **16***a*, **16***b* and at least one energy storage element, such as a capacitor. In some embodiments, the energy buffer network **18** comprises a "capacitor stack"—i.e., a set of one or more capacitors in which line-frequency energy is buffered (they may or may not comprise a physical "stack"). In operation, the converters **16***a*, **16***b* can operate at high frequency, drawing energy from an ac grid and charging the capacitors within the energy buffer network **18**. The energy buffer network **18**, in turn, provides buffered energy to subsequent stages.

The power combining and isolation network **20**, which may not be included in all embodiments, combines power from multiple energy buffer outputs (which may corresponding to multiple "stacked" capacitors) into a single output. The network **20** may also provide conversion, isolation, transformation, and/or regulation functionality. In some embodiments, network **20** may be advantageously realized using two isolated telecom "brick" power supplies having their outputs tied either in series or in parallel. In other embodiments, network **20** may be advantageously realized as a multiple-input, single-output isolated dc-dc converter.

Referring to FIG. **2**, an illustrative circuit **40** has an input port **41** configured to receive an ac input signal (V_{in}) and a reconfigurable rectifier **42** coupled to the input port **41**. A first converter **44***a* and a second converter **44***b*, are coupled to the reconfigurable rectifier **42** in a manner which allows converters **44***a*, **44***b* to receive and process different portions of the signal provided from reconfigurable rectifier **42**. An energy buffer network **46** is coupled to the converters **44***a*, **44***b* and to an output port **80** to provide a regulated dc output voltage (V_{out}). It will be appreciated that the circuit **40** utilizes portions of the architecture **10** from FIG. **1** and may be used, for example, as a PFC stage in a power converter.

In the illustrative embodiment of FIG. **2**, the reconfigurable rectifier **42** comprises a full bridge rectifier having a configuration switch **48** coupled thereto to selectively enable use of a third output terminal. In particular, the reconfigurable rectifier **42** includes first and second input terminals **50***a* and **50***b* (which may correspond to input port **41**); first, second, and third output terminals **52***a*-**52***c*; a first diode **54***a* coupled in a forward direction between the first input terminal **50***a* and the first output terminal **52***a*; a second diode **54***b* coupled in a forward direction between the second input terminal **50***b* and the first output terminal **52***a*; a third diode **54***c* coupled in a reverse direction between the first input terminal **50***a* and the third output terminal **52***c*; a fourth diode **54***d* coupled in a reverse direction between the second input terminal **50***b* and the third output terminal **52***c*; and a configuration switch **48** coupled between the second input terminal **50***b* and the second output terminal **52***b*.

The reconfigurable rectifier **42** may further include a first smoothing capacitor **56***a* coupled between the first and second output terminals **52***a* and **52***b*, and a second smoothing capacitor **56***b* coupled between the second and third output terminals **52***b* and **52***c*, as shown. The capacitance values of capacitors **56***a*, **56***b* are selected in accordance with the expected needs of a particular application and the specific capacitor characteristics are selected, at least in part, based upon the expected voltage levels and signal fluctuations to which the capacitors will be exposed. In particular, capacitors **56***a* and **56***b* may be selected to filter/bypass the switching frequency components of currents from converters **44***a* and **44***b* (with low impedance and small voltage ripple at those frequencies), while providing relatively high impedance to line-frequency currents from the reconfigurable rectifier **42** (with substantial voltage ripple at line frequency).

The configuration switch **48** may be provided as any suitable type of switch (e.g. provided from one or more switching elements). In some embodiments, the switch **48** is provided as a low-frequency, low-loss switch. In the illustrative embodiment of FIG. **2**, the configuration switch **48** comprises a pair of field-effect transistor (FET) switches **60***a*, **60***b* arranged in series between nodes **50***b* and **52***b* (the terms "node" and "terminal" are used interchangeably herein). Alternatively, a relay, latching relay, solid-state relay, Triac, or 4-quadrant switch could be used.

Gate terminals of FET switches **60***a*, **60***b* may be coupled to a switch control terminal **62** which in turn may be coupled to a controller such as controller **22** described above in conjunction with FIG. **1**. The controller (or other suitable circuit) provides gate bias signals to switch the FETs **60***a*, **60***b* between their conductive and non-conductive states corresponding, respectively, to "ON" (or "closed") and "OFF" (or "open") states of configuration switch **48**. In it's OFF state, configuration switch **48** provides a high impedance path (ideally an open circuit impedance path) between nodes **50***b* and **52***b*. Conversely, its ON state, configuration switch **48** provides a low impedance path (ideally a shorts circuit impedance path) between nodes **50***b* and **52***b*. As noted above, configuration switch **48** may be driven by any suitable means. For reasons which will become apparent from the description herein below, in some embodiments, the configuration switch **48** is placed into its open state when the peak ac line voltage exceeds 200 V (or some other predetermined threshold voltage), and is placed into its a closed state otherwise.

Converters **44***a*, **44***b* may be provided with their inputs stacked in series, as shown. In particular, the converter **44***a* is provided having an input port corresponding to nodes **52***a* and **52***b* and an output port corresponding to nodes **64** and **66**, whereas converter **44***a* is provided having an input port corresponding to nodes **52***b* and **52***c* and an output port corresponding to nodes **66** and **68**.

The illustrative converter **44***a* comprises an active switch **70***a* and an inductor **72***a* serially coupled between nodes **52***a* and **64**, and a diode **74***a* having an anode terminal coupled to nodes **52***b* and **66** and a cathode terminal coupled between the active switch **70***a* and the inductor **72***a*, as shown. The illustrative converter **44***b* includes an active switch **70***b* and an inductor **72***b* coupled in series between nodes **52***c* and **68**, and a diode **74***b* having a cathode terminal coupled to nodes **52***b* and **66** and an anode terminal coupled between the active switch **70***b* and the inductor **72***b*, as shown. It will be appreciated that converters **44***a*, **44***b* both utilize a resonant-transition buck converter design, with the converter **44***b* being inverted relative to converter **44***a*. The inductors **72***a*, **72***b* may be selected to provide approximately 100% ripple ratio at the desired switching frequency range and to ring with diode **74***b* and switch capacitance for zero-voltage switching in a time significantly shorter than the desired switching period for an operating point. Illustrative designs of such resonant-transition buck converters (either inverted or noninverted) are described in Lim, et. al. "Two-Stage Power Conversion Architecture Suitable for Wide Range Input Voltage", IEEE Transactions on Power Electronics, Vol. 30, No. 2, pp. 805-816, February 2015.

In this illustrative embodiment, converters **44***a*, **44***b* are coupled across a single output port formed by energy storage elements **76***a*, **76***b* (here shown as capacitors **76***a*, **76***b*) coupled between nodes **64** and **68**. In other embodiments, each converter provides a separate output port. In such embodiments, a power combining circuit may be included to combine the individual converter outputs.

In some embodiments, capacitors **76***a* and **76***b* may be selected to principally filter the switching frequency components of the outputs of buck converters **44***a* and **44***b*, while capacitor **77** (at higher voltage and higher energy storage capability) may provide buffering of twice-line-frequency energy and/or holdup energy to power the system output in the event of a temporary interruption in line power. In other embodiments, these duties—twice-line-frequency energy buffering, holdup energy and switching ripple filtering—may be distributed among the three capacitor elements **76***a*, **76***b*, and **77**. It is also noted that while single capacitors **76***a*, **76***b*, and **77** are shown, these may each be realized as paralleled capacitors of similar and/or different types, including ceramic capacitors, film capacitors and electrolytic capacitors. Electrolytic capacitors may be preferable for energy buffering, while film and ceramic capacitors may be preferred for switching ripple filtering.

The illustrative energy buffer network **46** includes an input port corresponding to nodes **64** and **68**, an output port **80** corresponding to nodes **78***a* and **78***b*, and a plurality of stacked output capacitors **76** (with two output capacitors **76***a* and **76***b* shown in this example). A first output capacitor **76***a* may be coupled between nodes **64** and **66** and a second output capacitor **76***b* coupled between nodes **66** and **68**. The energy buffer network **46** may also include a capacitor **77** coupled in parallel with the output capacitors **76**, as shown.

In various embodiments, capacitor **77** has a substantially larger capacitance compared to capacitors **76***a*, **76***b*.

The minimum size of capacitors **76***a* and **76***b* may be selected such that they can pass the switching ripple current from inductors **72***a* and **72***b* with small switching voltage ripple. In embodiments when capacitor **77** provides the dominant energy buffering element, its minimum size may be selected to provide buffering of the twice-line-frequency energy with relatively small voltage ripple and to provide a sufficient rms current rating to pass the twice-line-frequency current components. Twice-line-frequency energy may be, for example, on the order of $P_{average}/(2\pi^* f_{line})$, where $P_{average}$ is the maximum average system output power and f_{line} is the minimum ac line frequency) with relatively small voltage ripple and has a sufficient rms current rating to pass the twice-line-frequency current components. In applications where holdup energy is required, capacitor **77** may be sized such that it can provide the desired output power for the required duration with acceptable voltage droop for the following stage. In cases where both capacitors **76***a* and **76***b* provide energy buffering, the net storage of the three capacitors **76***a*, **76***b*, and **77** can be sized according to the above guidelines.

It should be appreciated that capacitors **76***a*, **76***b*, and/or **77** may be implemented either as part of the converter circuit, as part of an energy buffer circuit, or both.

The circuit **40** can operate to provide ac to dc power conversion over a wide range of peak ac input voltages (e.g., 85-264 Vrms) and is suitable for operation in the mega-Hertz (MHz) frequency range.

The instantaneous operation of the converters **44***a*, **44***b* depends upon the reconfigurable rectifier **42**, which in turn depends on the state of the configuration switch **48**. With the configuration switch **48** in the open state (e.g., for operation with ac line voltages above predetermined threshold voltage—e.g. 200 V), the reconfigurable rectifier **42** functions as a full-wave rectifier delivering power across the first and third output terminals **52***a*, **52***c* (which may correspond to first output port). Thus, the two converters **44***a*, **44***b* draw the same current from the input (sharing input voltage equally) and deliver the same current to the combined output (i.e., across terminals **64**, **68**).

With the configuration switch **48** in the closed state (e.g., for operation with ac line voltages less than or equal to the predetermined threshold voltage—e.g. 200 V), the reconfigurable rectifier **42** functions similar to a voltage doubler. The top converter **44***a* operates when the ac line voltage is positive and the bottom converter **44***b* operates when the ac line voltage is negative. Thus, each converter **44***a*, **44***b* operates to process full power for approximately half the line cycle.

As a consequence of this circuit reconfiguration, the HF converters **44***a*, **44***b* can be optimized for a narrower operating range (voltage and currents ranges) and can operate at lower voltage compared to conventional approaches. These factors both facilitate scaling the power stage to high frequency. In particular, the converters **44***a*, **44***b* can be rated for a peak input voltage of half the maximum ac input voltage, and for an rms input current that is only 0.707 times the maximum rms ac input current. In one example, with peak input voltages of each of the stacked converters **44**, **44***b* below 200 V, high efficiency can be achieved for output of the converters **44***a*, **44***b*, each in the range of 65-85 V, for a total output voltage selected in the range of 130-170 V (where the actual output voltage may be selected based on desired output voltage and input power factor).

The pair of converters **44***a*, **44***b* can operate as a soft-switched HF power stage. Combined with the circuit reconfiguration, the stacked arrangement of the converters **44***a*, **44***b* reduces the individual input voltages of the converters (e.g., to <200 V each) for "universal" ac input voltage (e.g., input voltage in the range 85-264 Vrms). Moreover, the topology used for the converters **44***a*, **44***b* can operate with minimum voltage stress and using relatively small magnetic components at high efficiency. Each of these factors benefits achieving greatly increased frequency.

The size of the electrical components (e.g., capacitors and inductors) used with the circuit **40** may be selected based on the desired PFC output voltage (Vout) and the required input power factor. Line-frequency energy and holdup energy buffering is done by the output capacitors, and required energy buffer capacitor size can be reduced by allowing a greater swing across the output capacitor.

FIGS. **3**A-**3**F illustrate the operation of circuit **40** (FIG. **2**) for various ac input voltages. Each of FIGS. **3**A-**3**F shows a graph of electrical characteristics (voltage and current) at a particular node (or pair of nodes) with the circuit. Within each of the FIGS. **3**A-**3**F, time is indicated by the x axis, voltage is indicated by a respective voltage waveform **90***a*-**90***f* and by the left-side y axis, and current is indicated by a respective current waveform **92***a*-**92***f* and by the right-side y axis.

FIG. **3**A illustrates voltage **90***a* and current **92***a* of a 240 Vrms ac input signal over one line cycle (60 Hz). The voltage **90***a* and current **92***a* may correspond to measurements taken at input port **41** of FIG. **2**. FIGS. **3**B and **3**C illustrate voltage and current delivered to the top converter **44***a* and the bottom converter **44***b*, respectively, in response to the input signal of FIG. **3**A when the configuration switch **48** is open. With the configuration switch open, each converter **44***a*, **44***b* operates at 120 Hz conducting every half-line cycle, as shown.

FIG. **3**D illustrates voltage **90***d* and current **92***d* of a 120 Vrms ac input signal over one ac cycle (60 Hz). FIGS. **3**E and **3**F illustrate voltage and current delivered to the top converter **44***a* and the bottom converter **44***b*, respectively, in response to the input signal of FIG. **3**D when the configuration switch **48** is closed. With the configuration switch closed, the top converter **44***a* conducts when the line voltage is positive, and the top converter **44***b* conducts when the line voltage is negative, as shown.

As shown in FIGS. **3**A-**3**F, when operating with the configuration switch **48** closed (e.g., with a 120 Vrms input), the converters **44***a*, **44***b* may be required to process twice the peak power over a line cycle compared to operation with the configuration switch **48** open (e.g., with a 240 Vrms input). This is because the converters **44***a*, **44***b* each operate only half the time. Thus, the converters **44***a*, **44***b* must designed for a larger peak power, which may require using larger component sizes (e.g., larger-volume inductors **72***a*, **72***b*).

Referring to FIG. **4**, a circuit **82** is similar to circuit **40** of FIG. **2**, but includes a voltage balancer **84** coupled between a reconfigurable rectifier **85** and stacked converters **88***a*, **88***b*. In particular, the voltage balancer **84** may be coupled to three output terminals **86***a*-**86***c* of the reconfigurable rectifier **85**, as shown.

The voltage balancer **84** is configured to distribute energy to both converters **88***a*, **88***b* (preferably equally) when a configuration switch **87** is closed. With this configuration, the converters **88***a*, **88***b* can operate during the same fraction of the line cycle and draw the same current regardless of whether the configuration switch **87** is open or closed.

Thus, the peak power rating of the converters **88***a*, **88***b* can be reduced compared to circuit design of FIG. **2**. Example implementations of a voltage balancer **84** are shown in FIGS. **7** and **8** and described below in conjunction therewith.

FIG. **5** illustrates a circuit design for use in a power conversion system. One limitation of the circuit design of FIG. **2** is that one of the HF buck converters (i.e., converter **88***a*) has its active switch referenced to a so-called "flying node" (i.e., a node coupled to receive relatively high-frequency signals). This approach may limit the frequency or efficiency at which that converter can operate. The circuit design of FIG. **5** removes this limitation by using two "inverted" resonant-transition buck converters, both of which have their switches referenced to relatively slowly moving nodes. With this design, the HF stage has two separate outputs that must be combined, either by a dedicated non-isolated combing stage or by an isolation/transformation/regulation stage.

Turning to FIG. **5**, an illustrative circuit **100** comprises an input port **102** configured to receive an ac input signal (V_{in}); a reconfigurable rectifier **104** coupled to the input port **102**; a first ("top") converter **106***a* and a second ("bottom") converter **106***b*, both of which are coupled to the reconfigurable rectifier **102**; and a power combining circuit **108** coupled to both converters **106***a*, **106***b* and configured to provide combined output voltage (V_{out}) at an output port **110**. It will be appreciated that the circuit **100** utilizes portions of the architecture **10** from FIG. **1** and may be used, for example, as a PFC stage in a power converter.

The reconfigurable rectifier **104**, which has first, second, and third output terminals **112***a*-**112***c*, may be the same as or similar to the reconfigurable rectifier **42** of FIG. **2**.

Both the top and bottom converters **106***a*, **106***b* in FIG. **5** maybe the same as or similar to the bottom converter **44***b* of FIG. **2**. That is, both converters **106***a*, **106***b* may utilize an inverted buck converter design, including an inverted resonant-transition buck converter.

The illustrative top converter **106***a* includes a first output terminal **118** coupled to node **112***a*, a second output terminal **120**, an energy storage element **122***a* (here shown as a capacitor **122***a*) coupled between the first and second output terminals **118**, **120**, an active switch **114***a* and an inductor **116***a* coupled in series between nodes **112***b* and **120**, and a diode **124***a* having a cathode terminal coupled to node **112***a* and an anode terminal coupled between the active switch **114***a* and the inductor **116***a*, as shown.

The illustrative bottom converter **106***b* includes a first output terminal **126** coupled to node **112***b*, a second output terminal **128**, an energy storage element **122***b* (here shown as a capacitor **122***b*) coupled between the first and second output terminals **126**, **128**, an active switch **114***b* and an inductor **116***b* coupled in series between nodes **112***c* and **128**, and a diode **124***b* having a cathode terminal coupled to nodes **112***b* and an anode terminal coupled between the active switch **114***b* and the inductor **116***b*, as shown.

Thus, whereas the stacked converters **44***a*, **44***b* of FIG. **2** provide a single output port (i.e., across nodes **64** and **68**), the converters **106***a* and **106***b* in FIG. **5** each provides a separate output, denoted Vc**1** and Vc**2**, respectively. In circuit **100**, capacitors **122***a* and **122***b* may thus provide both ripple frequency filtering and energy buffering, including twice-line-frequency energy buffering and providing holdup energy in the case of a temporary interruption of the ac line voltage.

The power combining circuit **108** is configured to combine the two converter outputs Vc**1** and Vc**2**. The circuit **108** may also provide other functionality, such as buffering, isolation, transformation, and/or regulation. The power combining circuit **108** can be implemented using any suitable circuit design.

One approach to efficiently combining the two converter outputs is to use a switched-capacitor power combining circuit. Since relatively large capacitors must be already present in the system to satisfy holdup and line-frequency energy buffering requirement, a switched-capacitor power combining stage can be implemented with very high efficiency and negligible impact on size.

A second approach to combining the two converter outputs Vc**1** and Vc**2** is to realize the circuit **108** as an isolation/transformation/regulation stage. Because the individual outputs Vc**1**, Vc**2** can be selected to have voltages in the range below 75 V, one can realize the circuit **108** with a pair of standard high efficiency "brick" converters with their inputs connected to Vc**1** and Vc**2**, respectively, and their outputs connected in series or parallel on the isolated output side to supply a voltage (Vout) at output port **110**. Control can be realized through appropriate modulation of the current sharing and enable controls often provided in such converters. This design approach can thus take advantage of standardized high-volume converter designs for the second stage. This may even enable elimination of downstream conversion stages (e.g., to logic-level voltages) in some applications.

A third approach to implementing the power combining circuit **108** is to realize a true dual-input, single-output magnetic stage (e.g., including isolation). Such a design, when customized to the application, can achieve higher densities and efficiencies that are possible with standard "brick" style converters. Moreover, this approach is amendable to being realized at high frequencies using "integrated magnetics," in which multilayer transformers are printed as part of the circuit board.

Referring to FIG. **6**, a circuit **130** is similar to circuit **100** of FIG. **5**, but includes a voltage balancer **132** coupled between a reconfigurable rectifier **134** and two converters **136***a*, **136***b*. As explained above in conjunction with FIG. **4**, a voltage balancer **132** can be configured to distribute energy to both converters **136***a*, **136***b* (preferably equally) in response to a first configuration of reconfigurable rectifier **134** (e.g. when a configuration switch is closed). Thus, in operation, both converters **136***a*, **136***b* operate during the same fraction of the line cycle and draw the same current regardless of whether the configuration switch is open or closed and the peak power rating of the HF buck converters **136***a*, **136***b* can be reduced compared to the design of FIG. **5**.

FIGS. **7** and **8** show illustrative circuit designs that may be used within a voltage balancer, such as voltage balancer **84** in FIG. **4** and/or voltage balancer **132** in FIG. **6**. It will be appreciated that while FIGS. **7** and **8** show switched-capacitor voltage balancers, one may also utilize switched inductor voltage balancers, resonant switched capacitor voltage balancers, and other known balancer circuits.

Referring to FIG. **7**, an illustrative circuit **140** comprises a first port **144** corresponding to terminals **142***a* and **142***b*, a second port **146** corresponding to terminals **142***b* and **142***c*, a first capacitor **148** coupled across the first port **144**, a second capacitor **150** coupled across the second port **146**, a first switch **152***a* coupled to nodes **142***a* and **154**, a second switch **152***b* coupled to nodes **154** and **142***b*, a third switch **152***c* coupled to nodes **142***b* and **156**, a fourth switch **152***d* coupled to nodes **156** and **142***c*, and a third capacitor **155** coupled to nodes **154** and **156**. Capacitance values can be selected to provide the desired peak energy transfer rated at a desired switching frequency and efficiency in accordance with well-known design approaches for switched-capacitor converters, such as described in M. Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," IEEE Transactions on Power Electronics, vol. 23, no. 2, March 2008.

Each of the switches **152***a*-**152***d* has an open state (i.e., a state in which a substantially open circuit impedance path exists between the switch terminals) and a closed state (i.e. a state in which a substantially short circuit impedance path exists between the switch terminals). The first and third switches **152***a* and **152***c* (collectively referred to as switch "A") may be configured to be opened and closed in unison. Likewise, the second and fourth switches **152***b* and **152***d* (collectively referred to as switch "B") may be configured to be opened and closed in unison. The switches can be driven by any suitable means, such as via controller **22** shown in FIG. **1**.

In one embodiment, switches A and B are operated in complementary fashion (i.e. when one is on the other is off), as shown in TABLE 1. The switches A and B may each be operated with 50% duty ratio. As a result, the third (or "flying") capacitor **155** shuffles charge from the first (or "top") capacitor **148** to the second (or "bottom") capacitor **150**, or vice versa. For practice control reasons, all switches may be turned off for a least a portion of the duty cycle (sometimes referred to as "dead times").

TABLE 1

	Switch	
	A	B
State 1	Open	Closed
State 2	Closed	Open

The circuit **140** can function as a voltage balancer coupled between a reconfigurable rectifier and a pair of converters. In particular, the three terminals **142***a*-**142***c* may be coupled to three output terminals of the reconfigurable rectifier. For example, the terminals **142***a*, **142***b*, and **142***c* may be coupled to terminals **86***a*, **86***b*, and **86***c* of FIG. **4**, respectively. If the switching frequency of circuit **140** is significantly higher than ac input line frequency, a voltage level (Vtop) at the first port **144** will have approximately the same value in steady state as the voltage level (Vbot) at the second port **146**. Thus, the circuit **140** can provide approximately equal voltages to both converters (e.g., converters **88***a* and **88***b* of FIG. **4**) regardless of whether the configuration switch is open or closed.

The switching frequency of circuit **140** can be dynamically adapted over the line cycle and/or with power to maximize efficiency, and it can be entirely turned off when the configuration switch is open (e.g., when a signal having a voltage level above a predetermined threshold level is provided to the input of a reconfigurable rectifier such as reconfigurable rectifier **42** in FIG. **2**).

FIG. **8** shows another illustrative circuit **160** that can be used within a voltage balancer. The illustrative circuit **160** comprises a first port **164** corresponding to terminals **162***a* and **162***b*, a second port **166** corresponding to terminals **162***b* and **162***c*, a first capacitor **168** coupled across the first port **164**, a second capacitor **170** coupled across the second port **166**, a first switch **172***a* coupled to nodes **162***a* and **174**, a second switch **172***b* coupled to nodes **174** and **162***b*, a third switch **172***c* coupled to nodes **162***b* and **176**, a fourth switch

172*d* coupled to nodes **176** and **162***c*, a third capacitor **178** coupled to nodes **174** and **176**, a fifth switch **172***e* coupled to nodes **162***a* and **180**, a sixth switch **172***f* coupled to nodes **180** and **162***b*, a seventh switch **172***g* coupled to nodes **162***b* and **182**, an eighth switch **172***h* coupled to nodes **182** and **162***c*, and a fourth capacitor **184** coupled to nodes **180** and **182**. These capacitor values may be selected for a given desired switching frequency (which may be in the tens to hundreds of kHz in many applications) based on well-known design principles as described above in conjunction with FIG. **7**.

The interleaved circuit design shown in FIG. **8** has twice as many switches and drivers as the circuit **140** of FIG. **7**, but has the advantage of requiring smaller overall capacitance and reducing the current ripple significantly, effectively decreasing the volume of input-side filters, such as EMI filters.

The four switches **172***b*, **172***d*, **172***e*, and **172***g* (collectively referred to as switch "A") are may be configured to be opened and closed in unison. Likewise, the four switches **172***a*, **172***c*, **172***f*, and **172***h* (collectively referred to as switch "B") are may be configured to be opened and closed in unison. The two switches A and B may be operated in complementary fashion, as shown in TABLE 1 and as described above in conjunction with FIG. **7**. In operation, the third and fourth capacitors **178** and **184** "shuffle" charge from the first capacitor **168** to the second capacitor **178**, and vice versa. Each half of the circuit operates 180 degrees out of phase, which can cancel a current ripple in capacitors **168** and **170**.

As with circuit **140** of FIG. **7**, the circuit **160** can be coupled between a reconfigurable rectifier and a pair of converters, and the switching frequency of circuit **140** can be dynamically adapted over the line cycle and/or with power to maximize efficiency.

FIGS. **9** and **10** show how industry standard telecom converters (e.g., "brick" converters, "half-brick" converters, "quarter-brick" converters, "eighth brick" converters, etc.) can be used within a power combining and isolation circuit (e.g., circuit **20** of FIG. **1**). Such converters have galvanic isolation, which allows the outputs to be coupled in series or parallel, depending on the desired output voltage and what is best available among such converters in the marketplace. For example, for a 100 W PFC converter, each output brick converter might be designed to operate at 50 W and a 5 V output. Depending on the application, the outputs of the brick converters could be coupled in such a way to obtain an output of 5 V and 20 A (outputs coupled parallel) or 10 V and 10 A (outputs coupled in series).

Referring FIG. **9**, an illustrative circuit **190** includes a reconfigurable rectifier **192**, a voltage balancer circuit **194**, two converters **196***a* and **196***b*, an energy buffer circuit **198**, and a power combining and isolation circuit **200**. The circuit portions **192-200** may be coupled as shown, or in any other suitable manner.

The power combining and isolation circuit **200** includes two isolated converters **202** and **204**, which may be provided as standard telecom converters. A first isolated converter **202** includes a first input terminal **202***a*, a second input terminal **202***b*, a first output terminal **202***c*, and a second output terminal **202***d*. A second isolated converter **204** includes a first input terminal **204***a*, a second input terminal **204***b*, a first output terminal **204***c*, and a second output terminal **204***d*. The isolated converter outputs are coupled in series, with the second output terminal **202***d* of converter **202** coupled to the first output terminal **204***c* of converter **204**. The input terminals of the isolated converters **202**, **204** can be coupled such that each converter is fed from one of the converters **196***a*, **196***b*, as shown.

The first output terminal **202***c* of the converter **202** and the second output terminal **204***d* of the converter **204** may correspond to the output port **206** of the circuit **190**.

Referring to FIG. **10** in which like elements of FIG. **9** are shown having like reference designations, a circuit **210** includes two isolated converters **212** and **214**, whose outputs may be coupled in parallel. A first isolated converter **212** includes a first input port **212***a*, a second input port **212***b*, a first output port **212***c*, and a second output port **212***d*. A second isolated converter **214** includes a first input port **214***a*, a second input port **214***b*, a first output port **214***c*, and a second output port **214***d*. The first output terminal **212***c* of converter **212** may be coupled to the first output terminal **214***c* of converter **214**, and the second output terminal **212***d* of converter **212** may be coupled to the second output terminal **214***d* of converter **214**, as shown. An output port **216** of the circuit **210** corresponds to terminals **212***c*/**214***c* and **212***d*/**214***d*. It is appreciated that connecting the isolated converter outputs in parallel effectively provides the converter with two different regulated output voltages that can be realized depending on the desired application.

FIG. **11** shows another circuit **220** that can be used within a power converter. The illustrative circuit **220** includes a reconfigurable rectifier **222**, a voltage balancer **230**, two converters **232***a* and **232***b*, an energy buffer circuit **234**, and a power combining and isolation circuit **236**, which may be coupled as shown or in any other suitable manner.

It will be appreciated that the reconfigurable rectifier **222** utilizes a different design compared some of the circuits described above. For example, compared to the reconfigurable rectifier **42** of FIG. **2**, the bottom two diodes **54***c*, **54***d* are replaced by active switches **226***a*, **226***b* (e.g., transistors) and two diodes **225***a*, **225***b* are added that will conduct only when a configuration switch **228** is closed. In the embodiment show, a first diode **225***a* is coupled between a first input terminal **227***a* and a first terminal **228***a* of the configuration switch **228**, and a second diode **225***b* is coupled between a second input terminal **227***b* and the first terminal **228***a* of the configuration switch **228**.

One benefit of this design is that it reduces the number of diode drops in the power path from two to one when the configuration switch **228** is open. Because diodes **225***a* and **225***b* are only used when the configuration switch is closed (which may correspond to low-voltage ac input), these diodes can be rated for lower voltage stress compared to the diodes **224***a* and **224***b*.

The active switches **226***a*, **226***b* can be configured to operate at substantially the same frequency as the ac input signal (i.e., the line frequency) and can have their source voltage referenced to a stable voltage. In some embodiments, the active switches **226***a*, **226***b* are driven by a controller, such as controller **22** of FIG. **1**. In particular, switch **226***a* may be on during the negative half portion of the ac line cycle and switch **226***b* may be on during the positive portion of the ac line cycle.

FIG. **12** shows another circuit **240** that can be used within a power converter. The illustrative circuit **240** includes a reconfigurable rectifier **242**, two converters **244***a* and **244***b*, and a power combining and isolation circuit **246**, which may be coupled as shown or in any other suitable manner.

The illustrative reconfigurable rectifier **242** includes first and second input terminals **250***a* and **250***b* (corresponding to an input port **250**); four output terminals **252***a*-**252***d*; a first diode **254***a* coupled in a forward direction between the first input terminal **250***a* and the first output terminal **252***a*; a second diode **254***b* coupled in a forward direction between the second input terminal **250***b* and the first output terminal **252***a*; a third diode **254***c* coupled in a reverse direction between the first input terminal **250***a* and the fourth output terminal **252***d*; a fourth diode **254***d* coupled in a reverse direction between the second input terminal **250***b* and the fourth output terminal **252***d*; and a relay **248** having a first input terminal **256***a* coupled to terminal **252***d*, a second input terminal **256***b* coupled to terminal **252***a*, a first output terminal **258***a* coupled to terminal **252***b*, and a second output terminal **258***b* coupled to terminal **252***c*.

The relay **258** is configured to connect the converters **244***a* either in series (as shown with the relay positions in FIG. **12**) or in parallel. The series connection may be used for high voltage operation such as 240 Vac line voltage and the parallel connection may be used for low voltage operation such as 120 Vac. This eliminates the need for the voltage balancer circuit used in some of the other implementations. The relay **248** may be provided as a latching relay to reduce (and ideally eliminate) power dissipation. A non-latching relay or solid-state switches could also be used.

Having described certain embodiments, which serve to illustrate various concepts, structures, and techniques sought to be protected herein, it will be apparent to those of ordinary skill in the art that other embodiments incorporating these concepts, structures, and techniques may be used. Elements of different embodiments described hereinabove may be combined to form other embodiments not specifically set forth above and, further, elements described in the context of a single embodiment may be provided separately or in any suitable sub-combination. Accordingly, it is submitted that scope of protection sought herein should not be limited to the described embodiments but rather should be limited only by the spirit and scope of the following claims.

The invention claimed is:

1. A circuit comprising:

a reconfigurable rectifier having an input port configured to receive an alternating current (ac) input signal and first, second, and third output ports, wherein in a first configuration the reconfigurable rectifier is configured to deliver power at the first output port and in a second configuration the reconfigurable rectifier is configured to deliver power to at least the second output port;

a voltage balancer having first and second input ports and first and second output ports, with the first and second input ports of the voltage balancer coupled to the second and third output ports of the reconfigurable rectifier and configured to balance a voltage at the first and second output ports;

a first converter having an input coupled to the first port of the voltage balancer and having an output at which a first converted voltage signal is provided;

a second converter having an input coupled to the second port of the voltage balancer and having an output at which a second converted voltage signal is provided; and

wherein, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second output port, wherein the voltage balancer is configured to transfer power received from the second output port of the reconfigurable rectifier such that the first and second converters may process substantially equal power levels.

2. The circuit of claim **1** wherein, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second and third output ports in alternating half ac cycles, wherein the voltage balancer is configured to transfer power received from the second and third output ports of the reconfigurable rectifier such that the first and second converters may process substantially equal power levels.

3. The circuit of claim **1** further comprising at least one configuration switch having a first state to place the reconfigurable rectifier in the first configuration and a second state to place the reconfigurable rectifier in the second configuration.

4. The circuit of claim **1** further comprising a controller, wherein in response to a value of the ac input signal, the controller places the configuration switch in the first or second state.

5. The circuit of claim **1** wherein the first and second converters are provided as buck converters.

6. The circuit of claim **5** wherein the first converter is provided as a resonant-transition buck converter and the second converter is provided as an inverted resonant-transition buck converter.

7. The circuit of claim **1** further comprising an energy buffer circuit network having an input coupled to the outputs of the first and second converters and at least one energy storage element, the energy buffer circuit network configured to provide buffering of twice-line-frequency energy.

8. The circuit of claim **7** wherein the outputs of the first and second converters are connected such that the energy buffer circuit network appears across the sum of the output voltages of the first and second converters.

9. The circuit of claim **7** wherein the at least one energy storage element comprises at least one capacitor.

10. The circuit of claim **7** wherein the energy buffer circuit network comprises three capacitors connected in a delta fashion.

11. A circuit comprising:

a reconfigurable rectifier having an input port configured to receive an alternating current (ac) input signal and first, second, and third output ports, wherein in a first configuration the reconfigurable rectifier is configured to deliver power at the first output port and in a second configuration the reconfigurable rectifier is configured to deliver power to at least the second output port;

a voltage balancer having first and second input ports and first and second output ports, with the first and second input ports of the voltage balancer coupled to the second and third output ports of the reconfigurable rectifier and configured to balance a voltage at the first and second output ports;

a first converter having an input coupled to the first port of the voltage balancer and having an output at which a first converted voltage signal is provided;

a second converter having an input coupled to the second port of the voltage balancer and having an output at which a second converted voltage signal is provided; and

wherein, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second and third output ports in alternating half ac cycles, wherein the voltage balancer is configured to transfer power received from the second and third output ports of the reconfigurable rectifier such that the first and second converters may process substantially equal power levels.

12. The circuit of claim **11** wherein, in the second configuration, the reconfigurable rectifier is configured to deliver power to the second output port, wherein the voltage balancer is configured to transfer power received from the second output port of the reconfigurable rectifier such that the first and second converters may process substantially equal power levels.

13. The circuit of claim **11** further comprising at least one configuration switch having a first state to place the reconfigurable rectifier in the first configuration and a second state to place the reconfigurable rectifier in the second configuration.

14. The circuit of claim **11** further comprising a controller, wherein in response to a value of the ac input signal, the controller places the configuration switch in the first or second state.

15. The circuit of claim **11** wherein the first and second converters are provided as buck converters.

16. The circuit of claim **15** wherein the first converter is provided as a resonant-transition buck converter and the second converter is provided as an inverted resonant-transition buck converter.

17. The circuit of claim **11** further comprising an energy buffer circuit network having an input coupled to the outputs of the first and second converters and at least one energy storage element, the energy buffer circuit network configured to provide buffering of twice-line-frequency energy.

18. The circuit of claim **17** wherein the outputs of the first and second converters are connected such that the energy buffer circuit network appears across the sum of the output voltages of the first and second converters.

19. The circuit of claim **17** wherein the at least one energy storage element comprises at least one capacitor.

20. The circuit of claim **17** wherein the energy buffer circuit network comprises three capacitors connected in a delta fashion.

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