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Energy and Size Reduction of Grid-Interfaced Energy Buffers Through Line Waveform Control

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***Abstract*—Grid-interface converters with power factor correction (PFC) generally require large energy buffer capacitors to maintain a constant power output. These buffer capacitors can occupy 20-30 % of total system volume, and their size is unaffected by typical methods of miniaturizing power converters such as increasing efficiency or changing switching frequency. Here we investigate an approach in which harmonic current is intentionally drawn from the grid (within allowed regulations) to reduce the required energy storage. We show that this method can substantially reduce the energy storage requirement under every IEC/EN 61000-3-2 regulation class, including Class A (> 60 % reduction), Class B (> 80 %), Class C > 25 W (> 25 %), Class C ≤ 25 W (> 70 %) and Class D (62 %). This benefit can generally be achieved solely through controls without additional hardware and can be applied across PFC converter topologies. A valley-switched boost PFC converter is used to validate that harmonic injection achieves the calculated energy storage reduction with little impact on efficiency. We also show that, for a variable-frequency PFC, the proposed approach beneficially compresses the switching frequency range. This technique thus provides a high-impact, low-cost approach to miniaturizing the energy buffer in grid-interface power converters.**

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The paper is an extension of a conference paper, "A. F. Martin, A. J. Hanson, and D. J. Perreault, "Energy and Size Reduction of Grid-Interfaced Energy Buffers Through Line Waveform Control," in *IEEE Workshop on Control and Modeling of Power Electronics (COMPEL)*, June 2018" [1]. Here we extend the work to cover all IEC/EN 61000-3-2 regulation classes.

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I. Introduction

Grid-interface converters are often required to provide power factor correction (PFC) [2], [3] wherein they draw current having strictly limited harmonic content. The ideal unity power factor case (PF = 1), which draws only sinusoidal current in phase with the grid voltage, leads to a pulsating power waveform ($\propto \sin^2$) with very large instantaneous differences from the (typically) constant load power. The converter must buffer this twice-line-frequency power pulsation, and the resulting low-frequency energy storage $E_{store} = P_o/\omega_{grid}$ is necessarily very large. This storage is typically achieved with electrolytic capacitors, which have low lifetime and can occupy over 50 % of PFC converter volume [4] (20-30 % of overall system volume).

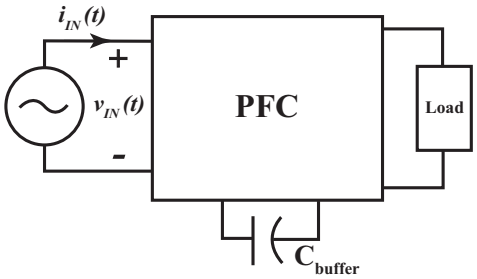

Fig. 1. Three-terminal representation for power converter with PFC, including input from grid source, dc output to load, and ac buffer capacitor.

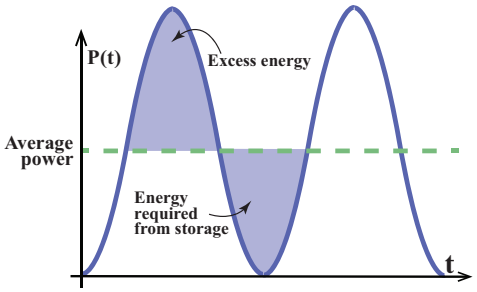

Fig. 2. When PF = 1, power oscillates $\propto \sin^2$; integrating the difference between the input power and the output power gives the energy storage requirement over a line cycle, shown as shaded.

Energy buffer capacitors are stubbornly immune to typical miniaturization approaches when PF = 1 because the energy storage requirement is fixed by factors outside of the circuit designer's control – the power rating of the converter and the frequency of the grid. In other words, the energy storage requirement is not a function of efficiency, topology, architecture, or switching frequency [5].

Some research has observed that the usable energy storage depends on both the buffer capacitance and its voltage swing:

$$E_{store} = \frac{1}{2}CV_{peak}^2 - \frac{1}{2}CV_{trough}^2 = CV_{mid}\Delta V \quad (1)$$

where V_{peak} is the maximum capacitor voltage, V_{trough} is the minimum capacitor voltage, V_{mid} is the arithmetic average of V_{peak} and V_{trough}, and ΔV is the arithmetic difference between V_{peak} and V_{trough}. These works have used high voltage swings ΔV to permit lower capacitance C. Entire converters (sometimes called active buffers) have been designed to emulate a large capacitor while taking advantage of this observation [6]–[9]. These approaches have largely been successful at miniaturizing the energy buffer, but suffer primarily from added component counts while still buffering the same amount of energy.[1]

Here we investigate an alternative approach which fundamentally reduces the amount of twice-line-frequency energy that needs to be stored, which sets the buffer size for many applications.[2] It accomplishes this by purposefully drawing harmonic current, resulting in a more constant input power and therefore less required energy storage. While operating within line harmonic current regulations, we show that this method can substantially reduce energy storage requirements – and consequently energy buffer size – for every IEC/EN 61000-3-2 regulation class (A-D). This approach usually requires no additional hardware and can be applied to many existing PFC converters solely by a change in control.

Energy storage reduction has been explored before, mainly in the context of LED drivers which fall under Class C regulations [14]–[21], but this method has not thoroughly been explored in other classes which are sometimes thought to have substantially stricter regulations [22].[3] Here, in addition to extending the analysis of Class C, we show that this approach maintains substantial benefit for devices operated under Class D and even Classes A and B well into the kilowatt range.

In addition, the side effects introduced by this approach (e.g. loss, frequency variation, etc.) have not been thoroughly explored previously but are investigated here. In particular, we investigate a valley-switched boost PFC both theoretically and with a hardware prototype. For this implementation, we find negligible changes in loss by introducing harmonic input current. We also find a beneficial compression in the operating frequency range (from 4:1 to 1.4:1 for a given average power), which alleviates some of the challenges with using high-efficiency, variable-frequency converters like the valley-switched boost, resonant converters, etc. in PFC applications.

II. The ideal case: No buffer

If we first imagine our goal is to eliminate the need for an energy buffer entirely, in the absence of regulations or notions of power factor, then we would need to draw constant power from the grid, implying that the input line current must be:

$$i_{in,C=0}(t) = \frac{P_{out}}{V_{in}} \frac{1}{\sin(\omega t)} \quad (2)$$

where P_{out} is the dc output power of the PFC stage and V_{in} is the ac line voltage amplitude.

When drawing such a current, since there would be no instantaneous mismatch in power, the energy buffer size could be reduced by 100 % (i.e. no buffer). Undoubtedly, this is not a feasible current to draw, as it clearly violates harmonic limits (Table I) and requires infinite current at zero-crossings of the grid voltage, as illustrated in Fig. 3. Nevertheless, we can take inspiration from this approach and analyze the harmonic content of $i_{in,C=0}$ which is composed of an

[1]For a good review of techniques with reduced component count, see [10]; some techniques require no additional switching devices, but may still add energy storage components [11].

[2]Some uninterruptible applications (e.g. servers and aerospace applications [12]) impose an additional hold-up time requirement wherein the converter must maintain its output power for some duration (e.g. one line cycle) in the event of a voltage interruption. This requirement may dwarf the twice-line-frequency energy buffering requirement and such converters may be unaffected by the proposed technique. Nevertheless, the proposed approach has broad applicability in charger, adapter, appliance, and motor drive applications which have no hold-up time requirement. Note that active power decoupling techniques may have utility in fully utilizing stored energy in hold-up circumstances [13]; nevertheless, since all energy delivered to the load must come from stored energy, the fundamental requirement on stored energy cannot be affected.

[3]Exceptions include [23], [24] which only consider Class D and [25] which considers all classes but with limited harmonic inclusion and a highly specific control implementation.

infinite, equally weighted sum of all odd harmonics of the fundamental line frequency.

$$\frac{1}{\sin(\omega t)} = 2\sum_{n=1}^{\infty} \sin(n \times \omega t) \tag{3}$$

One interpretation of (3) is that intentionally drawing harmonic currents can be used to reduce the energy buffer size. While we may not achieve the full 100 % reduction in energy buffer size, we can draw a subset of current harmonics, with weights limited by regulations, and achieve some (indeed much) of the same benefit.

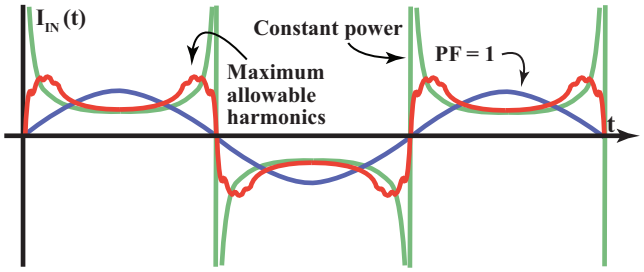

Fig. 3. Input current waveforms for PF = 1 (blue), zero-buffer solution (green), and maximum Class D harmonic current (red). The maximum harmonic current waveform closely approximates the zero-buffer current for a large portion of line cycle.

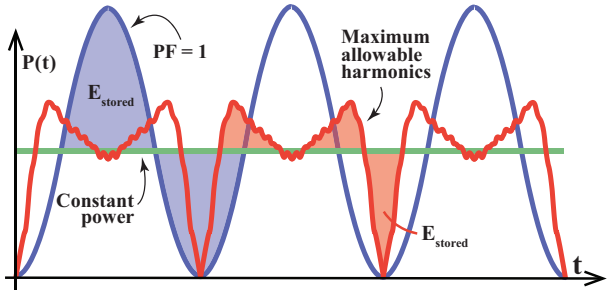

Fig. 4. The energy storage requirement when using maximum allowable Class D harmonics (shaded area,red) is significantly decreased from the energy storage required at PF = 1 (shaded area,blue).

III. Operating at Regulation Limits

To appreciate the limits that regulations impose on this approach, consider the IEC/EN 61000-3-2 Class D requirements [2], which apply to devices in the 75-600 W power range, governing all odd harmonics to the 39th. These current limits are expressed in terms of device power (mA_{rms}/W), with decreasing amplitudes for higher order harmonics (Table I). Beyond 600 W, most devices fall under the Class A regulation, which imposes constant limits on all odd harmonic components, independent of device power.[4]

TABLE I
IEC/EN 61000-3-2 Class D & Class A Limits on Odd Harmonics

n-th Harmonic	Class D Limit (mA/W)	Class A Absolute Maximum (A)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	$3.85/n$	0.21
$15 \le n \le 39$	$3.85/n$	$0.15 * 15/n$

There are infinitely many ways to incorporate harmonic current across a many-dimensional space. To constrain the problem, we choose two approaches: first, by introducing all governed harmonics together in equal percentages p of their individual maximum allowable values; and second, by introducing each harmonic individually to its maximum before introducing the next. Both methods are investigated numerically.

The former method allows us to observe what happens in the most extreme case of utilizing the maximum of every regulated harmonic within the IEC/EN 61000-3-2 regulations. Let the input current be

$$i_{in}(t) = \sum_{n=1}^{39} I_n \sin(n \times \omega t) \tag{4}$$

where, in Class D, each harmonic coefficient is proportional to the regulated limit $I_{reg,n}$ (mA/W) and to the output power:

$$I_n = \sqrt{2}(I_{reg,n} \times p)P_{out}. \tag{5}$$

By increasing the percentage p of all harmonics, the energy storage requirement monotonically decreases (Fig. 5), yielding up to a 62 % decrease in the energy storage requirement at $p = 1$. This can be seen geometrically in Fig. 3 where the current approximates (2) and also in Fig. 4 where the shaded energy storage area is clearly reduced.

While using the maximum allowable amount of of each harmonic current yields the largest drop in storage, it is an undeniably difficult function to generate

[4]Class A also governs even harmonics, but systems with power electronic front ends typically have half-wave-symmetric input currents which have no even harmonics. Even harmonics are also not useful for twice-line-frequency energy storage reduction, and are not considered further.

reliably without violating regulations. Fortunately, as described below, it is still possible to benefit from the majority of these storage savings by only incorporating third and fifth harmonic terms.

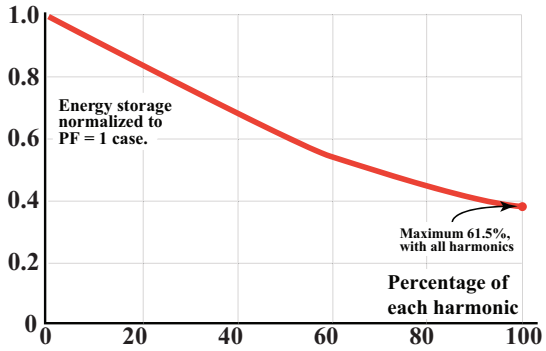

Fig. 5. Energy storage requirement as all harmonics are included at the same percentage p of their individual allowed maxima under Class D. By including all every available harmonic, the energy storage requirement can be reduced by nearly 62 %

IV. Incorporating Harmonics Sequentially

Instead of drawing all harmonics in equal proportion to their individual maxima, we can instead include one harmonic at a time. Let us start by drawing only third harmonic current,

$$i_{in}(t) = I_1 \sin(\omega t) + I_3 \sin(3\omega t). \quad (6)$$

as shown in Fig. 6 where I_3 is varied from 0-100 % of its allowed maximum value in class D.

With the inclusion of I_3, we see that the resulting input power begins to approximate the input power of Fig. 4, with reduced peak power and more constant power overall.[5] We also observe a significant impact on energy storage (Fig. 7), even when operating well within the allowable Class D harmonic limits. Introducing the third harmonic component alone can yield up to a 44 % improvement in the storage requirement, which is approximately two thirds of the maximum possible reduction under Class D.

Once we have included 100 % of $I_{reg,3}$, we can further improve the result by incorporating incremental amounts of a new fifth harmonic term

$$i_{in}(t) = I_1 \sin(\omega t) + I_{3,max} \sin(3\omega t) + I_5 \sin(5\omega t). \quad (7)$$

[5]As we increase I_3 beyond 65 % of its maximum allowable value, the input power at high voltage falls below the constant desired output. This area should not be included in the integral to calculate energy storage requirements, as the minor ΔV associated with this time does not affect the overall peak-to-peak ripple voltage on the energy buffer capacitor.

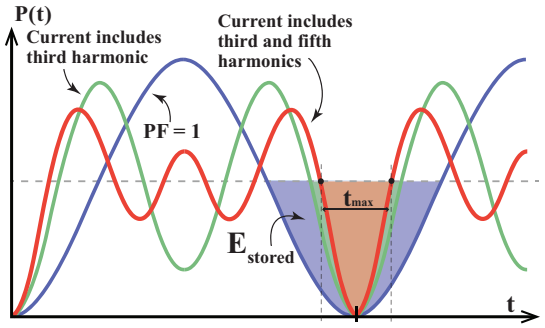

Fig. 6. Introducing the maximum allowed third harmonic reduces the central peak (blue) and divides it into smaller peaks (green); introducing fifth harmonic further corrects the extremities (red). Shaded regions correspond to time of maximum capacitor depletion (e.g. t_{max} of line cycle using fifth harmonic), and correspond to required energy storage.

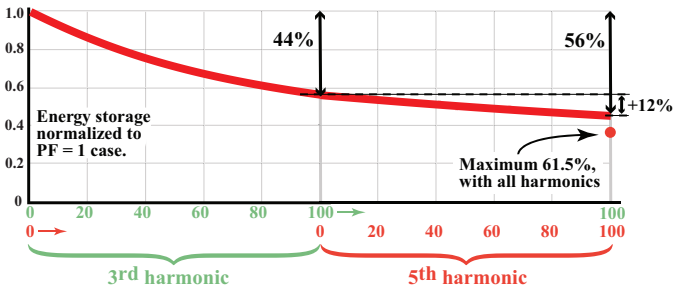

Fig. 7. Reduction in energy storage requirement by incorporating third harmonic current up to its regulation limit, then adding fifth harmonic up to its limit. These two harmonics contribute substantially towards the maximum achievable energy storage reduction.

The energy storage requirement continues to decrease (Fig. 7) although the additional energy savings are much less substantial. Maximizing the fifth harmonic contributes an additional 12 % reduction to the storage requirement, significantly less than the third harmonic. The same logic applies to each successive harmonic, each having less impact on overall energy storage due to the tighter limits on higher-order harmonic currents (e.g. introducing the maximum seventh harmonic contributes an additional 4 % reduction to the storage requirement).

V. Impact Across Device Classes

The previous discussion was based on the Class D requirements of IEC/EN 61000-3-2, which apply to power supplies for personal computers and similar devices up to 600 W. Devices in other classes (A,B,C) must meet other requirements.

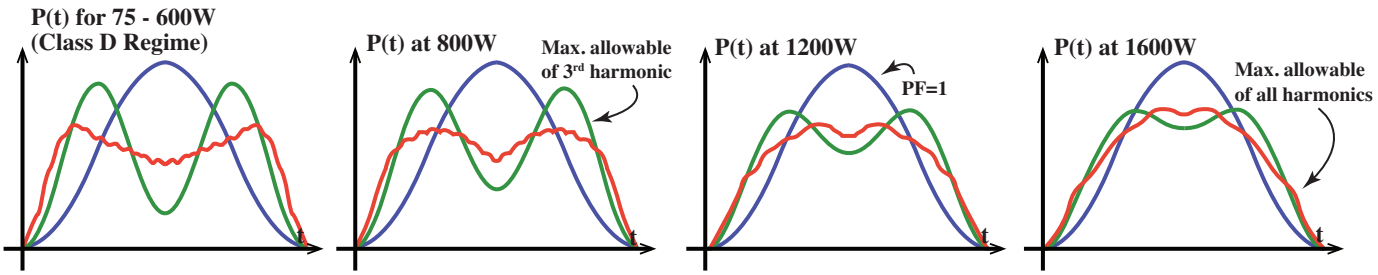

Fig. 8. Power waveforms when including all available harmonic currents are identical across the 75 W-600 W Class D range. Beyond 600 W (in Class A), the benefit of using harmonic currents diminishes as their weight relative to the fundamental decreases. Still, this method yields up to a 35 % reduction in energy storage at 1600 W.

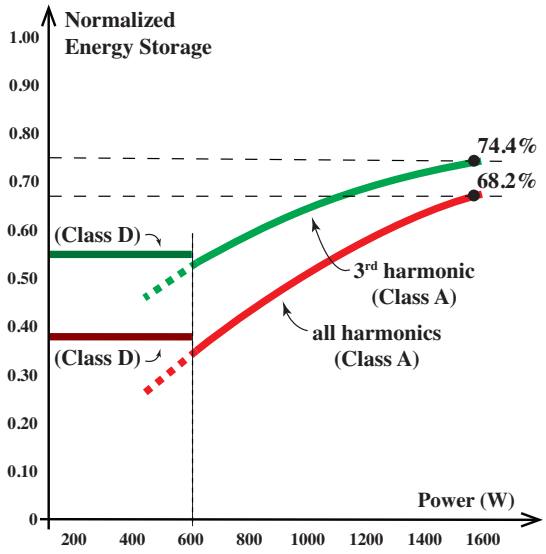

Fig. 9. Available energy storage reduction decreases with power in Class A (with fixed harmonic maxima) as opposed to Class D (with harmonic maxima that scale with power); still, significant energy storage reduction is available even when approaching the power limits of single-phase equipment. Class D regulation limits do not seamlessly transition into their Class A maxima at 600 W, hence the discontinuity in achievable energy storage at this boundary.

A. Class A

Devices not belonging to any other class belong to Class A. This includes a variety of device types, as well as devices rated for more than 600 W that would otherwise be considered Class D. Class A regulations define maximum permissible harmonic current values independent of power (Table I) As power is increased, the allowed harmonics become smaller relative to the fundamental and we observe (Fig. 8) that the power waveform with maximum harmonic content begins to recede toward the PF = 1 shape. This is a significant departure from Class D; because Class D harmonic limits scale with power, the results are largely the same across the entire power range.[6]

This trend obviously decreases the available benefit from harmonic inclusion at higher powers, but the benefit is still substantial well into the kilowatt range (Fig. 9). Indeed, at 1600 W, a roughly 35 % energy storage reduction from harmonic inclusion is still available.

B. Class B

Portable tools and some arc welding equipment belong to Class B (regardless of power), which has the same requirements as Class A with the harmonic limits multiplied by 1.5. The normalized energy storage by using the maximum[7] available harmonic content is shown in Fig. 10. Using the third harmonic alone, a maximum of 50 % energy storage reduction is possible at about 750 W. Below this power, the third harmonic limit is higher than the fundamental, and using a higher magnitude would only increase the required energy storage again.

When all harmonics are used, the energy storage reduction continues to scale as power is decreased. As power approaches zero, the fundamental becomes less than every harmonic limit and it becomes possible (in theory) to replicate (3) and achieve complete elimination of the energy storage requirement. Nevertheless, reducing the normalized energy storage requirement below ∼20 % requires a very large number of harmonics, making it practically unfeasible. Nevertheless, for

[6]The results are identical for devices operating at or below 584 W. At 584 W, the higher-order 15th-39th harmonics reach the Class D absolute limits on maximum permissible harmonic current. This has negligible impact on the available energy storage savings, as high-order harmonics are already tightly regulated.

[7]Due to the constant limits in both Class A and Class B, at low power some harmonic limits may exceed the fundamental current. In these cases, the magnitude of those harmonics are set equal to the fundamental to minimize the energy storage requirement.

portable tools of moderate power (400-800 W), it is both feasible and permissible to reduce the energy storage requirement by roughly two thirds from the PF = 1 case.

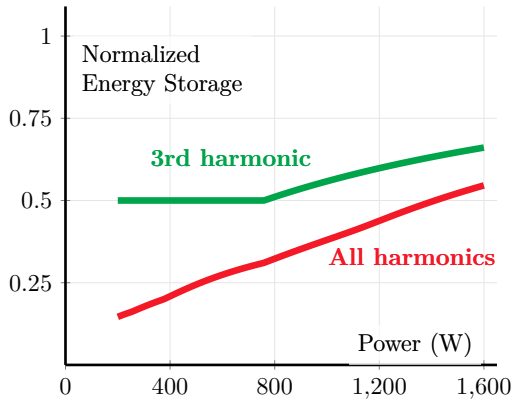

Fig. 10. Energy storage normalized to PF = 1 conditions when using the maximum allowed third harmonic and the maximum allowed of all harmonics for Class B. For a given power, if an allowed harmonic limit is more than the fundamental, that harmonic current is set equal to the fundamental.

While IEC/EN 61000-3-2 is usually the relevant regulation, not power factor, it may still be valuable to examine the power factor when harmonic injection is used. The results for Class A and Class B (under the same cases as Figs. 9,10) are shown in Fig. 11. For those applications requiring power factor above a certain value, refer to Section VI.

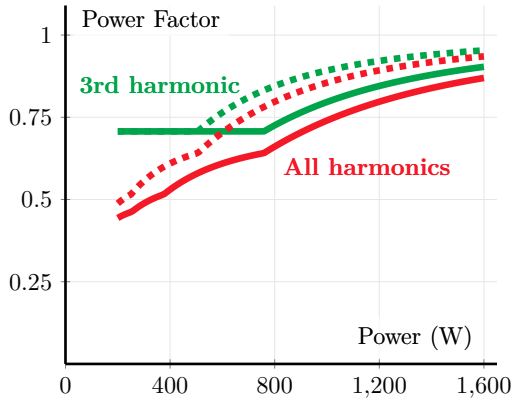

Fig. 11. Power factor for Class A (dotted) and Class B (solid) when the maximum allowable harmonic content is used across power levels. When a harmonic is allowed to be greater than the fundamental, the magnitude of that harmonic is set equal to the fundamental for this calculation.

C. Class C

Lighting equipment exclusively falls under Class C. Most of the past research on using harmonics for reduced energy storage requirements has targeted this class in an effort to eliminate electrolytic capacitors from LED drivers to extend their lifetime. Nevertheless, much of this research has examined specific designs and control strategies or uses incomplete or outdated limits to investigate the available energy storage reduction; therefore, we investigate the general limits of this technique on Class C here.

Class C is divided into a higher power (> 25 W) regime and a lower power (≤ 25 W) regime. In the higher power regime, harmonic limits are set as a percentage of the fundamental current (Table II). Therefore, as in Class D, the available energy storage reduction is not a function of power in this regime. In addition, the allowed third harmonic is a function of the circuit power factor. To investigate the limit of the available energy storage reduction, we consider the fifth and seventh harmonics as percentages of their individual allowed maxima. For a given combination of fifth and seventh harmonic content, we calculate the maximum third harmonic content based on the power factor constraint:

$$\mathrm{PF} = \sqrt{\frac{I_{1,rms}^2}{\sum_{n=1}^{\infty} I_{n,rms}^2}} = \sqrt{\frac{1}{1+p_3^2+\ldots}} \tag{8}$$

where p_n is the nth harmonic content as a percentage of the fundamental (expressed as a decimal). With third, fifth, and seventh harmonics included and setting $PF = p_3/0.3$ as the specification requires, solving for p_3 yields

$$p_3^2 = \frac{-\left(1+p_5^2+p_7^2\right) + \sqrt{\left(1+p_5^2+p_7^2\right)^2 + 4\times 0.3^2}}{2} \tag{9}$$

For a given combination of fifth and seventh harmonic, the maximum allowed third harmonic was calculated and the energy storage requirement was calculated with these three harmonics included (Fig. 12). Due to the tight limits on the fifth and seventh harmonics, they have relatively little impact on the result; higher order harmonics would have a smaller impact still. In addition, because the available third harmonic content is a function of the power factor, including larger quantities of higher order harmonics is not always desirable; in Fig. 12, the energy storage requirement improves and then worsens as seventh harmonic is increased. Overall, the energy storage requirement can be reduced by approximately 25 % (from the PF = 1 case) in this higher power regime of Class C.

In the lower power regime (≤ 25 W), there are three separate options to satisfy the IEC/EN 61000-

TABLE II
IEC/EN 61000-3-2 Class C (>25 W) Limits on Odd Harmonics

n-th Harmonic	>25 W limits (% of fundamental)
3	$30 \times$ PF
5	10
7	7
9	5
$11 \leq n \leq 39$	3

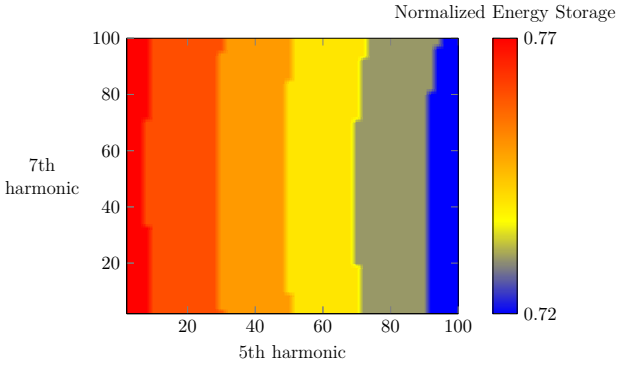

Fig. 12. Energy storage for the high power class C case using max 5th and 7th harmonics (as percentages of their fixed maxima) and allocating the maximum allowable 3rd harmonic that fits the PF spec. Power factor is approximately 0.95 and, since very little 5th and 7th harmonics are allowed, does not vary much across these variables and is not plotted.

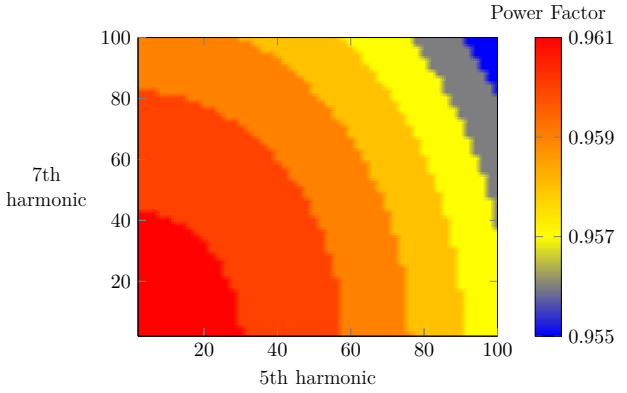

Fig. 13. Power factor for the high power class C case using given amounts of fifth and seventh harmonics (as percentages of their individually allowed maxima) and using the maximum allowable third harmonic consistent with the IEC/EN 61000-3-2 power factor specification for this class.

3-2 regulation:

1) Harmonics may meet Class D requirements;
2) Harmonics may meet $p_3 < 0.86$, $p_5 < 0.61$, as long as the current rises before a line angle of 60°, peaks before 65°, and returns to zero after 90°;
3) Harmonics may meet $p_3 < 0.35$, $p_5 < 0.25$, $p_7 < 0.3$, $p_9 < 0.2$, $p_{11} < 0.2$, and $p_2 < 0.05$, as long as the total harmonic distortion remains below 70 %. This option is new in the fifth edition (2018) of the IEC 61000-3-2 requirements [2].

We have already covered the first option (Class D), which permits a 62 % reduction in energy storage requirements. We also need not consider the third option, as it is less permissive than the second for controlled waveforms like the ones considered here. Therefore, we need only consider the second option.

To consider the limit of energy storage reduction in this case, we first use the maximum of the third and fifth harmonics (Fig. 14); adding more third and/or fifth harmonic at no point raises the energy storage requirement, so we proceed considering the maximum usage. We then include seventh and ninth harmonics, each up to a maximum of 100 % of the fundamental (Fig. 16). As in the higher power regime, we see that additional harmonic content does not always reduce the energy storage requirement; however, in this case, appropriately adding higher order harmonic content can reduce the energy storage requirement substantially (from ∼37 % of the PF = 1 case with only third and fifth to ∼26 % with seventh and ninth also included). Thus, in this regime, the second regulation option offers even more energy storage reduction than the first option (i.e. Class D limits).

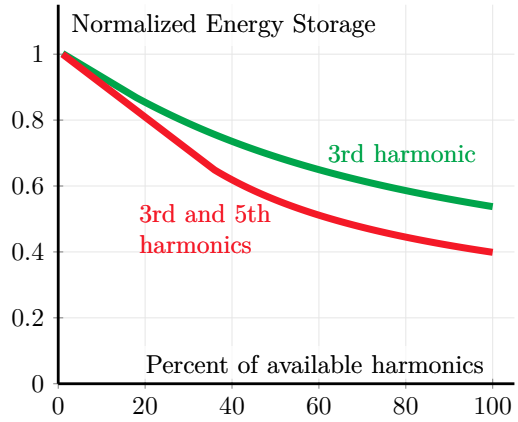

Fig. 14. Energy storage for the low power class C case (second option) using only the third harmonic and using the third and fifth harmonics. As including more harmonic content never raises the energy storage requirement, one can maximize the third and fifth and consider further harmonics (Fig. 16).

VI. Limited Power Factor and Energy Star

In some cases, designers may be constrained to operate above a certain power factor limitation. Although we know of no case where this is required by

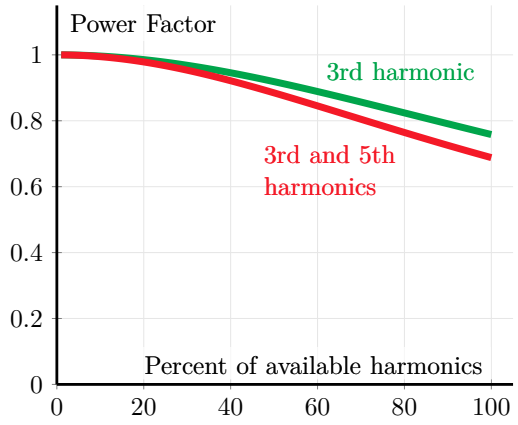

Fig. 15. Power factor reduction when considering third and fifth harmonic inclusion. If a power factor above a certain quantity is desired, compare with Fig. 14 to determine the corresponding energy storage reduction.

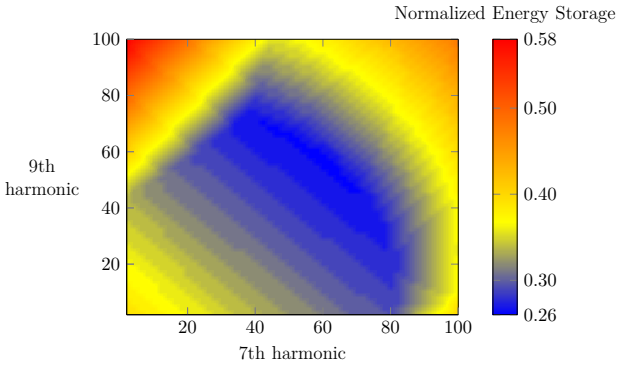

Fig. 16. Energy storage for the low power class C case (second option) using the maximum allowable third and fifth harmonics and allocating seventh and ninth harmonic as percentages of the fundamental (seventh and ninth harmonics are not regulated directly in this option).

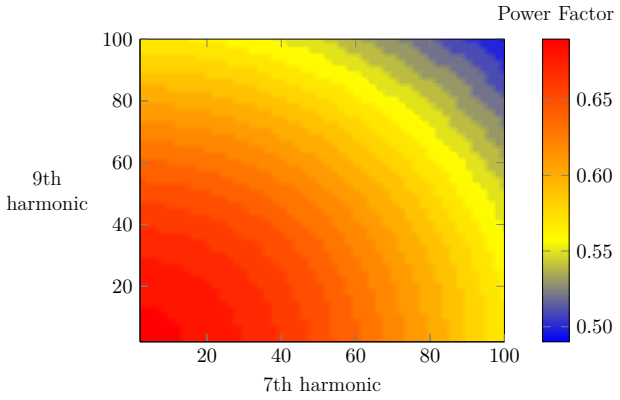

Fig. 17. Power factor for the low power class C case (second option) using the maximum allowable third and fifth harmonics and allocating seventh and ninth harmonics as percentages of the fundamental.

regulation for the classes of devices considered here, it is required for voluntary Energy Star compliance in the United States and may be an effective industrial standard in other sectors.

As an example, we may consider Energy Star compliance, which corresponds to a power factor of 0.9 for most kinds of equipment. We investigate the energy storage requirement as third harmonic is added until power factor is reduced to 0.9. Higher order harmonics are not included as they impact power factor at the same rate as the third harmonic but provide less energy storage reduction. Power factor can be expressed as

$$\mathrm{PF} = \frac{I_{1,rms}}{\sqrt{I_{1,rms}^2 + I_{3,rms}^2}} \tag{10}$$

which may be solved for $p_3 = I_{3,rms}/I_{1,rms}$

$$p_3 = \frac{I_{3,rms}}{I_{1,rms}} = \sqrt{\left(\frac{1}{\mathrm{PF}^2} - 1\right)^2} = 0.484 \tag{11}$$

which corresponds to an energy storage of 65.7 % compared to the PF = 1 case, or approximately 35 % savings on the energy buffer size.

By comparing with Figs. 11,13,15,17, it can be seen that this particular choice of harmonic content is already allowed by IEC/EN 61000-3-2 for Class A, Class B, Class C (low power) and Class D. The only exception is Class C above 25 W, which has stringent enough standards within IEC/EN 61000-3-2 that PF > 0.9 is already guaranteed, and a maximum of approximately 25 % energy storage reduction is available.

VII. Impact on Losses

Although reducing energy buffer size can be an important gain for power density, the increased current drawn is not necessarily free (e.g. in terms of loss) and the side effects of using harmonic current have not been thoroughly explored in the literature. Since this approach can be applied independent of the converter topology, one cannot quantify the exact impacts on system loss without considering detailed design, but we can attempt to model which converter components or stages will be affected and how.

Adding harmonic content increases the rms and average rectified current at the input, when compared to the PF = 1 case. Resistive losses will grow $\propto i_{rms}^2$, while diode losses are approximately proportional to their average currents. Adding harmonics will increase both of these metrics without increasing output power, lowering efficiency.

Nevertheless, not all components are affected equally, or at all, and loss reductions may also accrue in some cases.[8] As an example, consider a two-stage architecture with an input diode bridge, dc-side EMI filter, boost PFC stage, energy buffer capacitor holding approximately constant voltage, and a subsequent isolated dc/dc step-down stage, as in Fig. 18.

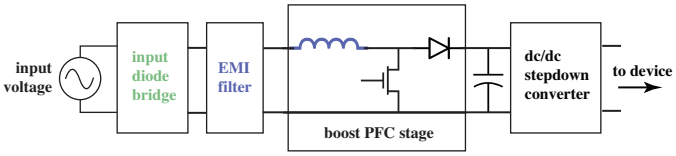

Fig. 18. The two-stage converter with boost PFC is a very popular grid-interface architecture. For this example, incorporating input current harmonics may negatively impact losses in the diode bridge, EMI filter, and boost inductor, should not affect the conduction losses in the boost diode or dc/dc step-down converter, and may improve losses in the buffer capacitor and boost switch.

By drawing additional harmonic current at the input, the diode bridge and EMI filter will see increased average and rms currents, increasing their loss. These losses extend to the boost inductor of the PFC, but not to all PFC stage components. Since the PFC output voltage is approximately constant in this example, the PCF output current tracks the power waveform in Fig. 4 which has the same average value regardless of harmonic content. Since $i_{D,ave} = i_{out,ave}$, it can be reasonably argued that the boost diode conduction losses should be largely unaffected by drawing harmonic input current. Additionally, the output current actually has a lower rms value when the input harmonics are included and the boost switch conduction losses may even improve (although they remain also functions of duty cycle). The energy buffer capacitor sees reduced rms currents and therefore reduced esr losses. Even if capacitance is reduced to maintain the same voltage ripple (and therefore esr is increased), the loss $P_{esr} = I_{C,rms}^2 R_{esr}$ is still reduced. Finally, downstream elements (in this example, the dc/dc step-down stage) should be entirely unaffected by the inclusion of input harmonics. Thus, only "input facing" components see additional losses by introducing input harmonic content.

We can begin to model the increased losses in affected components by examining the mean-square and average rectified input currents when utilizing all harmonic currents together (Fig. 19), subject to Class D regulations. Logically, the largest mean-square and average rectified input currents correspond to the largest harmonic currents. The same pattern is observed when only the third harmonic is included (Fig. 20). While currents and associated losses do increase, they may be a small fraction of overall loss. In addition, because losses and energy storage do not vary linearly, effective compromises are available. For example, incorporating 40 % of the third harmonic alone grants a nearly 30 % decrease in energy storage (in Class D) with a very small impact on the rms and average rectified input current metrics.

[8]For example, switching frequency range compression may be achieved which can be used to reduce skin/proximity effect losses, core losses, and frequency-dependent semiconductor losses like dynamic R_{on} and losses in C_{oss} capacitance [26]–[28].

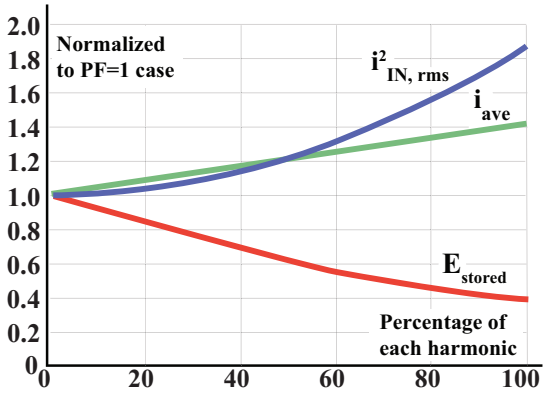

Fig. 19. Increases in $i_{in,ave}$ and $i_{in,rms}$ for a given amount of harmonic currents, each at equal percentages of their Class D limits.

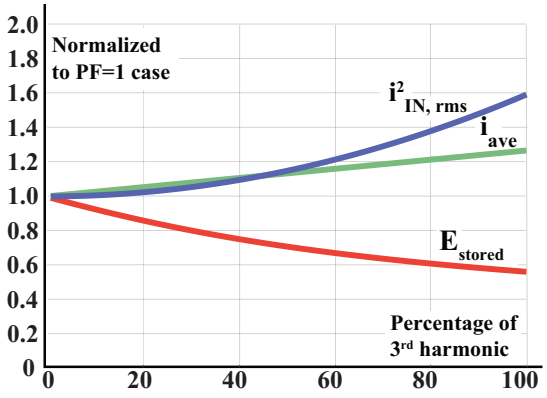

Fig. 20. Increases in $i_{in,ave}$ and $i_{in,rms}$ for a given amount of third harmonic current (as a percentage of its Class D limit).

VIII. Hardware Validation

Many PFC implementations can draw input currents with specified harmonics. Indeed, one benefit of this approach is its versatility across topologies without requiring additional hardware. Nevertheless, as a concrete example, we implemented a valley-switched boost PFC (Table III) which serves to demonstrate

experimentally the claimed performance benefits of using harmonic injection and investigate other practical effects. While implementation techniques for harmonic injection are not the focus of this work, for completeness we do include a brief overview of the control used here in Appendix B which is taken from [29].

TABLE III
PROTOTYPE DETAILS FOR ALL EXPERIMENTS

$V_{in,rms}$	220 V
$V_{out,ave}$	400 V
Power	250 W
Efficiency	96 % (see Fig. 25)
Boost Inductance	116 µH
Buffer Capacitors	10 µF × 10
Buffer Capacitor PN	Nichion UCY2H100MHD1TO
Boost Diode PN	C3D1P7060Q (SiC)
Boost FET PN	GS66506T (GaN)

The converter was operated at constant power and adjustable harmonic content, with third and fifth harmonics included up to the same percentage p of their individual allowed Class D maxima. Fig. 21 shows a series of oscilloscope captures for the specifications in Table III where p is increased and the peak-to-peak amplitude of the output voltage ripple decreases (recall from (1) that, for constant average bus voltage, energy storage is directly proportional to voltage ripple ΔV). The measured output voltage ripples are plotted Fig. 22, normalized to the ripple expected in PF = 1 conditions. The calculated reduction in energy storage is also plotted, and matches to within measurement precision.

The capacitor size is limited by the allowed output voltage ripple, so any decrease in voltage ripple for a specific power can also be interpreted as an available reduction in bus capacitance. Therefore, with modest amounts of third and fifth harmonics alone, the bus capacitor can be reduced by upwards of 50 %. This is verified in Figs. 23-24, where the converter is operated with output capacitance $C = 100\,\mu F$ and low harmonic content, and also with $C/2 = 50\,\mu F$ output capacitance and high harmonic content. It can be seen that the reduced voltage ripple from Fig. 22 can be translated into a capacitance reduction instead and that the impact on system volume is substantial (in this example, about a 1/3 reduction in PFC volume).

We also measured system losses for varying amounts

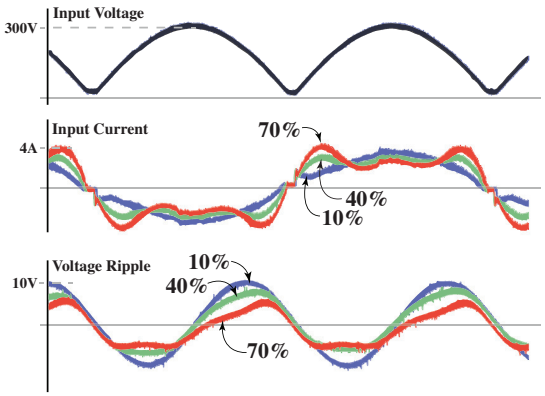

Fig. 21. Experimental input voltage, input current, and output voltage ripple for 10 % (blue), 40 % (green), and 70 % (red) of the allowed 3rd and 5th harmonic. The output voltage ripple decreases for fixed capacitance, as expected; the original voltage ripple magnitude could be restored with less capacitance and improved power density.

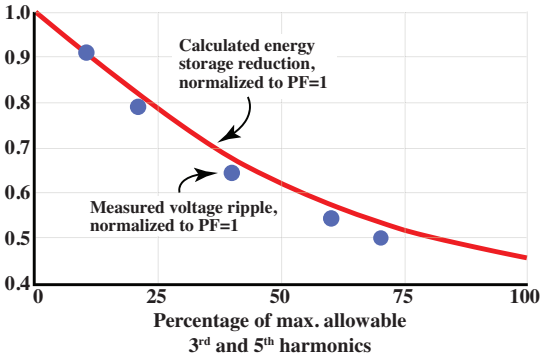

Fig. 22. Experimental output voltage ripple, normalized to the PF = 1 case, showing a close match to theory.

of harmonic currents,[9] plotted in Fig. 25. When introducing up to 70% of maximum allowable amounts of third and fifth harmonic currents, entire system losses across the input diode bridge, EMI filter, and PFC stage remained well within 10 % of the losses otherwise incurred by operating at perfect power factor. This is likely due to the converter being heavily dominated by conduction losses in the boost diode which is not expected to change with harmonic inclusion. This is verified thermally in Fig. 26.

Additionally, incorporating harmonic content introduces new benefits to the converter's switching frequency. Fig. 28 shows the measured converter switching frequency, across the rising half of each line half-cycle for different amounts of harmonic input current. In sinusoidal current (PF ≈ 1) operation,

[9]When measuring efficiency with input harmonics, it is important to remember that the real power into the system with no phase shift is $I_{1,rms} \times V_{rms}$, not $I_{rms} \times V_{rms}$.

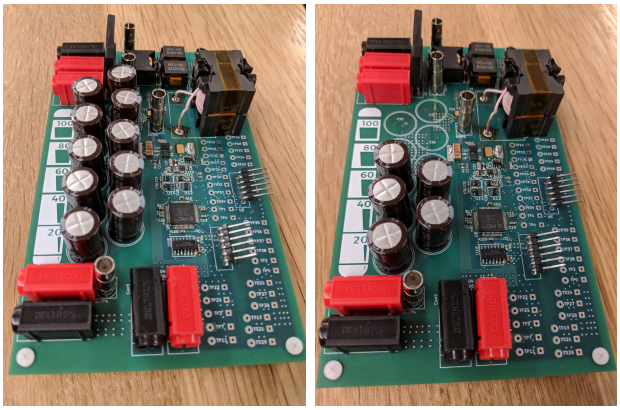

Fig. 23. Photograph of prototype PFC showing the available buffer size reduction when introducing 70 % of third and fifth harmonic Class D limits with constant output ripple. The capacitor reduction matches theory and is a major improvement to the system power density.

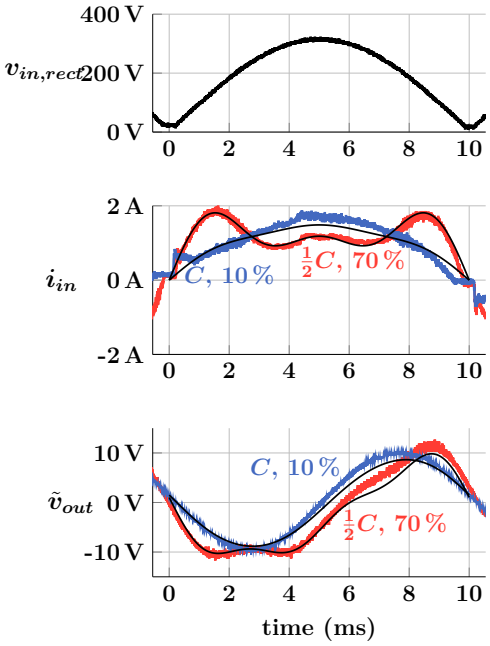

Fig. 24. Comparison of output voltage ripple when harmonics are included (10 % vs 70 % of the allowable third and fifth harmonics) and capacitance is reduced. The reduced voltage ripple of about 50 % in Fig. 22 is traded for 50 % less capacitance. Calculated waveforms are shown in black for comparison.

the switching frequency of the example boost PFC varies from 200 kHz near the peak of the line to almost 800 kHz at low voltages. When harmonics are introduced, more current is drawn at low line which reduces the switching frequency (this will generally hold for most variable-frequency converters). Indeed, when the example converter operates with approximately 50 % of the third and fifth harmonics allowed in Class D, the switching frequency variation is reduced

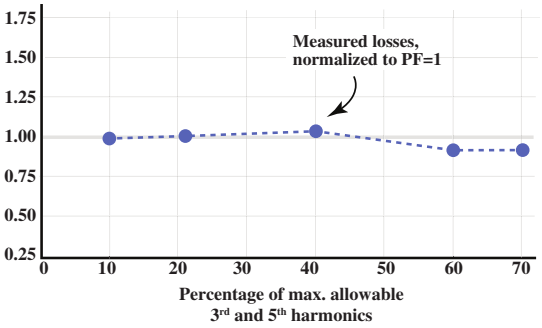

Fig. 25. Measured converter losses, normalized to the low-harmonic case (10 % harmonic usage, 96 % efficiency). In this prototype, which is dominated by diode losses, including significant harmonic content has negligible effect on efficiency.

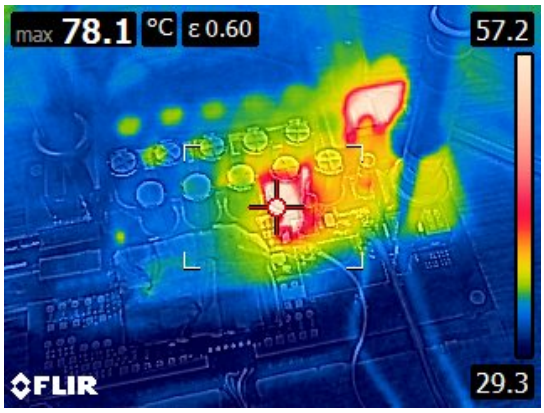

Fig. 26. Thermal capture of the converter operating with 70 % of allowable harmonics, showing that diode losses (which are harmonic-independent) dominate in this prototype. The hot spot in the center is the boost diode, and the hot spot in the upper right is the diode bridge.

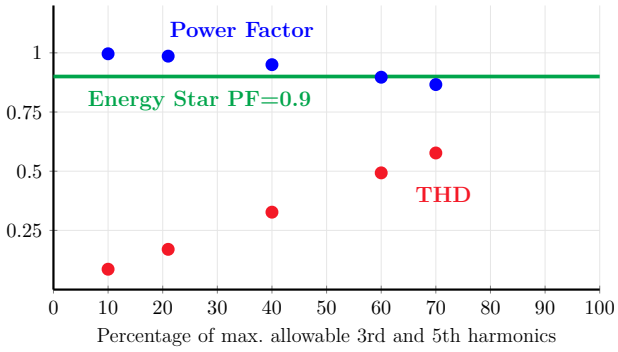

Fig. 27. Experimental power factor and THD for the prototype converter for different levels of harmonic inclusion showing that significant energy storage reduction can be achieved even with reasonable power factor constraints (compare Fig. 22).

to 250-300 kHz, or a ratio of 1.4:1. This compression has a variety of benefits, including for EMI filter and magnetic component design and for avoiding dynamic R_{on} and C_{oss} loss penalties. Indeed, by suppressing

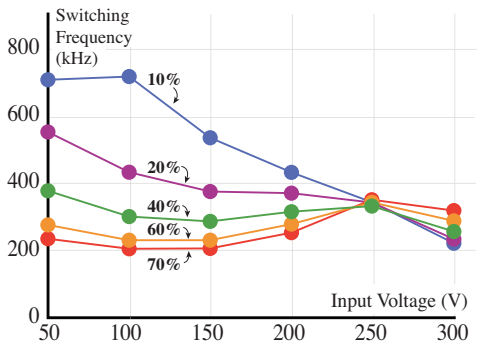

Fig. 28. Local operating frequency of the valley-switched boost PFC across the first half of the rectified input voltage half-cycle. The variable frequency introduced by the valley-switched boost is greatly mitigated with the inclusion of input harmonics by drawing more current at low voltage. For each curve, third and fifth harmonics are each included at the listed percentage of their individually allowed maxima.

the highest operating frequencies, the inclusion of harmonics may improve the loss in the boost inductor, which may contribute to the flat loss characteristic in Fig. 25.

Overall, the prototype demonstrates many of the benefits (and costs) of purposefully drawing higher order harmonic currents discussed earlier. While drawing many harmonics offers the greatest volume reduction, by using only third and fifth harmonics one can achieve a substantial amount of that reduction while still operating well within harmonic limits. Variable frequencies may beneficially have their ranges compressed, and additional losses may be reasonable and/or compensated by loss reductions and operating benefits.

IX. Conclusion

As increased efficiency and switching frequency improve the size of other components of ac/dc converters, energy buffers become more of a bottleneck to miniaturization. By intentionally drawing currents at harmonics of the grid voltage, designers can greatly reduce the energy that must be stored each cycle, and therefore significantly reduce the size of energy buffer capacitors. We show this for every regulation class, with energy storage reductions between 25-75 % available depending on the class and power level. In most cases, this technique is available with a change of controls only, which is an important advantage over other techniques for cost-constrained applications. We presented a prototype which validates the results without incurring a significant efficiency penalty and demonstrates frequency compression which may be valuable for implementing high-efficiency variable-frequency PFC stages.

Looking forward, we note that there is nothing fundamentally incompatible between this approach and others that aim for high voltage ripple or use "active buffers" to reduce the buffer size (e.g. [6]–[9]). The benefits available from each approach are compoundable, such that a 50 % energy buffer reduction from each approach should reduce the buffer to 25 % of its original volume.

Appendix A
Calculation Method

To calculate the energy storage associated with any particular harmonic combination, we calculate how the stored energy changes over a cycle. The maximum minus the minimum energy gives the required energy storage in a cycle, $E_{store} = E_{peak} - E_{trough}$.

This computation is performed numerically in the following manner:

1) Specify the conditions of the test, including input voltage $V_{in,rms}$, net power P (which is equivalent to selecting $I_{1,rms}$), and the values of $I_{n,rms}$ for harmonics $n > 1$.
2) Compute half-cycle input current waveform through $i_{in}(t) = \sum_{n=1}^{N} I_n \sin(\omega t)$ where N is the highest order harmonic one wishes to consider.
3) Compute half-cycle input power waveform through $p(t) = i_{in}(t) \times v_{in}(t)$
4) Integrate the difference between the input power and the output power $E(t) = \int_0^{T/2} [p(t) - P_{out}]\, dt$, where $P_{out} = I_{1,rms} \times V_{in,rms} = \langle P_{in} \rangle$ is a constant and the integration may be performed numerically using e.g. `cumtrapz` in MATLAB/Octave. The energy storage requirement is the difference `max(E)-min(E)` and is normalized against the PF = 1 case.
5) Power factor is computed for each case with $\mathrm{PF} = I_{1,rms} / \sqrt{\sum_{n=1}^{N} I_{n,rms}^2}$

This procedure is repeated by varying the test conditions (power level, harmonic content) within the specifications of the product class in question. For example, in Fig. 14, the third harmonic maximum is hard-coded based on Class C specifications, a vector of values for $I_{3,rms}$ is generated up to the hard-coded maximum, and the procedure above is followed for each values of the $I_{3,rms}$ vector. In most cases, harmonic content is swept. In some cases like Fig. 9,

power is swept and the maximum allowable harmonic content must be computed in Step 1 for each power point. The above procedure is easily replicated across multiple variables to produce plots like Fig. 12.

Appendix B
Control Overview

There are a variety of control techniques that may be used to achieve the types of input currents discussed in this paper, several of which are discussed in the references. The technique used here is a blended approach which uses feedforward to shape the input current waveform over the line cycle with a slower outer voltage feedback loop to set the output voltage (i.e. to control power). The feedforward line current shaping takes as inputs the desired harmonic rms currents as fractions of the fundamental, which itself is set by the slow outer voltage feedback loop. This approach is discussed in full in [29] and is not the main emphasis of this work. Nevertheless, we briefly outline the approach below.

We begin by observing that the average (over a switching cycle) line input current I_{in} is not equal to the converter input current I_{conv}, but rather is the sum of I_{conv} and current into any input capacitance I_C (e.g. in the EMI filter). Mathematically,

$$\begin{aligned} I_{conv} &= I_{in} - I_C \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\cos(\omega_{line}t) \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\sqrt{1-\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)^2} \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2V_{rms}^2 - V_{in}^2} \end{aligned} \tag{12}$$

where we have replaced $\omega_{line}t = \sin^{-1}\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)$ to make the above equation a function of instantaneous measurables. If we can further express the converter input current I_{conv} in terms of control inputs, then we can implement feedforward control based on directly measurable quantities. I_{in} can be set to be any desired waveform, e.g. a fundamental sinusoid with harmonics.

The converter input current $I_{conv}(t_{on})$ is derived in [29] and solved to yield the control variable t_{on} as a function of the desired net input current I_{in}:

$$\begin{aligned} t_{on} = \quad & 2\frac{L}{V_{in}}I_{in} \\ & + \sqrt{LC_p}\frac{1}{X}\left(1 - X + \sqrt{1-2X}\right) \\ & \mp 2LC_{in}\omega_{line}\sqrt{2\left(\frac{V_{rms}}{V_{in}}\right)^2 - 1} \end{aligned} \tag{13}$$

where the $\mp$ depends on whether the input voltage is rising ($-$) or falling ($+$), C_p represents the parasitic capacitance at the switching node, and $X = V_{in}/V_{out}$. We interpret the first term as a constant on-time (for PF $= 1$, i.e. $I_{in} \propto V_{in}$) which is often used in Boundary Conduction Mode boost converters; the second term corrects for the resonant transition time (significant at high frequency); the third term accounts for the effect of input capacitance.

In this instance, we may set $I_{in} = \sqrt{2}I_{1,rms}\sin(\omega t) + \sqrt{2}I_{3,rms}\sin(3\omega t) + \ldots$ and replace $\omega_{line}t = \sin^{-1}\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)$ as before, noting that $\sin(n \times \sin^{-1}(x))$ can be expressed as polynomials of x, e.g. $\sin(3 \times \sin^{-1}(x)) = 3x - 4x^3$ (such expressions are exact, not series approximations).

Thus, the control input t_{on} is continuously updated based on instantaneous measurements of input voltage and output voltage alone and can be made to conform with any desired waveform of the type discussed here.

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