

A High Frequency Inverter for Variable Load Operation

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Abstract—This paper presents a new inverter architecture suitable for driving widely-varying load impedances at high frequency (HF, 3-30 MHz) and above. We present the underlying theory and design considerations for the proposed architecture along with a physical prototype and efficiency optimizing controller. The high frequency variable load inverter (HFVLI) architecture comprises two HF inverters with independently controllable amplitude and phase connected together and to the load via a lossless power combining network, implemented here as an immittance converter. By controlling the amplitudes and relative phase of the two constituent inverters, the loading seen by each constituent inverter can be kept in a desirable range even for wide variations in load impedance. This allows for the use of highly efficient zero voltage switching inverters that would otherwise be precluded or limited in applications presenting wide impedance ranges, such as wireless power transfer and RF plasma generation.

The prototype HFVLI system demonstrates the benefits of the proposed approach. It operates at 13.56 MHz and can supply a maximum output power of 1kW into a $21.8+0.3j$ load at an efficiency of 95.4%, and is able to drive a wide range of capacitive and inductive loads at high power with high efficiency.

I. INTRODUCTION

Inverters operating at high frequency (HF, 3-30MHz) are important to numerous industrial and commercial applications such as induction heating, plasma generation, and wireless power transfer. A major challenge in these applications is that the load impedance can vary dynamically in both real and complex components over a wide range.

Addressing these applications at high efficiency is challenging owing to the constraints imposed by the combination of high-frequency operation and variable loading. Inverter designs at HF generally utilize fundamental-frequency inductive loading of the inverter transistor(s) to achieve the zero-voltage switching transitions necessary for high efficiency. For efficiency reasons, it is desirable to provide only the minimum amount of inductive loading necessary to support zero-voltage switching (along with the current needed to support the load). Operating into a highly-variable load impedance (especially with both inductive and capacitive variations) makes it difficult to maintain this desired inductive transistor loading without requiring a large inductive circulating current, which itself can induce substantial loss. Loading variation can directly limit the achievable operating range and efficiency of an inverter system (e.g., [1]), and these constraints become increasingly severe as frequency and power increase.

A commonly-used approach to addressing load impedance variations in such applications is to augment an inverter designed for a single load impedance (e.g., 50 Ohms) with a

tunable matching network (TMN) that dynamically matches the variable load impedance to the fixed value desired for the inverter (e.g., [2]–[4]). Such TMNs realize the adaptive tuning using variable passive components, such as motor-driven mechanically-variable capacitors, switched capacitor banks, or high-power varactors. While this approach is very effective, allowing the inverter to operate at its designed operating point for all loads within the tuning range of the TMN, the TMNs themselves are often some combination of expensive, bulky, slow and inefficient. An alternative to a tunable matching network is to design the load (e.g., including the plasma coils and matching system) such that a degree of self-compensation is provided; this can be accomplished with a set of matched loads and a resistance compression network, for example [5], [6], but requires a specially-designed load network (e.g., a special set of plasma coils) which may not be practical in many cases. It would be much more desirable to have a high-frequency inverter system that can directly support a wide range of load impedances.

In this paper, which expands upon our recent conference papers [7], [8], we describe a new inverter architecture that can directly drive a wide range of load impedances at high frequency. We present the underlying theory and design considerations for the proposed architecture and present a prototype system along with an efficiency optimizing controller. The architecture comprises two constituent inverters having independently-controllable amplitude and phase, connected together and to a load by a lossless power combining and impedance transformation network (which we implement here with an immittance converter). By varying the amplitudes and relative phase of the two constituent inverters, the loading on each can be kept in a desired resistive/inductive region despite large variations in the load impedance. This new architecture enables inverter systems that can directly provide efficient power delivery into highly variable load impedances.

Section II of the paper introduces the proposed high frequency variable-load inverter (HFVLI) architecture and provides a derivation of the achievable load range of the idealized system. Section III provides the design of a prototype HFVLI system. Section IV details the control requirements of the HFVLI architecture and presents the structure and implementation of an efficiency optimizing controller. Section V presents the modeled load range, efficiency, and loss breakdown of the HFVLI prototype, and Section VI presents experimental results from the prototype system demonstrating its performance over a wide load range. Section VII concludes the paper.

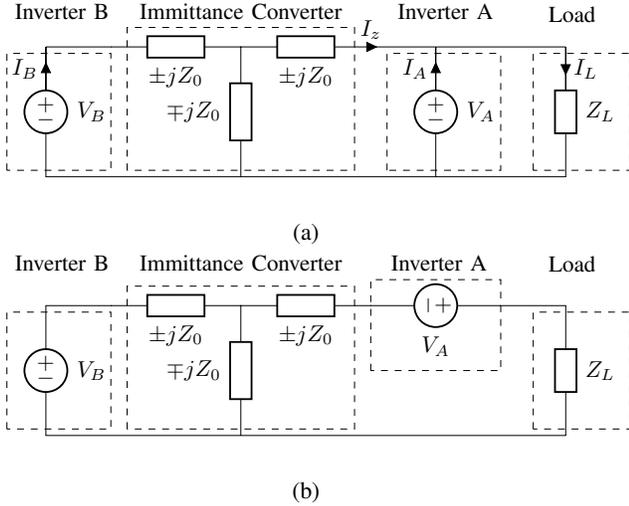


Fig. 1: Two implementations of the proposed HFVLI architecture utilizing an immittance converter: (a) parallel implementation, (b) series implementation.

II. THE HF VARIABLE LOAD INVERTER ARCHITECTURE

The HFVLI architecture was first proposed in our recent conference paper [7] and comprises two HF inverters with independently controllable amplitude and phase connected together via a specialized lossless power combining and transformation network, implemented in [7] as an immittance converter. By controlling the inverter amplitudes and relative phase the impedance seen by each inverter can be kept in a desirable operating range for wide variations in the load impedance. This is advantageous as there are highly efficient zero voltage switching (ZVS) inverters, such as class E and class D [9]–[11], which only operate efficiently into a range of resistive/inductive load impedances.

Here we consider an HFVLI in which the power combiner is implemented as an immittance converter as in [7]. While other lossless power combining structures could also be used, such as the Chireix-like network exploited in [12], the immittance converter provides highly desirable control and soft-switching current generation properties as described below. There are two variations of the immittance-converter-coupled HFVLI, a parallel implementation shown in Figure 1(a) and a series implementation shown in Figure 1(b). The two variants have the same broad capabilities but we focus on the parallel variant as it allows both inverters and the load to be easily ground referenced¹. In either case, one inverter (inverter A) is directly connected to the load (with an output in parallel or series with the load), while the other inverter (inverter B) is coupled to the load via an immittance converter (with one port of the immittance converter in parallel or series with the load).

The immittance converter in the HFVLI designs of Figure 1 serves to losslessly transform the voltage (current) delivered by inverter B at the first port of the immittance converter into

an appropriately-scaled and phase-shifted current (voltage) at the second port of the immittance converter and vice versa. Essentially, the immittance converter transforms capacitive loads that can not be driven by high-efficiency ZVS inverters into inductive loads than can. Here we analyze the parallel implementation presented in Figure 1(a) to show how this is achieved. For modeling purposes and to explain the operation of the proposed architecture, we treat the inverters as ideal ac voltage sources having controllable amplitude and phase. All voltages and currents in Figure 1 and in the equations below are phasors representing rms values².

The transformation provided by the immittance converter can be expressed as:

$$\begin{bmatrix} V_A \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & \mp j \cdot Z_0 \\ \mp j / Z_0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_B \\ I_B \end{bmatrix} \quad (1)$$

From an impedance perspective the immittance converter transforms a capacitive (inductive) reactance at one port into an inductive (capacitive) susceptance at the other, while from a circuits prospective a voltage applied to one port controls the current into the other port (with a phase shift). A capacitive impedance of magnitude Z_L appearing at one port of the immittance converter will become a inductive impedance of magnitude Z_0^2/Z_L appearing at the other. The magnitude inversion around Z_0 is a side effect, but what is most important is that a capacitive impedance that a ZVS switch-mode inverter could not drive is transformed into an inductive load that can. In the HFVLI of Figure 1(a) the inverter connected directly to the load, inverter A, can drive inductive load components while the inverter connected through the immittance converter, inverter B, can drive capacitive load components. Both inverters can contribute to driving the resistive component of the load.

The full system of equations for the system is derived from the action of the immittance converter and is useful in showing how the output voltage and relative phase of the two inverters can be varied to distribute the load between the two inverters:

$$I_L = V_A / Z_L \quad (2)$$

$$I_L = I_A + I_Z \quad (3)$$

$$I_Z = -j \cdot V_B / Z_0 \quad (4)$$

$$I_B = j \cdot V_A / Z_0 \quad (5)$$

$$P = \text{Re}(V_A \cdot I_L^*) \quad (6)$$

In this analysis we assume that the load impedance, Z_L , is constant. As inverter A is connected directly to the load and to the immittance converter, its output voltage, V_A , constrains the system output power, P , the output current of inverter B, I_B , and the load current, I_L . The distribution of the load current between the output current of inverter A, I_A , and the output current of the immittance converter, I_Z , is determined by the amplitude and phase of the output voltage of inverter B, V_B . Here the phase of V_A is always taken to be zero³. From a

¹A difference between these dual implementations is that the variant of Fig. 1(a) is more suitable for supplying loads requiring large transient currents at limited voltage, while the variant of Fig. 1(b) is advantageous for supplying loads requiring large transient voltages at limited current.

²In [7] the equations were presented in terms of peak valued phasors, but we have changed to the rms form here for clarity.

³One of course has the freedom to set the absolute phase of the load voltage or current by setting the phase of V_A , and setting the phase of V_B with respect to the reference provided by V_A .

systems control prospective, given a load impedance and target power level, the output voltage of inverter B, V_B , is under-constrained and is set to achieve some desired distribution of load current between the two inverters. The most basic set of constraints to apply in choosing V_B would be a maximum rms output voltage, V_m , maximum RMS output current, I_m , and a restriction to a resistive/inductive load range for both inverters:

$$V_m \geq V_A, V_B \quad (7)$$

$$I_m \geq I_A, I_B \quad (8)$$

$$0 \leq \angle\left(\frac{V_A}{I_A}\right) \leq \frac{\pi}{2} \quad (9)$$

$$0 \leq \angle\left(\frac{V_B}{I_B}\right) \leq \frac{\pi}{2} \quad (10)$$

However, these restrictions still do not fully constrain the system for most load impedance / power level combinations and some additional constraint, such as a cost function, will need to be applied. The under-constrained system also allows for additional reactive currents to be synthesized via the immittance converter and circulated between the two inverters. This is beneficial as some ZVS inverter topologies require a minimum inductive loading to achieve ZVS, which can be synthesized independently of the load impedance.

Figure 2 shows example phasor diagrams for the relation between the two constituent inverters in the HFVLI system with (a) showing a resistive/inductive load, (b) showing a resistive/capacitive load, and (c) showing synthesized inductive loading on the two constituent inverters via the immittance converter with no external load. For all three of these conditions both inverters have some degree of inductive loading, as shown by V_A leading I_A and V_B leading I_B . Additionally a fixed 90 degree phase difference between V_A and I_B and between V_B and I_Z can be observed due to the action of the immittance converter.

The allowable HFVLI load range depends on the desired output power level, P , maximum inverter rms output voltage, V_m , maximum inverter rms output current, I_m , and any additional load constraints of the constituent inverters (e.g., their requirements for inductive currents for ZVS switching). As in [7] we present the analysis in terms of admittance as it allows for easier manipulation of the components of the load current, however here we use rms values for voltages and currents instead of peak values as used in the original analysis. We assume that the constituent inverters can drive any resistive/inductive load, subject only to voltage and current limits, and that the characteristic impedance of the immittance converter is chosen to maximize inverter utilization, $Z_0 = V_m/I_m$. Each inverter can deliver a maximum output power of P_{ri} into a resistance of value Z_0 , with maximum output power reducing as the resistive component of the load deviates from this value or the reactive component increases from zero. Due to the identical inverters and the transformation provided by the immittance converter we might think of the system as two inverters in parallel with identical maximum output voltage and current, with one inverter capable of driving resistive/inductive loads and the other capable of driving resistive/capacitive loads.

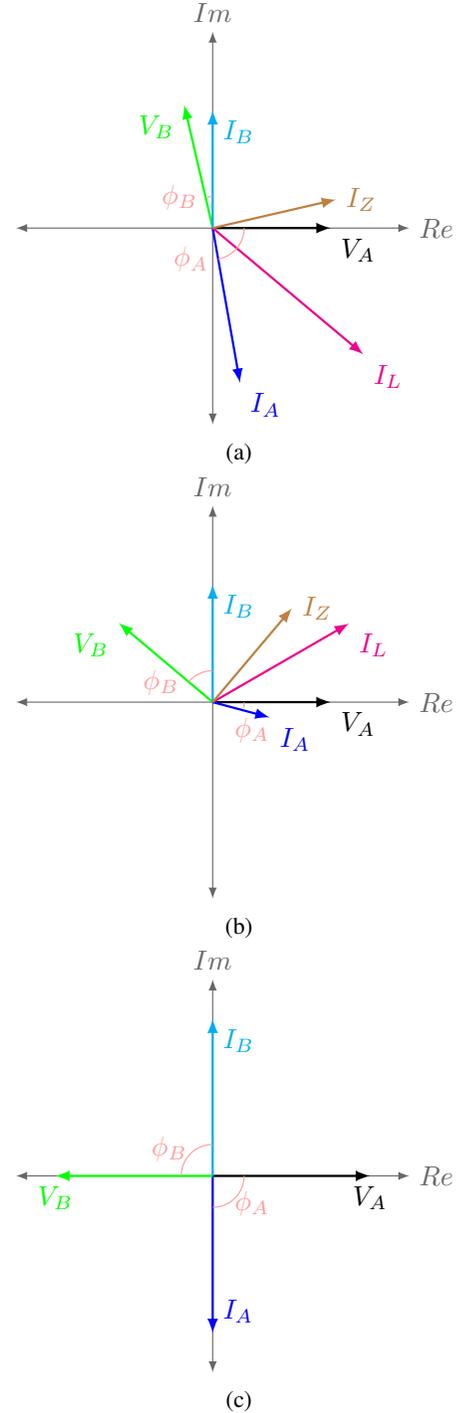


Fig. 2: Phasor diagrams for HFVLI system for (a) resistive/inductive load, (b) resistive/capacitive load, (c) no load with synthesized inductive load current.

The real power delivered by a single inverter depends on the conductive portion of the load admittance it sees. We can express the rms magnitude of the output voltage, $|V_{out}|$, and the rms magnitude of the output current, $|I_{out}|$, of a single inverter as a function of the desired output power, P , and

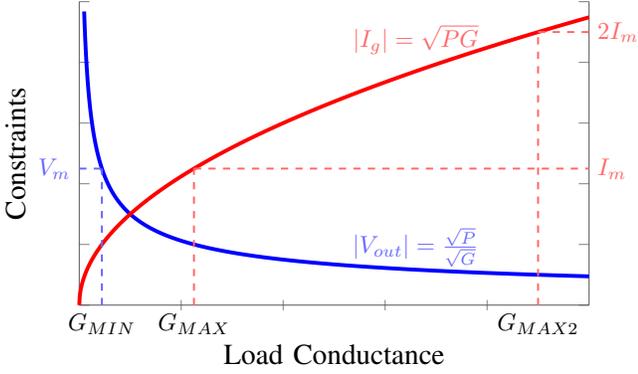


Fig. 3: Voltage and current constraints determining allowable inverter operating range as a function of load conductance. The voltage constraint is shown in blue, and the current constraint is shown in red.

load conductance, G :

$$|V_{out}| = \frac{\sqrt{P}}{\sqrt{G}} \quad (11)$$

$$|I_{out}| = \sqrt{PG} \quad (12)$$

Given a desired output power these equations can be used to calculate the range of allowable load conductances; a minimum conductance, G_{MIN} , based on the maximum inverter output voltage, V_m , and a maximum conductance, G_{MAX} , based on the maximum inverter rms output current, I_m . As the two inverters together can source up to $2I_m$ we can also determine a maximum load conductance for the two inverters together, G_{MAX2} . We give these equations below and plot the relation between the conductance and inverter ratings for a fixed power level in Figure 3.

$$G_{MIN} = \frac{P}{V_m^2} \quad (13)$$

$$G_{MAX} = \frac{I_m^2}{P} \quad (14)$$

$$G_{MAX2} = \frac{4I_m^2}{P} \quad (15)$$

Now that the relation between the desired output power and achievable conductance range is known we can analyze how the load susceptance impacts the load range. Of the two inverters one can drive capacitive susceptances while the other can drive inductive susceptances. Therefore, only a single inverter can drive a given load susceptance but both inverters can contribute to driving the load conductance. For load conductances between G_{MIN} and G_{MAX} , the conductive portion of the load can be driven by a single inverter, leaving the full output current capacity of the second inverter to drive the load susceptance. For this operating range the maximum load susceptance is determined by the maximum rms inverter output current, I_m , and the output voltage. For load conductances between G_{MAX} and G_{MAX2} , some portion of the output current capacity of the second inverter is used to drive a portion of the load conductance. The maximum load susceptance in this case is determined by the remaining output

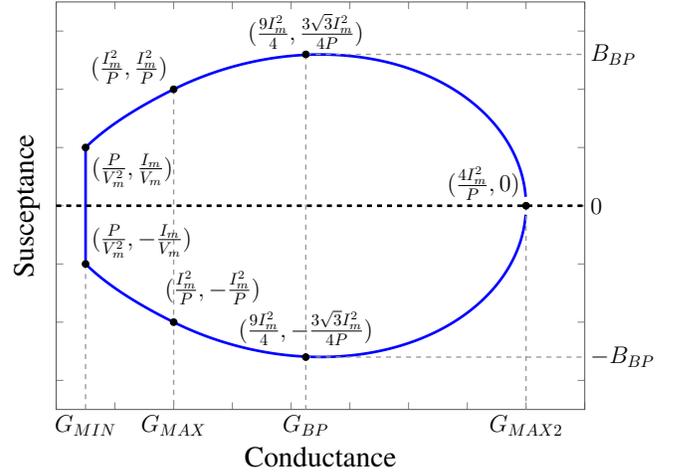


Fig. 4: HFLI admittance plane load region for $P \leq P_{ri}$.

current capacity and the output voltage. These equations are shown below and plotted in Figure 4.

$$|B_{MAX}|_{G_{MIN} \leq G \leq G_{MAX}} = \frac{I_m \sqrt{G}}{\sqrt{P}} \quad (16)$$

$$|B_{MAX}|_{G_{MAX} \leq G \leq G_{MAX2}} = \sqrt{2 \frac{G}{P}} \cdot (I_m \sqrt{PG} - PG) \quad (17)$$

Additionally, the maximum susceptance, B_{BP} , that can be driven while providing the desired output power, P , can be determined by solving for the inflection point of (17). The equation for this is given below and the point of maximum susceptance is also marked in Figure 4.

$$B_{BP} = \frac{3\sqrt{3}I_m^2}{4} \quad (18)$$

$$G_{BP} = \frac{9I_m^2}{4P} \quad (19)$$

For $P < P_{ri}$ the system operates in the two regions as plotted, $[G_{MIN}, G_{MAX}]$ and $[G_{MAX}, G_{MAX2}]$. However, when $P_{ri} \leq P < 2P_{ri}$ only one region applies as $G_{MIN} \geq G_{MAX}$. Under this regime the behavior of the system is determined by (17) over the range of $[G_{MIN}, G_{MAX2}]$. As desired output power increases beyond P_{ri} , the achievable load range decreases further, reaching a single point of conductance $2I_m/V_m$ at a power level of $2P_{ri}$. Figure 5 provides contour plots of the maximum output power for the idealized HFVLI system as a function of (a) load admittance and (b) load impedance, with V_m , I_m , and Z_0 all normalized to 1.

III. PROTOTYPE DESIGN

A prototype inverter system has been constructed to validate the proposed concept. The prototype HFVLI system operates at 13.56 MHz, and is rated to deliver a maximum power of 1 kW into its optimum load and a reduced power into a wide range of load impedances, including both inductive and capacitive loads. Figure 6 shows a simplified version of the system schematic with associated component values provided in Table I, Table II provides the design specifications of the system, and Figure 7 shows a picture of the prototype.

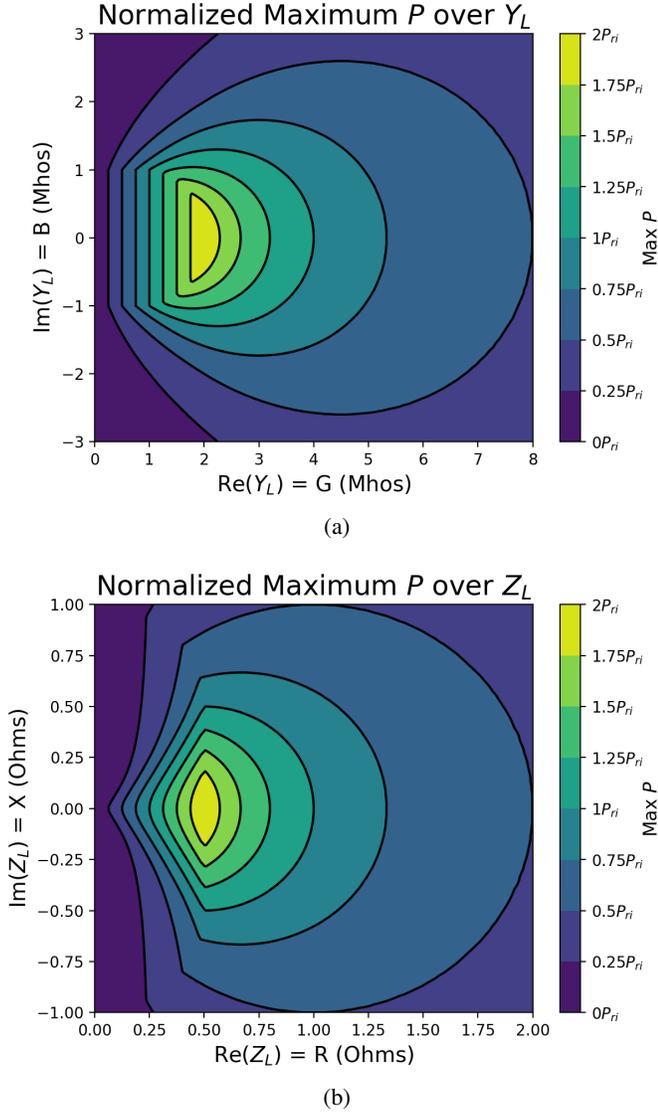


Fig. 5: Normalized maximum P over (a) load admittance and (b) load impedance for idealized HFVLI system, with $V_m = 1$, $I_m = 1$ and $Z_0 = 1$.

The HFVLI system requires two constituent inverters having adjustable relative phases and independently adjustable output voltages and an immittance converter. As described in detail below, we utilize two ZVS class-D inverters to realize the constituent inverters. Output amplitude modulation is achieved by adjusting the inverter dc power supply inputs over a range of 5-375 V using controllable lab power supplies (KLP 600-4-1200 and XLN60026). Relative phase adjustment is achieved through gate waveform timing of the constituent inverters. Here we detail the design of the constituent inverters, immittance converter, and control circuitry. Further details of the prototype system can be found in [13].

A. Constituent Inverter Topology

The analysis of the HFVLI system presented in Section II was based on ideal inverters that could operate into any

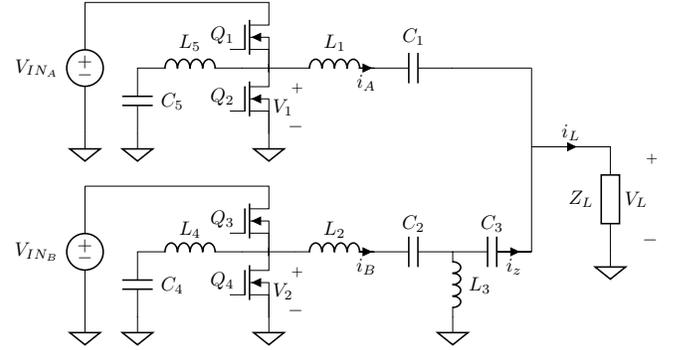


Fig. 6: Simplified schematic of the prototype HFVLI system. Component values are indicated in Table I. Full schematics and design details may be found in [13].

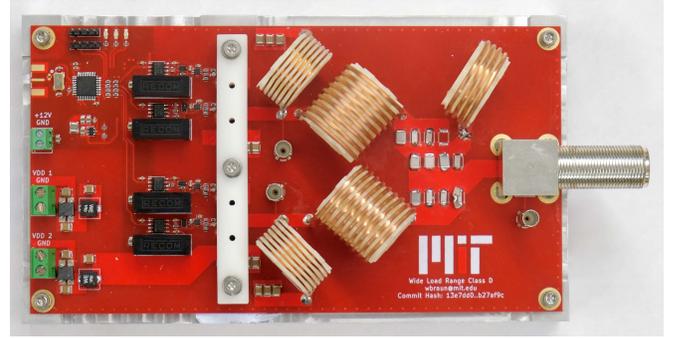


Fig. 7: Photograph of the prototype HFVLI system.

resistive/inductive load. There are many high-frequency inverter designs that can operate within the constraints of resistive/inductive loading described above. One option is a ZVS class D or class DE inverter [11], [14] having either a matching network or inductive pre-load network (or commutating network) such that it can operate with soft switching into a variable resistive/inductive load. Another option is

TABLE I: Component values for Figure 6, simplified schematic of HFVLI system.

Component	Value	Implementation
Q1, Q2, Q3, Q4	$C_{oss} \approx 37$ pF $R_{on} \approx 140$ m Ω	PGA26E19BA
L1, L2	1.14 μ H $Q \approx 520$	9 turns 1.6mm wire 22mm diameter, 2.75mm pitch
L3	496 nH $Q \approx 470$	4 turns 1.6mm wire 26mm diameter, 2.4mm pitch
L4, L5	950 nH $Q \approx 360$	6 turns 0.7mm wire 25mm diameter, 1.8mm pitch
C1	121 pF	Parallel 3KV C0G Capacitors
C2	84 pF	Parallel 3KV C0G Capacitors
C3	327 pF	Parallel 3KV C0G Capacitors
C4, C5	0.3 μ F	3x 0.1 μ F 500 V X7R C1210C104KCRCTU

TABLE II: Prototype HFVLI system parameters.

Output Frequency	13.56 MHz
Inverter Nominal Load Impedance	21.3 Ω
System Power Rating	1 kW
Maximum Inverter dc Input Voltage	375 V
Bounding Box Dimensions	190mm x 110mm x 60mm

an appropriately-designed single-switch inverter (e.g., class E, class ϕ -2, etc.). While classical Class-E inverter designs impose significant constraints on loading to maintain ZVS operation (e.g., [9], [15], [16]), some single-switch inverters are suitable for variable-load operation. In particular, the variable-load class E design introduced in [10] can operate with low loss across a wide range of resistive, resistive/inductive and inductive loads. (While [10] only explicitly treats design for variable load resistance, the resulting inverter designs can maintain ZVS and low loss for resistive/inductive and pure inductive loads as well, so long as the active switch has an antiparallel diode or equivalently provides reverse conduction.) Modulation of the individual inverter output amplitudes (as necessary for the proposed architecture) is most easily realized by modulating the inverter supply voltages as done here (i.e., using dc-dc converters to vary the inverter dc supplies, also known as drain modulation), though other means are also possible.

Due to its superior switch utilization and the availability of suitably effective high dv/dt level shifters and gate drivers, the ZVS class D half bridge was chosen for the two constituent inverters. A series resonant output filter is added to reduce harmonics which could distort the output waveform.

The load range of the ZVS class D half bridge is bounded by a minimum inductive load current required to achieve zero voltage switching, maximum output current and output voltage limits, and a maximum dv/dt limit imposed by the digital isolators used for level shifting in the gate drive circuitry. The dv/dt limit imposes a maximum inductive load current, since $dv/dt = I/C$, where I is the current during the switching transition and C is the capacitance of the switching node, including the output capacitance of the devices.

B. Constituent Inverter Switch Selection and Gate Drive

The class D half bridge requires two switching devices that experience identical voltage and current stresses. The high switching frequency of 13.56 MHz and the maximum dc bus voltage of 375 V favors 600/650 V class GaN FETs. Based on its superior $C_{oss} \cdot R_{on}$ figure of merit for resonant switching applications [17], the PGA26E19BA device from Panasonic was chosen. GaN devices often exhibit a high C_{oss} loss (even under ZVS switching) and a higher R_{on} value than indicated in the manufacturer provided datasheet when operating at high frequencies [18], [19]. Based on analytical data from [18], [19] the maximum constituent inverter supply voltage and output current (375V DC, 4A rms) were chosen in an attempt to maximize efficiency by balancing the supply voltage related C_{oss} losses and R_{on} related conduction losses, maximizing the system output power and load range given the thermal limitations of the GaN devices used. This leads to a maximum output power impedance for a single constituent inverter of $Z_m = 42.5\Omega$.

Gate drive circuitry is needed to drive the PGA26E19BA switching device from signals generated from the control circuitry. The gate of the high-side switching device is referenced to the switching node so there is a need for isolation or level shifting of the high-side gate drive signal. In order to simplify

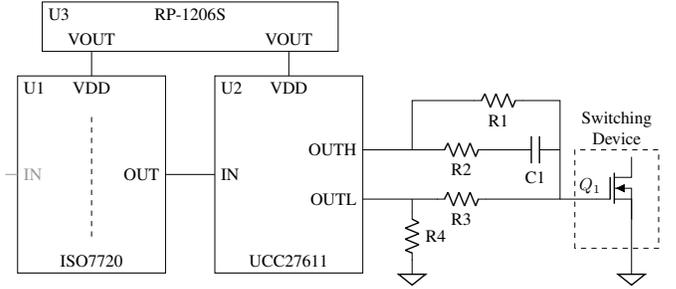


Fig. 8: Simplified schematic of gate drive circuitry for a single transistor in the constituent inverter.

TABLE III: Component values for Figure 8, simplified schematic of inverter gate drive circuitry.

Component	Value	Implementation
U1	Digital Isolator CMTI: 85V/ns	ISO7720
U2	GaN Gate Driver 4A Sink 6A Source	UCC27611
U3	Isolated dc/dc Converter 6V, 1W	RP-1206S
R1	270 Ω	Thin Film, SMD 0603
R2	2.2 Ω	Thin Film, SMD 0603
R3	1 Ω	Thin Film, SMD 0603
R4	10k Ω	Thin Film, SMD 0603
C1	2.1nF	C0G, SMD 0603

the gate drive and ensure matching delays, identical gate drive circuitry was used for both the high-side and low-side switching devices. The gate drive circuitry consists of a digital isolator having a high common-mode transient immunity (CMTI) of 85 V/ns, an isolated dc/dc converter, and a gate drive IC. The gate drive is mildly complicated by the fact that the PGA26E19BA switching device has what the manufacturer describes as a ‘‘Charge Injection’’ gate which conducts current above a threshold voltage, similar to a diode. This does not impact the selection of the gate drive IC, but a passive network is needed between the gate drive IC and the transistor gate to limit the maximum charge delivered to the gate and set the steady state gate current [20]. Figure 8 provides the schematic of the gate drive circuitry with component values provided in Table III. R_2 and R_3 limit the maximum turn-on and turn-off gate current while R_1 determines the dc gate current and C_1 determines the total charge delivered to the gate.

C. Constituent Inverter Shunt Pre-Load Inductance

Regardless of the load placed on the HFVLI system, at least one of the constituent inverters will need additional inductive current to enable zero-voltage switching of the devices. The inductive current required for ZVS can be synthesized via the immittance converter or provided by a ‘‘pre-load’’ inductance placed in parallel with the half-bridge output [21]. Synthesizing inductive current via the immittance converter allows for the inductive current component to be finely adjusted but requires circulating power between the two constituent inverters, increasing conduction losses in the output filters, both inverters, and the immittance converter. A shunt pre-load inductance at each half-bridge output provides the same

aid in achieving ZVS with reduced losses when compared to synthesizing current via the immittance converter. It avoids additional losses in the output filters and immittance converter, and additionally, it provides the same switching benefit (current provided at the switching transition) with reduced inverter losses due to the quasi-triangular current waveform [21]. However, the inductive current the pre-load inductance provides is dependent on the supply voltage and can not otherwise be controlled during operation.

To realize ZVS of the transistors a combination of shunt pre-load inductances, shown as L_4 and L_5 with associated dc blocking capacitors C_4 and C_5 in Figure 6, and synthesis of inductive load current via the immittance converter (realized with C_2 , C_3 , and L_3) was used. The pre-load inductance was sized such that it would supply the minimum needed inductive load current at the maximum supply voltage with any additional inductive load current needed at other operating points synthesized via the immittance converter. This allows for both the lower loss of inductive load current provided by the pre-load inductor and the fine control over the inductive switching current achievable through utilizing the immittance converter.

D. Immittance Converter

There are numerous means of realizing immittance conversion, including many lumped component implementations [22]. The immittance converter in the prototype HFVLI system was implemented as a T network as illustrated in Figure 1. As described in Section II the characteristic impedance of the immittance inverter, Z_0 , should be selected equal to the maximum power output impedance of a single constituent inverter, Z_m , to maximize inverter utilization and the load range of the HFVLI system. In Section III-B we give the constituent inverter maximum output power impedance, Z_m , as 42.5Ω , yielding $Z_0 = Z_m = 42.5\Omega$.

The selected immittance converter implementation requires one element of $\pm Z_0$ and two elements of $\mp Z_0$. In simplest form, this corresponds to one inductor and two capacitors or two inductors and one capacitor, each having an impedance of magnitude Z_0 at the operating frequency. Out of a desire to reduce the number of unique inductors required for the system it was chosen to implement the immittance converter as two capacitors and one inductor, leading to an immittance converter with high-pass characteristics. A side effect of this high-pass immittance converter is increased harmonic distortion on the output of the system. While this design choice did not have a major impact on system performance, a low-pass implementation of the immittance converter would be preferable in many implementations.

Referring to Figure 6, the immittance converter is implemented with C_2 , C_3 , and L_3 . On the side of the immittance converter connected to the constituent inverter, the capacitance of the output filter and the capacitance of the immittance converter are combined into one component, C_2 .

E. Control Circuitry

The HFVLI requires that the two constituent inverters have adjustable phase relative to one another. The class D half

bridge topology chosen for the constituent inverter requires two complimentary gate drive signals with an adjustable dead-time (duty cycle), as the optimal dead-time for the ZVS class D inverter varies with loading. Digital pulse width modulation (PWM) provided by a microcontroller fits this application well as it is easy to create signals with arbitrary timing and phase to one another through PWM and a microcontroller allows for digital control over the system. An STM32F334 microcontroller is used to generate gate drive signals through its high resolution PWM with a timing resolution less than 200 ps, allowing for accurate control of the duty cycle and relative phase despite the high operating frequency. Code running on the microcontroller allows for control of the gate drive waveforms in real time over a serial connection to a computer.

IV. CONTROL SCHEME

A controller is needed for the HFVLI system to generate values for the amplitude and relative phase of the constituent inverters such that correct loading for zero voltage switching is maintained as load impedance and desired output power level vary. The prototype HFVLI system shares the base system of equations with the idealized system presented in Section II. However, realizable inverters have additional load limitations and control parameters compared to the idealized inverters previously used to analyze the system. Additionally, as the system of equations describing the HFVLI system is often under-constrained, it is desirable to have a controller that can select operating points that optimize performance of the system based on some metric, such as efficiency. This section, augmented by Appendix A, presents an efficiency optimizing controller for the HFVLI system that is structured such that it is easy to incorporate arbitrary inverter limitations and additional control parameters.

A. Quasi-Static Model Prediction Control

The control requirements for the HFVLI differ from those of many other power electronics applications in two key ways which impact the structure of the controller. First, due to the high switching frequency and modest associated energy storage in the HFVLI, the system reaches steady state operating conditions on a time scale that is significantly shorter than typical required control speeds. This is also significantly shorter than the time scale at which the load impedance typically varies for many applications of interest, such as wireless power transfer and plasma generation. The fast transient dynamics means that from a control perspective the HFVLI can be treated as effectively static (i.e., operating in periodic steady state) and there is no need to store or track the detailed system state or dynamics (e.g., as in [23], [24]). This approximation holds up so long as one adjusts control variables, such as commanded power, slowly compared to the open-loop settling time of the system; is satisfied to respond to disturbances, such as changes in load impedance, at that speed; and can accept the open-loop dynamic transient response that may occur in response to such disturbances.

The second difference in the behavior of the HFVLI from that of many power electronic systems is that one of the

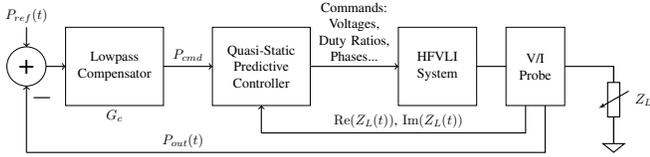


Fig. 9: Block diagram for HFVLI controller with closed loop feedback.

most important parameters of the system, the presence of zero voltage switching for the constituent inverters, is effectively a hidden parameter. ZVS is needed to achieve acceptable efficiency and prevent thermal damage, and the presence of ZVS determines the acceptable load range for the constituent inverters. One possible control approach would be to have some loose bounds on the impedance range of each inverter and then maintain ZVS by monitoring the switching waveforms and changing the drive signals in response, an approach previously used in other ZVS converters (e.g. [25], [26]). However, due to the high switching frequency, it is often impractical to have the controller directly measure ZVS conditions or maintain them under closed-loop control. We instead use a detailed model of the constituent inverters that can predict ZVS based on other operating parameters and allows us to constrain operation without the need for measuring the presence of ZVS.

Due to these two aspects we term our control strategy quasi-static model prediction control. The quasi-static assumption of periodic-steady-state operation for the behavior of the HFVLI system allows us to ignore stored system state. The model prediction term comes from the fact that we use a more accurate model of the constituent inverters than would otherwise be required in order to predict the presence of ZVS, eliminating the need to directly observe it. This control strategy effectively utilizes feed-forward, as each query to the controller provides an open-loop estimate of behavior based on the periodic steady state behavior. Characteristic of such a control approach, our controller exhibits a steady state output power error. However, to address this, one can implement a feedback loop controlling power around the controller presented here, where the output power is compared to the target value and a compensator is used to generate an input to the model.

Figure 9 presents a block diagram for the HFVLI controller with closed loop feedback utilizing this configuration. The main constraint of closed loop operation is that the outer loop compensator should have slow dynamics relative to that of the HFVLI plant, such that it provides the bandwidth limit of the system. For the combination of the HFVLI plant and quasi-static predictor controller the commanded power is monotonic with delivered power and the stability of the closed loop controller is dependent on the load and compensator characteristics. Here we focus on the quasi-static predictor controller; in our experiments the outer loop was realized through a computer-controlled adaptive system that incrementally adjusts the target output power between runs to achieve a more accurate value of delivered power, effectively acting as a compensator with a very slow response speed.

The quasi-static model prediction controller for the HFVLI

takes in as inputs the real and imaginary load impedances (which are measured by a V/I probe at the system output) and a commanded output power, and returns commands controlling the dc supply voltages of the constituent inverters (or equivalently the inverter output amplitudes), and the duty ratios and relative phases of the gate drive commands. Such a mapping from command to output may be either pre-computed and stored in lookup tables, or - as done in the prototype system - be computed in real time. The limiting factors of the update rate for closed loop operation are the required computation in mapping from command to output for the HFVLI controller and the bandwidth of the V/I probe. V/I probes used in commercial applications have relatively high bandwidth but advances in high-bandwidth impedance measurement would be beneficial for this application.

In the prototype HFVLI system, the quasi-static model prediction controller is structured as two independent parts: a model of the constituent inverters and a search function. Given an operating point consisting of output power and load impedance, the search function searches over the possible distribution of the load between the two constituent inverters. The search function evaluates possible load distributions through querying the constituent inverter model to find the load distribution that achieves zero voltage switching for each inverter and is most optimal according to some cost function. In the current implementation of the controller the cost function minimizes the sum of the (predicted) power dissipated by the two inverters, which approximates maximizing system efficiency. The details of the constituent inverter modeling and quasi-static model prediction controller design are presented in Appendix A.

V. MODELED PERFORMANCE

Using the model developed for control, including the constituent inverter model, it is possible to extract the predicted performance data of the experimental system. In this section we present the modeled load range and predicted efficiency for the prototype HFVLI system derived in this way.

A. Modeled Load Impedance Range

By repeatedly querying the controller model developed in Appendix A it is possible to find the maximum achievable output power level of the HFVLI prototype for a given load impedance. This approach was used to generate plots of the maximum output power of the HFVLI prototype which can be compared to those of the idealized HFVLI system. In Figure 10 we present (a) the normalized load range of the idealized system using the results of Section II and (b) the load range of the HFVLI prototype derived from the controller model.

As expected, the prototype has a reduced load range when compared to the idealized system. However, how the load range is reduced provides insights to the performance of the system. The two charts match closely at impedances above the maximum power output impedance (0.5Ω for the normalized idealized system, 21.3Ω for the prototype), with the majority of the difference in load range occurring below the maximum output power impedance. This discrepancy is largely due to the

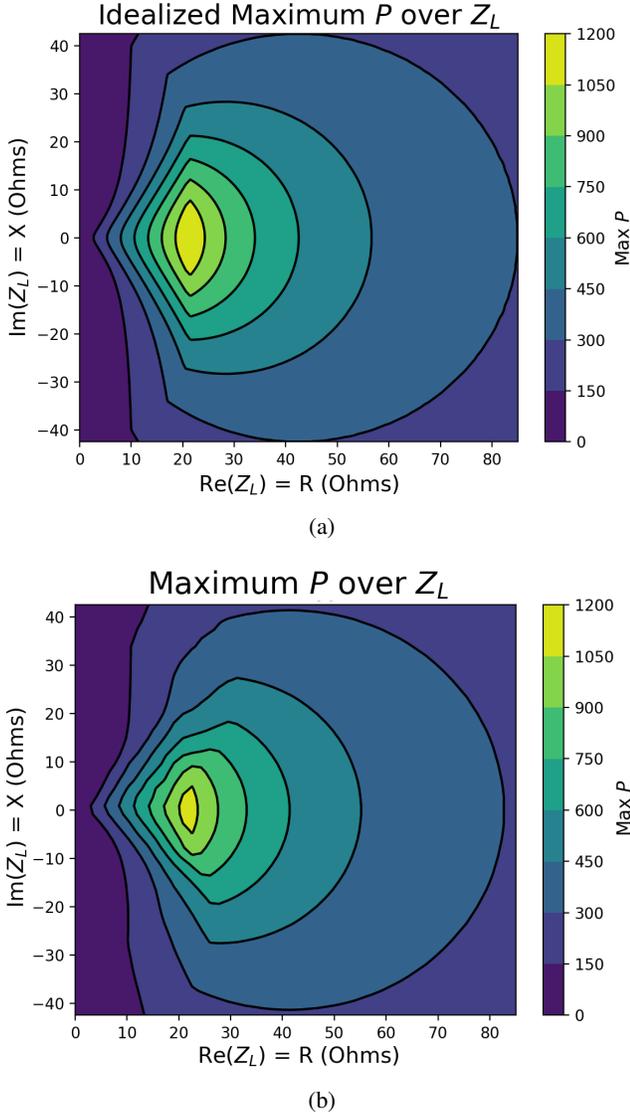


Fig. 10: Modeled maximum output power as a function of load impedance for: (a) an idealized HFVLI system based on the equations of Section II, (b) prototype HFVLI system based on the controller model, including dv/dt limits and loss limits.

switching period dv/dt limit of the constituent inverters that is imposed by the digital isolator used in the gate drive circuitry. This effectively imposes a limit on the maximum inductive load current that is smaller than the device and thermal limits, as $dv/dt = I/C$. To illustrate this fact Figure 11 presents the modeled load range of the prototype with the dv/dt limit removed from the controller. As can be seen, the load range extracted from the controller with the dv/dt limit removed matches the ideal load range much more closely. Remaining differences are largely due to the thermal limit imposed by the controller, reduction in available inverter output current due to inductive current synthesized through the immittance converter, and numerical limitations in the controller model.

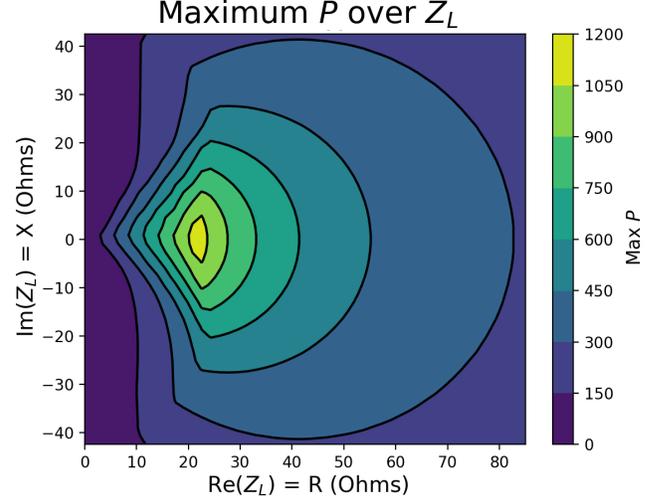


Fig. 11: Modeled maximum output power for the prototype HFVLI system with dv/dt limit removed.

TABLE IV: System parameters of loads a-c for predicted loss breakdown.

	A	B	C
Z_L	$21.3 + 0j$	$18.6 + 10.6j$	$18.6 - 10.6j$
P	500W	500W	500W
η	95.9%	95.2%	94.3%
Loss	21.2W	25.3W	30.3W
$ V_A $	103.2V	111.0V	111.0V
$ V_B $	66.3V	83.3V	148.1V
$ I_A $	3.5A	4.0A	2.9A
$ I_B $	2.4A	2.6A	2.6A
$ I_L $	4.8A	5.2A	5.2A
ϕ_{V_B}	66°	77°	29°

B. Modeled Efficiency and Loss Breakdown

The controller model calculates the power dissipated by each inverter in order to minimize the total power dissipation. For the predicted performance data presented in this section, the controller was modified to also calculate the losses in the output filters and the immittance converter based on the component quality factors and known waveforms. This allows for estimating the efficiency of the HFVLI prototype and for generating loss breakdowns, which would be difficult to measure in-situ. In Figure 12 we present the predicted loss breakdown of the prototype HFVLI system for (a) resistive, (b) resistive/inductive, and (c) resistive/capacitive loads at a 500W output power level and an impedance magnitude equal to the maximum output power impedance of the system. In Table IV we present the system operating parameters for these load points.

If inverter loss was dominated by conduction (I^2R) losses, it would be expected that the majority of the current would be sourced from inverter B, especially at the resistive load point (a), as inverter B's contribution to the load current is dependent on its output voltage due to the action of the immittance converter. However, as can be seen in the system parameters for load (a), the majority of the load current is supplied by inverter A, which also experiences the majority of the losses. This disparity is due to the voltage dependent

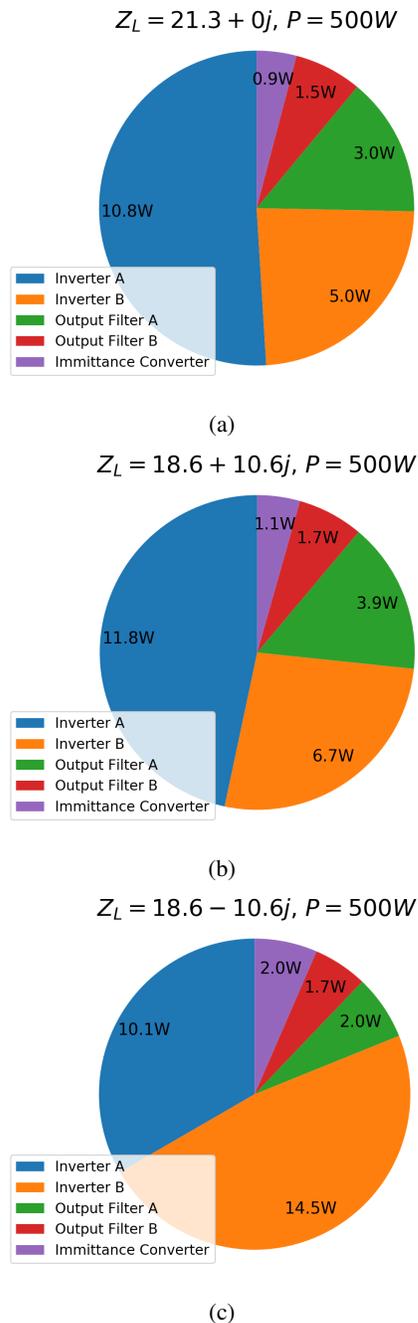


Fig. 12: Modeled loss breakdown of the prototype HFVLI system at a $500W$ power level for (a) resistive load, (b) resistive/inductive load, (c) resistive/capacitive load.

losses of the inverters. A higher supply voltage increases the inductive load current needed to achieve zero voltage switching, increasing conduction loss, and also increases the dv/dt related C_{oss} loss. As the output voltage of inverter B determines the output current of inverter A there is a trade off between the conduction loss of inverter A and the supply-voltage-related loss of inverter B. This optimization leads to the unequal distribution in loss between the inverters for the resistive load point.

For the modeled loss breakdown of (b), the resis-

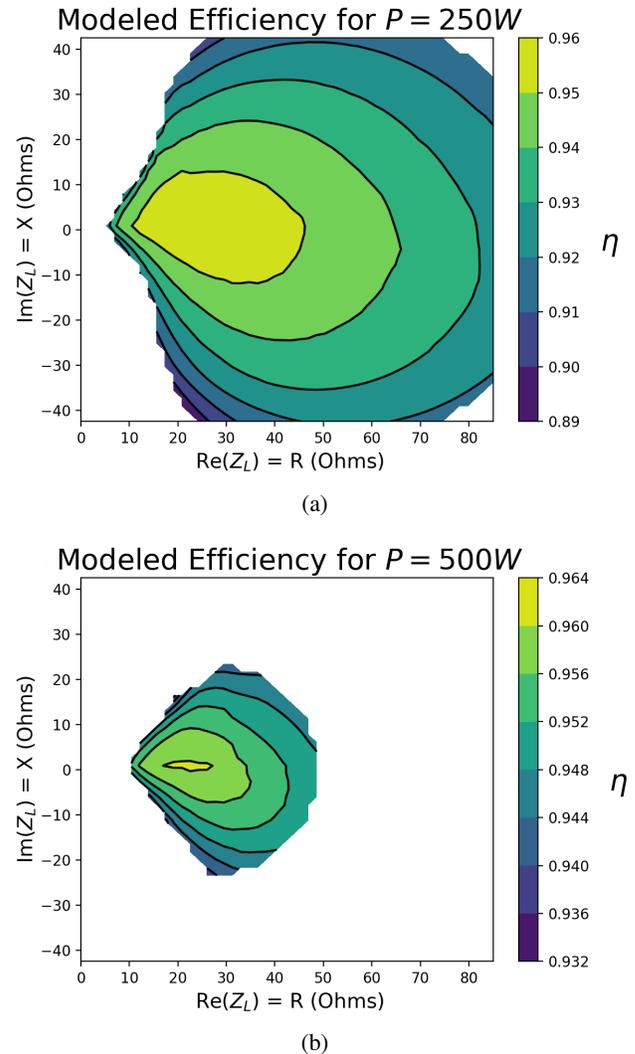


Fig. 13: Predicted efficiency across load range of the prototype HFVLI system at (a) $250W$, (b) $500W$.

tive/inductive load, inverter A must source the inductive load current and thus sustains the majority of the losses. For the modeled loss breakdown of (c), the resistive/capacitive load, inverter B must source the capacitive load current and thus sustains the majority of the losses. For all the load points the loss in the output filter is dependent on the output current of its respective inverter while the loss in the immittance converter is dependent on the output voltage and output current of inverter B.

In Figure 13 we present the predicted efficiency for the prototype HFVLI system across the achievable load range for operation at (a) $250W$ and (b) $500W$. As can be observed for both power levels the predicted efficiency is highest close to the maximum output power impedance of 21.3Ω , decreases as reactive loading increases, and, at lower impedances, is slightly higher for resistive/inductive loads when compared to a resistive/capacitive load of the same magnitude and opposite phase angle. Predicted efficiency is lower for reactive loads as reactive power supplied by the prototype contributes to

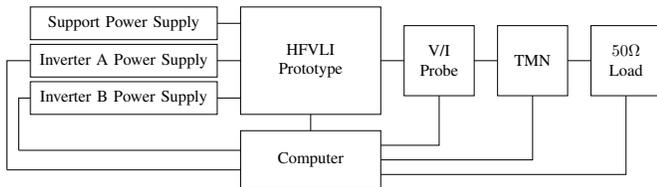


Fig. 14: Block diagram of prototype test setup.

TABLE V: List of equipment used in prototype testing.

Equipment	Specifications	Model
Support Power Supply	0-60V, 3.5A	GW Instek PSP-603
Inverter A Power Supply	5-600V, 2.6A	BK Precision XLN60026
Inverter B Power Supply	0-600V, 4A	KEPCO KLP 600-4-1200
V/I Probe	50Ω Nominal Impedance	MKS Model 000-1106-117
Tunable Matching Network (TMN)	13.56MHz, 50Ω Input	MKS model MWH-100
RF Load	50Ω, 500W	BIRD model 8201
Oscilloscope	4 Channel, 500MHz bandwidth	Tektronix MSO4054B
Oscilloscope Probes	4kV, 100X, 400MHz bandwidth	LeCroy PPE4KV

losses in the constituent inverters while not contributing to delivered power. Predicted efficiency is somewhat lower for resistive/capacitive loads compared to resistive/inductive loads of the same magnitude and opposite phase angle, as delivering a capacitive load current through the action of the immittance converter requires a higher output voltage for inverter B, increasing supply voltage related losses. Predicted efficiency is highest close to, but not exactly at, the maximum output power impedance. This is influenced by the impedance of the immittance converter and the fact that the constituent inverters have a “maximum efficiency” impedance that varies with the desired output voltage where incremental changes in conduction loss and supply voltage related loss are balanced. The controller has the greatest freedom to optimize the distribution of load between the two inverters at impedances close to the maximum output power impedance point, but the true point of highest efficiency depends on the inverter characteristics and the desired output power level.

Overall, these plots predict that the HFVLI prototype is capable of driving a wide range of load impedances while maintaining high efficiency.

VI. EXPERIMENTAL RESULTS

A. Experimental Setup

The experimental setup consists of the HFVLI prototype, two adjustable power supplies to supply power to the constituent inverters, a power supply for the control and gate drive circuitry, a 50 ohm RF load and tunable matching network to provide a variable load impedance, and a V/I probe to measure the load impedance and power delivered by the prototype. An oscilloscope was used to collect waveforms when applicable. Figure 14 presents a block diagram of the core test setup, Table V provides details about the test equipment used, and Figure 15 provides a photograph of the test setup. The prototype system and test equipment, excluding oscilloscope, were connected to a computer to allow for automation of some of the testing, drastically increasing the number of load impedance and output power level combinations that could be evaluated.

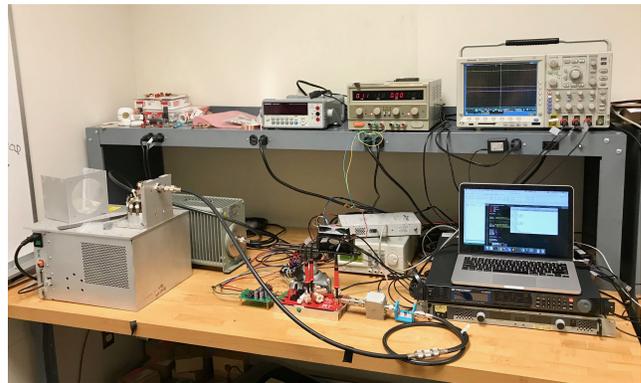


Fig. 15: Photograph of prototype system test setup. The variable load provided by a tunable matching network and 50Ω RF load can be seen at the left side of the bench. The HFVLI can be seen at the center of the bench, with the V/I probe on its right side, coupled in series with the output coaxial cable. The controlled power supplies and laptop for system control can be seen at the right side of the bench.

TABLE VI: Operating parameters of the prototype system for loads a-c.

	A	B	C
Z_L	$21.6 + 0.7j$	$18.6 + 10.6j$	$18.6 - 10.4j$
P	497W	497W	498W
η	95.8%	90.7%	92.1%
V_{INA}	246V	258V	242V
V_{INB}	194V	288V	351V
Duty A	0.35	0.39	0.34
Duty B	0.35	0.33	0.39
ϕ_B	69°	74°	26°

B. Operating Waveforms

The first set of tests were conducted to capture switching waveforms and measure operating parameters of the system at specific load points. This is important to validate the ability of the controller to generate correct sets of operating conditions and validate the maximum power output of the system. In Figure 16 we present waveforms from testing at resistive, resistive/inductive, and resistive/capacitive load points of equal magnitude and a 500W power level. In Table VI we present the operating conditions for these three points. Due to some phenomena not fully modeled in the system controller and slight mis-tuning of the output filters and immittance converter, the realized output power is typically lower than the desired value provided to the controller, so the reference value of desired output power provided to the controller was iteratively adjusted to achieve the desired output power (as would be realized under closed-loop control).

The converter waveforms show that zero voltage switching of both constituent inverters and high efficiency is achieved for all three impedances. Some distortion in the output voltage of the system can be observed, especially for the capacitive load point, load (c). This is due to a number of factors including the performance of the output filter, the high-pass characteristic of the immittance converter topology chosen, and the frequency dependence of the impedance presented by the load. Although the distortion has little impact on efficiency or performance

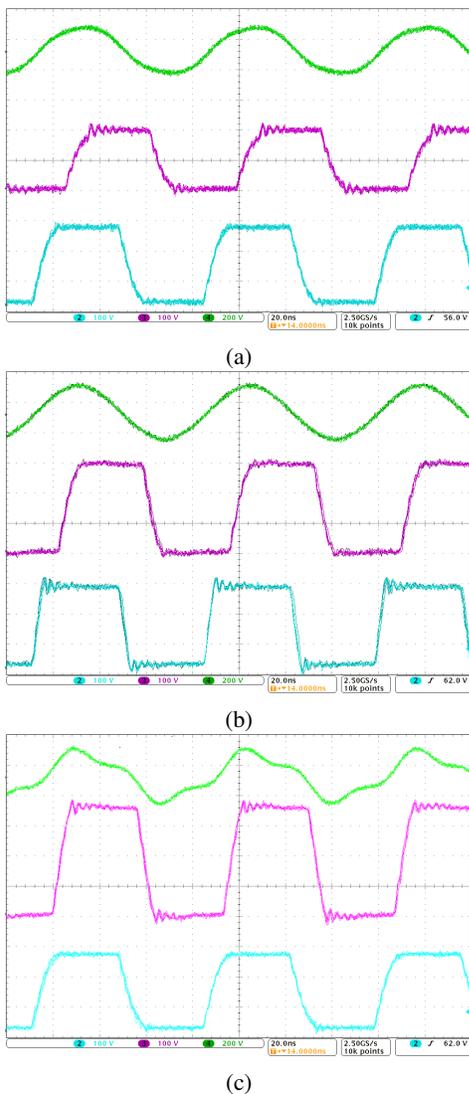


Fig. 16: Experimental inverter waveforms at a 500W power level for loads a-c in Table VI showing zero voltage switching. From top to bottom in each capture: output voltage in Green (200V/div), inverter B switching node in purple (100V/div), inverter A switching node in turquoise (100V/div).

in this application, it could be reduced by increasing the impedance the output filter to harmonics, adding a parallel resonant filter to shunt harmonics to ground, or by using an immittance converter with low-pass characteristics.

Here we also present waveforms, in Figure 17, and operating conditions, in Table VII, for operation into a load close to the maximum output power load impedance of 21.3Ω at power levels of 750W and 1000W. The 1000W point represents the maximum power output of the system that was validated in testing. As can be seen in waveform (e) inverter B does not fully achieve full zero voltage switching, switching instead with around 50 V on the incoming transistor. However, the efficiency remains quite high, indicating that this has little impact on performance.

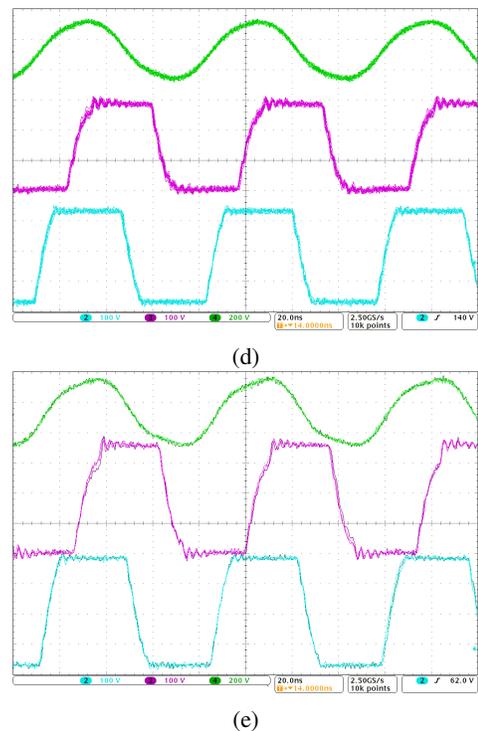


Fig. 17: Experimental inverter waveforms at 750W and 1000W power level for loads d-e in Table VII showing zero voltage switching. From top to bottom in each capture: output voltage in Green (200V/div), inverter B switching node in purple (100V/div), inverter A switching node in turquoise (100V/div).

TABLE VII: Operating parameters of the prototype system for loads d-e.

	D	E
Z_L	$21.7 + 0.7j$	$21.8 + 0.3j$
P	749W	1009W
η	95.5%	95.4%
V_{IN_A}	299V	350V
V_{IN_B}	279V	350V
Duty A	0.36	0.35
Duty B	0.34	0.34
ϕ_B	74°	76°

C. Efficiency Measurements

Due to the computerized control of the test equipment it was possible to measure the efficiency of the system over a wide range of load impedances. Figure 18 presents the measured efficiency of the system across the achievable load range at nominal power levels of (a) 250W and (b) 500W. At a 250W power level the tested load impedance range was limited by the impedance range of the variable load, while at 500W the load impedance range was limited by the load range of the prototype system (as illustrated in Figs. 5 and 10 for ideal theory and model prediction, respectively). Overall, the trends in measured efficiency match the predicted efficiency provided in Figure 13; the highest efficiency is achieved at close to the maximum output power impedance of 21.3Ω and efficiency is slightly higher for inductive loads than capacitive loads.

At very reactive loads the efficiency was measurably lower

VII. CONCLUSION

In this work we present a high frequency variable load inverter architecture along with a physical prototype and efficiency optimizing controller. The proposed HFVLI architecture comprises two constituent inverters with a lossless power combining network, implemented here with an immittance converter. By varying the phase and relative amplitude of the two constituent inverters the loading seen by each can be kept in some desired range for large variations in the load impedance, allowing for the use of high efficiency zero voltage switching inverters in applications with widely varying load impedances. The prototype HFVLI system operates at 13.56 MHz and can supply a maximum output power of 1 kW, which was achieved into a load impedance of $21.8+0.3j$ at an efficiency of 95.4%. This efficiency is comparable to or better than other published HF inverters in this frequency, voltage and power range (e.g., [27]) when operating into an ideal load impedance. Notably, however, the demonstrated HFVLI system can also drive a wide range of capacitive and inductive loads while maintaining high efficiency, a feature which has typically required external circuitry such as the resistance compression network or a tunable matching network.

The efficiency optimizing controller proposed for this new system utilizes a quasi-static model prediction approach and is structured in a way that allows optimization of any measurable system parameter. The model of the constituent inverters and HFVLI system created for the controller allows for extraction of performance data and a comparison of the achievable load range of the HFVLI prototype and the idealized HFVLI system. The achievable load range of the physical prototype closely matches the load range of the idealized system except for highly reactive loads of low impedance, where a dv/dt limit imposed by the gate drive circuitry of the constituent inverters limits the maximum reactive load current.

The work shows that the proposed HFVLI architecture and control approach is viable and provides high and well-characterized performance. Compared to previous approaches to driving variable loads, such as the resistance compression network or use of a tunable matching network, the HFVLI requires no variable reactive components or changes to the structure of the load. This approach holds great promise in applications that require RF power to be delivered to widely varying loads such as wireless power transfer and plasma generation where it could lead to systems that are more efficient, more compact, and less expensive.

APPENDIX A

CONSTITUENT INVERTER MODELING AND MODEL PREDICTION CONTROLLER DESIGN

A. Constituent Inverter Model

The constituent inverter model can be considered a black box from the prospective of the search function. The inverter model receives a load point consisting of a desired output voltage and output current from the search function, determines if zero voltage switching is achievable for the load point, and if so, returns the operating parameters and an estimate of power dissipation so the search function can optimize efficiency.

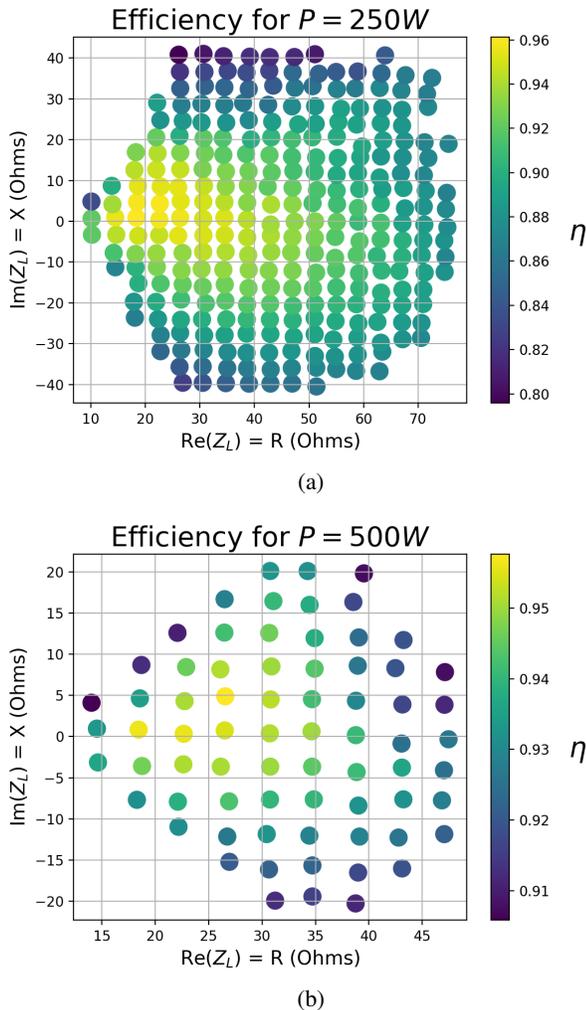


Fig. 18: Measured efficiency of prototype HFVLI system over load range for output power levels of (a) $250W \pm 10\%$ and (b) $500W \pm 20\%$.

than the predicted efficiency derived via the model. This difference could be due to some combination of inaccuracies in measuring the delivered power with the V/I probe, transistor loss mechanisms that were not correctly modeled, and failure of the controller to calculate conditions that ensure ZVS at all load points. The sharp drop off in efficiency for highly inductive loads on the 250W plot may be indicative of a possible loss of zero voltage switching, as zero voltage switching can be greatly affected by small changes in loading and strongly impacts efficiency.

Even with the reduced efficiency compared to what was modeled, the HFVLI prototype still exhibited a minimum efficiency of 90.6% across the entire load range at 500W, a minimum efficiency of 79.6% at 250W, and a high average efficiency across the entire load range. From these results it is evident that the HFVLI prototype is successful in the goal of driving a wide load range at high power levels.

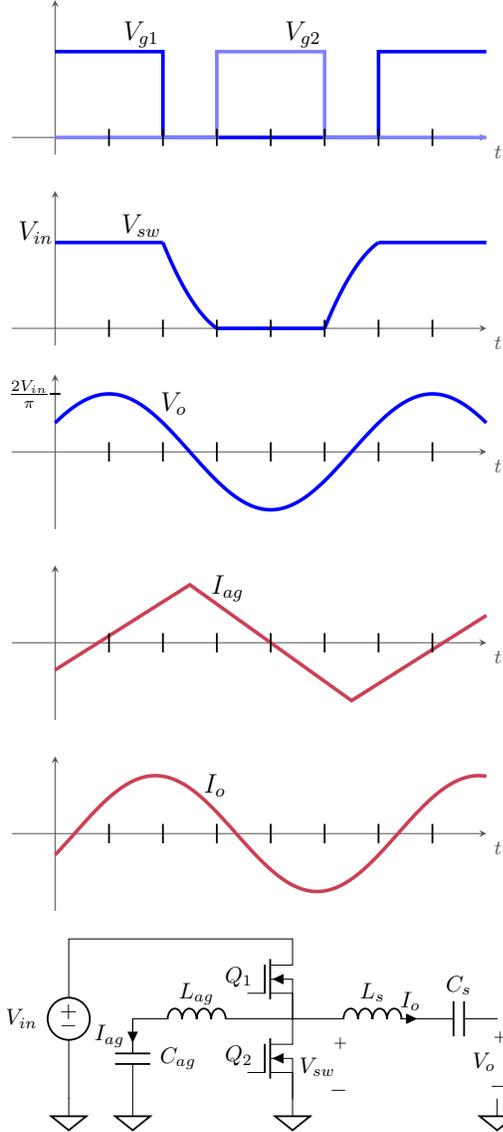


Fig. 19: Constituent Inverter Schematic with Idealized Waveforms for Arbitrary Resistive/Inductive Load

Additionally, for the class D half bridge inverter used, there is an additional control parameter that is calculated, the switch duty cycle.

Figure 19 presents a schematic of a constituent inverter and idealized waveforms for an arbitrary resistive/inductive load. Using the equations presented in [11] as a basis, we derived a system of equations that includes some simplifications and approximations, but also captures some mechanisms and losses not originally accounted for in [11].

The system of equations used to model the constituent inverters are provided below. V_o and I_o are the phasors representing the rms output voltage and current, both of which are assumed to be sinusoidal. The phase of V_o is taken to be zero with I_o having a phase relative to V_o , and the switching deadtime occurs symmetrically around $t = 0$. $C_{sw}(V_{in})$ is a function providing the total charge equivalent linear capacitance as a function of supply voltage for the switching device used and is derived from a polynomial fit

from the graph provided in the device datasheet. $i_{AG}(t, V_{in})$ represents the switching augmentation current provided by the added pre-load inductance. This current is assumed to be triangular and periodic, with amplitude dependent on V_{in} , and as an inductive current, lagging V_o by a quarter cycle. Q_{sw} is the charge delivered to the switching node while Q_{zvs} is the charge required to achieve zero voltage switching. $i_{SW}(t)$ is the current flowing into the switching node, used for subsequent equations.

$$V_{in} = \frac{|V_o|\pi\sqrt{2}}{2} \quad (20)$$

$$Q_{zvs} = 2V_{dss}(C_{sw}(V_{in}) + C_{static}) \quad (21)$$

$$i_{SW}(t) = -\sqrt{2} \operatorname{Re}(I_o e^{jt2\pi f_{sw}}) - i_{AG}(t, V_{in}) \quad (22)$$

$$Q_{sw} = \int_{-D/(2f_{sw})}^{D/(2f_{sw})} i_{SW}(t) dt \quad (23)$$

$$Q_{zvs} = Q_{zvs} \quad (24)$$

The two required inverter parameters, the input voltage, V_{in} , and switch duty cycle, D , can be solved for via this system of equations. The input voltage has a direct relation with the desired output voltage⁴ while the switch duty cycle is calculated by numerically solving the integral of Equation 23. For some load points there is no solution for the integral, representing points at which ZVS can not be achieved due to insufficient inductive load current.

Finding a valid duty cycle for which zero voltage switching can be achieved does not mean that the identified operating point is valid; there is still a need to check additional inverter constraints. There is a maximum supply voltage for the inverter, $V_{in,max}$, and a maximum output current $I_{o,max}$, both chosen to protect the switching devices. There is also a maximum power dissipation, P_{max} , chosen based on the maximum switching device junction temperature and the thermal resistance of the heatsink. The estimated power dissipated by each switching device comprises of P_{oss} and P_{rds} . P_{oss} is the power dissipated in the switching device capacitance, which can be significant for GaN devices, even under ZVS. $E_{oss_diss}(\cdot, \cdot)$ is a function used to calculate P_{oss} and returns the expected energy dissipated in the switching device capacitance per cycle based on the analytical data presented in [18]. P_{rds} is the I^2R loss due to the on resistance, R_{on} , of the switching devices, including dynamic R_{on} effects that were modeled based on analytical data from [19]. A maximum dv/dt limit is imposed by the CMTI of the digital isolator used in the gate drive circuitry. The equations for these checks

⁴in (20) we neglect the dependency of the rms output voltage on the switch duty ratio; this approximation has relatively modest effect on the results.

are shown below:

$$V_{in} \leq V_{in,max} \quad (25)$$

$$|I_o| \leq I_{o,max} \quad (26)$$

$$\frac{dv}{dt} = \max_{|t| \leq D/(2f_{sw})} \frac{i_{SW}(t)}{C_{sw}(V_{in})} \quad (27)$$

$$\frac{dv}{dt} \leq \frac{dv}{dt}|_{\max} \quad (28)$$

$$P_{coss} = 2f_{sw}E_{oss_diss}\left(\frac{dv}{dt}, V_{in}\right) \quad (29)$$

$$P_{rds} = \frac{2}{f_{sw}} \int_{(D/2)/f_{sw}}^{(1-D/2)/f_{sw}} R_{on}i_{SW}(t)^2 dt \quad (30)$$

$$P_{max} \geq P_{coss} + P_{rds} \quad (31)$$

If a valid duty cycle is calculated and all additional checks pass the inverter model returns that the operating point is valid, the required supply voltage, V_{in} , duty cycle, D , and any additional parameters required for optimization by the search function. Currently the only additional parameter returned is the power dissipation of the inverter which is used to minimize the total power dissipation.

B. Search Function

The search function is the top level component of the control system. Given values of desired output power and load impedance, the search function determines the full set of operating parameters for the system (output voltage and duty cycle of constituent inverters, phase between them) that optimizes performance according to some cost function. Due to the constituent inverter model we can abstract away the constituent inverters as voltage sources as done in the modeling of the idealized system and continue to use this base system of equations given in Section II, equations 2-6.

Given a desired output power and load impedance, the output voltage of inverter A, V_A , the load current, I_L , and the output current of inverter B, I_B , are fixed. For loads not on the boundary of achievable output power the system is unconstrained and there are many valid combinations of current delivered by inverter A, I_A , and current delivered by inverter B through the immittance converter, I_Z . Given a choice of I_A , the entire system, including I_Z , is constrained. The search function searches the space of I_A for a distribution of load current between I_A and I_Z that is deemed allowable by the constituent inverter model (achieving ZVS and satisfying all other inverter constraints) and is optimal according to some cost function. This includes points with synthesized inductive load current (where $\text{Im}(I_A) > \text{Im}(I_L)$). Given that I_A is a complex phasor, this represents a two dimensional search space; the real and imaginary components of I_A . This search space is of low enough dimensionality that search is not computationally difficult, either through exhaustive search (as used in the prototype system) or via some sort of gradient descent/peak finding.

As the search function searches through possible values of I_A it utilizes the constituent inverter model to evaluate the loading on each inverter. At each point the search function

queries the inverter model with the desired output voltage and current for each of the two inverters. As previously described, the inverter model returns if an inverter load point is valid, and if so, returns additional performance data used to evaluate the distribution in load between the two inverters. Currently the only performance data optimized over is the calculated power dissipation for the two inverters. The cost function used in the controller attempts to maximize efficiency by minimizing the sum of the power dissipated between the two constituent inverters and can be expressed as:

$$\text{Min}(P_{diss,A} + P_{diss,B}) \quad (32)$$

Regardless of the choice of cost function, if the search function returns the set of operating conditions for which the loading on both inverters is deemed valid by the constituent inverter model and for which the cost function evaluates most optimally. If no valid point was found the system is not capable of delivering the desired output power into the given load impedance.

C. Controller Implementation

The controller was implemented in Python2.7 and runs on the laptop used for testing the HFVLI system. Binary search is used to numerically solve the required integral for duty cycle of the constituent inverters and the search function performs a brute force search of I_A over a real component of $[0, \text{Re}(I_L)]$ and imaginary component of $[0, I_{max}]$ with approximately 4.5 bit precision on each.

As the initial goal was merely to generate optimized static operating conditions for the system, little effort was placed into optimizing the controller for speed in calculating operating conditions. The present unoptimized version of the controller takes approximately 180ms to generate a set of operating conditions (dual core x86-64 processor). However, there are multiple areas in the controller for which a rewrite could yield significant speedups, including a more optimized approach for the search function, porting the code base to a compiled programming language with lower overhead, and structuring the controller to utilize more than one CPU core. Porting to a compiled language would also allow for the controller to be ported to an embedded processor.

A likely implementation of the controller for a commercial application would be to use a lookup table based implementation where operating points are precomputed and stored in memory. As the system is quasi-static and the input space is only three dimensional (real and imaginary components of load impedance, output power), the controller maps well to this approach. A precomputed lookup table would allow for almost instantaneous generation of system operating conditions, with the main limitation being memory access speed. At 8 bit precision for all inputs and outputs, a lookup table implementation would take approximately 84MB of memory, and interpolation would enable significantly higher resolution without additional storage. External flash memory of this capacity is inexpensive, allowing the controller to be ported to even very low performance embedded devices if this approach is taken.

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