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Variable-Inverter-Rectifier-Transformer: A Hybrid Electronic and Magnetic Structure Enabling Adjustable High Step-Down Conversion Ratios

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***Abstract*—This paper proposes a hybrid electronic and magnetic structure named a Variable-Inverter-Rectifier-Transformer (VIRT) that enables a transformer with fractional and reconfigurable effective turns ratios (e.g. 12:0.5, 12:2/3, 12:1, and 12:2). This functionality is valuable in converters with wide operating voltage ranges and high step-up/down, as it offers a means to reduce the turns count and copper loss within the transformer while also facilitating voltage doubling and quadrupling. These properties are especially beneficial for miniaturizing the transformer stage in many power electronics applications, such as USB wall chargers. We introduce the principle of operation of the structure and present models for its magnetic and electrical behaviour. The instance of VIRT described in this paper comprises four half-bridge switching cells distributed around a planar magnetic core and connected to two "half-turns" wound through that core. By controlling the operating modes of the half-bridge cells, we gain control over the flux paths and current paths used in the transformer, and this hybridization enables fractional and reconfigurable effective turns ratios. An experimental prototype integrates the VIRT with a stacked-bridge LLC converter to accommodate a widely varying input (120–380 Vdc) and output (5–20 Vdc), and VIRT is shown to be highly beneficial in keeping efficiency high over this wide output voltage range.**

***Index Terms*—Magnetic circuits, transformers, fractional turns, planar magnetics, wide output voltage range conversion, VIRT, hybrid electronic and magnetic structures, USB Power Delivery**

I. Introduction

Advancements in switch technologies, such as the introduction of GaN FETs, have enabled tremendous gains in the size and performance of the active switches used in power electronic converters, but advances in the design of passive components have lagged. Presently, passive components dominate the size and performance of power electronic converters and therefore present the major bottleneck to miniaturization. While both capacitive and inductive elements limit miniaturization, power-stage magnetic components (i.e. those inductors and transformers that are fundamental to the power transfer mechanism of the converter) present an important limitation on achievable size and efficiency [1].

Many power electronic converters rely on transformers to satisfy isolation safety requirements and to achieve the bulk of their voltage conversion ratio. For example, wall chargers for conventional USB-powered portable devices must interface at their input to the ac grid (up to 375 V peak voltage in regions employing a 240 Vac grid) and must step-down to as low as 5 Vdc at their output, corresponding to a 75:1 voltage conversion ratio. To achieve such step-down, it is typical to employ a transformer with a large turns ratio (e.g. 22:1 [2]). This demanding specification aggravates the volume and efficiency limitations of the transformer for two key reasons.

First, in applications where the transformer processes low voltages and high currents (as in the output of many converters), it is likely that the copper loss of the transformer far outweighs the core loss, and this imbalance compromises the efficiency of the transformer [3]. For a given transformer conversion ratio (e.g. 22:1), the choice of the number of primary and secondary turns used to implement this ratio provides a means to re-balance core and copper loss inside the transformer to minimize total loss. Specifically, as the number of turns is scaled down, copper loss is reduced at the cost of increased core loss. In applications with low voltages and high currents, this is the desired trade-off. However, this trade-off is fundamentally limited since fractional turns cannot be employed in a conventional transformer. If the transformer losses are not minimized after scaling down to a single-turn on either of the windings, one must either accept the reduced efficiency of the transformer or find another means to optimize loss (typically by increasing the size and window area of the transformer core).

A second limitation of transformers requiring large turns ratios is that placing a high number of turns around a core can in itself be problematic or unfeasible. This is particularly important when planar transformers, which offer tremendous potential for improved fabrication and miniaturization, are employed (the benefits of planar transformers for miniaturization are discussed in [3], [4]; example studies where planar magnetics have been employed to great effect for miniaturization are provided in [5], [6]). In a planar transformer windings are routed as traces on a printed circuit board (PCB), and these traces must adhere to the trace width and spacing fabrication requirements of the PCB. Thus, in addition to meeting current and voltage requirements, the trace width and trace-to-trace spacing must each be wide enough to meet the PCB fabrication requirements. Not only does this manufacturing constraint increase the resistance and copper loss of the transformer, it creates the possibility that a required number of turns cannot

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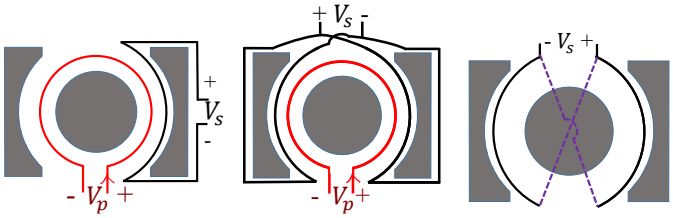
be accommodated at all in a given core window width.

An attractive means to mitigate these limitations is to use a transformer providing "fractional" turns ratios (e.g. 1:0.5). Such a transformer enables reduced turns counts in planar magnetics where window breadth is at a premium [3] while also offering the preferred trade-off between copper loss and core loss in applications with low output voltages and high output currents. One concept for a "fractional" turns transformer in power electronics was first introduced in the mid-1980s in the context of multichannel power supplies, with initial focus on its ability to fine-tune the turns ratio of unregulated transformer outputs [7], [8]. The key idea in these transformers is to wind a complete turn around a section of the transformer core that only carries a fraction of the primary-generated flux. For example, consider winding a single turn primary around the center-post of a conventional three-legged core and a single turn secondary around one of the outer legs, as shown in Fig. 1a. By symmetry of the core, half of the primary-generated flux enters each outer core leg. Thus, by Faraday's law, the voltage coupled onto the single-turn secondary is one half the voltage applied to the primary, creating an effective 1:0.5 transformer ratio (i.e. a "half turn" transformer). However, by extracting a "half turn" in this way, half of the primary-generated flux does not link to the secondary and instead circulates through the relatively low reluctance of the unused core leg, resulting in a leakage inductance on the order of the transformer's magnetizing inductance [9].

Permutations of this idea were proposed at the time, including using more complicated core shapes to further reduce the effective "turn fraction" of the secondary and developing special windings to cancel out the unwanted circulating flux [7]. A simple solution to the circulating flux problem is proposed in [8] and shown in Fig. 1b. Here, a single turn is wound around both outer legs of the three-legged core and then these windings are connected in parallel. In this configuration, half of the primary-generated flux is linked into each secondary winding, removing the "leakage" path of Fig. 1a. However, since these windings are connected in parallel, the secondary voltage V_s is still only induced by half of the primary-generated flux, thus the voltage conversion ratio remains V_p:V_s=1:0.5. An equivalent representation of the winding scheme in Fig. 1b is shown in Fig. 1c, proposed in [8] as means to further reduce the leakage inductance of the secondary. Here, two "half turns" achieve the same voltage coupling effect and improve on Fig. 1b as long as there is a means to parallel the voltages without going around the outer perimeter of the core. In a non-planar transformer, the wires can be brought "out of the page" and connected above the core, completing the turns around the core. However, this structure cannot be exploited as-is in a planar configuration. Moreover, it is important to note that with all of the above "fractional turns" design concepts, the amount of fluxed linked by windings is "fractionalized," but ac currents still appear around full loops of conductors around core sections, imposing associated conduction losses in the windings, so the turns are not "fractional" as regards conduction loss.

"Emulation" of fractional turns has also been proposed for push-pull topologies, where integer-and-a-half turns ratios



(a) A "fractional" turns ratio transformer yielding a 1:0.5 transformer ratio between primary and secondary [7], [8].

(b) Alternate configuration for a 1:0.5 transformer

(c) Alternate winding arrangement for Fig. 1b. The dotted lines represent connections made "out of the page."

Fig. 1: Previously proposed methods for achieving a transformer with a "fractional" turns ratio. (a) A single-turn secondary is wound around a core-leg that carries only half of the primary-generated flux, thus V_p:V_s=1:0.5. (b) An alternative configuration in [8]. The two outer leg windings are connected in parallel such that the secondary voltage V_s is induced by only half the primary-generated flux, thus V_p:V_s=1:0.5. (c) Also proposed in [8], two "half turns" achieve the same voltage coupling effect in Fig. 1b assuming there is a means to parallel the half-turns. For example, as proposed in [8] the wires could be brought "out of the page" and connected above the core (indicated by the dotted lines); these out-of-plane connections complete turns on sections of the transformer core, and impose additional conduction length on the secondary, greatly reducing the "half-turns" benefit in terms of conduction loss.

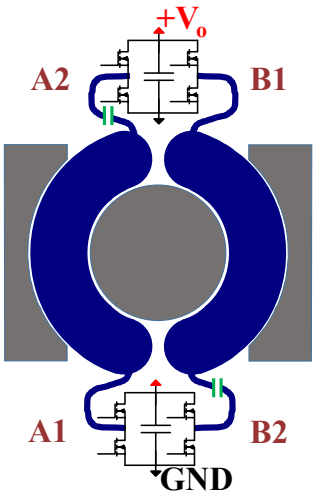
(e.g. 1:1.5) can be implemented via a center-tap transformer with an unequal number of secondary turns [10]. While this configuration may be attractive for achieving precise voltage conversion ratios, it is not suitable for miniaturization at high conversion ratios as it does not enable transformer ratios less than 1:1 (i.e. it cannot exploit a half-turns ratio) and it requires a center-tapped transformer, which can be problematic for achieving good current-handling capability if planar magnetics are used [3].

Transformers with the true ability to provide fractional turns would offer strong benefit for achieving miniaturization in applications with high step-up/down ratios. Additionally, in many power electronic converters where a transformer is employed to achieve large voltage conversion ratios, there is also a need to accommodate wide operating ranges. For example, Universal Serial Bus - Power Delivery (USB-PD) wall chargers must typically accommodate universal ac voltage (85 - 265 Vac) at their input, while regulating to voltages between 5 and 20 V_{dc} at their output [11]. In conventional designs, these wide operating ranges are managed by changing the operating point of the regulating converter (e.g. by changing the duty-cycle of a flyback converter). However, the combination of the large voltage conversion ratios and the large variations in conversion ratios represent a significant design challenge that compromises efficiency and limits the ability to miniaturize the system. Similar constraints exist in other wide-output-range applications such as Dynamic Voltage Scaling (DVS) for

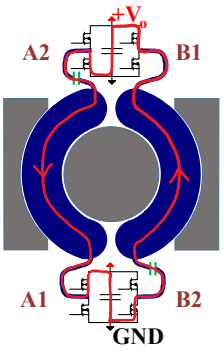
electronic loads and Adaptive Power Tracking for rf amplifiers.

This paper proposes a hybrid electronic and magnetic structure that realizes a transformer with a fractional and reconfigurable effective turns ratio. Unlike previous "fractional" turn designs, the strategy proposed here yields ac currents flowing in only fractions of a complete turn prior to rectification, enabling reduced conduction loss as compared to previous concepts. Moreover, the proposed approach enables dynamic electronic reconfigurability of the effective transformation ratio, providing added degrees of flexibility. Together, these qualities enable miniaturization of the transformer stage in converters where variable high step-up/down ratios are required. The proposed structure is called a "Variable-Inverter-Rectifier-Transformer" (VIRT), named this way because it fundamentally connects the rectifier stage (or inverter, or both) of a converter to the magnetic structure of the transformer and through this hybridization enables variable conversion ratios, fractional effective turns, and reduced conduction loss. While hybridization of passive and active electronic elements has been used to a limited extent in some applications (e.g., for rf power combining/matching [12], [13] and actively-controlled antennas [14]–[18]) this largely represents an untapped direction in power electronics, with significant potential benefits in many applications.

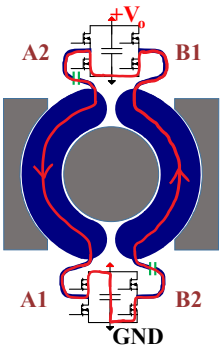
This paper expands on our preliminary conference publication in [19]. Section II provides intuition on the principle of operation of the VIRT as in [19]. In Sections III and IV we present comprehensive modeling and discussion of all of the achievable VIRT modes and their trade-offs, including a previously unexplored mode. In Section V we present a converter design with a wide-range output voltage of 5–20V and in designing for this expanded range we employ all of the available VIRT modes, offering insight into converter design using the full voltage adjustment capability offered by the VIRT. Finally, Section VI presents comprehensive experimental results, providing a detailed comparison of the operation of the different modes and highlighting the efficiency benefit the VIRT offers for applications requiring large and wide-range step-down conversion.



(a) VIRT structure



(b) Example current flow in FB/FB mode



(c) Example current flow in HB/0 mode

Fig. 2: (a) Illustration of the VIRT structure. A cross-section taken on the plane where the secondary half-turns are routed is shown. Note that the placement of the rectifier schematics reflects their physical location relative to the magnetic core. Blocking capacitors are included for each rectifier. (b) Example snapshot of induced secondary ac current when operating in FB/FB mode and (c) HB/0 mode.

II. Principle of Operation

An example VIRT structure is shown in Fig. 2a. Here, two full-bridge rectifiers are distributed around a magnetic core and connected through two half-turns on the secondary side. The primary winding is not shown but it comprises an arbitrary number of turns wound around the center-post. The two rectifiers are named A and B. Rectifier A comprises the half-bridge cells labelled A1 and A2, and rectifier B, cells B1 and B2. Each half-bridge cell is directly connected to the output bus through the terminals labelled $+V_o$ and GND, for example through power and ground planes that are routed outside the magnetic core.

Each rectifier can be operated in full-bridge (FB), half-bridge (HB), or "zero" mode. For example, if rectifier A is operated in FB mode, then both A1 and A2 are active and switching as a conventional full-bridge rectifier. In HB mode, cell A1 operates as a conventional HB rectifier while A2 is held in the low state. In zero mode, both cells A1 and A2 are held in the low state to provide an effective ac short of that section of the winding.

The principle of operation can be intuitively understood by considering the path of the induced secondary-side current. For example, consider operating in a full-bridge/full-bridge (FB/FB) manner in which rectifiers A and B are both in FB mode and cell A1 is switched in-phase with cell B1. Assume that flux through the core is generated by applying an ac voltage with peak V_p onto the N_p primary turns such that ac current is induced in the secondary winding. When operating in FB/FB mode, as illustrated in Fig. 2b, the induced current flows such that the output voltage V_o is effectively inserted twice into the secondary loop. Equating the V/N ratios in this case yields $V_o/V_p = 1/(2N_p)$. This is equivalent to the voltage conversion ratio of an N_p:0.5 transformer. Now consider operation in a half-bridge/half-bridge (HB/HB) manner where both rectifiers act as half-bridges. The path of induced secondary current is identical to the FB/FB case in

Fig. 2b but now only yields a single V_o insertion into the loop around the center-post due to the voltage-halving action of the half-bridges. The voltage conversion ratio is changed to $V_o/V_p = 1/N_p$, equivalent to the conversion ratio of an N_p:1 transformer. Thus, we can dynamically reconfigure the effective transformation ratio through the operating patterns of the rectifier. Moreover, as will be described in greater detail below, this is done with reduced secondary ac conduction path length, improving the achievable conduction loss.

FB/FB and HB/HB modes are "symmetric" operating modes in that we only have ac secondary currents in the paths around the center-post due to the identical operation of the rectifiers. However, there are other "asymmetric" operating modes that have some degree of ac current flow in full paths about the outer core legs, but which provide additional flexibility in voltage conversion. For example, by operating in the half-bridge/zero (HB/0) mode as in Fig. 2c[1], it is possible to achieve a conversion ratio of $V_o/V_p = 2/N_p$, equivalent to an N_p:2 transformer. Additionally, one can operate in full-bridge/half-bridge mode (FB/HB) to achieve a conversion ratio of $V_o/V_p = 2/(3N_p)$, equivalent to an N_p:2/3 transformer.

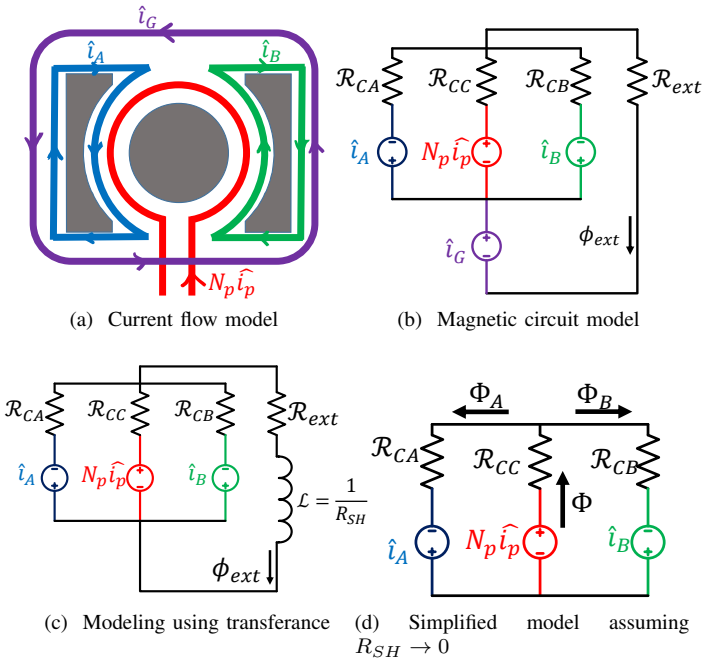
The ability to dictate the path of induced secondary side current, and in turn to choose the effective voltage applied to the secondary loop, enables a transformer with an effective variable turns ratio of N_p:1/2, N_p:2/3, N_p:1, and N_p:2. Note that this concept can be extended to other fractional turns ratios, including "integer-and-a-half" ratios, by appropriately selecting the number of secondary half-turns and/or core sections. For example, as illustrated in Appendix A, a 5-legged core provides multiple additional operating modes including an N_p:0.25 effective turns ratio; likewise, other rectifier configurations (e.g. multilevel rectifiers) and other combinations of core structures and rectifiers can be used to provide desired gain characteristics and reconfigurability.

III. Electrical Models

To derive electrical models of the different operating modes of the VIRT in Fig. 2a and to better elucidate the current and flux patterns in the transformer, we first develop a magnetic circuit model for each operating mode. We begin with a modeling procedure for the symmetric operating modes (FB/FB and HB/HB) and then extend this procedure for the asymmetric modes (FB/HB, FB/0, and HB/0). For reference, a summary of each VIRT mode is provided in Table I.

A. Symmetric VIRT Modes (FB/FB and HB/HB)

In the symmetric operating modes, we can model the current flow in the system as closed loops around the core as shown in Fig. 3a. In this figure $\hat{i}_A$ and $\hat{i}_B$ represent the currents that flow between the half-bridge cells in rectifiers A and B, respectively. For the purposes of modelling, these currents are drawn as returning outside the core via the ground plane. Note that in practice one would expect these current components to be equal (for the symmetric operating modes) since the two-half turns and the rectifiers are identical and symmetric, and effectively form a single loop onto which current is induced by flux passing through the center-post in Fig. 2a. In this case current is not expected to return around the core and so these current components outside of the core are deemed "virtual" - they are invoked for modelling purposes only. Another "virtual" current component $\hat{i}_G$ is included in the model where $\hat{i}_G = \hat{i}_A = \hat{i}_B$ such that the (virtual) outer current components of $\hat{i}_A$ and $\hat{i}_B$ are cancelled. The resulting net current flow in this model is equivalent to the physical current that flows through each half-turn as in Fig. 2.



(a) Current flow model (b) Magnetic circuit model

(c) Modeling using transferance (d) Simplified model assuming $R_{SH} \to 0$

Fig. 3: Derivation of the VIRT magnetic circuit model for the symmetric VIRT modes. (a) "Virtual" currents are employed such that all currents form closed loops around the core, (b) Associated magnetic circuit model, (c) The MMF associated with $\hat{i}_G$ can be modeled by a transferance element $\mathscr{L}$, which is defined by the resistance of the ground-plane surrounding the transformer, R_{SH}, (d) Assuming the ground plane has negligible resistance, $\mathscr{L} \to \infty$ and we arrive at the simplified magnetic circuit model.

From this model, it is straightforward to synthesize the magnetic circuit model shown in Fig. 3b. In practice, the magnetomotive force (MMF) associated with the "short-circuit" path of $\hat{i}_G$ is associated with a small induced voltage due to the small resistance R_{SH} of the ground-plane. The relationship between the flux and this MMF can be modeled by a transferance element $\mathscr{L}$ [20] as shown in Fig. 3c. In the limit where $R_{SH} \to 0$, $\mathscr{L} \to \infty$ and the circuit model simplifies to that of a standard three-winding transformer with a parallel magnetic circuit as shown in Fig. 3d. Thus, the simplified electrical model in Fig. 4 can be derived. In this circuit schematic

[1]In Fig. 2c we show the current returning through the half-turn associated with rectifier B for the benefit of intuitively understanding the principle of operation. In practice, the rectifier B half-turn is connected to the ground plane in the HB/0 mode and rectifier A current may return outside of the core via the ground plane. The path of the return current in this mode does not ideally change the derived voltage conversion ratio. The impact of this out-of-core current is addressed in Section IV-C.

TABLE I: Summary of each VIRT mode

VIRT mode	Description	Effective turns ratio	Mode type	Effective LLC load resistance	"Net" magnetizing inductance ($L_A + L_B$) †
FB/FB	All switches active	N_p:$\frac{1}{2}$	Symmetric	$R_e = 32N_p^2R_L/\pi^2$	$L_M = \frac{N_p^2}{2\mathscr{R}_{CC}}$
FB/HB	A1, A2, B1 active; B2 held in low state	N_p:$\frac{2}{3}$	Asymmetric	$R_e = 18N_p^2R_L/\pi^2$	$\frac{34}{35}L_M$
HB/HB	A1, B1 active; A2, B2 held in low state	N_p:1	Symmetric	$R_e = 8N_p^2R_L/\pi^2$	L_M
FB/0	A1, A2 active; B1, B2 held in low state	N_p:1	Asymmetric	$R_e = 8N_p^2R_L/\pi^2$	$\frac{2}{3}L_M$
HB/0	A1 active; A2, B1, B2 held in low state	N_p:2	Asymmetric	$R_e = 2N_p^2R_L/\pi^2$	$\frac{2}{3}L_M$

† For a fixed gap across all three core legs as discussed in Section III.

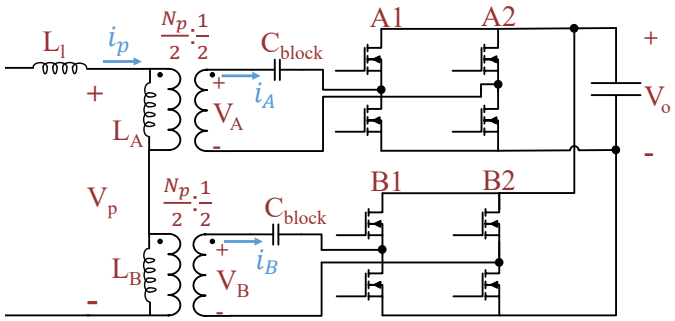


Fig. 4: Simplified electrical model of the VIRT implementation in Fig. 2a with N_p primary turns.

we show the two transformer ratios as $\frac{N_p}{2}$:$\frac{1}{2}$ to reflect the fact that there are N_p total turns wound on the primary. Assuming $\mathscr{R}_{CA} = \mathscr{R}_{CB}$, the magnetizing inductances are ideally $L_A = L_B = N_p^2/(2\mathscr{R}_{CC} + \mathscr{R}_{CA})$. If an identical gap length is used across all three core legs[2], and assuming the cross-sectional area of the center-post is twice that of the outer legs, then $\mathscr{R}_{CA} = 2\mathscr{R}_{CC}$ and

$$L_A = L_B = \frac{N_p^2}{4\mathscr{R}_{CC}}. \tag{1}$$

The complete port relationships of the transformer in this mode are derived in Appendix B–Part A.

B. FB/HB Mode

In FB/HB mode, one of the rectifiers (e.g. rectifier A) is driven as a full-bridge while the other rectifier (e.g. B) is driven as a half-bridge. The current flows in this operating mode can be described by Fig. 3a where, in general, $\hat{i}_G$ is a real current that may flow due to asymmetry in the rectifiers. However, since $\hat{i}_G$ is still associated with current flow in the ground plane, we may still model its MMF contribution by a transference element. Assuming the ideal case where the ground plane resistance is negligible, we arrive at the same magnetic circuit model as in Fig. 3d and therefore derive the same electrical model as shown in Fig. 4.

[2]We focus on the case where a fixed gap is placed across all three core legs because this configuration is used in the experimental prototype. Alternate gap configurations may be used and can be understood through a similar procedure to that presented in Appendix B.

A distinct feature of FB/HB mode is that the rectifiers impose different voltages onto the half-turns. For example, consider operating both rectifiers with square-wave modulation where rectifier A operates in a FB manner while rectifier B operates in a HB manner. In this case, $V_A = 2V_B$ in Fig. 4. Thus, the left-side core leg associated with rectifier A in Fig. 2a must process twice the flux of the right-side core leg associated with rectifier B. This flux constraint imposed by the rectifiers yields a new set of inductances L_A and L_B in the circuit model of Fig. 4. In the example case where $\mathscr{R}_{CA} = \mathscr{R}_{CB} = 2\mathscr{R}_{CC}$, the inductances in the FB/HB mode are

$$L_A = \frac{2}{7}\frac{N_p^2}{\mathscr{R}_{CC}} \tag{2}$$

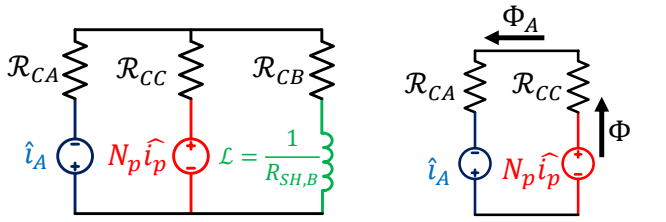
and

$$L_B = \frac{1}{5}\frac{N_p^2}{\mathscr{R}_{CC}}. \tag{3}$$

Where L_A and L_B are $8/7$ and $4/5$ times the symmetric mode value of (1), respectively. The complete port relationships of the transformer in this mode are derived in Appendix B–Part B.

C. FB/0 and HB/0 Modes

In the FB/0 or HB/0 modes one of the rectifiers (e.g. rectifier A) is active and operating in a full-bridge or half-bridge manner, respectively, while the other rectifier (e.g. B) is bypassed. The current flows in this operating mode can be described by Fig. 3a, where the current components outside of the core are again no longer virtual since current is expected to return outside of the core. As before we assume negligible ground plane resistance and arrive at the model of Fig. 3d. However, a key difference between this mode and the others is that the MMF associated with $\hat{i}_B$ is now defined by a small induced voltage due to the small resistance $R_{SH,B}$ comprising the on-state resistance of the bypassed switches and the resistances of the half-turn and ground plane. Thus, this MMF can be modeled by a transferance element as in Fig. 5a. In the limit where $R_{SH,B} \to 0$, flux is rejected from the part of the core associated with the bypassed winding and we can further simplify the model as shown in Fig. 5b. Finally, we arrive at the electrical circuit model in Fig. 6. Note that



(a) Model using transference (b) Simplified magnetic circuit model

Fig. 5: VIRT magnetic circuit model in FB/0 or HB/0 mode. (a) The MMF of the winding associated with the bypassed rectifier can be modeled by a transference element, (b) Simplification of the model assuming $R_{SH,B} \to 0$.

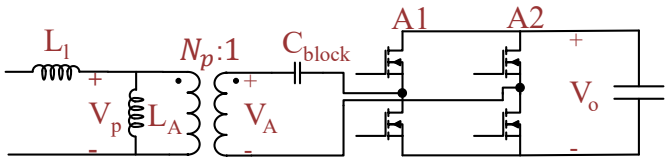


Fig. 6: Simplified electrical circuit model for FB/0 and HB/0 mode with rectifier B bypassed. This model is equivalent to that of Fig. 4 with $L_B = 0$.

this model is equivalent to Fig. 4 with L_B = 0. In the example case where $\mathscr{R}_{CA} = 2\mathscr{R}_{CC}$, the inductance L_A is

$$L_A = \frac{1}{3}\frac{N_p^2}{\mathscr{R}_{CC}}, \tag{4}$$

which is four-thirds of the corresponding value in the symmetric operating modes in (1). The complete port relationships of the transformer in this mode are derived in Appendix B–Part C.

IV. Comparison to a Conventional Transformer

In order to understand the performance gains of the VIRT it is insightful to compare it to the conventional $2N_p$:1 transformer and rectifier structure of Fig. 7. For ease of comparison it is assumed that all rectifier switches can be soft-switched and conduction loss is the dominant source of loss in the switches. This can be achieved, for example, if the transformers are connected as part of an LLC converter. We treat the symmetric rectifier modes, FB/FB and HB/HB, separately from the asymmetric FB/0, HB/0, and FB/HB modes since these asymmetric modes do not have a direct analogue to the conventional configuration.

A. Symmetric Modes (FB/FB and HB/HB)

In the FB/FB and HB/HB modes, the same voltage conversion ratios are achieved as when operating the conventional configuration of Fig. 7 in FB or HB mode, respectively. For example, when operating in FB/FB mode, and assuming square-wave modulation of the rectifiers for simplicity, the voltages V_A and V_B in Fig. 4 are square waves with peak V_o. Reflecting these voltages across the transformer yields $V_o/V_p = 1/(2N_p)$ as expected from the discussion in Section II. When operating

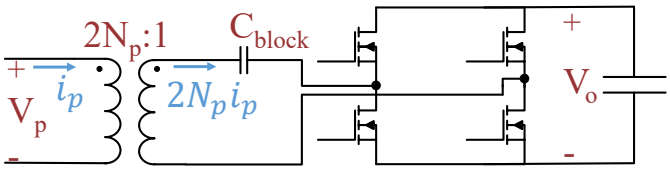


Fig. 7: Conventional $2N_p$:1 transformer connected to a full-bridge rectifier.

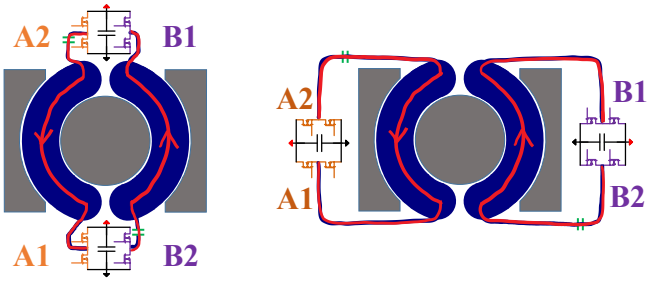
the conventional $2N_p$:1 transformer in full-bridge mode, the same relationship is derived. This equivalence is consistent with the idea of transitioning between a $2N_p$:1 transformer and an N_p:1/2 transformer: the voltage conversion ratio is not changed when the number of primary and secondary turns are scaled by the same multiple.

Although the VIRT requires twice the number of switches than the conventional full-bridge rectifier of Fig. 7, the conventional configuration must employ switches that are rated for twice the current. This is a result of the VIRT rectifiers being effectively paralleled in the FB/FB and HB/HB modes, allowing each of them to process half the current delivered to the output. In the conventional configuration, the full output current must be processed by the single rectifier. The net effect of this is that the transistor conduction loss in both configurations is identical for the same total transistor area. This too aligns with the expectation that the overall current flow across two transformers with the same voltage conversion ratio should not be impacted by the number of turns used to create that conversion ratio.

Viewing the VIRT as an implementation of an N_p:1/2 transformer, the trade-off between copper loss and core loss between it and the conventional configuration is also evident. For the same operating frequency and output voltage V_o, both configurations have the same primary voltage V_p but the $2N_p$:1 transformer in the conventional configuration has $2N_p$ primary turns and thus divides the primary voltage V_p on twice as many turns as the VIRT, reducing the peak flux density in the core and therefore reducing the core loss. Similarly, for the same current i_p in the primary, the $2N_p$:1 transformer has at least twice the dc resistance as the VIRT, and thus experiences increased copper loss.

Note that core loss is fixed between the FB/FB and HB/HB modes if the same primary voltage at the same operating frequency is applied to the VIRT. If the same primary current is applied, copper loss is also fixed. Transitioning between the modes does not inherently change the loss of the transformer unless each mode is operated with different primary voltages, currents, or operating frequencies.

Finally, note that the *schematic* of Fig. 4 is equivalent to a circuit where the two rectifiers are each connected to a single-turn wound around one of the two outer core legs as illustrated in Fig. 8. This configuration is therefore operationally identical to the VIRT with the very important exception that it comprises longer secondary ac conduction path lengths associated with the full turns on the outer legs. Specifically, in the VIRT design of Fig. 8a operated in a symmetric operating mode, the ac currents induced onto the secondary



(a) VIRT structure with example ac current flow path

(b) Operationally equivalent structure that does not exploit the half-turns benefit in terms of ac current flow path length

Fig. 8: Illustration of the reduction of the ac conduction path length in the VIRT compared to an alternate (otherwise equivalent) transformer and rectifier configuration. (a) In the VIRT structure, the induced ac secondary currents must only traverse half turns about the center-post before rectification, (b) In the alternate configuration, the induced currents must always traverse the two half turns *and* the perimeter of the core (forming full turns around the outer core legs) before rectification. This difference in ac path length can represent a substantial difference in conduction loss in low-voltage/high-current applications.

windings only traverse half-turns about the center post before rectification. Conversely, in the alternate configuration of Fig. 8b (and in previous techniques proposed for "fractional" turns) the induced secondary currents traverse complete single-turns around the outer core legs. The proposed VIRT technique can thus be highly advantageous in low-voltage, high-current designs where secondary winding loss is an important design factor.

B. FB/HB Mode

The conventional configuration of Fig. 7 has no counterpart for VIRT operation in FB/HB mode. Thus this mode represents an additional degree of operating freedom over the conventional configuration and we instead compare it to the symmetric VIRT operating modes.

Consider operating in FB/HB mode such that the half-bridges A1, A2, and B1 are switching while B2 is held in the low state. As derived in Section III-B, the circuit model of Fig. 4 is appropriate. Assuming square-wave modulation for simplicity, the voltage conversion ratio is $V_o/V_p = 2/(3N_p)$, representing a gain of $4/3$ over the FB/FB conversion ratio.

Unlike the symmetric operating modes, the rectifiers in FB/HB mode do not always equally share the output current. In cases where the magnetizing current contributions are negligible, however, the currents induced onto each half-turn are approximately equal and the FB rectifier processes (approximately) twice the power of the HB rectifier. Here, two-thirds of the output current is sourced by the FB, and this defines the current rating of each switch in the FB. Similarly, because the HB rectifier processes the same current in its corresponding half-turn, its switches must also be rated for two-thirds of the output current. This represents an increase in the current rating of each rectifier compared to the symmetric modes, which only require each rectifier to be rated for half of the output current. However, this detriment is mitigated if one operates in each mode at the same maximum power. For example a FB/FB rating of 5V/10A, HB/HB rating of 10V/5A, and FB/HB rating of 6.67V/7.5A can all be accommodated by rectifiers with the same current rating (neglecting magnetizing currents). In cases where the magnetizing currents are not negligible, this mode should be evaluated in the context of the surrounding circuits to determine an appropriate current rating for the rectifier switches.

A distinct feature of FB/HB mode is that the core legs process unequal and non-zero flux, and this slightly increases core loss for the same volt-seconds applied to the primary as in the symmetric modes. For example, consider operating in the FB/FB and FB/HB modes with the same primary voltage at the same frequency, with the rectifiers operating with square-wave modulation for simplicity. In FB/FB mode, the primary-generated flux splits evenly between the outer legs and, assuming the outer legs have half the cross-sectional area of the center-post, the flux density in the outer legs is equal to that of the center-post, B_p. In FB/HB mode, the core leg associated with the FB processes two-thirds of the primary-generated flux while the HB core leg processes one-third. Thus, if the center-post processes a flux density of B_p, the FB leg has a flux density of $\frac{4}{3}B_p$ and the HB leg $\frac{2}{3}B_p$. This amounts to increased total core loss compared to the FB/FB case due to the superlinear dependence of core loss on flux density.

C. FB/0 and HB/0 Modes

The final asymmetric operating modes for the VIRT implementation in Fig. 2a are the FB/0 and HB/0 modes, in which one of the rectifiers (e.g. rectifier A) is driven as a full-bridge or half-bridge, respectively, while the other rectifier (e.g. B) is bypassed. In this section we focus on the HB/0 mode as it enables a voltage conversion ratio that is unachievable in the conventional configuration of Fig. 7.

Consider operating in HB/0 mode such that the half-bridges A2, B1, and B2 are held in the low state while A1 remains switching. As derived in Section III-C, the circuit model of Fig. 6 is appropriate. The voltage conversion ratio is $V_o/V_p = 2/N_p$, representing a voltage quadrupling over the FB/FB conversion ratio. However, this additional operating benefit comes at the price of increased core loss. As discussed previously, assuming operation in HB/0 mode with rectifier B zeroed, an ac short-circuit is effectively created around the right-side core leg which theoretically forces all of the flux generated by the primary to be routed through the left-side core leg. This leg will therefore experience up to twice the peak flux density compared to symmetric operation, yielding an increase in core loss due to the superlinear dependence of core loss on flux density.

Note that the additional loss incurred in this mode yields a trade-off between this detriment in loss and the benefit of additional voltage gain, which may have value in a given design. For example, in Section VI-B we find HB/0 mode

operation to be beneficial at high output voltages compared to extending converter gain in HB/HB mode. The other "zero" mode, FB/0, does not offer this same trade-off since it has the same voltage gain as the symmetric HB/HB mode. Operation in FB/0 mode offers no additional functional benefit while incurring the additional losses associated with operation of the zeroed rectifier. Thus, HB/HB mode is preferred over FB/0 mode.

With rectifier B zeroed, the active rectifier (A) must process the full output current. However, current is still induced through the zeroed rectifier (B) which may be comparable to the full output current. Thus, both rectifiers must be rated for the full output current while in the symmetric operating modes they need only be rated for half the output current. As in the FB/HB case, this detriment is mitigated if one operates in each mode at the same maximum power. For example a FB/FB rating of 5V/10A, HB/HB rating of 10V/5A, and HB/0 rating of 20V/2.5A can all be accommodated by rectifiers with the same current rating.

Finally, "shorting" the winding by operating rectifier B in zero mode may change the effective magnetizing inductances of the transformer. For comparison purposes we define a "net" magnetizing inductance[3] $L_M = L_A + L_B$. Consider placing a uniform gap across all three core legs such that $\mathscr{R}_{CA} = \mathscr{R}_{CB} = 2\mathscr{R}_{CC}$. In the FB/0 or HB/0 modes, $L_M = \frac{N_p^2}{3\mathscr{R}_{CC}}$ while in the symmetric modes $L_M = \frac{N_p^2}{2\mathscr{R}_{CC}}$. This suggests a reduction in magnetizing inductance seen across the primary windings of the transformer (by two-thirds) when transitioning from a symmetric mode to either the FB/0 or HB/0 mode. This change may be a useful feature in some resonant topologies, such as an LLC, where it can provide a mechanism for changing the voltage gain curve for a fixed load [21]. Note that if this change is undesirable, it can be avoided by only placing a gap in the center-post. If this gap dominates the reluctances of the core then the "net" magnetizing inductance is theoretically unaffected by the transition to HB/0 mode.

V. Experimental Design

An experimental prototype of the VIRT architecture has been developed that supports a wide range of operating conditions as shown in Table II. The input voltage range is 120-380 V_{dc}, corresponding to the peak rectified voltages of the "universal-input" ac voltage range. The output voltage is between 5V and 20V at up to 36W and/or 5A output. This range is typical of grid-interface power supplies for USB-PD chargers. The demanding step-down ratio and wide-range of these operating points make them well-suited for application of the VIRT structure. Additionally, these points are pedagogically valuable as they represent the general case where the desired output voltages cannot be achieved by simple voltage scaling. In this case, because the output voltages

[3]In the symmetric operating modes, L_A and L_B identically load the VIRT rectifiers. Thus, these two inductances can be equivalently modeled by a single magnetizing inductance L_M in parallel with V_p in Fig. 4, providing physical meaning to the "net" magnetizing inductance term in these modes. In the HB/0 mode, L_M is directly defined by the magnetizing inductance of the transformer in Fig. 6.

TABLE II: Wide range operating points used in experimental prototype

Parameter	Value
Input voltage range, V_{in}	120–380 Vdc
Adjustable output voltage, V_o (Rated output current, rated output power)	Two ranges: 5–7.2V (5A fixed, 25–36W); 7.2–20V (5–1.8A, 36W fixed)

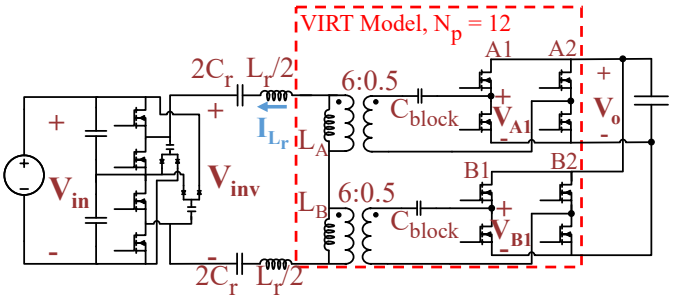


Fig. 9: Stacked-bridge LLC converter interfaced with a VIRT, used in experimental prototype.

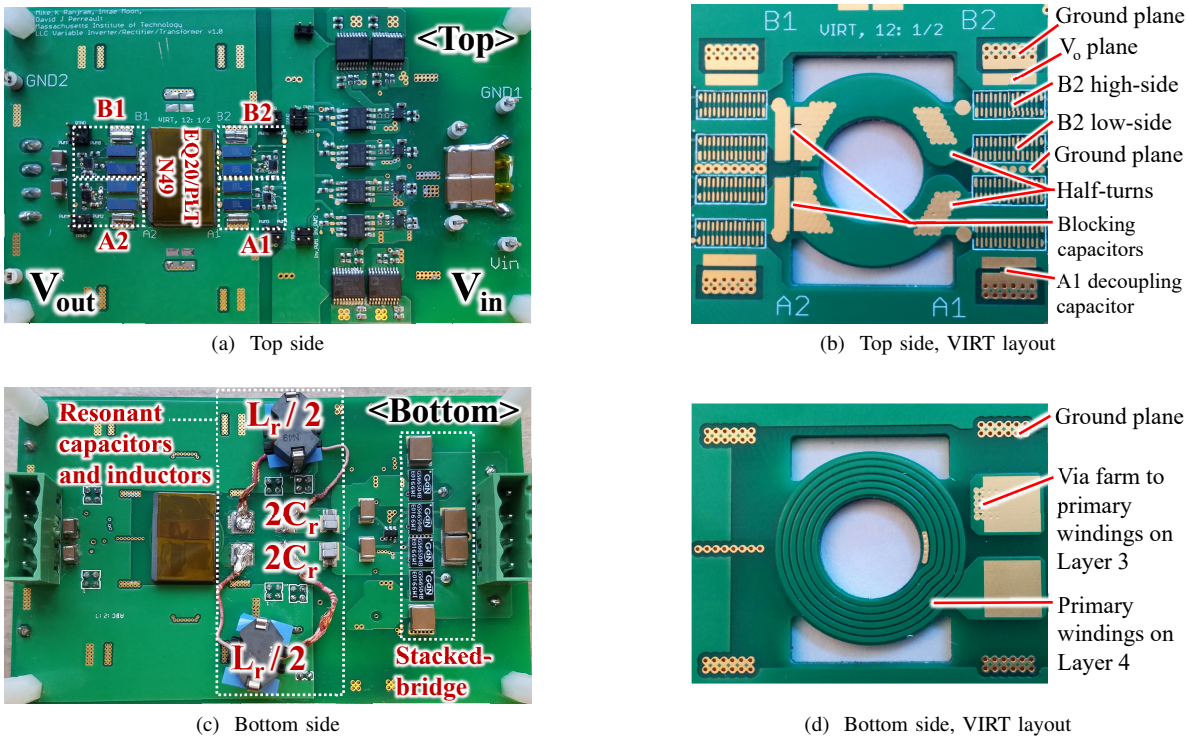
in the example specification comprise a range rather than fixed integer multiples, additional gain variability is required beyond the scaling offered by the VIRT. Similarly, choosing to employ the VIRT architecture only on the rectifier side for simplicity of demonstrating the technique, a means for dealing with the widely varying input voltage is also required. With these requirements in mind we employ a stacked-bridge LLC converter interfaced with a VIRT as shown in Fig. 9. The LLC parameters are listed in Table III and the components used in the experimental prototype are shown in Table IV. A labeled picture of the prototype converter is shown in Fig. 10.

A. VIRT Rectifier Implementation

The VIRT employs two full-bridge rectifiers where each switch is operated as a synchronous rectifier. From a design perspective, the VIRT provides output voltage compression capability that can be used to reduce the range of dc output voltages that the LLC converter must regulate, making the LLC easier to design for good efficiency across the range of voltages ([22] discusses LLC design as related to voltage range). In this example, we assign dc output voltages of 5–6V to FB/FB mode (no voltage compression), 6–8V to FB/HB mode (compression to 4.5–6V), 8–15V to HB/HB mode (compression to 4–7.5V), and 15–20V to HB/0 mode (compression to 3.75–5V). The assignment of the VIRT modes to the output voltage range is summarized in Table V.

B. VIRT Transformer Implementation

A planar transformer is employed on a two-ounce, four-layer, 0.063", FR4 printed circuit board with an EQ20/PLT+N49 core. A PCB core thickness of 0.025" provides greater than 2.5 kV isolation between primary and secondary [23] and the rectifier switches are placed only on the top layer in order to respect this "vertical" isolation barrier. The secondary is wound as two sets of half-turns (each set



(a) Top side

(b) Top side, VIRT layout

(c) Bottom side

(d) Bottom side, VIRT layout

Fig. 10: Labeled experimental prototype, including close-ups of the VIRT layout. The board dimensions are 115 mm x 70 mm.

TABLE III: LLC parameters

Parameter	Value
Resonant frequency	1.2 MHz
Operating frequency range	0.5 - 1.3 MHz
Number of primary turns (N_p)	12
Maximum transformer step-down ratio	12 : 0.5
Resonant capacitance (C_r)	3.47 nF
Resonant inductance (L_r)	5.1 μH
Magnetizing inductance (L_M)	38 μH

wound on layers 1 and 2 in parallel). The primary is wound as six turns on layers 3 and 4 connected in series, with 0.019" trace width and 0.008" trace-to-trace spacing.

The rectifiers are located symmetrically around the core and are tightly spaced to minimize the excursion of current outside the core, as seen in Fig. 10b. Output voltage and ground planes are routed outside the transformer to provide a low-resistance path for dc current between the half-bridge cells and the output bus connection at the edge of the board.

C. Inverter Implementation

The stacked-bridge inverter can be operated in two modes to achieve voltage-halving or voltage-quartering using the "Variable Frequency Multiplier" (VFX) technique as described in [24] and [25]. The inverter is operated with voltage-halving ("conventional mode") when the input voltage is between 120 and 190 V, and voltage-quartering ("VFX mode") when the input voltage is between 190 and 380 V. The result of this re-configuration is that the ac square-wave input to the LLC resonant tank has a peak voltage range of 47.5–95 V. Note that low-power balancer circuits are employed as shown in Fig. 9 to ensure voltage balancing between the input capacitors splitting the dc bus; this is similar to the balancing approach employed in [26].

D. LLC Design

The voltage gain of the converter can be expressed in a similar manner to that of a classic half-bridge LLC converter,

$$\frac{V_o}{V_{in}} = M_{g,LLC} M_{inv} \frac{N_s}{N_p}, \tag{5}$$

where $M_{g,LLC}$ represents the (variable) voltage gain of the LLC resonant tank, M_{inv} is the gain of the inverter topology, and N_p and N_s are the number of primary and secondary turns, respectively. In the case of a VIRT design, N_s/N_p represents the effective transformer turns ratio which is set by the VIRT operating mode,

$$\frac{N_s}{N_p} = \begin{cases} \frac{1}{2N_p}, & \text{FB/FB mode} \\ \frac{2}{3N_p}, & \text{FB/HB mode} \\ \frac{1}{N_p}, & \text{HB/HB (or FB/0) mode} \\ \frac{2}{N_p}, & \text{HB/0 mode} \end{cases} \tag{6}$$

M_{inv} is also a controllable quantity due to the stacked inverter topology and the ability to operate in VFX mode,

$$M_{inv} = \begin{cases} 1/2, & \text{Inverter Mode 1} \\ 1/4, & \text{Inverter Mode 2 (VFX)} \end{cases} \tag{7}$$

TABLE IV: Components used in prototype

Component	Value
Inverter	
GaN FETs	650V/15A GS66504B
Gate drivers	UCC27611
Signal isolators	SI8610
Isolated power	ADUM5010
Balancer diodes	MMBD3004BRM
Balancer capacitors	2x 1uF/450V
VIRT Rectifiers	
GaN FETs	30V/60A EPC2023
Gate drivers	LM5113
Blocking capacitors	3x 22uF/25V per rectifier
Decoupling capacitors	2x 4.7uF/25V per half-bridge
Output capacitors	4x 10uF/25V
LLC	
Resonant capacitor (split)	4x 3.47 nF; ea. 2x 1500pF/630V/C0G + 470pF/450V/C0G
Resonant inductors (split)	2x 1.79uH; ea. RM5I/N49, 3 turns 46AWG/180 Litz wire, 0.005" gap on all legs
VIRT Transformer	
Core	EQ20+PLT/N49, 0.006" gap on all legs
Primary windings	Six turns on each of Layers 3 and 4 connected in series, 0.019" trace width, 0.008" trace-to-trace spacing
Secondary windings	Two sets of half-turns (one set each on layers 1 and 2) connected in parallel
PCB	2oz, 4 layers, 0.063", FR4, 0.025" separation between layers 2 and 3 for galvanic isolation
Control	
Controller	TMS320F28379D

TABLE V: VIRT operating modes in experimental prototype

Mode	Output voltage range	Compressed voltage range	LLC voltage gain ($M_{g,LLC}$)
FB/FB	5–6 V	5–6 V	1.26–3.03 V/V
FB/HB	6–8 V	4.5–6 V	1.14–3.03 V/V
HB/HB	8–15 V	4–7.5 V	1–3.79 V/V
HB/0	15–20 V	3.75–5 V	0.95–2.53 V/V

Due to the re-configurability of the VIRT and the stacked-bridge, the LLC effectively interfaces a 47.5–95V input applied to the resonant tank to a 3.75–7.5V transformer output, corresponding to a reduction in the required step-down ratios from 6–76 V/V to 6.33–25.3 V/V. This four times gain variation can be reasonably accommodated by the LLC resonant tank, while the original 12.7 times gain variation would yield unacceptably large stress on the components of the LLC converter [22]. Note that previous LLC converters for charger applications in the literature have typically been designed for low input and output voltage variation [27]–[31], or for wide input voltage range and fixed output voltage [24], [32], [33]. In this work, an LLC converter design with both wide input range (enabled by the stacked-bridge inverter [24], [25]) and wide output voltage range (enabled by the VIRT) is achieved.

The LLC is designed using a conventional procedure as described in [22] and the resulting component values are shown in Table III. The LLC gain variation required in each VIRT mode is listed in Table V. The key addition to the LLC design procedure is that one must now consider the gain curve for each output voltage and output power pair separately since they may each provide a separate effective load resistance to the resonant tank, as discussed in Section V-E. As is conventional, the LLC is operated primarily at or below resonance to achieve Zero Voltage Switching (ZVS) on the inverter switches, which operate at high voltage, and Zero Current Switching (ZCS) on the secondary-side synchronous rectifiers, which operate at high current. The selected normalized tank parameters are Q = 0.185 and $L_n = 7.45$ (where Q is associated with full load at an output voltage of 8V in the HB/HB mode), chosen to yield sufficient gain at all of the operating points while also achieving primary-side ZVS.

Note that the resonant inductance is achieved in this case by a combination of the primary-referred leakage inductance of the transformer[4] ($\approx$2.1μH) and an external inductor ($\approx$3.5 μH). This external inductor is implemented in a split manner as two series-connected 1.75 μH inductors in order to ensure that the inverter is symmetrically loaded. Similarly, the resonant capacitor is implemented as two series 6.94 nF capacitors, each directly connecting to an inverter switching node as shown in Fig. 10c.

E. Effective Load Resistance and Magnetizing Inductance for LLC Design

The conventional LLC design procedure requires that the load resistance, R_L, be reflected through the output rectifier and across the transformer to synthesize an effective load resistance in parallel with the primary-referred magnetizing inductance [22]. Although the VIRT employs multiple rectifiers, a similar method can be used as in the conventional configuration to synthesize the effective load resistance. Additionally, because there is no "primary-referred magnetizing inductance" as such in all of the modes of the VIRT electrical model of Fig. 4, we instead utilize the "net" magnetizing inductance (the summation of L_A and L_B) in its place.

In a conventional LLC design with a single full-bridge rectifier connected to the secondary of an N_p:N_s transformer, the load resistance R_L is mapped to the primary-side magnetizing branch as $R_{e,FB} = \frac{8}{\pi^2}\left(\frac{N_p}{N_s}\right)^2 R_L$. In the case of operating the VIRT in FB/FB mode, the same equation applies except that $N_s = 0.5$, yielding, $R_{e,FB/FB} = \frac{32}{\pi^2}(N_p)^2 R_L$. The effective load resistance in most of the remaining cases can be similarly computed, and their values are listed in Table I.

A caveat to this derivation is that FB/HB mode is distinct from the other modes in that the flow of power through each rectifier in this mode is unknown at a given operating point of the LLC due to the magnetizing inductances L_A and L_B being unequal and non-zero. Thus, a value for R_e and a "net" magnetizing inductance cannot be derived a priori. In order to create a tractable FHA model we assume the magnetizing inductances negligibly impact the flow of current into each rectifier and thus that the FB processes two-thirds

[4]Note that the leakage inductance of the VIRT can be controlled in a conventional manner, including changing the spacing between primary and secondary windings or adding low-permeability magnetic shunts to the transformer core [34].

of the output power while the HB processes only one-third (as considered in Section IV-B). In this case, the equivalent resistance in parallel with L_A is $R_{FB} = \frac{12}{\pi^2}(N_p)^2 R_L$ while $R_{HB} = \frac{6}{\pi^2}(N_p)^2 R_L$ is in parallel with L_B in Fig. 4. From this circuit network, an equivalent parallel RL circuit can be synthesized assuming operation at the resonant frequency, and this equivalent magnetizing inductance and resistance can be used in the FHA analysis. Going a step further, R_{FB} and R_{HB} can be summed to create an equivalent net resistance $R_{e,FB/HB} = \frac{18}{\pi^2}(N_p)^2 R_L$ since we have already assumed that the magnetizing inductances do not influence the split of power. Similarly we define L_M as the sum of L_A and L_B in (2) and (3).

VI. Experimental Results

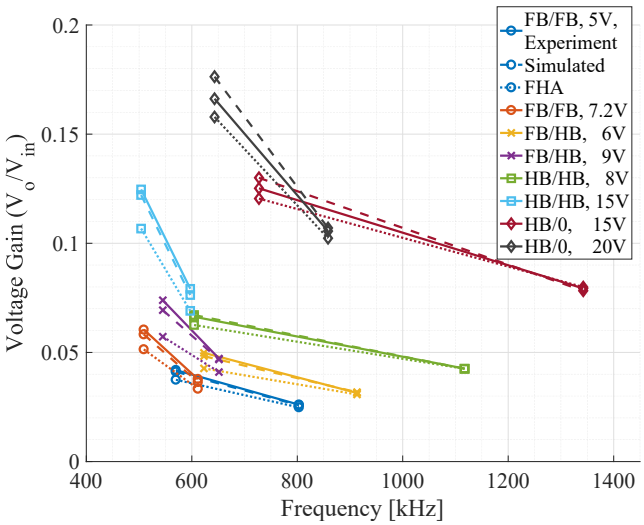
In this section, experimental results are presented to validate the modeling of the VIRT and demonstrate its efficiency benefit.

A. Model Validation

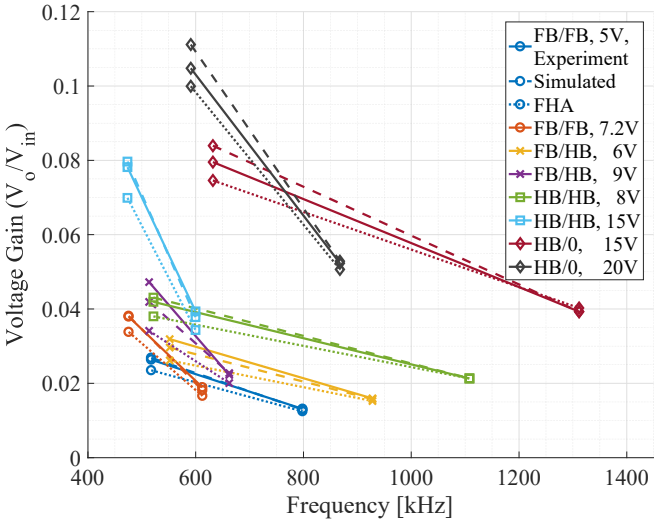
The gain versus operating frequency curves are extracted from the experimental prototype and are compared to an idealized simulation of the circuit in Fig. 9 and a conventional fundamental harmonic approximation (FHA) analysis. The results for Inverter Mode 1 operation ("conventional mode") are shown in Fig. 11a and Inverter Mode 2 ("VFX" mode) in Fig. 11b. The experimental results are in good agreement with simulation: within 5% of the expected gain in the symmetric modes, 6% in HB/0 mode, and 12% in FB/HB mode[5], with these errors decreasing as the converter is operated closer to the resonant frequency of the LLC. This agreement indicates that the circuit in Fig. 4 and the inductances derived in Section III are fair models of the physical system.

Both the experimental and simulated results yield LLC gains that are larger than the results of the FHA analysis, as is expected for operation below resonance [22]. However, FHA remains an effective first-pass design tool for this LLC converter and the use of VIRT does not further compromise its use[6].

The reconfigurable turns ratios offered by the VIRT are embedded within Fig. 11, roughly seen by the gain separation between the different VIRT modes when operating at similar



(a) Inverter Mode 1



(b) Inverter Mode 2

Fig. 11: Voltage gain curves for each inverter mode. Curves are shown for the low and high voltage associated with each VIRT mode, as listed in Table V. All measurements are taken at rated current or power according to Table II. In all cases there is good agreement between the experimental results and the simulated results, validating the modeling of the VIRT.

frequencies. However, these gain curves are also impacted by the differences in the loading of the LLC converter between the various operating conditions. For clarity, we present an example case where the turns-ratio reconfigurability of the VIRT is made explicit. Consider operating the converter with a 190V input in Inverter Mode 1 and 5V output in FB/FB mode with a 1Ω load resistance. We hold the voltage gain of the LLC converter constant between the VIRT modes by scaling the load resistance to keep R_e constant (ref. Table I) and by adjusting the operating frequency, if required. The results of this experiment are shown in Table VI. At a fixed frequency of 802 kHz, we get nearly perfect voltage doubling between the FB/FB and HB/HB modes. This is expected since both modes are modeled by Fig. 4 with identical values of L_A and

[5]The relative increase in FB/HB mode gain error compared to the other VIRT operating modes is an expected result of the modeling approach used. As we operate farther below the resonant frequency, the "square-wave modulation" assumption of the FB/HB model is less accurate and we expect a change in the distribution of flux between the core legs, thus changing the derived port relationships of the transformer. Although we also deviate from "square-wave modulation" operation when in the symmetric modes below resonance, their inherent symmetry imposes equal flux in the outer core legs and therefore the port relationships of the transformer are not altered. Nevertheless, the FB/HB model error is small and the model well captures the operation of the VIRT in this mode.

[6]The largest error in the FHA analysis is associated with the FB/HB mode operated far below resonance, as is expected by the break-down of the square-wave modulation approximation and the simplifying assumptions employed in deriving the FHA parameters in Section V-E. In this design, these largest errors are associated with regions of steepest gain and other design corners, such as HB/HB mode with an 8V output, instead dictate the LLC resonant tank parameters. In another design where FB/HB mode dictates the design of the tank parameters, FHA results should be diligently checked against simulation.

TABLE VI: Impact of VIRT mode shifts for constant LLC gain of 1.26V/V, with 190V input and the inverter operating in Mode 1

VIRT mode	Frequency [kHz]	Load resistance [Ω]	Output voltage	Voltage scaling
FB/FB	802	1	4.95	1
FB/HB	836	1.78	6.64	1.341
HB/HB	802	4	9.88	1.996
HB/0	881	16	20.00	4.04

L_B. We also achieve close to four-thirds scaling in the FB/HB mode, however we must operate at a slightly larger frequency (836 kHz), partly attributable to the reduced "net" magnetizing inductance as listed in Table I. Similarly, voltage-quadrupling is achieved by transitioning to the HB/0 mode, however the operating frequency must again be increased (to 881 kHz) to account for the further reduction of the "net" magnetizing inductance in this mode. These results clearly demonstrate the reconfigurable turns ratios of 12:0.5, 12:2/3, 12:1, and 12:2 that are enabled by the VIRT.

Finally, it is insightful to compare the time-domain waveforms corresponding to each VIRT mode in order to further assess the operational similarities and differences between each mode and their models. Fig. 12 shows the inverter voltage (V_{inv}), resonant inductor current (i_{L_r}), and the low-side voltage of half-bridges A1 and B1 (V_{A1} and V_{B1}, respectively) of the converter as labeled in Fig. 9, under constant voltage gain of the LLC associated with the operating points in Table VI. In the symmetric FB/FB operating mode (Fig. 12a) there is good matching between the rectifier waveforms, with only minor differences in the parasitic oscillations that occur during the discontinuous conduction state associated with below-resonance operation of the LLC. This is consistent with the VIRT electrical model of Fig. 4 where V_A and V_B are identical in the symmetric operating modes. In the HB/HB mode case of Fig. 12b we see nearly identical waveform shapes as in the FB/FB case of Fig. 12a, as is expected since both modes are operated with the same LLC voltage gain.

The asymmetry between the rectifiers in the FB/HB and HB/0 modes is also clear in Figs. 12c and 12d, respectively. In the FB/HB mode (ref. Fig. 12c), rectifier A (driven as a FB) operates in the expected manner for below-resonance operation of the LLC, while the voltage waveform of rectifier B (driven as a HB) suggests resonant or above-resonant operation. This asymmetry is attributable to the unequal loading of the rectifiers by the VIRT transformer and these "mixed" voltage waveforms are predicted by simulation of the circuit of Fig. 9 when using the FB/HB mode values of L_A and L_B in (2) and (3), respectively. In HB/0 mode (ref. Fig. 12d), the voltage of the active rectifier (A1) is similar in shape to the symmetric cases while the bypassed rectifier (B1) has only a small resistive voltage drop associated with its on-resistance and the current that is being induced into the "shorted winding" to reject flux from the corresponding core leg. Observe in this case that V_{A1} is twice as large as in the HB/HB case of Fig. 12b, representative of the fact that nearly all of the flux generated by the primary is now being coupled by the winding associated with rectifier A instead of being split between rectifiers A and B.

B. Efficiency Characteristics

The power-stage efficiency of the converter versus output voltage at rated load is shown in Fig. 13. Consider the Inverter Mode 1 results in Fig. 13a. The efficiency benefit of the VIRT mode changes is clear. Within the output voltage range allocated to each VIRT mode, efficiency generally reduces as the output voltage increases, reflecting increased core loss and winding loss at higher voltage gains due to higher flux swings and circulating currents. The voltage compression capability of the VIRT allows a designer to avoid these less efficient operating points, effectively "flattening out" the efficiency variation by keeping the LLC within a tighter region of its voltage-gain curves. The same trend exists in the Inverter Mode 2 results in Fig. 13b, where for a given input voltage there is always an output voltage at which it is sensible to shift VIRT operating modes in order to reduce power-stage losses[7].

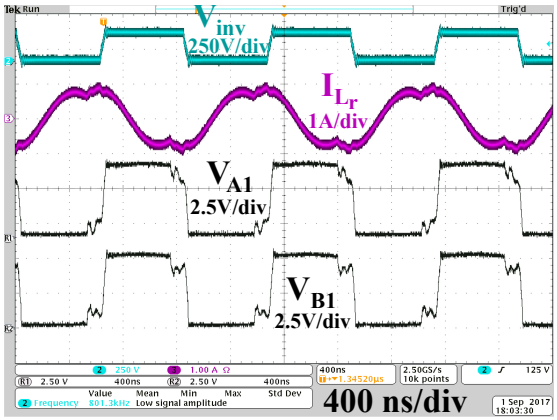
In Inverter Mode 1, efficiency is between 91.6% and 95.9%, while in Inverter Mode 2 the efficiency ranges from 89.5% to 95.5%. The reduction in efficiency in the 380V Inverter Mode 2 cases compared to 190V Inverter Mode 1 is attributable to the mode change of the inverter rather than the operation of the VIRT. For example, the 380V Inverter Mode 2 cases excite the LLC resonant tank in a theoretically identical manner as the 190V Mode 1 cases (i.e. V_{inv} are theoretically identical), and in experiment they are observed to yield nearly identical resonant inductor current and rectifier voltage waveforms, thus suggesting the inverter mode shift as the source of the additional loss.

The variation of efficiency versus input voltage is embedded in the efficiency versus output voltage curves plotted in Fig. 13 since these curves are presented for the boundaries of the input voltage range in each inverter mode. For completeness, an example efficiency versus input voltage curve is provided for each VIRT operating mode in Fig. 14. The benefit of the VIRT is seen here in the "vertical" grouping of the efficiency between these modes even though they operate with different output voltages.

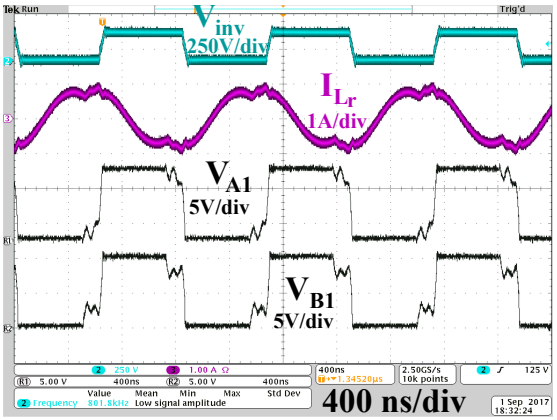
The variation of power-stage efficiency versus output power depends on the design of the LLC and is not directly impacted by the VIRT. Example curves of this type are provided for each VIRT mode in Fig. 15 to demonstrate that an LLC converter interfaced with a VIRT remains capable of achieving reasonable light-load efficiencies.

Finally, we would like to note that the ability to use the "fractional turn" capability of the VIRT was extremely valuable in realizing the proposed design at high performance. Indeed, the authors intended to realize a corresponding "conventional" converter design like that of Fig. 7 with the same transformer core for comparison. However, using a minimum

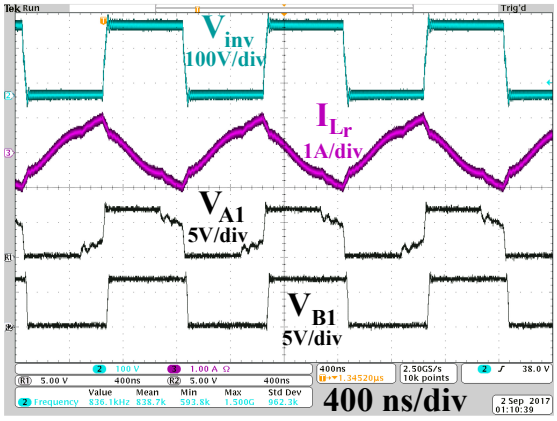
[7]Note that although HB/0 mode is known to suffer additional losses compared to the symmetric modes (ref. Section IV-C), it has demonstrable utility in this example design. This highlights that alternative means of achieving voltage quadrupling may yield worse detriments to efficiency than those experienced in HB/0 mode and that a detailed comparison must be made to correctly assess the value of HB/0 mode in a particular application.



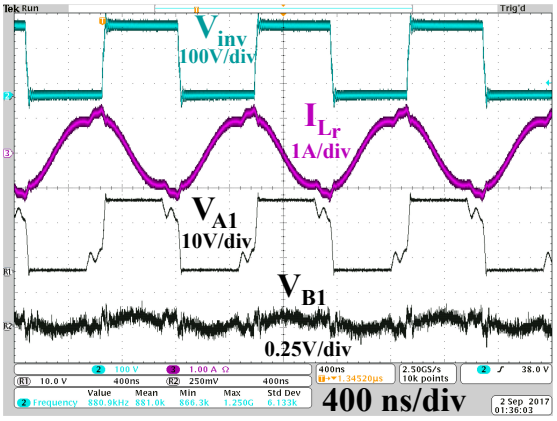
(a) FB/FB mode, 4.95V output, f_{sw} = 802 kHz with R_L = 1Ω (P_{out} = $24.5W$).



(b) HB/HB mode, 9.88V output, f_{sw} = 802 kHz with R_L = 4Ω (P_{out} = $24.4W$).



(c) FB/HB mode, 6.64V output, f_{sw} = 836 kHz with R_L = 1.78Ω (P_{out} = $24.8W$).



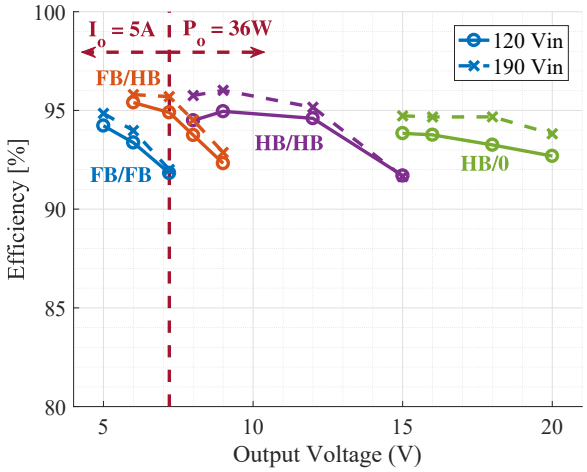
(d) HB/0 mode, 20V output, f_{sw} = 881 kHz with R_L = 16Ω (P_{out} = $25W$).

Fig. 12: Converter operating waveforms in Inverter Mode 1, $V_{in} = 190V$ with a constant LLC voltage gain of 1.26 V/V. The voltages and currents are labeled in Fig. 9.

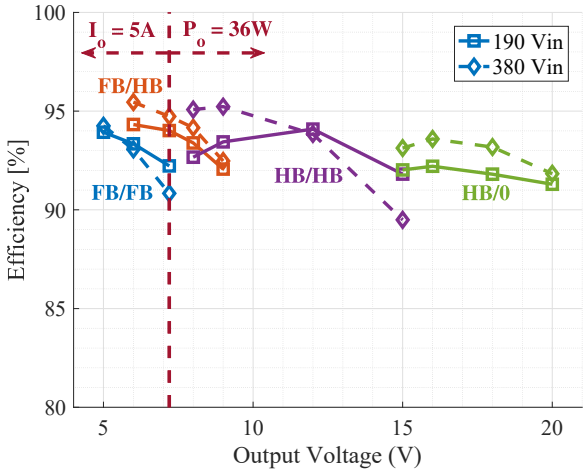
of a single-turn secondary would have required twice the number of primary turns. Unfortunately, the PCB manufacturer was unable to construct such a design, owing to the spacing limitations for the required number of primary turns. It can be concluded that the fractional turns capability of the VIRT architecture has significant implications for both transformer loss minimization and manufacturing of planar magnetics designs.

VII. Conclusion

In this work, a hybrid electronic and magnetic structure capable of fractional and reconfigurable effective turns ratios is presented. The proposed architecture, named VIRT, integrates the rectifier stage of a converter with the magnetic structure of a transformer, providing true "fractional turns" capability for transformer operation and enabling improved reconfigurability for wide operating ranges. Reconfigurability is achieved by controlling the operating modes (i.e. FB, HB, or zero) of the rectifier in conjunction with flux paths and current paths used in the transformer. A magnetic circuit model employing "virtual" currents enables derivation of an electrical circuit model, and an experimental prototype verifies the operation of the structure, demonstrating the achievement of fractional turns and variable conversion ratios. The proposed approach goes beyond previous conceptions of "fractional turns" transformers and provides both reduced loss and conversion reconfigurability. We present an example of the proposed structure utilizing full-bridge rectifiers and half-turn fractional magnetics. Four operating modes are derived and discussed in detail, FB/FB, FB/HB, HB/HB, and HB/0 mode, each offering a distinct effective transformer turns ratio (N_p:0.5, N_p:2/3, N_p:1, and N_p:2, respectively, where N_p is the number of primary turns). The prototype converter utilizes the VIRT interfaced with a stacked-bridge LLC converter to compress a 5–20V output voltage range to 3.75–7.5V, reducing the gain requirement of the LLC and allowing the converter to operate with high efficiency over a wide operating voltage range. The proposed structure is therefore valuable for applications with wide operating voltage ranges that require large and wide-range step-up/down conversion, such as USB wall chargers, and offers strong potential for miniaturization in these applications.



(a) Inverter Mode 1



(b) Inverter Mode 2

Fig. 13: Power-stage efficiency versus output voltage for each inverter mode. Curves for the low and high input voltage associated with each inverter mode, as described in Section V-C, are shown. As the output voltage increases, changing the VIRT mode is advantageous for maintaining high efficiency across the entire range. Note that the demarcation between the fixed rated output current of 5A and fixed rated output power of 36W occurs at V_o = 7.2V as shown.

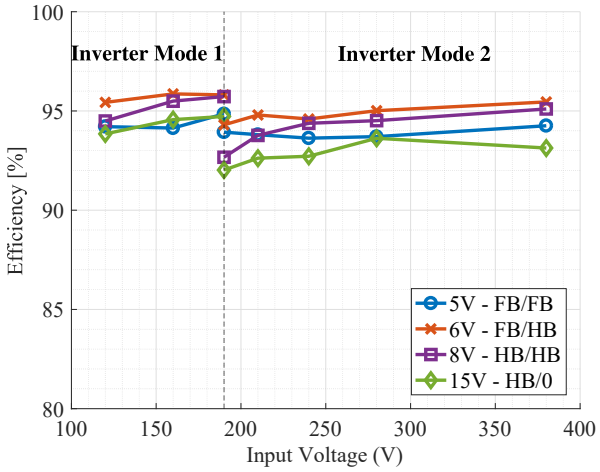


Fig. 14: Power-stage efficiency of the converter measured at full load for example output voltages in each VIRT mode. The efficiencies are well grouped for each inverter mode due to the properties of the VIRT.

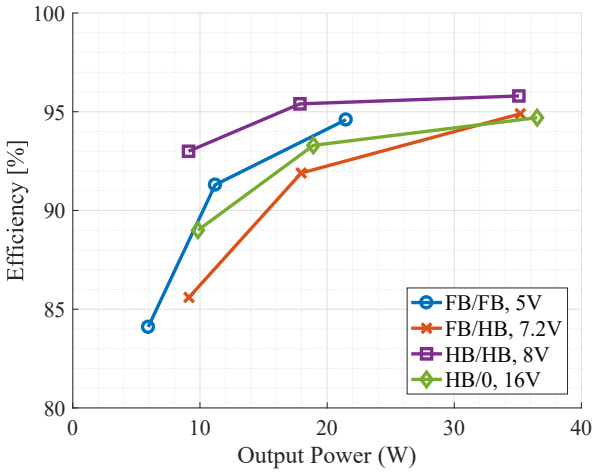


Fig. 15: Power-stage efficiency versus output power for example output voltages associated with each VIRT mode, V_{in} = 190V, Inverter Mode 1. The choice of VIRT operating mode does not directly impact the variation of efficiency with output power. Instead, these trends are primarily influenced by the point of operation on the voltage-gain curve of the LLC. The curves in this plot demonstrate that an LLC design with a VIRT is still capable of achieving reasonable light-load efficiencies.

VIII. Acknowledgements

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Appendix A
Example Implementation of a VIRT with Quarter-Turns

The instance of VIRT in Fig. 2a yields four unique effective turns ratios, including a half-turns ratio of N_p:0.5. Permutations of this fundamental structure can be implemented by changing the number of core sections and/or the rectifier types in order to achieve additional and extended conversion possibilities. For example, one can use full-bridge rectifiers connected through "quarter-turns" around a 5-legged core as illustrated in Fig. 16. When all the rectifiers are active and operating as full-bridges, the effective turns ratio is N_p:0.25. This enables a further trade-off between core loss and copper loss of the transformer compared to the N_p:0.5 turns ratio achievable in the VIRT structure of Fig. 2a, following a similar discussion to that of Section IV-A. This structure can achieve eight effective turns ratios, as listed in Table VII, and the details of each operating mode can be developed and understood using the modeling techniques presented in Section III.

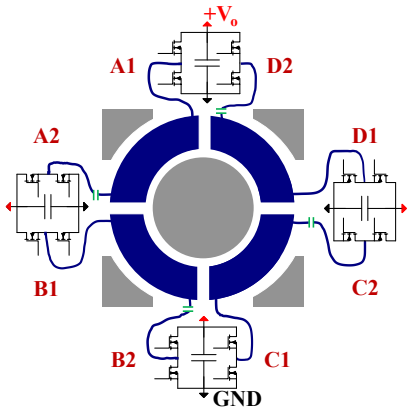

Fig. 16: VIRT implemented with eight half-bridge cells around a 5-legged core and connected with "quarter turns." These cells comprise four full-bridge rectifiers A, B, C, and D arranged as shown. There are N_p primary turns wound around the center-post (not shown). Multiple additional modes are achievable compared to the 3-legged core version presented in Fig. 2a, including "FB/FB/FB/FB" mode, which yields an $N_p : 0.25$ conversion ratio.

TABLE VII: Example effective turns ratios achievable in the 5-legged, quarter-turn VIRT configuration of Fig. 16.

VIRT mode	Effective turns ratio
FB / FB / FB / FB	$N_p : 1/4$
FB / FB / FB / HB	$N_p : 2/7$
FB / FB / HB / HB	$N_p : 1/3$
FB / HB / HB / HB	$N_p : 2/5$
HB / HB / HB / HB	$N_p : 1/2$
HB / HB / HB / 0	$N_p : 2/3$
HB / HB / 0 / 0	$N_p : 1$
HB / 0 / 0 / 0	$N_p : 2$

Appendix B
Derivation of Transformer Port Relationships in the VIRT Modes

In this appendix the full port relationships of the VIRT transformer models are derived. In all cases we first assume a fixed gap length across all three core legs such that

$$\mathscr{R}_{CA} = \mathscr{R}_{CB} = 2\mathscr{R}_{CC}. \tag{8}$$

This is the gap configuration used in the experimental prototype. Following this derivation we also provide the full port relationships for the common configuration where only a center-post gap is employed. In this case we assume

$$\mathscr{R}_{CC} >> \mathscr{R}_{CA} = \mathscr{R}_{CB}. \tag{9}$$

A. Symmetric Modes (FB/FB and HB/HB)

In the symmetric modes, the magnetic circuit model of Fig. 3d is appropriate. Assuming the reluctance relationship in (8) and applying KVL around both loops yields

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - \Phi_A\mathscr{R}_{CA} + \hat{i}_A = 0 \tag{10}$$

and

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - \Phi_B\mathscr{R}_{CB} + \hat{i}_B = 0. \tag{11}$$

Substituting the reluctance relationship defined in (8) into these equations,

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - 2\Phi_A\mathscr{R}_{CC} + \hat{i}_A = 0 \tag{12}$$

and

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - 2\Phi_B\mathscr{R}_{CC} + \hat{i}_B = 0. \tag{13}$$

By Faraday's Law $v_A = \frac{d\Phi_A}{dt}$ and $v_B = \frac{d\Phi_B}{dt}$, where Lenz's law is accounted for by the dot convention of the transformers in Fig. 4. Thus,

$$N_p\frac{d\hat{i}_p}{dt} - \mathscr{R}_{CC}v_B - 3\mathscr{R}_{CC}v_A + \frac{d\hat{i}_A}{dt} = 0 \tag{14}$$

and

$$N_p\frac{d\hat{i}_p}{dt} - \mathscr{R}_{CC}v_A - 3\mathscr{R}_{CC}v_B + \frac{d\hat{i}_B}{dt} = 0. \tag{15}$$

Solving (14) for v_A yields

$$v_A = \frac{N_p}{3\mathscr{R}_{CC}}\frac{d\hat{i}_p}{dt} - \frac{v_B}{3} + \frac{1}{3\mathscr{R}_{CC}}\frac{d\hat{i}_A}{dt}. \tag{16}$$

Voltage v_B is determined by substituting (16) into (15) and simplifying,

$$v_B = \frac{N_p}{4\mathscr{R}_{CC}}\frac{d\hat{i}_p}{dt} - \frac{1}{8\mathscr{R}_{CC}}\frac{d\hat{i}_A}{dt} + \frac{3}{8\mathscr{R}_{CC}}\frac{d\hat{i}_B}{dt}. \tag{17}$$

Thus,

$$v_A = \frac{N_p}{4\mathscr{R}_{CC}}\frac{d\hat{i}_p}{dt} + \frac{3}{8\mathscr{R}_{CC}}\frac{d\hat{i}_A}{dt} - \frac{1}{8\mathscr{R}_{CC}}\frac{d\hat{i}_B}{dt}. \tag{18}$$

By Faraday's law, $v_p = N_p\frac{d}{dt}(\Phi_A + \Phi_B) = N_p(v_A + v_B)$. Thus the transformer port relationships in the FB/FB and HB/HB modes can be expressed in matrix form as

$$\begin{bmatrix} v_P \\ v_A \\ v_B \end{bmatrix} = \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} \frac{N_p^2}{2} & \frac{N_p}{4} & \frac{N_p}{4} \\ \frac{N_p}{4} & \frac{3}{8} & -\frac{1}{8} \\ \frac{N_p}{4} & -\frac{1}{8} & \frac{3}{8} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \\ \hat{i}_B \end{bmatrix}. \tag{19}$$

Note that the currents i_A and i_B defined in Fig. 4 can be expressed as $i_A = -\hat{i}_A$ and $i_B = -\hat{i}_B$. By setting $i_A = i_B = 0$, we extract the inductance values $L_A = N_pL_{21} = \frac{N_p^2}{4\mathscr{R}_{CC}}$ and $L_B = N_pL_{31} = \frac{N_p^2}{4\mathscr{R}_{CC}}$.

1) Center-post gap configuration: Assuming the reluctance relationship in (9) applies, $\hat{i}_A \approx \hat{i}_B$ and by symmetry of the rectifiers $v_A \approx v_B$. Performing KVL around both loops in the magnetic circuit model of Fig. 3d yields

$$N_p\hat{i}_p - 2\Phi_A\mathscr{R}_{CC} + \hat{i}_A \approx 0, \tag{20}$$

and $N_p\hat{i}_p - 2\Phi_B\mathscr{R}_{CC} + \hat{i}_B \approx 0$. From these expressions the port relationships are straightforwardly derived to be

$$\begin{bmatrix} v_P \\ v_A \\ v_B \end{bmatrix} \approx \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} N_p^2 & \frac{N_p}{2} & \frac{N_p}{2} \\ \frac{N_p}{2} & \frac{1}{2} & 0 \\ \frac{N_p}{2} & 0 & \frac{1}{2} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \\ \hat{i}_B \end{bmatrix}. \tag{21}$$

B. FB/HB mode

In FB/HB mode, the magnetic circuit model of Fig. 3d is appropriate. Assuming the reluctance relationship in (8) and applying KVL to the magnetic circuit model,

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - 2\Phi_A\mathscr{R}_{CC} + \hat{i}_A = 0 \tag{22}$$

and

$$N_p\hat{i}_p - (\Phi_A + \Phi_B)\mathscr{R}_{CC} - 2\Phi_B\mathscr{R}_{CC} + \hat{i}_B = 0. \tag{23}$$

Assuming square-wave modulation of the rectifiers, a fixed voltage relationship between v_A and v_B in Fig. 4 is imposed, $v_A = 2v_B$. This implies that the core legs split flux in a fixed ratio, $\Phi_A = \frac{2}{3}\Phi$ and $\Phi_B = \frac{1}{3}\Phi$. Substituting these flux relationships into (22) and simplifying yields an expression for the center-post flux, $\Phi = \frac{3}{7\mathscr{R}_{CC}}\left(N_p\hat{i}_P + \hat{i}_A\right)$. Similarly, from (23), $\Phi = \frac{3}{5\mathscr{R}_{CC}}\left(N_p\hat{i}_P + \hat{i}_B\right)$. By Faraday's law,

$$v_A = \frac{2}{3}\frac{d\Phi}{dt} = \frac{2}{7\mathscr{R}_{CC}}\left(N_p\frac{d\hat{i}_P}{dt} + \frac{d\hat{i}_A}{dt}\right), \tag{24}$$

$$v_B = \frac{1}{3}\frac{d\Phi}{dt} = \frac{1}{5\mathscr{R}_{CC}}\left(N_p\frac{d\hat{i}_P}{dt} + \frac{d\hat{i}_B}{dt}\right), \tag{25}$$

and $v_P = N_p\frac{d\Phi}{dt} = N_p\left(v_A + v_B\right)$. Thus the transformer port relationships can be expressed as

$$\begin{bmatrix} v_P \\ v_A \\ v_B \end{bmatrix} = \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} \frac{17N_p^2}{35} & \frac{2N_p}{7} & \frac{N_p}{5} \\ \frac{2N_p}{7} & \frac{2}{7} & 0 \\ \frac{N_p}{5} & 0 & \frac{1}{5} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \\ \hat{i}_B \end{bmatrix}. \tag{26}$$

By setting $i_A = i_B = 0$, we extract the values for L_A and L_B in Fig. 4, $L_A = \frac{2}{7}\frac{N_p^2}{\mathscr{R}_{CC}}$ and $L_B = \frac{1}{5}\frac{N_p^2}{\mathscr{R}_{CC}}$.

1) Center-post gap configuration: Assuming the reluctance relationship in (9) applies, $\hat{i}_A \approx \hat{i}_B$. Applying KVL to the magnetic circuit model in Fig. 3d, $\hat{i}_a \approx -N_p\hat{i}_p + \Phi\mathscr{R}_{CC}$. Thus, $\Phi \approx \frac{1}{\mathscr{R}_{CC}}\left(N_p\hat{i}_p + \hat{i}_A\right)$. Similarly, $\Phi \approx \frac{1}{\mathscr{R}_{CC}}\left(N_p\hat{i}_p + \hat{i}_B\right)$. Assuming $\Phi_A = \frac{2}{3}\Phi$ and $\Phi_B = \frac{1}{3}\Phi$ is enforced by the rectifiers,

$$v_A = \frac{2}{3}\frac{d\Phi}{dt} \approx \frac{2}{3\mathscr{R}_{CC}}\left(N_p\frac{d\hat{i}_P}{dt} + \frac{d\hat{i}_A}{dt}\right), \tag{27}$$

and

$$v_B = \frac{1}{3}\frac{d\Phi}{dt} \approx \frac{1}{3\mathscr{R}_{CC}}\left(N_p\frac{d\hat{i}_P}{dt} + \frac{d\hat{i}_B}{dt}\right). \tag{28}$$

Thus, the port relationships of the transformer are

$$\begin{bmatrix} v_P \\ v_A \\ v_B \end{bmatrix} \approx \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} N_p^2 & \frac{2N_p}{3} & \frac{N_p}{3} \\ \frac{2N_p}{3} & \frac{2}{3} & 0 \\ \frac{N_p}{3} & 0 & \frac{1}{3} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \\ \hat{i}_B \end{bmatrix}. \tag{29}$$

C. FB/0 and HB/0 Modes

In the FB/0 and HB/0 modes, the magnetic circuit model of Fig. 5b is appropriate. Applying KVL and assuming the reluctance relationship in (8), $N_p\hat{i}_p - 3\mathscr{R}_{CC}\Phi + i_A = 0$. Thus, $\Phi = \frac{1}{3\mathscr{R}_{CC}}(N_p\hat{i}_p + i_A)$. From this flux expression, v_A and v_P are straightforwardly derived by Faraday's Law and the port relationships are

$$\begin{bmatrix} v_P \\ v_A \end{bmatrix} = \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} \frac{N_p^2}{3} & \frac{N_p}{3} \\ \frac{N_p}{3} & \frac{1}{3} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \end{bmatrix}. \tag{30}$$

The inductance L_A is readily identifiable as $L_A = \frac{N_p^2}{3\mathscr{R}_{CC}}$.

1) Center-post gap configuration: Applying KVL to the magnetic circuit model in Fig. 5b and assuming the reluctance relationship in (9) applies, $N_p\hat{i}_p - \mathscr{R}_{CC}\Phi + i_A \approx 0$. Thus, $\Phi \approx \frac{1}{\mathscr{R}_{CC}}(N_p\hat{i}_p + i_A)$. The port relationships can be straightforwardly derived to be

$$\begin{bmatrix} v_P \\ v_A \end{bmatrix} \approx \frac{1}{\mathscr{R}_{CC}}\begin{bmatrix} N_p^2 & N_p \\ N_p & 1 \end{bmatrix}\frac{d}{dt}\begin{bmatrix} \hat{i}_p \\ \hat{i}_A \end{bmatrix}. \tag{31}$$

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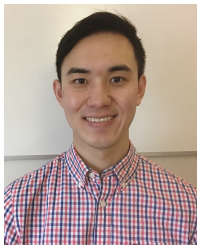

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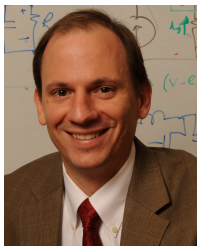

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