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Design and Evaluation of a Reconfigurable Stacked Active Bridge dc/dc Converter for Efficient Wide Load-Range Operation

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***Abstract*— This paper presents the design and implementation of a large-step-down soft-switched dc-dc converter based on the active bridge technique which overcomes some of the limitations of the conventional Dual Active Bridge (DAB) converter. The topology comprises a double stacked-bridge inverter coupled to a reconfigurable rectifier through a special three-winding leakage transformer. This particular combination of stages enables the converter to run in an additional low-power mode that greatly increases light-load efficiency by reducing core loss and extending the zero-voltage switching (ZVS) range. The converter is implemented with a single compact magnetic component, providing power combining, isolation, voltage transformation, and energy transfer inductance. A 175 kHz, 300 W, 380 V to 12 V GaN-based prototype converter achieves 95.9% efficiency at full load, a peak efficiency of 97.0%, an efficiency above 92.7% down to 10% load and an efficiency above 79.8% down to 3.3% load.**

***Index Terms*—dc/dc power conversion, phase control, transformer windings, magnetic cores**

I. Introduction

THERE is a growing need for high-efficiency, large-step-down dc-dc converters as dc loads and distribution systems become more prevalent. Dc-dc converters allow for easier integration with dc systems such as solar panels, micro-grid interfaces, LED lighting, and electric vehicle battery systems [1-3]. In addition, they are also used in dc distribution systems for data centers, where a high voltage (e.g. 380 V) must be converted down to a much lower voltage (e.g. 12 V) to provide power to server racks. These converters must maintain high efficiency across a wide load range, as servers can often remain in low-current or idle states depending on computational demand.

High-voltage (here, hundreds of volts), large conversion-ratio converters required by these applications face several challenges, such as large device switching loss and magnetic core loss. Soft-switching techniques such as zero-voltage switching (ZVS) or zero-current switching (ZCS) are often used to minimize switching losses. However, for many such converters, soft-switching can only be achieved under specific operating conditions, and the converters will lose soft-switching when operating outside of these conditions.

One popular topology for these applications is the Dual Active Bridge (DAB) converter, which consists of two phase-shifted full-bridges connected across a transformer and energy transfer inductance. The DAB is popular due to its ability to operate bi-directionally, its high power density, low component count, soft-switching capability for both input and output bridges, isolation, and high efficiency [4-5]. In addition, it can be operated at a fixed frequency under a simple phase-shift control scheme [4]. The DAB converter achieves very high efficiencies at high power where the converter achieves ZVS. However, core loss stays constant (for a given voltage conversion ratio) as power decreases, and therefore can represent a significant portion of total loss at light-load conditions. In addition, the DAB can lose ZVS at low currents, or when the operating voltage ratio deviates substantially from the ideal transformation ratio, as described in [5]. However, many of the above applications experience large input voltage or load variation, making it difficult to achieve ZVS over all desired operating conditions using the traditional DAB topology.

There has been a significant amount of work done to extend the soft-switching range of the DAB in order to increase efficiency at light-loads, including more complex control schemes, dead-time optimization, variable inductance or frequency techniques, and burst mode control; these are reviewed below.

A. Alternative Control Schemes

Standard phase-shift control can result in high conduction and switching losses when operating away from nominal conditions [6]. There are various waveform shaping control

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methods (e.g., [6-8]) that involve generating three-level transformer voltages with arbitrary duty cycles to reduce reactive power in the transformer and decrease switching loss. These control schemes can also introduce switching states where the inductor current is zero in order to achieve ZCS. However, while ZCS eliminates overlap losses, it does not necessarily eliminate losses associated with the charging and discharging of device output capacitances. Furthermore, these control schemes may not apply to the entire operating range. Finally, many of these control schemes are designed for full-bridge topologies, precluding the use of stacked-bridge architectures which can offer several performance benefits, as described in Section II.

B. Dead-time Control

As described in [9-10], the actual value of the switching dead-times can have a large impact on efficiency, especially at low loads or where the voltage transfer ratio is far from the nominal transformer turns ratio. This is because the dead-time can contribute to the total effective phase-shift, and—at low powers—can dramatically affect the actual output power delivered. Additionally, if the dead-time is longer than the amount of time required to charge or discharge the device output capacitances given the inductor current, the converter can experience additional losses due to body diode conduction or partial hard-switching due to switch drain-to-source resonant ring down. There are several methods to adaptively control the dead-time as a function of output power, (e.g., [9-11]), but these increase control and sensing circuitry complexity.

C. Variable Inductance and Frequency Control

The leakage inductance value also heavily influences the DAB's ZVS capability, as achieving ZVS requires that the stored energy in the leakage inductance at the switching transition be equal to or higher than the stored energy in the output parasitic capacitances of the devices being switched [12]. However, a high leakage inductance can result in a high RMS-to-average current ratio for the converter, resulting in higher conduction losses and lower efficiency at full load. Therefore, work has been done to try to vary the leakage inductance and current as a function of the load to allow the DAB converter to be optimized for high-efficiency at both full- and light-load conditions [12].

Some methods involve physically reconfiguring the leakage inductance, which requires additional control and physical components [12-13], while other methods involve varying the frequency as a function of desired output power. In variable frequency methods, lower frequencies are used at higher powers to reduce the required phase-shift, and therefore RMS currents, while higher frequencies are used at lower powers to increase the required phase-shift and allow the inductor current to ramp up to a high enough value to achieve ZVS [12]. However, this class of approaches makes it harder to optimize the magnetics and filter design [14].

D. Burst-Mode Control

Another method to increase the current at the switch transition in low power operation is burst-mode control. Here, the converter is turned on and off at a burst frequency that is much lower than the converter's switching frequency. Burst-mode control for the DAB converter is explored in [12] and [15]. Using burst-mode control, the converter is operated in its full-load condition during the on-time, so that the leakage inductor current is high enough to achieve ZVS, increasing the efficiency of the converter at light loads. However, transient events when the converter turns on and off can deviate substantially from the ideal operating waveforms. Additionally, at very low powers where the converter is only on for a small percentage of the burst period, these transients can represent a significant portion of the converter on-time, resulting in decreased efficiency.

E. The Proposed Approach

This paper refines and expands upon our earlier conference publication [16], proposing a new converter topology that is optimized for high efficiency at high power as well as under light-load conditions, and as such is especially attractive for the 380 V to 12 V conversion required for data center applications. The topology presented here provides a number of benefits resulting from its stacked inverter design, reconfigurable rectifier, and compact single-core three-winding leakage transformer. These components also allow for operation in a low-power operating mode designed to further increase light-load efficiency. Furthermore, the converter prototypes presented here are all operate at a fixed dead-time and fixed frequency, greatly simplifying the control (though more complex control techniques such as adaptive dead-time, variable-frequency operation, and burst-mode control could be additionally applied to both operating modes if desired, further extending the high-performance operating range).

Section II describes the architecture and proposed control scheme, Section III provides simulated comparisons of the proposed topology and more traditional DAB architectures, and Section IV describes the implementation of several prototype converters and presents experimental results. Finally, Section V summarizes the paper. Analysis of the core loss in the low-power mode is provided in Appendix A, while simulation results for transitions between the full-power and low-power modes are provided in Appendix B.

II. THEORY OF PROPOSED ARCHITECTURE

Fig. 1 shows a conventional single-phase DAB topology [4], which consists of two full-bridges that are phase-shifted from each other across a transformer with some leakage inductance, L. The phase-shift ϕ is used to control the output power, which can be expressed as:

$$P_{out} = \frac{V_p V_s N}{2\pi f_s L} \phi \left(1 - \frac{\phi}{\pi}\right) \quad (1)$$

where V_p is the effective primary voltage, V_s is the effective secondary voltage, N is the transformer turns ratio, f_s is the switching frequency in Hz, L is the primary-referred leakage inductance, and ϕ is the phase-shift in radians.

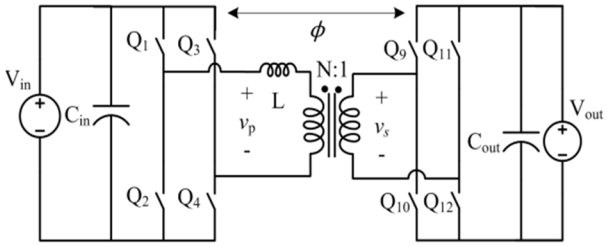


Fig. 1. A DAB converter with a full-bridge input and output. The two bridges are phase-shifted from each other across a transformer and an inductance, *L*.

A limitation of the traditional DAB is that it can lose ZVS in light-load conditions when the current is insufficient to provide the required voltage transitions given the device output capacitance [5]. The proposed topology, referred to here as the Double Stacked Active Bridge (DSAB) converter, addresses this limitation, and can achieve high efficiency over a wide power range because 1) its stacked inverter design allows for the use of lower-voltage rated devices that have lower device capacitance, allowing the converter to achieve ZVS at lower currents, and 2) the converter can operate in a low-power mode which both reduces core loss and gating loss, and further extends the ZVS range.

The DSAB topology is shown in Fig. 2. It comprises a double stacked-bridge inverter coupled to a reconfigurable rectifier via a special three-winding leakage transformer, represented here by the model given in the dashed red box. Each stacked full-bridge inverter feeds into a primary winding. For circuit analysis purposes, the three-winding transformer can be modeled as two transformers whose secondaries are connected in series. However, this model can be physically implemented by a single two-primary, single-secondary magnetic structure, as described later in the paper. The secondary winding then feeds into a reconfigurable rectifier, also described in a later section.

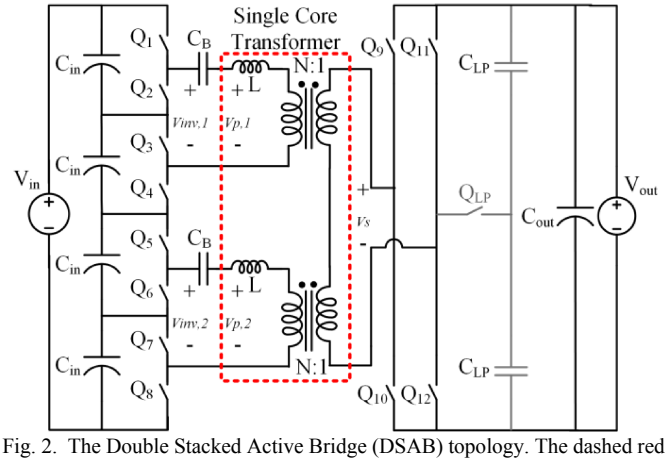


Fig. 2. The Double Stacked Active Bridge (DSAB) topology. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked bridges feeds a primary winding of a single-core, three-winding transformer. A blocking cap, C_B, is used to remove the DC component in the square-wave output of each stacked-bridge. The total primary-referred leakage inductance is modeled as being split between the two primaries (with *L* on each primary). An auxiliary switch, Q_{LP}, in the rectifier allows for a mode switch into a low-power mode.

A. Double Stacked-Bridge Inverter

The converter uses "double stacking" of two stacked full-bridge inverters to achieve efficient high-voltage

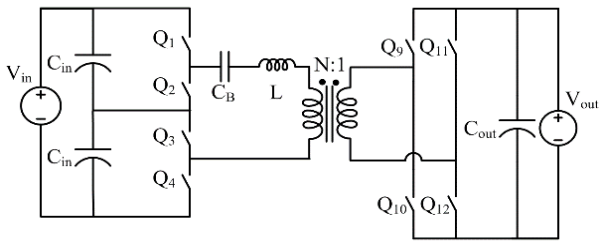


Fig. 3. A DAB converter with a stacked full-bridge on the input and a full-bridge on the output. A blocking cap, C_B, is used to remove the DC component in the square-wave output of the stacked-bridge.

conversion. A double stacked inverter has multiple benefits: 1) it decreases the individual inverter device voltage ratings, improving overall device performance; 2) it decreases the $\frac{1}{2}CV^2$ energy stored in the device capacitance, making ZVS easier to achieve for lower inductor currents; and 3) the two stacked inverters enable additional switching patterns that allow for a low-power mode designed to increase light-load efficiency.

The decrease in inverter device rating can be seen by comparing Figs. 1-3. The devices Q_1-Q_4 in Fig. 1 must be rated for the full input voltage, V_{in}. By comparison, switches Q_1-Q_4 for the single stacked-bridge inverter shown in Fig. 3 are rated for $V_{in}/2$, while switches Q_1-Q_8 for the proposed double-stacked topology in Fig. 2 are only rated for $V_{in}/4$.

Lower-voltage rated devices can demonstrate much better switching performance due to lower parasitic resistance, capacitance, or both. This can be seen by the general increase in the device figure-of-merit $R_{ds,on}C_{oss}$, which is proportional to $BV_{DSS}{}^k$, where BV_{DSS} is the breakdown voltage of the device and k is some exponent, where $k>2$ [17]. As this relationship grows superlinearly, stacking more devices can have lower loss associated with the switches due to the lower (and more favorable) figures-of-merit. Stacked topologies are especially attractive at higher input voltages, such as the 380 V application for which this converter is designed.

The figure-of-merit $R_{ds,on}C_{oss}$ was chosen to characterize the switching performance of the devices in this topology. This figure-of-merit precisely relates to the conduction loss in some high-frequency inverters, such as the classical Class E inverter [18], and represents two main loss mechanisms in the proposed topology's switches: 1) a higher $R_{ds,on}$ results in higher conduction loss, and 2) higher C_{oss} results in more energy stored in the parasitic device output capacitances. For hard-switched conditions, this means more power dissipated to charge and discharge C_{oss} during switch transitions. This loss (or a portion of it) will be present in a ZVS converter if the converter ever loses soft-switching.

In soft-switched applications such as the proposed topology, C_{oss} is charged and discharged inductively (i.e., with some inductance resonating with the output capacitance), so this energy does not contribute to power loss in the switch. However, a higher C_{oss} will require a greater amount of current to complete the necessary voltage transitions on the output capacitance in the given transition time (i.e. dead-time) in order to achieve ZVS, as described in [5]. The minimum leakage inductor current $i_{l,min}$ required to ensure that the voltage transitions are fully completed within the given dead-time can

be written as follows:

$$i_{l,min} = 2C_{oss}\left(\frac{dV_c}{dt}\right) = 2C_{oss}\left(\frac{\frac{V_{in}}{2}}{dt_{sw}}\right) \quad (2)$$

where dV_c is the change in voltage on the switch capacitance and dt_{sw} is the dead-time, which is the maximum time the voltage transition can take while still achieving ZVS. For the DSAB converter, ZVS requires that $dV_c = V_{in}/2$, as each stacked bridge swings from 0 to $V_{in}/2$. This analysis neglects the device turn-off time and assumes that the switch capacitance voltage changes very little during this turn-off time, but illustrates how larger values of C_{oss} require higher minimum currents for a given dead-time to achieve ZVS.

While the dead-time can be lengthened to allow the inductor current a longer time to ramp up to a higher peak value, this increases conduction losses. Additionally, there is still a current level below which no amount of dead-time is sufficient to provide ZVS, as there is not enough energy in the leakage inductance to fully transition the device voltages.

As devices that have very low values of $R_{ds,on}$ typically have higher values of C_{oss} due to the semiconductor construction, minimizing the product of $R_{ds,on}C_{oss}$ is a reasonable metric to use to minimize the overall losses associated with the switches. Because one of the main goals of this work is to demonstrate a topology with high efficiency even at light loads, devices with low $R_{ds,on}C_{oss}$ values were preferentially chosen. Reference [19] gives more detail on the device selection process.

B. Single Magnetic Component

The transformer structure in the DSAB converter is a special three-winding transformer which provides power combining, voltage transformation, isolation, and energy transfer leakage inductance all in a single compact planar PCB magnetic structure. This three-winding, three-core-leg transformer has two primary windings, both of which are coupled to a single secondary winding. This can be physically realized in a single magnetic structure by winding each primary around the outer leg of an E-I core, and winding the secondary around the middle leg, as shown in Fig. 4. The transformer windings have a turns ratio of $N_1{:}N_2{:}N_3 = N{:}N{:}1$, where N_1 and N_2 are the number of turns in the primary windings and N_3 is the number of turns in the secondary winding.

A simplified magnetic circuit model neglecting reluctance paths outside the core is shown in Fig. 5. N_1i_1 through N_3i_3 represent the magnetomotive forces of each winding, while $\mathcal{R}_1$ through $\mathcal{R}_3$ represent the reluctances of the core for each leg (where the horizontal sections of the core have been lumped into the reluctance terms for each leg for simplification). In the limit where the core reluctances are very small, and given $N_1 = N_2 = N$ and $N_3 = 1$, we can write $Ni_1 = Ni_2 = i_3$. Further analysis of this simple magnetic circuit then yields the following idealized voltage relations:

$$\frac{v_1}{N_1} + \frac{v_2}{N_2} + \frac{v_3}{N_3} = \frac{v_p}{N} + \frac{v_p}{N} - \frac{v_s}{1} = 0 \quad (3)$$

where v_1 through v_3 and N_1 through N_3 are defined as in Fig. 5, v_p is the voltage on each primary winding, v_s is the voltage on the secondary winding, and N is the primary-to-secondary turns ratio as shown in Fig. 2. Equation (3) can be rearranged to arrive at the following relationship, which states that the secondary voltage is the sum of the two primary voltages, transformed by the primary-to-secondary turns ratio, $N{:}1$,

$$\frac{2v_p}{N} = v_s \rightarrow \frac{2v_p}{v_s} = N \quad (4)$$

The leakage inductance is realized by the same physical structure, yielding an equivalent circuit model as shown in the dashed red box in Fig. 2. In this model, each primary winding is assigned an identical leakage inductance L. A more complicated model for multi-winding transformers could be used (e.g. see the cantilever model in [20]), but the symmetric topological structure and drive of this transformer make this model adequate for this analysis. The leakage inductance arises from the fact that a substantial portion of each primary winding lies outside the core, resulting in substantial fringing fields in that region. More details on physical implementation of this leakage inductance are provided in Section IV.

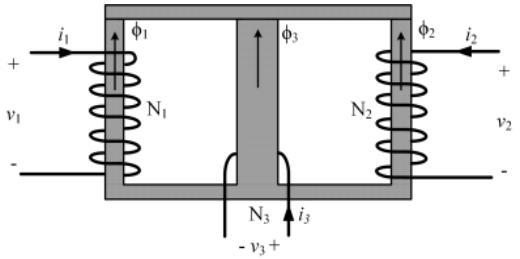


Fig. 4. A winding diagram of the three-winding transformer. The primary windings are wound around the outer legs (windings 1 and 2), while the secondary is wound around the middle leg (winding 3) of an E-I core. In standard operation, let $v_1 = v_2 = v_p$, $v_3 = -v_s$, $N_1 = N_2 = N$, and $N_3 = 1$.

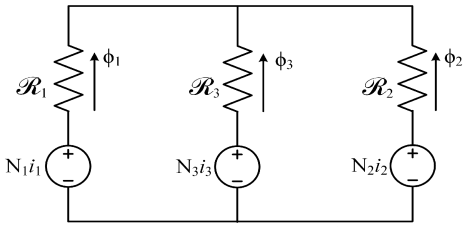


Fig. 5. A magnetic circuit model for the three-winding transformer. N_1i_1, N_2i_2, and N_3i_3 represent the magnetomotive forces of each winding, while $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ represent the reluctances of the core for each leg.

C. Operating Modes

The DSAB converter can be operated in both a full-power mode (normal operation) and a low-power mode designed to decrease switching and core losses. The mode can be changed by adjusting the inverter and rectifier switching patterns and closing or opening an auxiliary switch Q_{LP}, shown in Fig. 2.

1) Full-Power Mode: From (4), it is apparent that the effective primary voltage is the sum of the voltages applied to each primary winding. The effective secondary voltage is that applied by the rectifier. For an input V_{in}, the voltage on each primary, v_p, will be a square wave of amplitude $V_{in}/4$, assuming the two bridges have evenly balanced input voltages. For a full-bridge rectifier, the secondary winding voltage is a square wave of amplitude $v_s = V_{out}$. Therefore, under full-power mode operation with both stacked-bridge inverters operating in square-wave mode and the rectifier operating as a full-bridge rectifier, the output power characteristic is given by:

$$P_{out,FP} = \frac{\left(\frac{V_{in}}{4}+\frac{V_{in}}{4}\right)V_{out}N}{2\pi f_s(2L)}\phi\left(1-\frac{\phi}{\pi}\right) \quad (5)$$

where $2L$ is the total primary-referred leakage inductance of the transformer as shown in Fig. 2, V_{in} is the dc input voltage, V_{out} is the dc output voltage, f_s is the switching frequency in Hz and ϕ is the phase-shift between the inverter and rectifier in radians.

Fig. 6 shows the switching waveforms for the inverter gate drive signals V_{gate1} through V_{gate8} for inverter devices Q_1 through Q_8, and the resulting primary waveforms V_{p1} and V_{p2}. Both primaries are energized with in-phase square-waves of the same amplitude, and these individual primary waveforms are summed to produce an effective primary voltage of amplitude $V_{in}/2$. The dead-time between inverter switches is labeled dt_{inv}, and is required to prevent shoot-through and allow time for ZVS transitions (i.e. for the voltage on the device capacitances to fully transition).

Fig. 7 (a) shows the full-power mode switching waveforms for the rectifier gate drive signals V_{gate9} through V_{gate12} for rectifier devices Q_9 through Q_{12}. The rectifier is driven as a full-bridge, and the auxiliary switch Q_{LP} is held open during full-power mode operation. The rectifier waveforms are shifted from the inverter waveforms by a time t_{shift}, which is related to the phase-shift by the expression $\phi = 2\pi t_{shift} f_s$. The dead-time between rectifier switches is labeled dt_{rect}, and also prevents shoot-through and allows for ZVS transitions.

2) Low-Power Mode: A challenge of the traditional DAB converter is that as the power decreases, so too does the current available to ensure ZVS transitions. The proposed converter can be configured in a low-power mode that increases the current at the switch transitions, by taking advantage of the two-primary magnetic structure in order to energize the primaries in an alternating manner. This operation mode could not be achieved with a single inverter with one primary winding.

The low-power mode is designed to operate naturally at a lower power. Power reduction is achieved by effectively halving the net voltages at the transformer primary and secondary. The inverter is configured to only energize one primary at a time while holding zero voltage on the other primary. To maintain charge balance on the input capacitors as well as to fully utilize the transformer core, the proposed control scheme alternates which primary is energized or shorted (held at zero voltage) every other switching period. However, this alternation could be done on a longer time basis. To maintain the correct voltage transformation ratio across the transformer, the rectifier is reconfigured to operate as a half-bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP}.

Fig. 8 shows the low-power mode switching waveforms for the inverter gate drive signals V_{gate1} through V_{gate8} for inverter devices Q_1 through Q_8. Primary voltage V_{p1} is shown held at zero voltage for the first switching period. This is achieved by holding Q_2 and Q_4 closed while Q_5 through Q_8 are switched in a normal stacked full-bridge fashion. (Note, Q_1 and Q_3 could be held closed instead, which would simply result in a change in polarity of the primary voltage waveforms). To hold zero voltage on the primary voltage V_{p2} during the second switching period, Q_6 and Q_8 are held closed while Q_1 through Q_4 are switched. Since one primary is always held at zero, the total effective primary voltage is now half that of the full-power mode.

Fig. 7 (b) shows the low-power switching waveforms for the rectifier gate drive signals V_{gate9} through V_{gate12} for rectifier devices Q_9 through Q_{12}. The rectifier is configured as a half-bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP} so that the bottom terminal of the secondary winding is now connected to the midpoint of two series-connected capacitors, which are connected across the output such that each holds $V_{out}/2$ across it. The rectifier ac voltage now has an

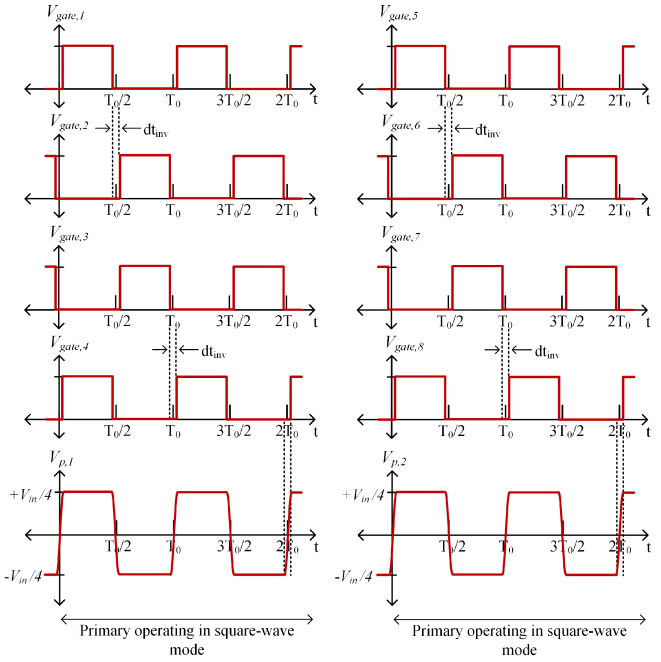


Fig. 6. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the full-power mode.

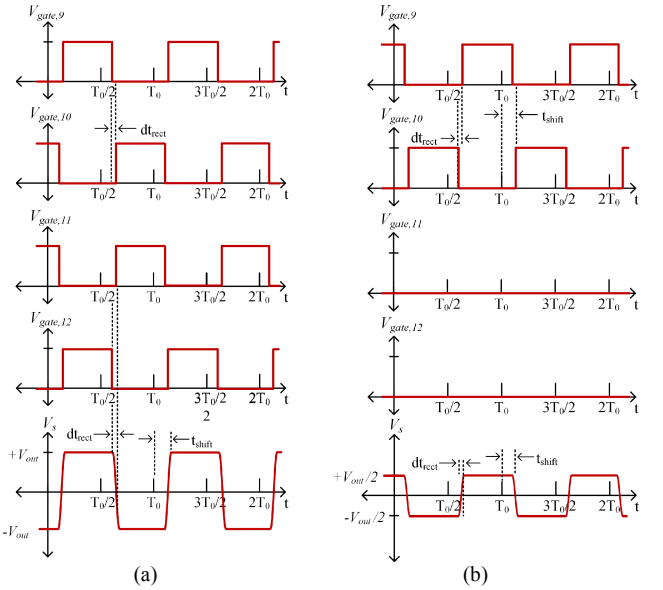


Fig. 7. Switching diagram for the rectifier secondary voltage, while the converter is operating in (a) full-power mode and (b) low-power mode.

amplitude of $V_{out}/2$. The inverter and rectifier voltages are therefore both halved compared to the full-power mode, thereby maintaining the correct voltage transformation ratio across the transformer.

The output power characteristic for the low-power mode can be found by substituting the new values for the effective primary and secondary voltages into (1), and is given by:

$$P_{out,LP} = \frac{\left(\frac{V_{in}}{4}+0\right)\left(\frac{V_{out}}{2}\right)N}{2\pi f_S(2L)}\phi\left(1-\frac{\phi}{\pi}\right) \quad (6)$$

As can be seen from (5) and (6), $P_{out,LP} = 1/4 P_{out,FP}$. For a given phase-shift ϕ, the converter operating in the low-power mode therefore naturally delivers a quarter of the power compared to the full-power mode. Alternatively, this can be viewed as the low-power mode operating at a higher phase-shift compared to the full-power mode for a given output power. This view highlights the ability of the low-power mode to extend the ZVS range by increasing the current available to charge and discharge the device output capacitances during the switch transition, as the inductor current is now given a longer time to ramp up.

a) Core loss in the low-power mode: In the traditional DAB converter topology, core loss remains constant over the entire load range for a given voltage transformation ratio, and therefore accounts for a substantial portion of total loss at low loads. The low-power mode proposed here decreases core loss by only energizing one primary (and exciting only one core leg) at a time. This also results in reduced flux density in the center leg of the core, due to the single-primary drive of the low-power mode.

A magnetic circuit model for the transformer operating in the low-power mode is given in Fig. 9. For simplicity, the leakage

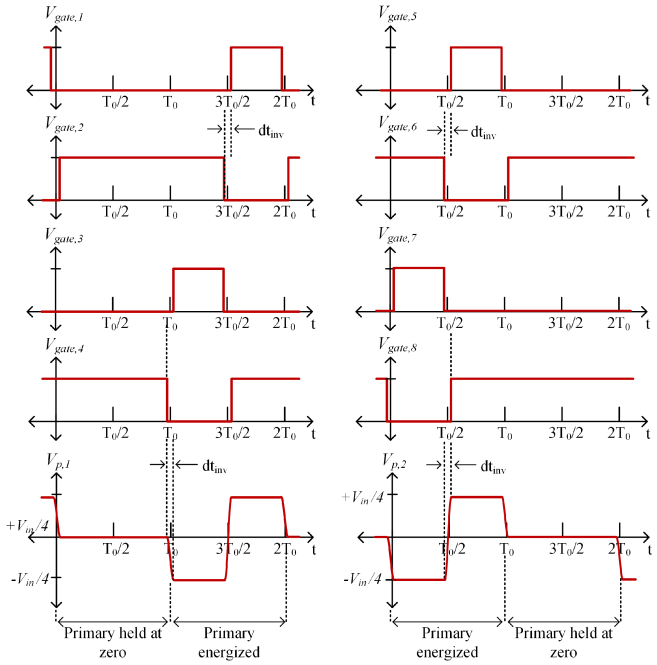


Fig. 8. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the low-power mode.

flux outside the core is ignored. This circuit model represents the case where primary winding 2 is held at zero voltage. The

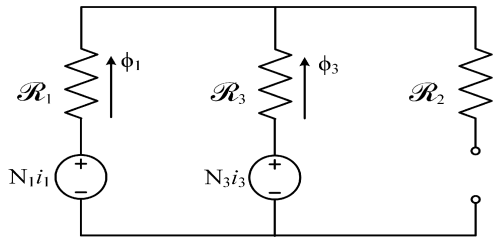
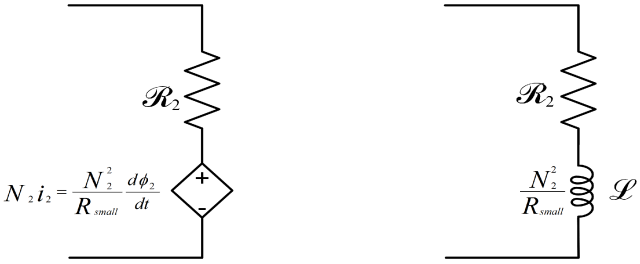


Fig. 9. Simplified magnetic circuit model for the three-winding transformer operating in the low-power mode, for the case when primary winding 2 is held at zero voltage, by connecting an ac short across it. Let $N_1 = N$ and $N_3 = 1$.



(a) dependent source $N_2 i_2$ (b) transference, $\mathscr{L}$

Fig. 10. (a) A model of the shorted winding (here, shown as winding 2), represented as a dependent source that produces a current i_2 to effectively cancel all flux in that leg. Nonidealities such as path resistance are represented by some small resistance R_{small}. (b) Equivalent transference model for the shorted winding, modeling it with some transference, $\mathcal{L} = (N_2)^2/R_{small}$.

total flux through this winding will therefore be zero. The winding will carry whatever current is necessary to keep net flux from flowing through it, which can be modeled in the ideal case by an open circuit in the flux path. The current flowing through the shorted primary is the same current flowing through the energized primary, minus the magnetizing current in the energized primary.

Fig. 10 shows a more detailed model of the open-circuited flux path in . The shorted winding can be modeled as a dependent source that generates the necessary current to cancel the flux flowing through its corresponding core leg, as shown in Fig. 10 (a). The current generated is the observed $N_2 i_2$, such that

$$N_2 i_2 = \frac{N_2^2}{R_{small}}\left(\frac{d\phi_2}{dt}\right) \quad (7)$$

where R_{small} is some small resistance in the flux path. The dependent source can also be modeled by an equivalent transference model [21], where winding 2 has some transference, given by

$$\mathcal{L} = \frac{N_2^2}{R_{small}} \quad (8)$$

For our purposes here, the shorted winding can simply be treated as providing an open-circuit to the flux path. As shown in Appendix A, the low-power mode substantially reduces core loss, owing to elimination of flux in one of the core legs and reduction of flux in the centerpost leg.

b) *Switching loss in the low-power mode:* The low-power mode naturally increases the converter currents for a given output power, thereby extending the range of powers for which ZVS is achieved and increasing efficiency at light-loads. Additionally, as can be seen by comparing Figs. 6 and 8, the low-power mode has fewer switching transitions on the inverter, which can further reduce switching losses at ultra-low

powers where ZVS is not possible. Furthermore, gating losses are reduced because only one inverter stacked full-bridge and one rectifier half-bridge are operated at a time. Because relatively low power is delivered in this mode relative to the conductor area available, conduction losses are also not severe.

D. Transitioning Between Modes

The converter can be started in either the full-power or low-power mode, which allows coarse-level matching of the operating mode to the load conditions. However, it is often desirable to be able to switch modes while the converter is running to account for dynamically changing load conditions. This is especially of importance for data center applications, where the load may change rapidly based on computational demand.

A simple hysteretic control method can be used, so that below a certain power level (ideally, the quarter-power point), the converter will operate in the low-power mode, and above a certain power level the converter will operate in the full-power mode. Ideally, the control will include some hysteresis to prevent the converter from repeatedly changing between modes if the demanded output power oscillates around the threshold power level for the mode switch, i.e. the quarter-power point.

In both modes, the phase-shift between the input and output bridges is decreased to decrease the output power. As the phase-shift decreases, the amplitude of the current through the leakage inductance will correspondingly decrease.

Let us denote the phase-shift for the converter operating in the full-power mode in radians as:

$$\phi_{FP} = \frac{\pi - \sqrt{\pi^2 - \frac{4\pi P_{out}}{x}}}{2} \tag{9}$$

where

$$x = \frac{\left(\frac{V_{in}}{4} + \frac{V_{in}}{4}\right)(V_{out})N}{2\pi f_s(2L)} \tag{10}$$

For a duration equal to $t_{shift} = \phi_{FP}/2\pi f_s$, the inductor current will ramp due to the applied voltage across it, with a slope given by:

$$\frac{\Delta i_{L,FP}}{\Delta t} = \frac{V_{in}}{4L} + \frac{NV_{out}}{2L} \tag{11}$$

In practice, at very low powers where losses become more substantial, the actual phase-shift required to achieve the desired output power can be much higher than the theoretical phase-shift due to dead-time effects and other non-idealities. This can result in a difference between the predicted and actual phase-shifts required for a given power at light-load conditions.

During the low-power mode, the operating phase-shift required for a given power is increased compared to that of the converter operating in the full-power mode, and the amplitude of the current therefore increases as well. The low-power phase-shift in radians can then be expressed as:

$$\phi_{LP} = \frac{\pi - \sqrt{\pi^2 - \frac{4\pi P_{out}}{y}}}{2} \tag{12}$$

where

$$y = \frac{\left(\frac{V_{in}}{4} + 0\right)\left(\frac{V_{out}}{2}\right)N}{2\pi f_s(2L)} \tag{13}$$

During this phase-shift, the inductor current will ramp with a slope of:

$$\frac{\Delta i_{L,LP}}{\Delta t} = \frac{V_{in}}{8L} + \frac{NV_{out}}{4L} \tag{14}$$

We now present a method to use a transitional phase-shift when switching operating modes to provide a smooth transition between the different phase-shifts required for the full-power and low-power modes.

1) Transition from Full-Power to Low-Power Mode: Fig. 11 illustrates what the transformer primary and secondary voltages look like during the transition from full-power mode to low-power mode. The converter is shown initially operating in the full-power mode, with a phase-shift between the primary and secondary voltages calculated according to the full-power mode power characteristic given in (5), and labeled as the time $t_{shift,FP} = \phi_{FP}/2\pi f_s$ in Fig. 11.

The transition from full-power mode to low-power mode is shown starting at $3T_0/2$, where T_0 is equal to the switching period, $1/f_s$. At this point, the primary waveforms immediately switch into the low-power mode configuration, where each primary is alternately energized every other switching cycle. In the case of the secondary, the rectifier also immediately switches from the full-power mode full-bridge rectifier to the low-power mode half-bridge rectifier by closing the auxiliary switch Q_{LP} and opening Q_{11} and Q_{12}. However, during the

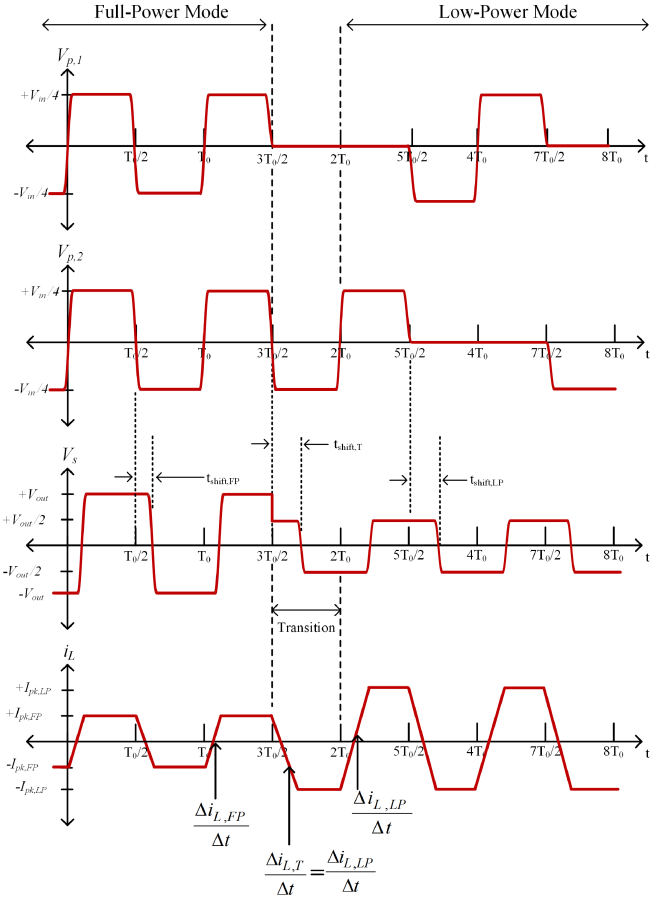


Fig. 11. Converter primary and secondary winding voltages and leakage inductor current, during a mode switch from the full-power mode to the low-power mode. The slopes of the inductor current waveform are labeled.

transition, the secondary waveforms are phase-shifted by a transitionary time, $t_{shift,T}$, which allows the primary inductor current to ramp down from $+I_{pk,FP}$, its full-power mode amplitude, to $-I_{pk,LP}$, its low-power mode amplitude. After this transition time, the secondary waveform operates at the standard low-power phase-shift, corresponding to the time $t_{shift,LP} = ø_{LP}/f_s$ shown in Fig. 11.

Since the primary and secondary voltage waveforms switch to those of the low-power mode (at time $t = 3T_0/2$), the voltage across the inductor during the phase-shift is dependent on the low-power mode primary and secondary voltages. Therefore, the time needed to ramp the inductor current from the full-power amplitude to the low-power amplitude is calculated using the low-power slope of (14).

In full-power mode, the current would require the full phase-shift time, $t_{shift,FP}$, to transition from $+I_{pk,FP}$ to $-I_{pk,FP}$, and only half that to go from $+I_{pk,FP}$ to 0. Because the slope of the inductor current in the low-power mode is half that of the slope of the inductor current in the full-power mode, it will take twice as long for the current to ramp a given amount in the low-power mode. Therefore, when transitioning from the full-power amplitude to the low-power amplitude, the current would require a time $t_{shift,FP}$ to transition from $+I_{pk,FP}$ to 0.

Since the low-power mode requires a time $t_{shift,LP}$ to transition from $+I_{pk,LP}$ to $-I_{pk,LP}$, when transitioning from full-power to low-power, an additional time of $1/2t_{shift,LP}$ is required to complete the transition from 0 to $-I_{pk,LP}$. Combining these, we can denote the total time for the transition from full-power to low-power mode as:

$$t_{shift,T} = t_{shift,FP} + \frac{1}{2}t_{shift,LP} \tag{15}$$

This can be expressed as a transitional phase-shift in radians, given by:

$$\phi_T = \phi_{FP} + \frac{1}{2}\phi_{LP} \tag{16}$$

2) Transition from Low-Power to Full-Power Mode: Fig. 12 illustrates what the transformer primary and secondary voltages look like during the transition from low-power mode to full-power mode. The converter is shown initially operating in the low-power mode, with a phase-shift corresponding to a time $t_{shift,LP} = \phi_{LP}/2\pi f_s$ between the primary and secondary voltages. The transition from full-power mode to low-power mode is shown starting at $2T_0$ in Fig. 12. At this point, the primary waveforms immediately switch into the full-power mode pattern, where both primaries are simultaneously energized. As before, the rectifier also immediately switches modes, now from the low-power mode half-bridge rectifier to the full-bridge rectifier. This is achieved by opening the auxiliary switch Q_{LP} and switching Q_{11} and Q_{12} as in a full-bridge rectifier, along with Q_9 and Q_{10}.

During the transition, the secondary waveforms are phase-shifted by a transitionary time, $t_{shift,T}$, which allows the primary inductor current to ramp down from $+I_{pk,LP}$, its low-power mode amplitude, to $-I_{pk,FP}$, its full-power mode amplitude. After this transition time, the secondary waveform then operates at the standard full-power phase-shift, corresponding to the time $t_{shift,FP} = ø_{FP}/2\pi f_s$, as shown in Fig. 12.

Because the primary and secondary voltage waveforms immediately switch to those of the full-power mode at the transition time (time $t = 2T_0$), the voltage across the inductor for the phase-shift is dependent on the full-power mode primary and secondary voltages (which are each double that of the low-power mode voltages). Therefore the time needed to ramp the inductor from the full-power amplitude to the low-power amplitude is calculated using the full-power slope of (11).

In the full-power mode, the current would require the full phase-shift time, $t_{shift,FP}$, to transition from $+I_{pk,FP}$ to $-I_{pk,FP}$. Since the slope of the full-power mode current is twice that of the low-power mode, it will only take $1/4t_{shift,LP}$ to transition from $+I_{pk,LP}$ to 0, and will then take a further $1/2t_{shift,FP}$ to transition from 0 to $-I_{pk,FP}$. Combining these terms, we can denote the total time for the transition between low-power to full-power mode as:

$$t_{shift,T} = \frac{1}{2}t_{shift,FP} + \frac{1}{4}t_{shift,LP} \tag{17}$$

This can be expressed as a phase-shift in radians, given by:

$$\phi_T = \frac{1}{2}\phi_{FP} + \frac{1}{4}\phi_{LP} \tag{18}$$

Both mode transitions were simulated using LTSpice, and the results are shown in Appendix B. The mode transitions demonstrate rapid settling in each direction across the transition boundary for both continuously adjusted power and for sudden load steps.

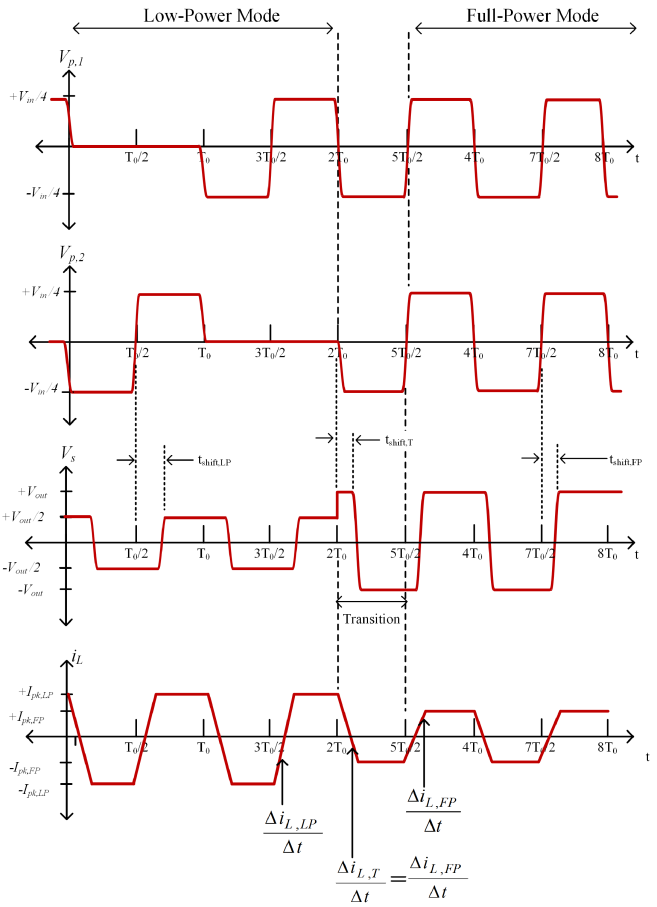


Fig. 12. Converter primary and secondary winding voltages and inductor current, during a mode switch from the low-power mode to the full-power mode. The slopes of the inductor current waveform are labeled.

TABLE I
SELECTED DEVICES FOR SIMULATION

Topology	GaN	Si	Superjunction
DSAB	EPC2012C	FQD10N20L	N/A
Single Stacked DAB	EPC2025*	N/A	IPD50R280CE
Full-Bridge DAB	GS66516T*	N/A	IPD50R280CE*

*Denotes device was only simulated in circuit, not experimentally tested

TABLE II
DEVICE PARAMETERS FOR SPICE MODEL

	Device	$R_{ds,on}$ (mΩ)	C_{oss} (pF)
Inverter	EPC2012C	105	102.5
	FQD10N20L	525	116
	EPC2025	141.75	108.125
	IPD50R280CE	450	72.5
	GS66516T	46.875	134
Rectifier	EPC2023	1.5	1854

III. SIMULATION COMPARISON

Simulations of the DSAB topology, a single-stacked full-bridge DAB topology, and a traditional full-bridge DAB topology were performed using LTSpice, to validate the DSAB's operation and compare its performance to more traditional topologies. The three topologies were simulated with both GaN and Si inverter devices, and the DSAB was simulated in both the full-power and low-power modes. All three topologies were simulated over a wide load range, to assess the ZVS performance and efficiency at light load conditions. Reference [19] gives more information about the specific models and setup used to simulate each converter, and also includes LTSpice netlists and schematics in an appendix. Table I lists the inverter devices used for each simulation, where an asterisk denotes that the device was only used in simulation and not in an experimental prototype. Table II gives the values of $R_{ds,on}$ and C_{oss} used in each simulation to assess efficiency and ZVS performance across output power.

Of these simulations, the GaN and Si DSAB and the Si single-stacked DAB converters were experimentally implemented, and results are given in Section IV.

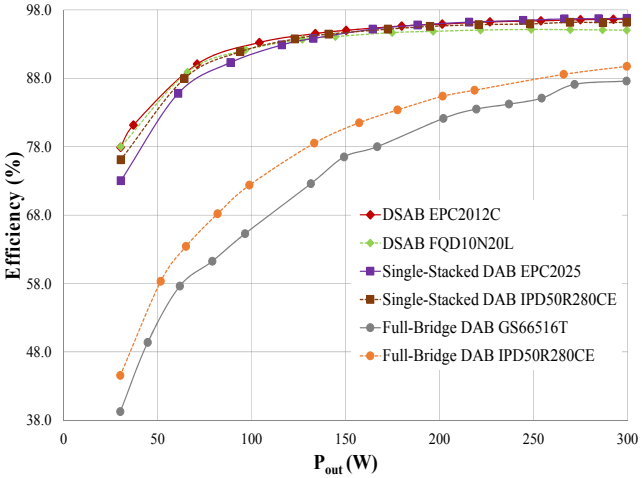


Fig. 13. Simulated efficiency curves for all topologies with all device combinations. The full-bridge DAB converter (shown in orange and gray), has much lower efficiency across the entire power range compared to the stacked topologies. While the single-stacked DAB has similar efficiencies to that of the DSAB at full-power, it becomes much less efficient with decreasing output power, due to losing ZVS earlier than the DSAB converter.

A. Simulated Efficiency Results

Efficiency values over a wide range of output powers were calculated by sweeping the phase-shift for each converter and device combination. Switch dead-times were kept constant over the entire load range for each device type to simplify the simulation process.

Fig. 13 shows efficiency curves for the three different topologies, with each topology simulated with both Si and GaN devices. The full-bridge topology shows significantly lower efficiency compared to both the single-stacked DAB and the DSAB topologies across the entire load range, but especially below 200 W. This is in great part due to the fact that the full-bridge DAB cannot achieve full-ZVS even at full-power and maximum dead-time, due to the large voltage transitions required across the switches (additionally, the high-voltage GaN devices necessary for the full-bridge DAB had higher C_{oss} than any of the other devices). For the stacked full-bridge and DSAB topologies, the dead-time was chosen to be large enough to allow for ZVS at low powers, but less than the maximum dead-time to avoid losses due to body-diode conduction or resonant ring down. Exact parameters are given in [19].

At high powers, the GaN single-stacked DAB and the GaN DSAB topologies have similar efficiencies, as both have similar $R_{ds,on}$ and C_{oss} values. However, at lower powers both the GaN and Si single-stacked DAB topologies start to drop in efficiency compared to the DSAB converters. This is due to the fact that the single-stacked DAB converters lose ZVS more quickly than either of the DSAB converters, even given the relatively low C_{oss} values of the devices used. This showcases a benefit of the DSAB converter topology, as the devices only have to charge and discharge half the voltage on the switches as compared to the single-stacked DAB, and can maintain ZVS down to a much lower power level than the single-stacked DAB.

The low-power mode was also simulated for both the GaN and Si DSAB converters. The low-power mode has a simulated efficiency that is 7-10 percentage points higher than the full-power mode for output powers lower than 50 W. Fig. 14 shows simulated efficiency curves for the both the Si and GaN

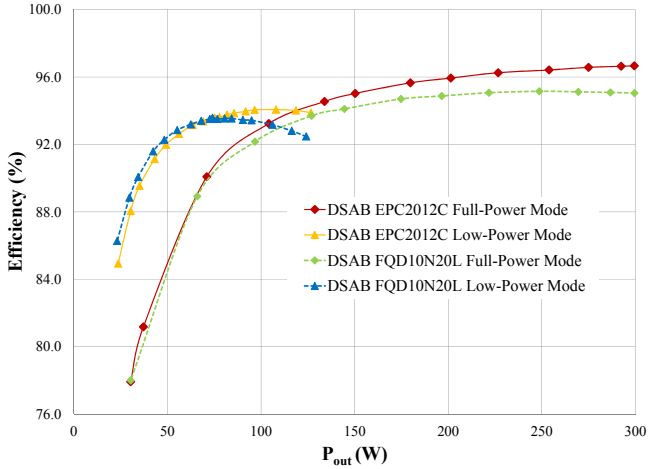


Fig. 14. Simulated efficiency curves for the Si and GaN DSAB converters operating in the full-power and low-power modes.

DSAB converters operating in the full-power and low-power modes. The Si and GaN low-power modes have similar efficiency, as at these low-powers switching loss dominates over conduction loss, so the device C_{oss} has a larger impact on the overall efficiency than the $R_{ds,on}$. The C_{oss} values for the Si and GaN devices were very close, so their ZVS behavior is very similar.

Based on the simulation results, the DSAB converter with GaN EPC2012C inverter devices was predicted to be the most efficient topology overall, and the DSAB's low-power mode showed significant improvement in efficiency at low output powers for both the Si and GaN versions.

IV. Experimental Validation

To illustrate the value of the proposed approach, we present results from multiple converters, all using the same core and PCB windings and designed for a nominal operating point of 380 V input, 12 V output at 300 W and operating at 175 kHz. The three prototypes each have a different inverter stage, to allow for comparisons between device technology as well as between a single-stacked inverter design and a double-stacked inverter design. These variations are: 1) the proposed double-stacked topology with 200 V EPC GaN devices; 2) the proposed double-stacked topology with 200 V Fairchild Si MOSFETs; and 3) a dual-active bridge with a stacked inverter (see Fig. 3), using the same transformer design but with the two primaries connected in series to form one primary winding, and with 550 V Infineon Superjunction Si MOSFETs

The inverter devices were selected on the basis of minimizing the product $R_{ds,on}C_{oss}$ while preferentially selecting devices with low C_{oss} to allow the converter to achieve ZVS at lower powers. 200 V devices were chosen for the double-stacked converter to allow for some headroom on the blocking voltage. 550 V Si Superjunction devices were chosen for the single-stacked topology even though the single-stacked full bridge inverter devices only needed to block (380 V)/2 = 190 V. This was because the Superjunction devices offered a better $R_{ds,on}C_{oss}$ product than the available 250 V – 300 V MOSFETs, and their standard DPAK package allowed the same Si-based DSAB converter PCB to be used, reducing prototyping costs.

The design of each prototype is summarized in Table III, and the top side of the GaN DSAB converter is shown in Fig. 15.

A. Transformer Design

A single core magnetic component was used to implement the three-winding transformer as well as the leakage inductance used to realize the energy transfer inductors; the design realizes the function modeled in Fig 2. The nominal operating point of the DSAB converter was chosen to satisfy the requirements for a 380 V dc bus in data centers with dc distribution, with a 380 V nominal input voltage (with 350 V to 410 V input voltage range) and a constant 12 V output voltage [22]. Using (4) and the values of 380 V and 12 V for the system input and output voltages, the transformer turns ratio was designed for the nominal condition so that:

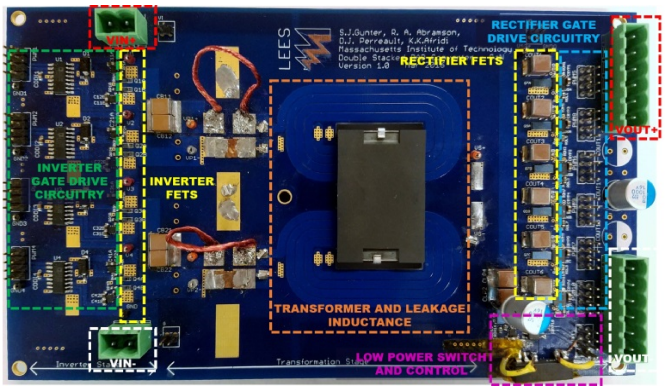


Fig. 15. Top side of the GaN-based DSAB prototype. The inverter and rectifier devices and control circuitry are labeled, as is the single-core magnetic component.

TABLE III
Components for Prototype Converters

Component	Description		Value / Device
Q_1-Q_8	Inverter switch	DSAB GaN	EPC2012C
		DSAB Si	FQD10N20L
		Single-Stacked DAB Si[a]	IPD50R280CE
Q_9-Q_{12}	Rectifier switch	3x EPC2023 30 V/60 A eGaN FETs connected in parallel	
Q_{LP}	Low-power switch	2x EPC2023 30 V/60 A eGaN FET, source connected 2 sets in parallel	
N	Transformer turns ratio	16:1, primary-to-secondary	
L	Leakage inductance	32 µH total primary-referred[b] EPCOS EILP43-N49 core 8-layer PCB, 4 oz copper internal layers, 2oz copper external layers	
C_{in}	Input capacitors	DSAB	3x 3.3 µF 250 V ceramic
		Single-Stacked DAB	4x 2.2 µF 450 V ceramic
C_{out}	Output capacitors	12x 100 µF 16 V ceramic	
C_{LP}	Low-power capacitors	2x 100 µF 16 V ceramic 1x 1000 µF 16 V electrolytic	
C_B	Blocking capacitors	DSAB	2x 3.3 µF 250 V ceramic
		Single-Stacked DAB	2x 2.2 µF 450 V ceramic
C_{bal}	Balancer capacitors	1 µF 250 V ceramic	
D	Balancer diodes	Diode Array 300 V 225 mA 2 pair series connection	

[a] Single-stacked DAB only requires inverter switches Q_1-Q_4
[b] Value from experimental data, based on both impedance analyzer measurements across one primary with the other windings shorted and experimental power transfer data

$$N = \frac{2v_p}{v_s} = \frac{190\ V}{12\ V} = 15.833 \approx 16 \qquad (19)$$

where 16 was chosen as the closest integer value. The primary-to-secondary turns ratio was then found to be 16:1.

For the reasons summarized in [23], a planar winding design was chosen to implement the three-winding leakage transformer. An 8-layer PCB stack-up was used to allow for interleaving between the primary and secondary windings to reduce ac resistance, as well as to allow for paralleled secondary windings to increase current carrying capability and decrease dc resistance. A simplified representation of the PCB stack-up is shown in Fig. 16. The primary windings are shown in red (primary winding #1) and light blue (primary winding

#2) and wrap around the outer legs; the secondary winding is shown in yellow and wraps around the center leg. The primary and secondary windings are interleaved inside the core window, but the primary windings on the outside of the core are not interleaved as there is no secondary winding in that section of PCB. Each primary winding has 16 turns and the secondary consists of only one turn. Each primary has four dedicated PCB layers, and each layer contains four turns.

The four layers are then connected in series to form a total of 16 turns, as required. The secondary winding is also split over four layers. However, because it carries high current and only requires one turn, each trace is made almost as wide as the core window and the four secondary layers are then paralleled to further decrease dc resistance by increasing trace cross-sectional area. To reduce proximity effect and decrease ac resistance, the secondary and primary layers are fully interleaved. 4 oz. copper was used on the six internal PCB layers to mitigate skin effects, while 2 oz. copper was used on the external layers to allow for the required trace spacing and

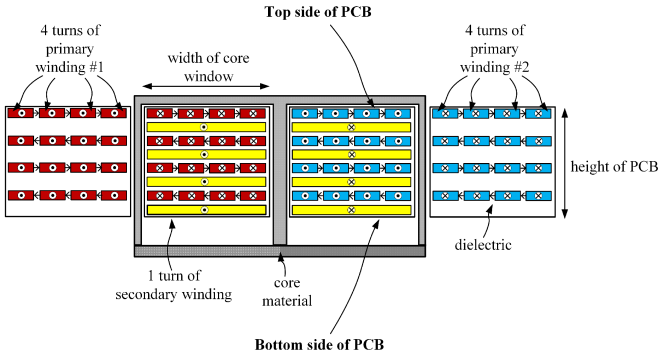


Fig. 16. Cross-section of the magnetic core and PCB layer stack-up for the three-winding transformer. The red and light blue primary windings are interleaved inside the core window with the yellow secondary windings.

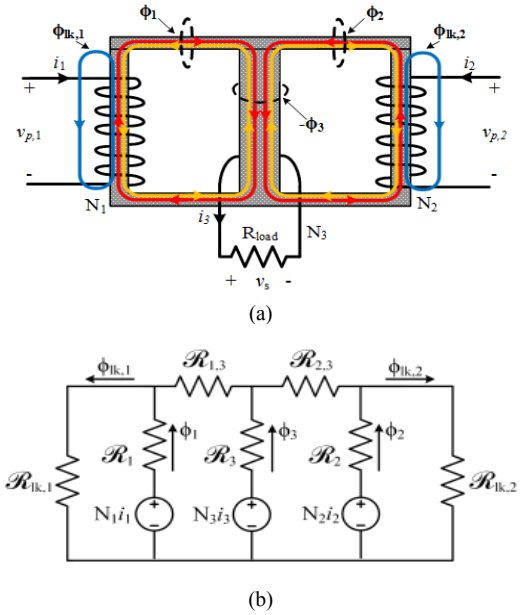


Fig. 17. (a) Diagram of the flux paths of the three-winding transformer. Fluxes ϕ_1 and ϕ_2 in the outer legs link the secondary, and $-\phi_3$ is the flux through the center leg. Fluxes $\phi_{lk,1}$ and $\phi_{lk,2}$ are the primary winding leakage fluxes that do not link to the secondary. (b) The equivalent magnetic circuit model that includes the primary-side leakage paths, as well as the main flux paths through the core legs.

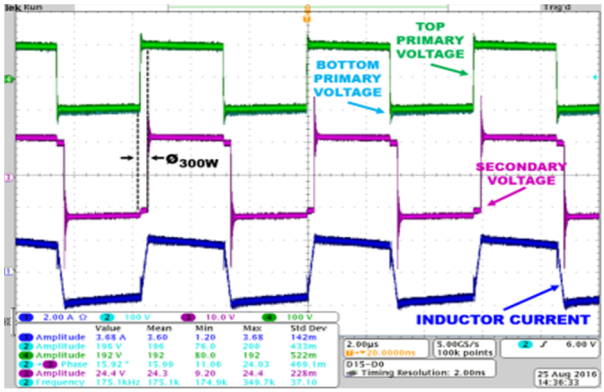


Fig. 18. Operating waveforms for the GaN DSAB converter operating in full-power mode with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 17.2° to deliver 300 W (100% load).

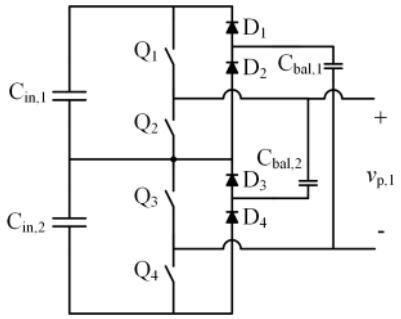


Fig. 19. Balancer circuit used to balance the input capacitors within one stacked full-bridge inverter. $C_{in,1}$ and $C_{in,2}$ are balanced with respect to each other using $C_{bal,1}$ and $C_{bal,2}$. Only the top inverter, connected to $V_{inv,1}$ is shown here; the same circuit is used on the bottom inverter. Values for the balancer components are given in Table III.

width in the footprints of the GaN devices. Further details can be found in [19] and [24].

The leakage inductance is also realized by this structure. A significant portion of the leakage arises due to the sections of primary winding that are outside the core window. These outside sections of winding generate magnetic field lines which do not link to the secondary, increasing leakage inductance. Fig. 17 (a) shows the main flux paths for the transformer, including these leakage paths. Fig. 17 (b) shows the corresponding magnetic circuit model.

The resulting leakage was measured on an impedance analyzer to be approximately 32 µH when referred to the primary side, so that L = 16 µH in Fig. 2. To verify this, the value of the total leakage was also found experimentally by operating the converter and using the power characteristic of (5) to back-solve for L, given all other parameters.

B. Prototype Performance

Wave forms of the GaN-based DSAB converter operating at the nominal operating point of 380 V input and 12 V output at 300 W and running in the full-power mode are shown in Fig. 18. The top and bottom primary voltages can be seen to be right on top of each other, showing good voltage balancing between the inverters without the need for active balancing circuits.

Small passive balancing circuits are used within each individual stacked full-bridge inverter (but not between the two inverters), as illustrated in Fig. 19; these circuits process

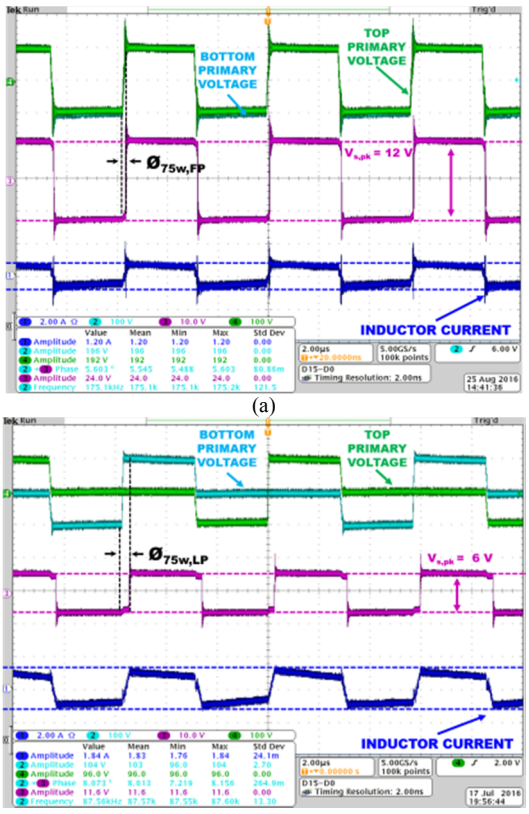


Fig. 20. Operating waveforms for the GaN DSAB converter with an input voltage of 380 V, an output voltage of 12 V, and an output power of 75 W in (a) full-power mode at a phase shift of 8.1° (0.141 rad), and (b) low-power mode at a phase shift of 18.0° (0.314 rad).

negligible power. The current waveform is the desired flat-topped trapezoid.

Operating waveforms are also shown for the converter at one quarter of the rated output power. Fig. 20 shows a comparison of the waveforms for the GaN DSAB converter operating at 75 W (the quarter-power point) in (a) the full-power mode and (b) the low-power mode. As can be seen, the low-power mode results in an increase in the peak inductor current relative to the full-power mode, as $\varnothing_{75W,LP}$ is larger than $\varnothing_{75W,FP}$ (8.1° (0.141 rad) compared to 18.0° (0.314 rad)), so the inductor current is allowed to ramp longer and therefore reaches a higher peak value. This results in the converter achieving ZVS down to a lower output power.

Fi g. 21 shows a comparison of the switch transitions for the GaN DSAB converter in both full-power and low-power mode, by showing the V_{ds} and V_{gs} waveforms for the high-side and low-side devices in one inverter half-bridge. Fig. 21 (a) shows the switch transition for the converter operating in full-power mode at an output power of 75 W. The switches are hard-switched (with only a fraction of device capacitive energy saved), as evidenced by the large ringing on the V_{ds} waveform, and the fact that the V_{ds} voltage does not rise or fall all the way to its final value by the end of the dead-time (the time when both top- and bottom-side V_{gs} signals are zero). Fig. 21 (b) shows the converter operating in the low-power mode, also at 75 W. In the low-power mode, it was observed that the rise and fall transitions on the inverter devices had slightly different

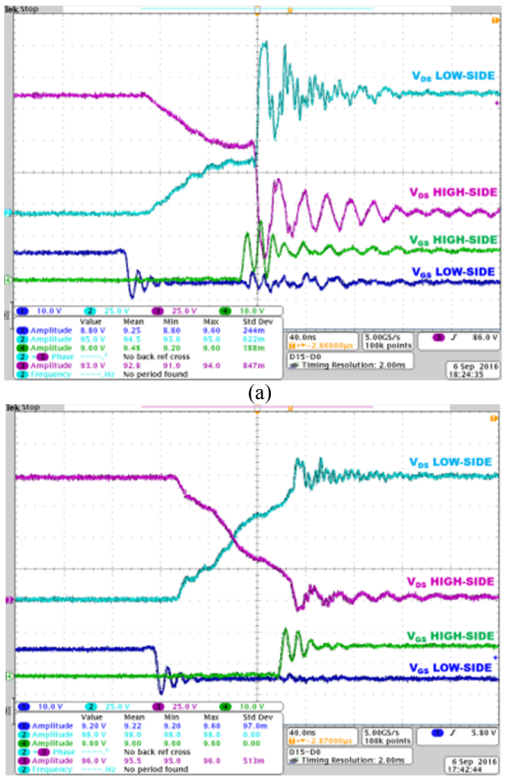


Fig. 21. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating at 75 W in (a) the full-power mode and (b) the low power mode. The low-power mode is able to mostly achieve soft-switching, while the full-power mode experiences substantial hard-switching.

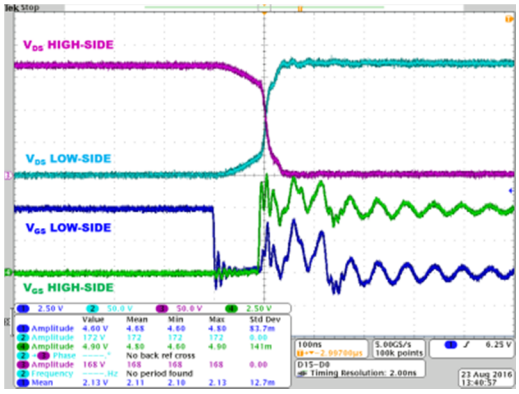


Fig. 22. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the Si single-stacked DAB converter operating with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 14.7° (0.257 rad) to deliver 150 W. The switches are hard-switched for most of the switch transition.

ZVS capability, possibly due to the asymmetry in the primary drive signals.

Fig. 21 (b), we show the transition that achieved the least amount of soft-switching. As can be seen, however, most of the transition is still soft-switched, with only slight ringing on the V_{ds} waveform. The low-power mode was able to maintain ZVS on at least one of the rise and/or fall transitions down to 52 W, while the full-power mode started to lose ZVS around 150 W, showing that the low-power mode was successful at maintaining ZVS down to a much lower power than the full-power mode.

The single-stacked DAB converter's ZVS performance was also investigated, and performed worse than either the

full-power or low-power modes of the GaN DSAB. While the single-stacked DAB was able to achieve ZVS at full-power, by 50% load (150 W), the converter switch transitions were not close to full ZVS, as shown in Fig. 22.

The converter efficiency was tested over a wide input range of 350 V to 410 V to match the standard input voltage variation expected in a data center application. Fig. 23 shows the experimental efficiency of the Si DSAB converter from 350 V to 410 V at an output power of 300 W. The efficiency stays above 94% over the entire voltage range, and increases with increasing voltage, due to the lower RMS currents at the high end of the input voltage range.

Fig. 24 shows the operating waveforms for the Si DSAB converter at (a) 410 V input and (b) 350 V input at an output power of 300 W. At 410 V, the inductor current slopes up because the input voltage is higher than the nominal voltage. At

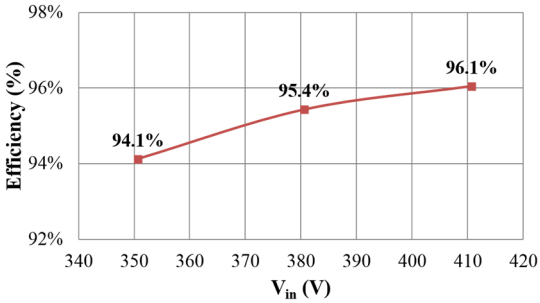


Fig. 23. Experimental efficiency of the Si DSAB converter delivering 300 W over an input voltage range of 350 V to 410 V.

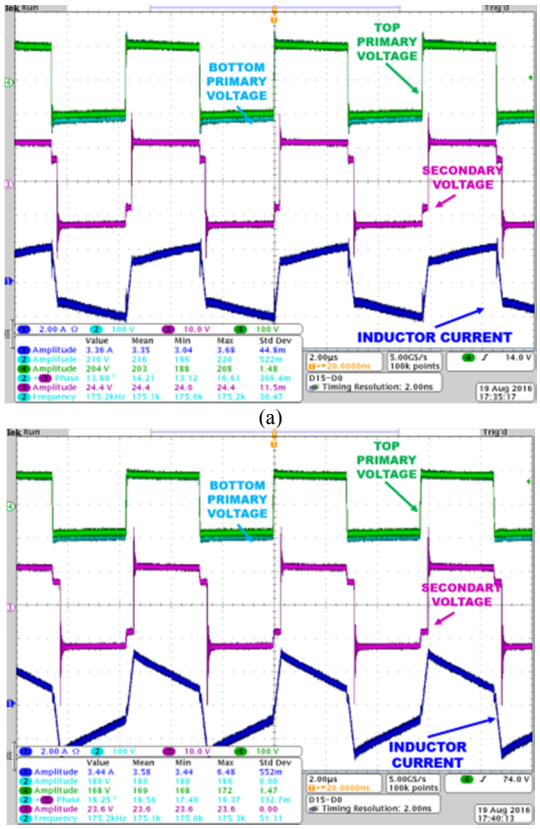


Fig. 24. Si DSAB converter operating waveforms at an input voltage of (a) 410 V and (b) 350 V, both at an output voltage of 12 V and an output power of 300 W.

350 V the inductor current slopes downward as the input voltage is lower than nominal, and has a very steep slope due to the voltage transformation ratio mismatch. Because the current slopes downward, the actual current value at the inverter switch transition has decreased, and as the input voltage is further decreased, the converter will lose ZVS due to the shape of the current waveform, a well-known limitation of the traditional DAB converter. While this converter can still be operated across a reasonably wide input voltage range with high efficiency, the true benefit of the proposed topology and control scheme is seen across a very wide output power range.

Efficiency curves for operation across a wide output power range were obtained for all three topologies mentioned above, as well as for the low-power modes for the double-stacked topologies (the single-stacked converter is not capable of low-power mode operation). As shown in Fig. 25 and Table IV, the three converters' efficiencies are close above 250 W (but favoring the double-stacked (DS) GaN design); however, below this, the efficiencies of the single-stacked (SS) designs drop dramatically compared to the DSAB designs. As shown in Section III, simulations indicated that a traditional full-bridge DAB converter would have even worse efficiency performance [19], [24]. The DSAB converter thus provides significant

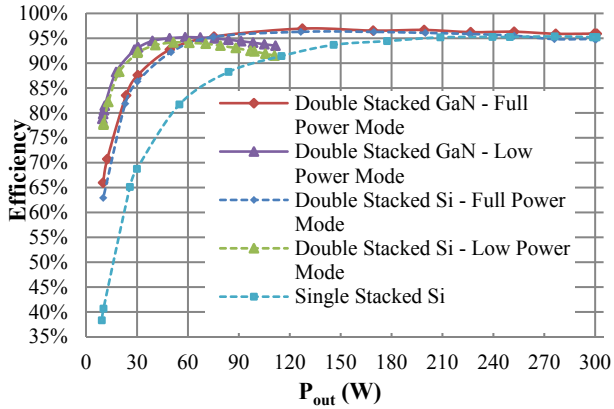


Fig. 25. Experimental efficiency curves across output power for double stacked converters populated with GaN and Si switches operating in full power and low-power modes, as well as a curve for a single stacked converter with Superjunction Si switches.

TABLE IV
EFFICIENCY AT 300 W (100% LOAD)

Topology	P_{out} (W)	Efficiency (%)
DS GaN – full-power mode	299.6	95.9%
DS Si – full-power mode	299.7	94.9%
SS Si	299.1	95.2%

TABLE V
EFFICIENCY AT 10 W (3.3% LOAD)

Topology	P_{out} (W)	Efficiency (%)
DS GaN – full-power mode	9.97	66.0%
DS GaN – low-power mode	10.01	79.8%
DS Si – full-power mode	10.07	62.9%
DS Si – low-power mode	10.19	77.6%
SS Si	10.20	41.4%

efficiency benefit across output power compared to a single-stacked design, even when only used in full-power mode.

Below 20% load, the DSAB's low-power mode significantly improves the efficiency of the converter as compared to the

full-power mode, increasing the efficiency from 66.0% to 79.8% for the GaN DSAB converter, which represents a roughly 40% reduction in loss; see Table V. The GaN-based double-stacked topology has an efficiency of greater than 92.7% down to 10% load. In comparison, the single-stacked topology drops to 69.5% across this range. The double-stacked GaN design in low power mode is 79.8% efficient at 3.3% load, while the single-stacked is only 41.4% efficient, highlighting the proposed topology's ability to achieve high-efficiency operation across a wide power range.

Additionally, the GaN DSAB converter showed better performance compared to the Si DSAB converter at high powers due to its lower $R_{ds,on}$, achieving 0.8-1.2% improvement in efficiency (or equivalently a roughly 20% reduction in loss). Using Si devices, the DSAB converter was able to achieve an efficiency of 94.9% at full load, a peak efficiency of 96.3%, an efficiency above 92.3% down to 10% load, and an efficiency above 77.6% down to 3.3% load. By comparison, the GaN-based DSAB converter was able to achieve an efficiency of 95.9% at full load, a peak efficiency of 97.0%, an efficiency above 92.7% at 10% load, and an efficiency above 79.8% at 3.3% load.

V. Conclusion

This paper has presented the design and implementation of a new converter topology designed to achieve high efficiency under both full-load and light-load conditions. This was done through 1) the use of a double stacked-bridge inverter, which allowed for the use of lower-voltage rated devices that can provide better ZVS performance; 2) a compact single-core three-winding leakage transformer; and 3) a reconfigurable rectifier and alternative switching patterns providing a low-power mode that reduces core loss and extends the ZVS range of the converter. The low-power mode is implemented with an auxiliary switch and a change in inverter and rectifier drive signals, which can be pre-programmed into a controller for easy configuration. The converter is operated with simple phase-shift control and with fixed dead-times for both modes. This paper also presented experimental results from three prototype converters: GaN and Si DSAB converters, as well as a Si Superjunction single-stacked converter. The GaN DSAB topology proved to be the most efficient over the entire load range, and was capable of achieving a peak efficiency of 97.0%, an efficiency greater than 92.7% down to 10% load, and an efficiency greater than 79.8% down to 3.3% load.

Appendix A
Core Loss in the Low-Power Mode

The low-power mode substantially reduces core loss, due to the reduction of flux in the core volume. Using the Steinmetz equation, the core loss for the three-winding transformer can be compared for the full-power and low-power modes. The peak magnetic flux density for each core leg wound with a primary winding can be expressed as:

$$B_{pk1} = \frac{V_{pk}\left(\frac{T}{2}\right)}{N\left(\frac{A_e}{2}\right)} = \frac{\frac{V_{in}}{4}}{N f_s A_e} = B_{pk2} \quad (20)$$

where B_{pk1} and B_{pk2} are the peak magnetic flux densities in the core leg sections for primary windings 1 and 2, V_{pk} is the magnitude of the voltage excitation on the primary, T is the period of the voltage excitation on the primary, N is the number of primary turns, A_e is the area of the core (specifically the core center-post), and f_s is the frequency of the voltage excitation on the primary. The magnitude of the primary voltage waveform can be expressed in terms of the dc input voltage, which is $V_{in}/4$ as described previously. The core area is divided by two in the above expression since each primary is wound around the outer leg of the E-I core, which has half the area of the centerpost for the chosen core.

The power loss in the core while operating in the full-power mode can then be expressed as:

$$P_{core,FP} = K p_{v,sin} \left(\frac{f_s}{f_0}\right)^{\alpha} \left(\left(\frac{B_{pk1}}{B_0}\right)^{\beta} + \left(\frac{B_{pk2}}{B_0}\right)^{\beta}\right)\left(\frac{V_c}{2}\right) \quad (21)$$

where K is a multiplication factor for the specific core shape used; $p_{v,sin}$ is the loss density at a specified temperature, base frequency, f_0, and peak sinusoidal flux density B_0; α is the Steinmetz exponent for frequency; and β is the Steinmetz exponent for flux density for the core material, and V_c is the volume of the core. Core volume is divided by two here because there are two primaries each contributing flux, but their individual fluxes can be imagined as only traveling through half the volume of the core. It is also noted that to use typical Steinmetz loss data, the loss for a triangular flux waveform (as in the double stacked-bridge converter) is being modeled the same as for a sinusoid of the same peak flux value. This is only a rough approximation, but is sufficient for illustrating how loss scales between the full-power and low-power modes.

For the low-power mode, the peak magnetic flux density remains the same, but now only one primary is energized at a time. The amplitude of the primary voltage waveform is the same as that of the full-power mode, but there is also a period where the voltage is zero. If we assume no flux in the outer leg that corresponds to the shorted winding, the center leg will have reduced flux density due to the one-primary drive. An overestimation of the core loss can be found by letting one of the B_{pk} terms go to zero, as shown below:

$$P_{core,LP} = K p_{v,sin} \left(\frac{f_s}{f_0}\right)^{\alpha} \left(\frac{B_{pk1}}{B_0}\right)^{\beta} \left(\frac{V_c}{2}\right) \quad (22)$$

$P_{core,LP}$ is therefore much lower than the core loss in the full-power mode. Note that because the center leg flux is reduced due to only one primary driving flux into it at a time during the low-power mode, the actual core loss will be a little bit lower.

Appendix B
Simulated Mode Transitions

The DSAB converter was simulated during mode switches from 1) the full-power mode to the low-power mode and from 2) the low-power mode to the full-power mode. For simplicity, the simulations were performed only for the GaN DSAB converter. All simulations of the mode transitions used the same dead-times and output capacitance parameters as for the steady-state simulations that evaluated efficiency. This was done to try to get as realistic results as possible.

A. *Transition from Full-Power to Low-Power Mode*

The converter was simulated switching from the full-power mode to the low-power mode under two conditions:

1. While remaining at 75 W in both modes, to demonstrate the ability of the transitional phase-shift to deliver constant power across the mode shift at the quarter-power point.
2. While stepping from 100 W in the full-power mode to 50 W in the low-power to show an exaggerated transient load step, in order to examine the stability of the operating waveforms.

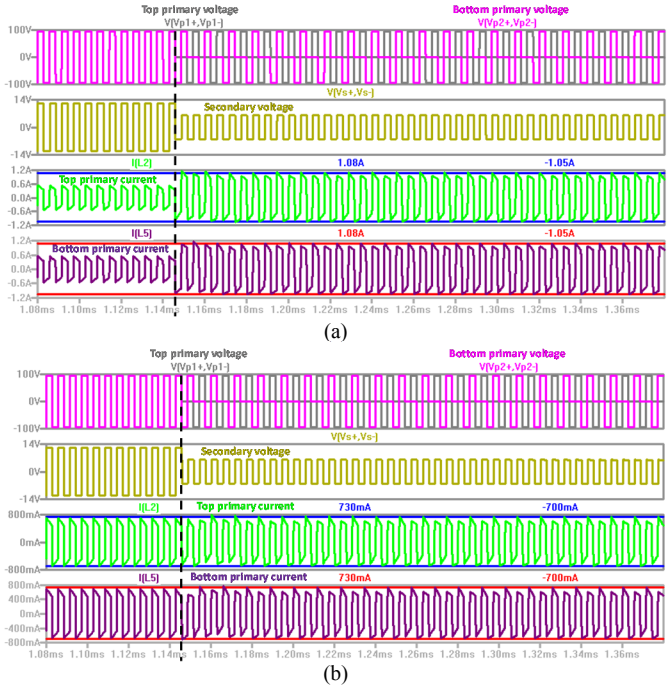


Fig. 26. Simulated operating waveforms for the GaN DSAB converter for (a) a transition from the full-power mode to low-power mode at a constant 75 W, and (b) a transition from the full-power mode to low-power mode for a step in output power from 100 W to 50 W. The blue and red sets of horizontal lines show the steady-state amplitude of the current.

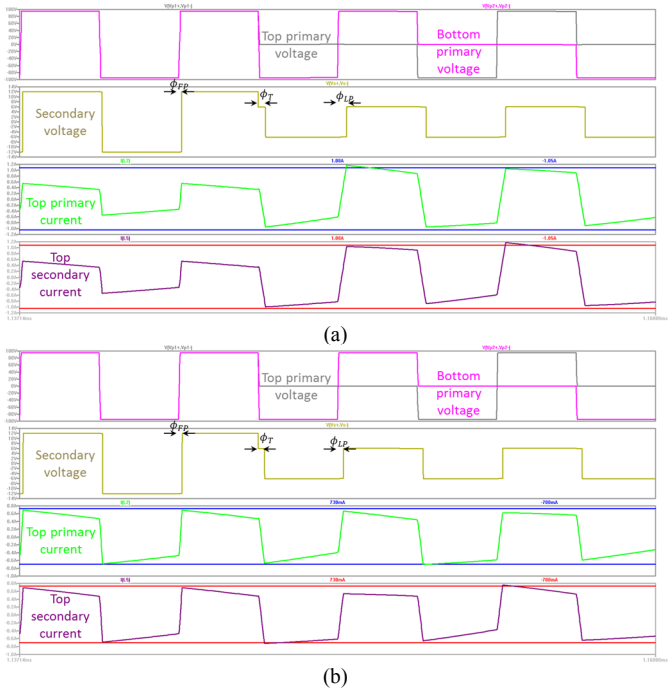


Fig. 27. Zoomed in simulated operating waveforms for the GaN DSAB converter for (a) a transition from low-power to full-power mode, while remaining at 75 W, and (b) a transition from low-power to full-power mode for a step in output power from 100 W to 50 W. The full-power phase-shift ϕ_{FP}, low-power phase-shift ϕ_{LP}, and transition phase-shift ϕ_T, are labeled.

Fig. 26 shows the operating waveforms for the converter (a) switching from full-power to low-power while maintaining a constant 75 W output, and (b) switching from full-power to low-power while stepping from 100 W to 50 W output. The top and bottom primary voltages ($V_{p,1}$ and $V_{p,2}$ in Fig. 2) are shown in the top pane, followed by the secondary voltage (V_s in Fig. 2), and the top and bottom primary currents (the currents through the leakage inductors of value L in Fig. 2). The transition point is marked by the dotted black line, and can also be seen by a change from the in-phase primary waveforms of the full-power mode to the alternately energized primary waveforms of the low-power mode, and by the halving of the transformer secondary voltage. The blue and red horizontal limit lines plotted with the primary currents show the steady-state amplitude after the converter has been operating in the low-power mode after about 1 ms. As can be seen in the figure, the current amplitude only slightly exceeds these limits right after the transition, and quickly settles to the steady-state value in both Fig. 26 (a) and Fig. 26 (b). The primary and secondary voltages show no transients, other than the explicitly defined transitionary step in the secondary voltage.

Of note in Fig. 26 (a) and (b) is that the inductor current has different slopes during the flat-topped portion of the trapezoidal current waveform, with these slopes alternating every switching period. This is due to the fact that during the low-power mode, the same current flows through the top and bottom leakage inductances due to the shorted winding configuration, with the exception that the primary branch that is currently being energized will have an additional current component due to the voltage applied across its magnetizing inductance. Comparing the top and bottom inductor currents, it is evident that the currents have the opposite slope for each switching period, as each primary is alternately energized.

Fig. 27 shows zoomed-in waveforms for the same operating conditions shown in Fig. 26, and more clearly shows the transitionary step down in the secondary voltage due to the change from the full-power full-bridge rectifier mode to the low-power half-bridge rectifier mode at the transition time. The full-power phase-shift ϕ_{FP}, low-power phase-shift ϕ_{LP}, and transition phase-shift ϕ_T, are also labeled.

B. *Transition from Low-Power to Full-Power Mode*

The converter was also simulated for a mode-switch in the opposite direction, from low-power to full-power mode. This was again done under two conditions:

1. While remaining at 75 W in both modes.
2. While stepping from 50 W in the low-power mode to 100 W in the full-power to show an exaggerated transient load step, now with a transition in the opposite direction.

Fig. 28 shows the operating waveforms for the converter switching from low-power to full-power while maintaining a constant 75 W output, and (b) switching from low-power to

full-power while stepping from 50 W to 100 W. The transition point is again marked with a dotted black line, and can also be seen by the change in the primary waveforms and by the doubling of the transformer secondary voltage.

Fig. 28 (a) shows the output power held constant at 75 W

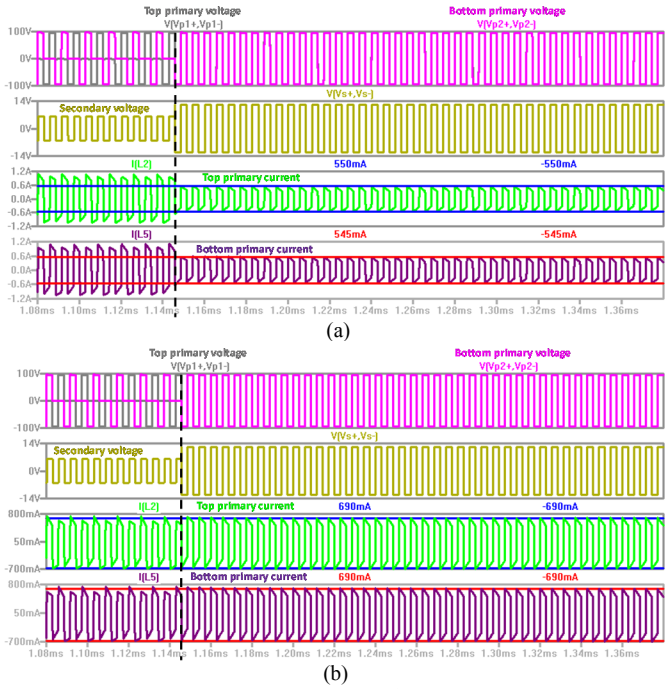


Fig. 28. Simulated operating waveforms for the GaN DSAB converter for (a) a transition from the full-power mode to low-power mode at a constant 75 W, and (b) a transition from the full-power mode to low-power mode for a step in output power from 100 W to 50 W. The blue and red sets of horizontal lines show the steady-state amplitude of the current.

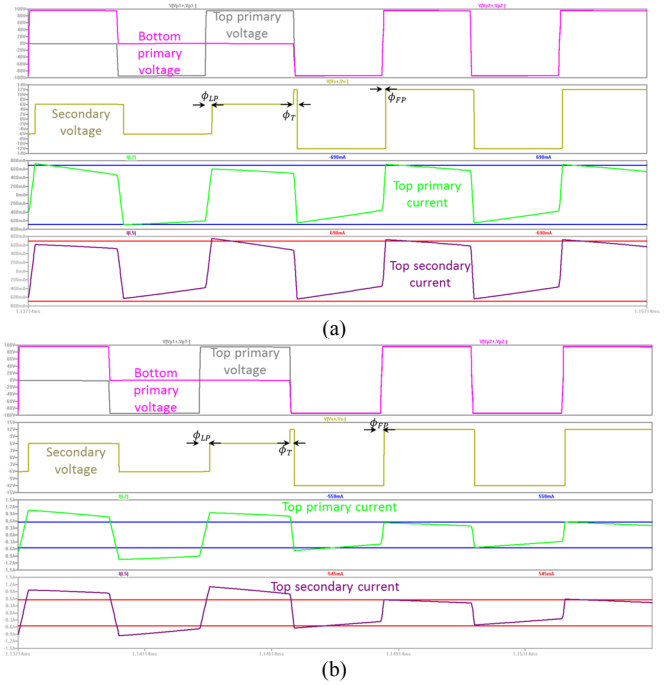


Fig. 29. Zoomed in simulated operating waveforms for the GaN DSAB converter for (a) a transition from the full-power mode to low-power mode, while maintaining the output power at 75 W across the mode-switch, and (b) a transition from the full-power mode to low-power mode for a step in output power from 100 W to 50 W. The full-power phase-shift ϕ_{FP}, low-power phase-shift ϕ_{LP}, and transition phase-shift ϕ_T, are labeled.

TABLE VI
OUTPUT POWER DURING MODE TRANSITIONS

Transition	$P_{out,FP}$ (W)	$P_{out,LP}$ (W)	$P_{out,T}$ (W)
Full-Power to Low-Power	75.2	75.1	74.0
	100.4	49.9	70.1
	$P_{out,LP}$ (W)	$P_{out,LP}$ (W)	$P_{out,T}$ (W)
Low-Power to Full-Power	75.1	75.1	77.5
	49.9	100.4	77.5

while the converter is switched from low-power to full-power. The current decreases as a result of switching to the lower full-power phase-shift, the opposite of the case shown in Fig. 26 (a). The blue and red limit lines again show the steady-state amplitude after the converter has been operating in the full-power mode after about 1 ms. As can be seen in the figure, the current amplitude during the transition very quickly settles to the steady-state value. Fig. 28 (b) shows a load step from 50 W to 100 W. Here, the primary currents exceed the limits by a small amount right after the mode-switch, but again display a very nice step in operating waveforms without significant transients.

Fig. 29 shows zoomed-in waveforms for the same operating conditions as in Fig. 28, and shows the transitionary step up in the secondary voltage due to the switch from the half-bridge rectifier configuration to the full-bridge rectifier configuration. The full-power phase-shift ϕ_{FP}, low-power phase-shift ϕ_{LP}, and transition phase-shift ϕ_T, are again labeled.

Table VI gives the measured values for output power before and after the mode-switch for both the full-power to low-power and low-power to full-power mode transitions. $P_{out,T}$ is the rms output power over four switching periods, centered around the transition point. For the case where the output power remains constant between the full-power and low-power modes, the transition power also remains constant. This demonstrates that the converter can switch modes while delivering constant output power. In the case where the output power is stepped down, the transition power is about half-way between the start and end output power, as the rms operation essentially averages the full-power and low-power operating powers.

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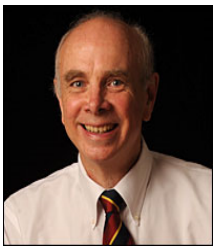

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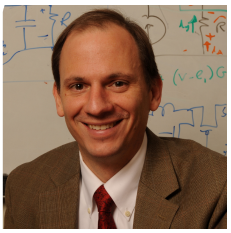
Werner-von-Siemens Chair for Power Electronics in 2008. From 2009 to 2014 he was a Visiting Associate Professor in the Department of Electrical Engineering and Computer Science at MIT. Since January 2014 he is an Assistant Professor in the Department of Electrical, Computer and Energy Engineering at the University of Colorado (CU) Boulder. His research interests are in power electronics and energy systems incorporating power electronic controls. Dr. Afridi is a recipient of Caltech's Carnation Merit Award, CU Boulder's College of Engineering and Applied Science Dean's Professional Progress Award, the BMW Scientific Award, and the NSF CAREER Award. He is co-author of two IEEE prize papers.



David J. Perreault (S'91, M'97, SM '06, F'13) received the B.S. degree from Boston University, Boston, MA, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA. In 1997 he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate, and became a Research Scientist in the laboratory in 1999. In 2001, he joined the MIT Department of Electrical Engineering and Computer Science, where he is presently Professor of Electrical Engineering. He has held multiple roles within the EECS department, most recently as Associate Department Head from November 2013 – December 2016.

His research interests include design, manufacturing, and control techniques for power electronic systems and components, and in their use in a wide range of applications. He also consults in industry, and co-founded of Eta Devices, inc. (acquired by Nokia in 2016) and Eta Wireless, inc., startup companies focusing on high-efficiency RF power amplifiers. Dr. Perreault received the Richard M. Bass Outstanding Young Power Electronics Engineer Award, the R. David Middlebrook Achievement Award, the ONR Young Investigator Award, and the SAE Ralph R. Teetor Educational Award, and is co-author of seven IEEE prize papers.