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A High Frequency Power Factor Correction Converter with Soft Switching

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***Abstract*—Power factor correction (PFC) converters are typically operated at low frequency to mitigate switching losses and to simplify control; this in turn requires large passive components. Soft switching techniques could permit higher frequency operation, but most soft-switched converters do not maintain high performance across the wide voltage and power ranges required for PFC applications. Here we present a PFC converter which enables high frequency operation by maintaining soft switching and by using a control scheme which requires no current sensing. These advantages are verified with a prototype which achieves power factors above 0.996 (THD $< 10\,\%$) while maintaining ZVS across voltage and power for efficiencies $\sim 97\,\%$. By using increased switching frequency ($\sim$ 10x over conventional designs), this converter can take advantage of greatly reduced passive component values for power conversion and EMI filtering.**

I. Introduction

Electrical loads process real power by drawing current at the same frequency as (and in phase with) the source voltage. Other frequency components of the input current result in reactive power and deliver no net energy to the load; these currents are nevertheless physically real and may dissipate energy in any source impedance (e.g. resistance in mains distribution lines and transformers). Currents at harmonic frequencies of the grid voltage are therefore regulated according to international standards, e.g. IEC/EN 61000-3-2. Power conversion stages which draw compliant currents by design are called Power Factor Correction (PFC) converters [1]–[3].

Power factor correction stages often make up a significant fraction of the overall power converter volume. Miniaturization using MHz switching frequencies is attractive, but fCV^2 switching losses become intolerable at grid voltages without "zero voltage (soft) switching" (ZVS). Most soft switching techniques are only suitable for narrow operating voltages and/or powers and therefore have not been widely used in PFC stages [4], limiting them to low frequency (LF, 30–300 kHz) operation[1] with large passive components for both power conversion and EMI filtering.

To illustrate the problem, consider the boost converter PFC as part of a two-stage architecture – arguably the most common combination in use. The PFC boosts from universal input 85–265 Vrms to a dc bus around 400 V. Operated near boundary conduction mode, the boost converter may allow a resonant transition to reduce its switch node voltage prior to turn-on. This process results in true ZVS for $V_{in} < V_{out}/2$, and "valley-switching" at $v_{min} = 2V_{in} - V_{out}$ otherwise. For much of the line cycle, the switch still turns on with hundreds of volts across it, making high frequency operation untenable.

Here we present a PFC converter which achieves ZVS for any step-up voltage conversion ratio. It can therefore act as a soft-switched replacement for popular boost PFC stages without any modifications to the rest of the system architecture. In addition, the converter uses a blended feedforward/feedback control scheme which eliminates the need for current sensing (both high-frequency inductor current and low-frequency input current). These features enable switching frequencies in the MHz regime and the opportunity for greatly reduced inductor and EMI filter sizes [14].

The proposed converter is based on a dc-dc converter with wide operating range [4]; this paper focuses on new aspects required for its adaptation to ac-dc PFC applications. In Section II, the basic converter operation is cursorily reviewed, but readers are referred to [4] for more thorough background. Section III proposes a blended feedforward/feedback control technique to achieve power factor correction without the need to sense input current or inductor current. Section IV presents a prototype and discusses details which are important for practical implementation. Section V presents experimental results showing that the converter reliably achieves ZVS at MHZ frequencies across the line cycle with power factors around 0.998 (THD$\sim 6\%$). We conclude that the converter has potential for high power density in a wide array of existing applications, including those with stringent power quality requirements.

II. Abridged Operation Overview

The proposed converter (Fig. 1) has a power stage that is topologically identical to the four-switch buck-boost converter, but is controlled to achieve zero-voltage soft switching (unlike pure boost converters) with low rms current (unlike pure buck-boost converters) across the line cycle. The proposed converter can thus operate at much higher frequencies without incurring high loss penalties. The converter has two distinct modes of operation.

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[1]Some PFC converters exceed this frequency range by achieving soft switching at the expense of additional lossy circuitry or by only partly achieving soft switching [5], [6]. Other approaches can achieve ZVS using complex switching networks [7], [8], stacked architectures [9], [10], or wide frequency ranges [11]–[13]. See [4] for further discussion.

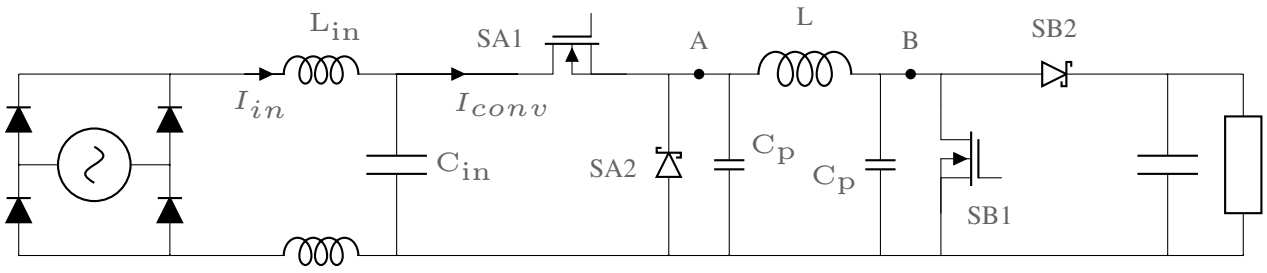

Fig. 1. The proposed power factor correction topology, which is identical to the four-switch buck-boost converter (the advantages of the proposed converter arise through control). Lumped parasitic capacitances C_p are drawn explicitly, and rectification bridge and an example emi filter are shown for completeness.

Low Voltage / Boost Mode: The converter may be operated as a conventional boost converter by turning switch SA1 on for the entire switching cycle. This mode (see Fig. 2) has an energy storage phase (SB1 on), a direct delivery phase (SB2 on), and a resonant phase to achieve ZVS (SB1 and SB2 off). The LC resonant phase begins with zero initial current, a dc offset voltage V_{in}, and an initial capacitor voltage V_{out}; as such, v_B will ring down to zero as long as $V_{in} < V_{out}/2$. Switch SB1 is turned on in response to the zero voltage condition (see Sec. III and Fig. 4) which may occur before the inductor current returns to zero; as such, the current at turn-on i_0 may be somewhat negative.

The high voltage mode below would also achieve ZVS at low voltage, but the boost mode is preferred as it maximizes the direct delivery time and has lower rms current.

High Voltage Mode: A second mode is proposed in [4] which achieves ZVS for any $V_{in} < V_{out}$. The progression of switching states includes an energy storage phase (SA1 and SB1 on), a direct delivery phase (SA1 and SB2 on), an indirect delivery phase (SA2 and SB2 on), and a resonant phase (all switches off). During the resonant phase, switch SA1 turns on when node A reaches V_{in}, while switch SB1 turns on Δt later when node B reaches zero; this does not significantly affect the understanding of the switching states, but must be accounted for in control.

The advantage of this mode lies in its "CLC" resonant phase, unlike the "LC" resonant phase in the low voltage mode. Node A begins at zero, node B begins at V_{out}, and there is no voltage offset (i.e. from the input voltage source). This scenario is guaranteed to return node B to zero and node A to (at least) V_{in} for *any* $V_{in} < V_{out}$.

The progression of switching states may be understood as that of a boost converter with an indirect delivery phase added to the end, thereby creating the necessary conditions in the resonant period to achieve ZVS. (The resonant phase distinguishes this approach from previous uses of this topology in CCM [15] or DCM [16], [17], thus supplying the important advantage of soft switching.) The progression of states may alternatively be understood as that of the conventional four-switch buck-boost converter (i.e. with a triangular inductor current waveform) with a direct delivery phase added in the middle, thereby reducing the rms current required for the same power.

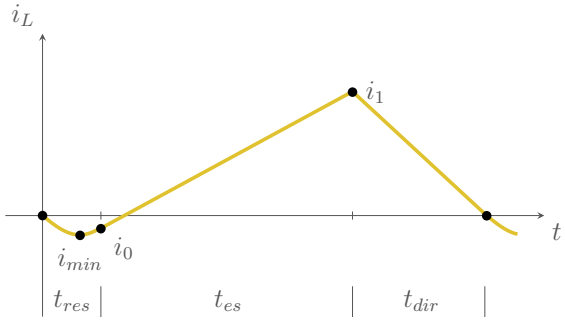

Fig. 2. Low Voltage (Boost) Mode inductor current waveform. This mode achieves ZVS when $V_{in} < V_{out}/2$. The switching cycle is divided into a resonant phase (SB1, SB2 off), an energy storage phase (SB1 on), and a direct delivery phase (SB2 on).

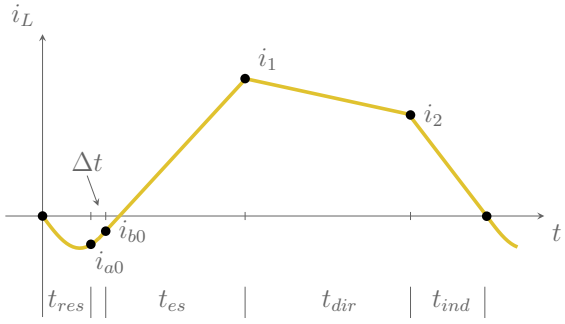

Fig. 3. High Voltage Mode inductor current waveform. This mode achieves ZVS when $V_{in} < V_{out}$, but is most useful where the Boost mode loses ZVS, i.e. $V_{in} > V_{out}/2$. The switching cycle differs from the Boost mode primarily with the indirect delivery phase (SA2, SB2 on).

There is a minimum value for the inductor current at the end of the direct delivery phase, denoted i_2 in Fig. 3. In order to properly commute from SA1 turning off to SA2 turning on, the inductor energy $\frac{1}{2}Li_2^2$ must be sufficient to discharge the parasitic capacitance C_p at node A. To the extent that this condition is violated, node B will not ring all the way down to zero volts in the final resonant transition. Maintaining i_2 above its minimum value will be an important constraint on control.

It is important to note that the inductor current may be inferred from on-times without measuring switching-frequency current. Indeed, in the high voltage mode, t_{res}, Δt, i_{a0}, and

i_{b0} may be computed from voltage measurements and circuit parameters alone. The converter chooses switch on-times, from which t_{es}, i_1, t_{dir}, i_2, and t_{ind} may also be calculated. A similar logic applies to the traditional boost mode. This observation means that any desired features of the inductor current waveform (esp. the average input current and i_2) may simply be computed and executed without current measurement or feedback. This is an important advantage where complex control is required (as in PFCs) while maintaining ZVS at high frequency. The only additional requirement is a control circuit that can (1) respond to ZVS detection by turning a switch on with sufficiently low delay and (2) hold the switch on for a programmable duration. Such a circuit is described in Sec. III and Fig. 4.

III. Control

The control of the proposed converter is different from many converters, though simply understood. A dedicated high-speed control circuit, like that shown in Fig. 4, is required for each controlled switch.[2] A given switch (e.g. SA1, SB1) is turned on when its corresponding ZVS Detector senses low voltage across the switch. The switch is then kept on for a certain on-time by way of its corresponding Ramp Timer, whose time-out is dictated by a dc control voltage. After the switch turns off, the cycle repeats as long as ZVS is eventually achieved again.

The switch turn-on and turn-off actions are thus, in a sense, passive. No input from a microcontroller is required, except to select the dc or slowly varying ZVS trigger voltage $\mathrm{REF_{ZVS}}$ and on-time control voltage $\mathrm{REF_{TMR}}$. The turn-on and turn-off events for a switch are asynchronous from the microcontroller clock, and indeed even from the events of the other switches. Therefore, the proposed converter control should not be understood as pulse-width-modulation or frequency control, though pulse-widths and frequencies will both vary. The most apt description would be "on-time control," though this phrase risks confusion with different methods having unfortunately similar names (e.g. constant on-time control, adaptive on-time control, etc.). In this case, "on-time control" simply means that the on-times are the only control variables, and the off-times and the timings of the turn-on/turn-off events are not directly commanded.

With the concept of on-time control understood, we turn to the proposed converter in particular. A possible control approach for this converter using constant on-times was suggested in [4]; despite its commendable simplicity, this prior approach was underspecified, had limited control of input current, and forced the converter into inefficient operation.

Here we propose an approach which achieves higher efficiency and grants the designer arbitrary control of the input current waveform (including high power factor/low THD waveforms) at the expense of only superficial complexity. The approach modulates on-times across the line cycle to control the input current shape; this is done in a feedforward manner using only input/output voltage measurements and pre-programmed circuit parameters. Thus, the designer need not measure input current nor design a feedback loop for this purpose. Though feedforward control in general is rightly avoided for its inaccuracy under uncertain parameters, inaccurate measurements, and incomplete models, we will show that feedforward control may be sufficiently reliable for purposes of power factor correction.[3]

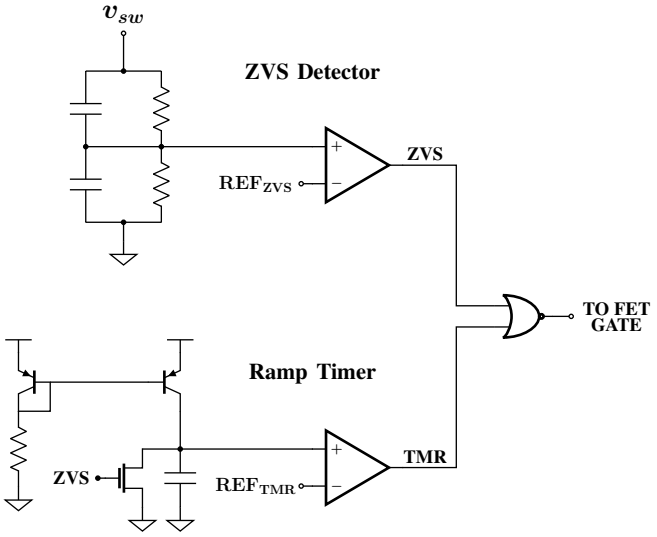

Fig. 4. Auxiliary comparator-based control circuit used for each active switch in the proposed topology, allowing for turn-on in response to zero-voltage conditions and a programmable on-time. Minor variations to this circuit may be required as discussed in Section IV.

With two control variables ($t_{a,on}$, $t_{b,on}$), we may select two features of the inductor current waveform to target. We choose to target the average (over a switching cycle) input current I_{in} and the corner current i_2. We wish to maintain the corner current i_2 at its minimum allowable value, minimizing rms currents while maintaining ZVS. We target the average input current, of course, for power factor correction.

To meet these targets, we need a mathematical model relating switch on-times to I_{in} and i_2. The analysis is simply explained, though the actual computations are messy and left to the Appendix. We quote only the driving logic and the final results here. To maintain precision, we use capital symbols to denote values that are constant or averages across a switching cycle; we use lower-case symbols to denote values that change within a switching cycle or that only have meaning within a switching cycle. We also introduce the notation $X = V_{in}/V_{out}$, as this ratio appears frequently. Finally, because we use V_{in} for the local input voltage (averaged over a switching cycle), we instead use V_{rms} to refer to the rms input voltage (taken over the line cycle). The peak of the input voltage waveform is then $\sqrt{2}V_{rms}$.

[2]The control circuit in Fig. 4 is improved over the one in [4] by using a current mirror (instead of a lone resistor) in the Ramp Timer. This solution is easily executed either on- or off-chip and results in a much more linear ramp.

[3]In addition to the feedforwad "inner loop" controlling the input current *shape* over the line cycle, a traditional feedback "outer loop" (slower than the line cycle) controls the output voltage by way of the *magnitude* of the input current waveform. There is nothing unique about this feedback loop, and it is mentioned only for completeness.

The logic for input current control is as follows. We are able to use a feedforward approach to because the converter always returns to the same state each cycle (at $t = 0$ in Figs. 2, 3). In principle, the entire behavior of the switching cycle can be predicted from circuit parameters, measured input/output voltages, and the commanded on-times. Starting at $t = 0$, we can determine when v_A will reach zero (t_{res}), what the inductor current will be (i_{a0}), then at what point will v_B reach zero (Δt later), etc. With selected on-times, the required variables are all known and the entire switching cycle is predictable. We can then compute I_{conv} and i_2.

In practice, the above analysis is reversed. One begins with a desired average input current I_{in} (determined by the position in the line cycle and also the voltage feedback controller) and then accounts for the current into C_{in} to obtain a required average converter input current I_{conv}:

$$I_{conv} = I_{in} - C_{in}\omega_{line}\sqrt{2V_{rms}^2 - V_{in}^2} \tag{1}$$

With a required I_{conv} and a desired i_2, the required i_1 may be computed:

$$i_1 = I_{conv} + \sqrt{I_{conv}^2 + i_2^2 X - 2I_{conv}i_2X^2 + 2I_{conv}i_2DX(1-X)} \tag{2}$$

where $X = V_{in}/V_{out}$, $D = t_{res2}V_{out}/Li_2$ and $t_{res2} = \frac{1}{2}\frac{2\pi}{\omega_2} = \pi\sqrt{LC_p/2}$. From there, the required times $t_{a,on} = \Delta t + t_{es} + t_{dir}$ and $t_{b,on} = t_{es}$ can be backed out and then commanded:

$$t_{b,on} = L\frac{i_1}{V_{in}} + L\frac{V_{out}\sqrt{\frac{C_p}{L}}(1-X)}{V_{in}} \tag{3}$$

$$t_{a,on} = t_{b,on} + L\frac{i_1 - i_2}{V_{out} - V_{in}} + \frac{2\sqrt{2LC}(1-X)}{\sqrt{X - X^2} + \sqrt{2}(1-X)} \tag{4}$$

While the equations for this feedforward approach appear complicated on paper, the approach is actually simple to implement in hardware. A microcontroller or ASIC measures the input/output voltages and has pre-programmed values for circuit parameters. It then simply performs a few calculations and commands the switch on-times by way of the control voltages $\mathrm{REF}_{\mathrm{TMRa,b}}$. The actual turn-on and turn-off events are executed with the dedicated high-speed circuitry and need not be "controlled" *per se*. Finally, we emphasize once again that no current measurement is required, neither high-frequency inductor current nor low-frequency input current.

Although the discussion above treats the proposed high voltage operating mode, similar logic applies to the low voltage boost mode. The calculations for the low voltage boost mode also appear in the Appendix.

The waveform quality available with the above approach can be seen in Fig. 5 showing experimental waveforms from the prototype in Sec. IV. Note in particular that the mode transition, often troublesome in multi-mode converters, is indiscernible. The converter achieved THD below 10 % under all conditions, with the majority of THD attributable to zero-crossing distortion. Nothing prevents further refinements to the model (in particular the assumption that the C_p charging/discharing times after t_{es},t_{dir} are negligble) from reducing THD further if desired.

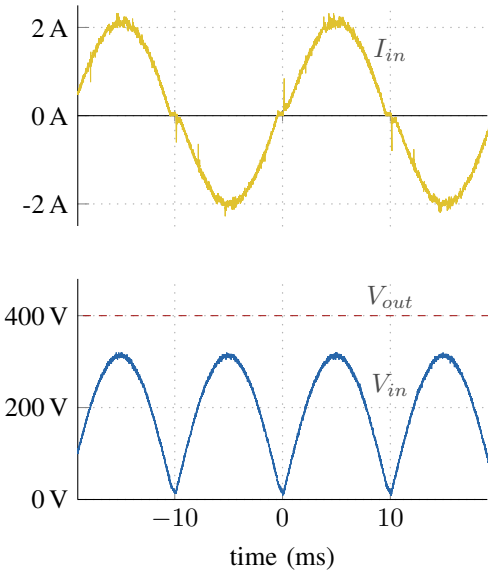

Fig. 5. Experimental operating waveforms for the proposed converter. The filtered input current has high power quality (THD < 10 %), with no discernible distortion from mode transitions. Zero-crossing distortion is the major source of THD, and can be eliminated with more detailed modeling.

IV. Implementation Details

The PFC converter was implemented in a hardware prototype utilizing GaN FETs, SiC diodes and advanced high frequency magnetics [18] (Table I). The design operates with dynamic frequency variation in the 2–4 MHz range, approximately 10x that of conventional PFC systems, with commensurate reductions in passive component values.

In addition to the power stage components, the high speed control circuit components used are also listed in Table I. The control circuit for SB1 is straightforward to implement, since SB1 is ground referenced. For SA1, there are two options:

1) Use the circuit in Fig. 4 and reference the control circuit to the source (node A) and v_{sw} to the drain V_{in}. The $\mathrm{REF}_{\mathrm{ZVS}}$ and $\mathrm{REF}_{\mathrm{TMR}}$ signals must be obtained in an isolated way, but no high frequency signals have an isolator in their path. This implementation is theoretically faster, but susceptible to noise as the signal "ground" is referenced to a switching node. This approach is difficult but feasible, and was used in [4].
2) Reference the control circuit to ground and connect v_{sw} to node A. In this case the ZVS Detector is not watching for v_{sw} to ring down, but rather to ring up – as such, the polarity of the ZVS comparator should be reversed.

Additionally, the ZVS trigger signal $\mathrm{REF}_{\mathrm{ZVS}}$ must be modulated as V_{in} changes (as opposed to the ZVS trigger for SB1 which need not change). This implementation requires isolation to bring the gate drive signal to the SA1 source voltage domain, thus placing a delay in the high-frequency path. The advantage of the ground-referenced controls is substantial, however, and we use this approach in this prototype.

The inductor was implemented with a high-frequency structure (see [18] for details) using Fair-Rite 67, a magnetic material appropriate to the frequency range [14]. The prototype thus served as a platform to explore both the proposed topology and the magnetic structure in [18].

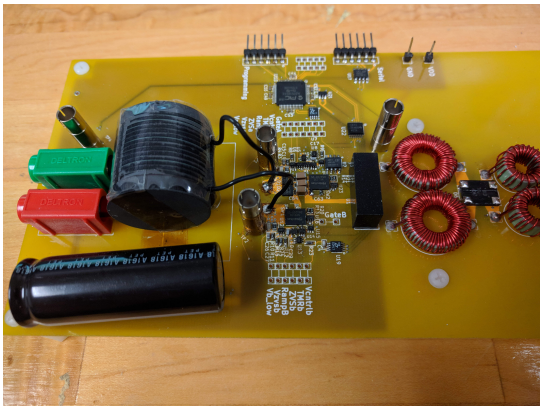

Fig. 6. Photograph of the prototype converter, including twice-line-frequency energy buffer capacitor, power stage inductor, switching and control elements, and input filter and rectifier.

TABLE I
PART SELECTION FOR THE PROTOTYPE

Component	Part/Value
FET SA1,SB1	Navitas 6131
Diode SA2,SB2	Wolfspeed/Cree C3D1P7060Q (2 each)
Capacitor C_{out}	220 µF
Inductor L	13.5 µH
Core Material	Fair-Rite 67
Inductor Design	$Q = 620$ at 3 MHz [18]
Diode Bridge	Z4DGP406L-HF
Comparators	ADCMP601
Current Mirror BJTs	2SA1873
Ramp Reset FET	SN74LVC1G06
Gate Drive	"TinyLogic" NC7WZ16
Microcontroller	PIC32MZ0512EFE064

V. Experimental Results

Measured efficiencies and input THD under varying load conditions show that the prototype achieves a combination of high performance, high frequency and high power quality (Fig. 7). The converter achieved ZVS across the line cycle for the full range of powers and at switching frequencies of 2–4 MHz, as predicted in Section II. By contrast, the conventional boost PFC would lose ZVS with hundreds of volts at turn-on (for universal input). As such, the conventional solution would not be feasible at these frequencies

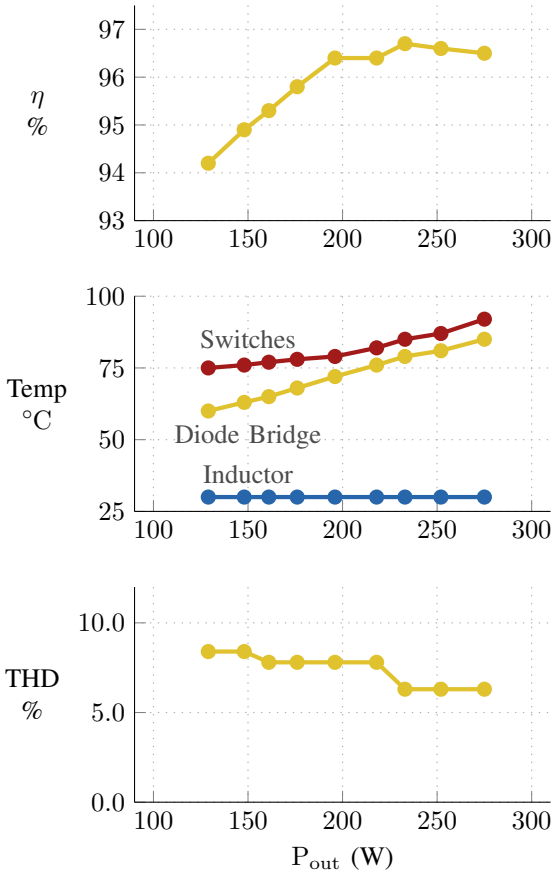

Fig. 7. Measured prototype performance, showing high efficiency and high power quality. Experiments were performed at 220 Vrms input and 400 Vdc output maintained by low-bandwidth digital closed-loop control for a resistive load. Modest forced convection was applied to the switches, though the devices used are primarily bottom-side cooled.

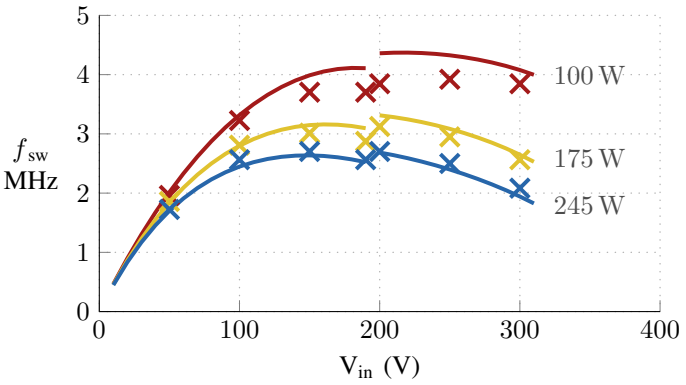

Fig. 8. Instantaneous frequencies across the rising half of the line cycle, showing reasonable frequency variation across voltage/power. Measured values agree well with curves calculated from the model in the Appendix.

with available semiconductor devices and loss allowances; the conventional boost solution is thus limited to lower frequencies and larger passive values.

The switching frequency was also measured for the rising

portion of the line cycle (Fig. 8), showing that frequency variation is low for a particular power and reasonable across powers. Experimental frequency measurements validate the model used in the Appendix, with the largest deviations at low power where model idealizations break down. These idealizations can be corrected with a more detailed model, if necessary.

The prototype was not optimized for volume. The inductor size in particular was driven by concerns related to the experimental nature of its structure and hence difficulty/expense in prototyping. Nevertheless, thermal measurements (Fig. 7) indicate that the inductor has very low loss and temperature rise ($\Delta T < 5\,^{\circ}\mathrm{C}$); we infer that the inductor volume could be greatly reduced without impacting thermal limits or efficiency. The high frequencies, small passive component values (e.g. L =13.5 µH), and high efficiencies make it clear that the converter has potential for high density.

We also infer from Fig. 7 that the input diode bridge is a significant source of loss. This may appear to be a disadvantage compared to now-popular "bridgeless" PFC topologies; however, this loss can be largely mitigated by using active rectification [19]. Any apparent disadvantage should also be weighed judiciously against other factors; for example, converters with a front-end bridge may take advantage of smaller emi filter components on the rectified side (this becomes increasingly important with reductions in the power stage volume). Finally, the added control flexibilty and variety of accessible modes of the proposed converter allows the designer to meet a variety of demands, including high frequency with ZVS, tolerable frequency range, variable output voltage, etc.

VI. Conclusion

The proposed converter has been shown to achieve ZVS for any step-up voltage conversion ratio with effective high frequency controls which require no current sensing, making it suitable for developing PFC converters operating at MHz frequencies. We validated the design approach and controls in a hardware prototype and demonstrated that the converter can maintain high efficiency ($\sim 97\,\%$) at 2–4 MHz switching frequencies, allowing small-valued passive components. We also show that a feedforward control approach can be used to meet IEC/EN 61000-3-2 input harmonic requirements, and even more stringent requirements for low THD.

In addition, the prototype highlights the potential offered by advanced magnetic materials [14] and design [18] when operated at high frequency. Converter performance may be improved further with refinements to wide-bandgap switch technology, which limits both the operating frequency and efficiency through C_{oss} and $R_{DS,on}$. Overall, we expect the opportunities enabled by this converter to improve the power density of PFC stages and EMI filters for grid-interface power converters.

Appendix A
Converter Analysis for Feedforward Control

One critical feature of the proposed converter is that the inductor current always returns to zero. From this point, based on constant circuit parameters and the instantaneous input and output voltages, the entire circuit behavior is predictable. The switch on-times can be computed to produce a desired inductor current waveform without actually sensing the inductor current. Indeed,the circuit need not even sense the converter input current for power factor correction, as even the average converter input current I_{conv} is calculable from an appropriately accurate model. This totally feed-forward approach avoids the need for current sensing altogether.

The remainder of this section outlines how to model the converter for this purpose. The end goal of the model is to compute the required switch on-times as functions of *only* constant circuit parameters and measureables the controller will already have. The results will be $t_{a,on}$ and $t_{b,on}$ as functions of

- the values of the inductor L, parasitic capacitors C_p, and input capacitor C_{in},
- the measured input voltage V_{in}, output voltage V_{out}, line frequency ω_{line} and line rms voltage V_{rms}, and
- the desired values of i_2 and I_{in} (I_{in} is varied over the line cycle for input current shaping, and varied in magnitude more slowly as part of the output voltage feedback loop).

We remind the reader that capital symbols denote constants or averages across a switching cycle and lower-case symbols denote truly instantaneous values or those that only have meaning within a switching cycle. For compact notation, we also use $X = V_{in}/V_{out}$, $\omega_1 = 1/\sqrt{LC_p}$ for the LC resonant frequency and $\omega_2 = 1/\sqrt{LC_p/2}$ for the CLC resonant frequency.

A. Low Voltage Mode

We analyze the low-voltage mode in accordance with Fig. 2, assuming that i_1 is sufficient to charge C_p in negligible time after SB1 turns off. We wish to derive a model to relate the average input current I_{in} to the on-time of SB1. To do this, we first recognize that the input current I_{in} is not equal to the converter input current I_{conv}, but rather is the sum of I_{conv} and current into the input capacitance I_C. For simplicity, we model the input capacitance as a lumped linear sum of any EMI filter capacitor values. Using this simplified model, we compute the required I_{conv} in terms of the desired I_{in} and the I_C drawn by the input capacitance.

$$\begin{aligned} I_{conv} &= I_{in} - I_C \\ &= I_{in} - C_{in}\frac{dV_c}{dt} \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\cos(\omega_{line}t) \end{aligned} \tag{5}$$

We can replace $\omega_{line}t = \sin^{-1}\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)$ to make the above equation a function of instantaneous measurables instead,

$$\begin{aligned} I_{conv} &= I_{in} - C_{in}\omega_{line}\sqrt{2}V_{rms}\sqrt{1-\left(\frac{V_{in}}{\sqrt{2}V_{rms}}\right)^2} \\ &= I_{in} - C_{in}\omega_{line}\sqrt{2V_{rms}^2 - V_{in}^2} \end{aligned} \tag{6}$$

Next, we must express I_{conv} as a function of the control input $t_{b,on}$. To do this, we first compute the current at turn-on i_0 and the most negative inductor current during resonance i_{min}. During resonance:

$$v_B = (V_{out} - V_{in})\cos(\omega_1 t) + V_{in} \tag{7}$$

$$i_L = i_{C_p} = C_p\frac{dv_B}{dt} = -C_p(V_{out} - V_{in})\omega_1\sin(\omega_1 t) \tag{8}$$

The minimum inductor current is easily computed,

$$i_{min} = -C_p\omega_1(V_{out} - V_{in}) \tag{9}$$

The current at turn-on is related to the time t_0 from the beginning of resonance until the time that node B reaches zero volts and SB1 turns on, $t_0 = \frac{1}{\omega_1}\cos^{-1}\left(\frac{-V_{in}}{V_{out}-V_{in}}\right)$.

$$\begin{aligned} i_0 &= -C_p\omega_1(V_{out} - V_{in})\sin\left(\cos^{-1}\left(\frac{-V_{in}}{V_{out}-V_{in}}\right)\right) \\ &= -C_p\omega_1 V_{out}\sqrt{1-2X} \end{aligned} \tag{10}$$

By making a piecewise-linear approximation for the inductor current, we compute the average converter input current as:

$$I_{conv} \approx \frac{i_1 + i_{min}}{2} = \frac{1}{2}\left(i_0 + \frac{V_{in}t_{b,on}}{L} + i_{min}\right) \tag{11}$$

Plugging in for I_{conv}, i_0, and i_{min} and rearranging, we get

$$\begin{aligned} t_{b,on} = \quad & 2\frac{L}{V_{in}}I_{in} \\ & + \sqrt{LC_p}\frac{1}{X}\left(1 - X + \sqrt{1-2X}\right) \\ & \mp 2LC_{in}\omega_{line}\sqrt{2\left(\frac{V_{rms}}{V_{in}}\right)^2 - 1} \end{aligned} \tag{12}$$

where the $\mp$ depends on whether the input voltage is rising ($-$) or falling ($+$). Note that this expression is easily interpreted: the first term is equivalent to the popular constant-on-time control used in true Boundary Conduction Mode; the second term corrects for the resonant transition time (significant at high frequency); the third term accounts for the effect of input capacitance.

B. High Voltage Mode

The model for the high voltage mode proceeds in a similar fashion. We take the input capacitance into account in the same way. We need only compute the relationship between the switch on-times and our design targets, I_{conv} and i_2. The average input current during the HV mode is given by:

$$\begin{aligned} I_{conv} &= \frac{1}{T}\left[\frac{1}{2}i_1 t_{es} + \frac{1}{2}(i_1 + i_2)t_{dir}\right] \\ &= \frac{1}{2}\frac{\frac{i_1^2}{V_{in}} - \frac{i_2^2}{V_{out}-V_{in}} + \frac{i_1^2}{V_{out}-V_{in}}}{\frac{i_1}{V_{in}} + \frac{i_1-i_2}{V_{out}-V_{in}} + \frac{i_2}{V_{out}} + \frac{t_{res2}}{L}} \\ &= \frac{i_2}{2}\frac{(i_1/i_2)^2 - X}{i_1/i_2 - (X)^2 + DX(1-X)} \end{aligned} \tag{13}$$

where $D = t_{res2}V_{out}/Li_2$ and $t_{res2} = \frac{1}{2}\frac{2\pi}{\omega_2} = \pi\sqrt{LC_p/2}$, recalling that we use $C_p/2$ because there are two such capacitors in series in the CLC case. The above equation reduces to a quadratic in i_1/i_2 which is easily solved,

$$\begin{aligned} i_1 = I_{conv} + \\ \sqrt{I_{conv}^2 + i_2^2 X - 2I_{conv}i_2X^2 + 2I_{conv}i_2DX(1-X)} \end{aligned} \tag{14}$$

Having set i_2 to maximize efficiency and i_1 to achieve the correct average converter input current, we only need to specify the on-times of the switches. To do this, we must understand when the switches turn on (equivalently, when the switch voltages reach zero). Switch SA1 will turn on first, with the inductor current equal to i_{a0} after a time t_{res}

$$t_{res} = \frac{1}{\omega_2}\cos^{-1}(1-2X) \tag{15}$$

$$\begin{aligned} i_{a0} &= -\frac{1}{2}CV_{out}\omega_2\sin\left(\cos^{-1}(1-2X)\right) \\ &= -C_p\omega_2\sqrt{V_{out}V_{in} - V_{in}^2} \end{aligned} \tag{16}$$

Once SA1 turns on, the equivalent circuit changes from an undriven CLC resonant circuit to an LC resonant circuit with a low impedance input V_{in}. Taking t_{res} as an initial condition, we may use an energy argument to calculate i_{b0}:

$$\frac{1}{2}C_p\left[V_{in} - (V_{out} - V_{in})\right]^2 + \frac{1}{2}Li_{a0}^2 = \frac{1}{2}C_pV_{in}^2 + \frac{1}{2}Li_{b0}^2 \tag{17}$$

$$\begin{aligned} i_{b0} &= \sqrt{\frac{C_p}{L}(V_{in} - V_{out} + V_{in})^2 - \frac{C_p}{L}V_{in}^2 + i_{a0}^2} \\ &= \sqrt{\frac{C_p}{L}}V_{out}(1-X) \end{aligned} \tag{18}$$

Finally, we may estimate $\Delta t = t_{b0} - t_{a0}$ by assuming the parasitic capacitance is discharged by an average current $\frac{1}{2}(i_{a0} + i_{b0})$ from its initial voltage $V_{out} - V_{in}$ to zero.

$$\begin{aligned}\Delta t &= (V_{out} - V_{in})C_p / \left(\frac{i_{a0} + i_{b0}}{2}\right) \\ &= \frac{2\sqrt{2LC_p}\,(1-X)}{\sqrt{X - (X)^2} + \sqrt{2}\,(1-X)}\end{aligned} \tag{19}$$

Now, the on-time for SB1 is simply based on a linear inductor current ramp from i_{b0} to i_1,

$$t_{b,on} = L\frac{i_1}{V_{in}} + L\frac{V_{out}\sqrt{\frac{C_p}{L}}\,(1-X)}{V_{in}} \tag{20}$$

And finally, the on-time for SA1 is simply equal to the on-time for SB1, plus the direct delivery time, plus Δt.

$$\begin{aligned}t_{a,on} = t_{b,on} &+ L\frac{i_1 - i_2}{V_{out} - V_{in}} \\ &+ \frac{2\sqrt{2LC_p}\,(1-X)}{\sqrt{X - (X)^2} + \sqrt{2}\,(1-X)}\end{aligned} \tag{21}$$

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