Integrated CMOS Energy Harvesting Converter with Digital Maximum Power Point Tracking for a Portable Thermophotovoltaic Power Generator

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***Abstract*—This paper presents an integrated maximum power point tracking system for use with a thermophotovoltaic (TPV) portable power generator. The design, implemented in 0.35 μm CMOS technology, consists of a low-power control stage and a dc-dc boost power stage with soft-switching capability. With a nominal input voltage of 1 V, and an output voltage of 4 V, we demonstrate a peak conversion efficiency under nominal conditions of over 94% (overall peak efficiency over 95%), at a power level of 300 mW. The control stage uses lossless current sensing together with a custom low-power time-based ADC to minimize control losses. The converter employs a fully integrated digital implementation of a peak power tracking algorithm, and achieves a measured tracking efficiency above 98%. A detailed study of achievable efficiency versus inductor size is also presented, with calculated and measured results.**

I. Introduction

THE static conversion of heat to electricity through thermophotovoltaic (TPV) systems was first proposed in the 1950s [1]. Recently, advances in material science, most notably in low-bandgap semiconductors and photonic crystals, has enabled the development of TPV power generators with significantly higher power density and conversion efficiency than what was previously achievable. Thermophotovoltaics, while similar to photovoltaics (PV), has several key differences. The wavelengths of light captured by TPV systems is mostly in the infrared (IR) region (1-2.5 μm), compared to light in the visible spectrum that is captured by conventional photovoltaics. For this reason, TPV diodes have considerably lower bandgaps than PV cells (0.8-0.5 eV), to enable the conversion of lower-energy photons. Furthermore, TPV power generation is often achieved not directly from sunlight (although it is possible to do so), but from a thermal emitter that is heated up through various means. Because the radiated thermal output power of the emitter can be controlled, and the TPV cell distance from the emitter can be made very small, TPV cells can be made to operate at power densities more than two orders of magnitude higher than solar PV cells [2]. Fig. 1 shows the centimeter-scale TPV power system that is the motivation for this work. The heat source, a silicon micro-fabricated fuel reactor [3] that generates radiant heat, is surrounded by GaInAsSb TPV diodes with bandgap of 0.54 eV [4], power electronics, and heatsinks. The system, suitable for centimeter-scale power generation, allows multiple fuel options, and promises high energy density and high efficiency. Another attractive feature of the system is the lack of any moving parts, which enables long lifetime and robust operation. Moreover, the system is compatible with batch manufacturing that can drastically reduce the production cost in large volumes, as well as enable modular implementations with customizable power configurations depending on user needs.

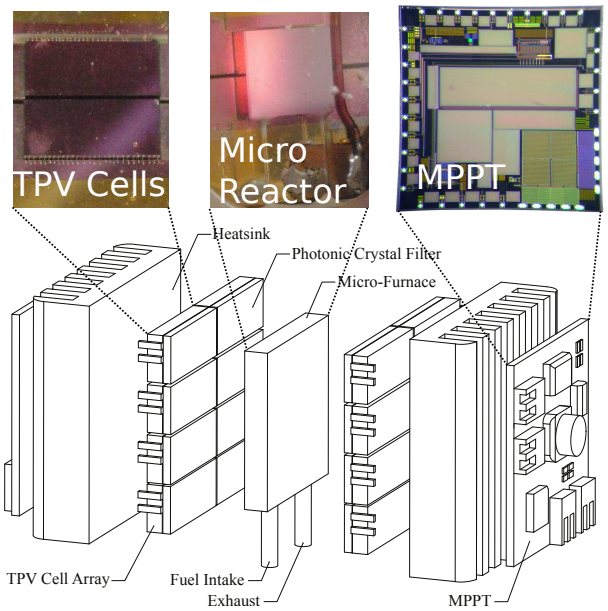

Fig. 1. Illustration of portable power generation TPV system including burner, TPV cells and power electronics.

Much of the previous work on TPV power generation has focused on device-level performance, with little attention given to the system-level considerations [5], [6]. As described in [7], substantial performance improvements can be realized with the proper integration of power electronics in the system architecture. In this paper, we present a distributed maximum power point tracking system developed in 0.35 μm CMOS technology for use in the system depicted in Fig. 1. This MPPT system includes both power point tracking controls and

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an integrated dc-dc boost converter. Although the application we are describing in this work is a micro-generator TPV system, the approach has applications in other TPV systems such as solar-TPV, radioisotope TPV, as well as for energy harvesting with conventional photovoltaic cells. This work represents an expansion of our earlier conference paper [8], and includes a more detailed description of the control implementation, additional details regarding the CMOS circuitry, a more extensive design trade-off discussion for the digital MPPT implementation, as well as additional references to related work.

Section II of the paper gives an overview of the electrical characteristics of the TPV cells, and the system-level challenges that we seek to address. Section III presents our power management system architecture, and section IV provides a detailed analysis of the fully-integrated control architecture to achieve maximum power point operation. In section V we show the design and operation of the integrated power stage, together with experimental and model-based design insights into the trade-off between converter efficiency and size, in particular as it pertains to the magnetics design. Experimental results are presented in section VI, and section VII concludes the paper.

II. MPPT Architecture

Shown in Fig. 2 are current and voltage characteristics of four series-connected GaInAsSb TPV cells (one TPV module) [4], when operated under typical conditions in the micro-generator [9]. As seen in the plots, the individual maximum power points (MPPs) differ both in current and voltage when the irradiation is reduced. In general, the MPP current changes linearly with irradiation, while the MPP voltage changes non-linearly both with irradiation and temperature. In the application considered here, the mismatch will primarily be caused by irradiation differences, but temperature variations will also produce a secondary effect. As illustrated in Fig. 2, when two modules with different irradiation are connected in series (and hence forced to operate with equal currents), the resulting operating points for both modules is below their individual MPPs. This mode of operation (forced current equalization) thus leads to reduced overall energy harvest compared to the theoretical maximum, and is undesirable.

A. Conventional MPPT Architecture

Figures 3a and 3b illustrate two common methods to connect photovoltaic cells to their loads. In Figure 3a all the cells are connected in series, and are directly connected to the load, a battery in this example. A diode is typically placed in series with the cells to prevent the battery from discharging through the cells during low light conditions. This approach, while simple, is typically very inefficient. Ignoring the small voltage drop across the diode, the string voltage V_{string} is restricted to be equal to the battery voltage V_{out} at all times, which is typically not the same as the MPP voltage (V_{MPP}). For a particular operating irradiation level and temperature, the series-connected cells' V_{MPP} may coincide with V_{out}, but at all other times, less than the maximum power is extracted from

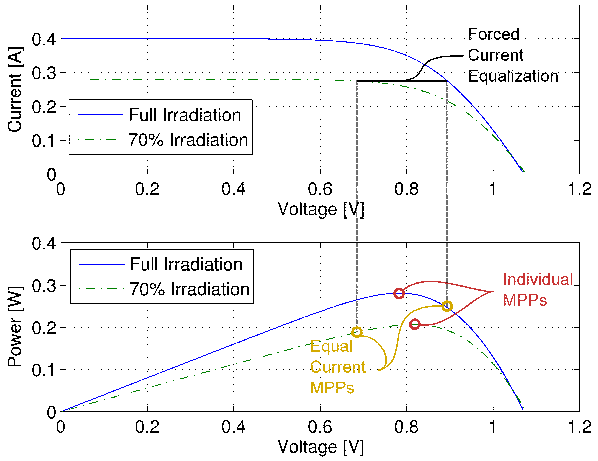

Fig. 2. I-V (top) and P-V (bottom) characteristic of 4 series-connected TPV cells used in this work for two typical operating irradiation and temperature levels.

the cells. Figure 3b shows a method which is typically used to circumvent this limitation. By placing a dc-dc converter between the series-connected cells and the load, the string voltage V_{string} can be controlled to equal V_{MPP} at all times. The dc-dc converter, acting as a maximum power point tracker (MPPT), continuously tracks V_{MPP} by adjusting its conversion ratio in response to changes in operating conditions.

The method of Figure 3b is often adequate for solar photovoltaic applications, where the solar irradiation is a plane-wave, ensuring uniform illumination of all cells in the series string. Provided the cells are properly matched in terms of their electrical characteristics, they will then produce equal currents. The situation is different in the TPV application considered here. Since the burner is positioned close to the TPV diode (2-3 millimeters), the irradiation is non-uniform and depends on the relative position of the diode with respect to the burner. In addition, the temperature distribution across the burner surface is non-uniform and resonant cavity effects and reflections furthermore distort the uniformity of irradiation. This leads to mismatched cell photocurrents, with the cell receiving the most irradiation producing the most current. If a method similar to that of Figure 3b is employed in this situation, the string current I_{string} is limited to the value of the least irradiated cell. Thus, all other cells are operating at a cell current that is below their peak current, resulting in a total output power that can be substantially lower than the maximum achievable. The result is similar to that observed in solar panels with partial shading, as discussed in [10]–[12]. The non-uniform irradiation in this application prevents efficient energy extraction with the stacking of many cells in series to achieve a high output voltage. Considerable efforts have gone into modeling and understanding this uniformity in our application [13]–[15], which is further complicated by the addition of a photonic crystal (PhC) filter in our system that performs spectral control. Through a combination of a selective emitter which preferentially emits convertible photons and a front surface reflector (PhC filter) which recuperates

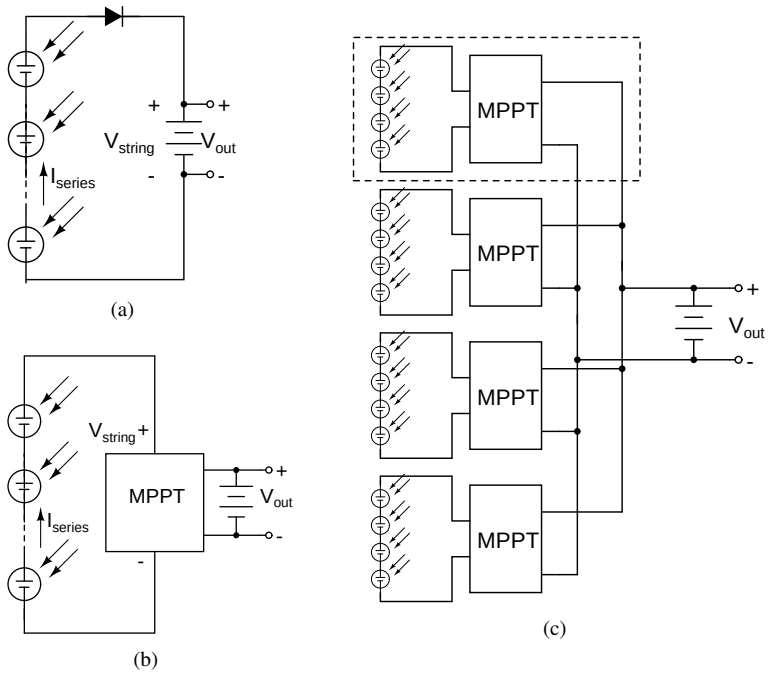

Fig. 3. (a) Simple cell connection, which does not extract the maximum power from the cell. (b) Conventional method with series-connected cells attached to a single MPPT. (c) Multi-MPPT method employed in this work.

non-convertible photons, improved TPV conversion efficiency can be achieved, but at the cost of increased modeling complexity. Nevertheless, efforts were made in [14] to model the irradiation distribution in a micro-reactor system using computational fluid dynamics, which confirmed the relatively large (i.e., 200 °C) variation across the micro burner surface. Unfortunately, it is very difficult to mitigate this mismatch through material and mechanical design changes alone, as it would require precise control over micro-reactor dimensions such as the channel geometry. In addition to requiring more sophisticated processing, it would require many iterations in an expensive fabrication process to fine tune performance. This motivates the exploration of mismatch compensation through electrical means, which is the focus of this work.

B. Distributed MPPT Architecture

Figure 3c shows the architecture we propose to ameliorate these concerns. In this architecture, four diodes are connected in series and form a module. Each module is then connected to its own individual MPPT, and the outputs of all MPPTs are connected in parallel. The choice of four cells per module was made to provide a large enough working voltage (approximately 1 V) for the MPPTs to ensure efficient power conversion by the electronics. Additionally, this voltage is below the reverse breakdown voltage of a typical TPV cell [16], such that stronger TPV cells in a single module will not cause an under-performing cell to be reverse biased. Using this architecture, current mismatch is limited to only four cells, all of which are placed in close proximity to each other, thereby minimizing the negative effects of non-uniform irradiation. The boxed area of Figure 3c highlights the system components that are considered in this work, which constitute four series-connected cells and one MPPT. The parallel output connection of the individual MPPT converters can be further utilized for interleaved operation and ripple cancellation [17], [18], enabling smaller individual output capacitance for each converter. Moreover, since our proposed MPPT converter provides maximization of its input power, there is no inadvertent coupling between parallel MPPT converters. The shared output battery shown in Figure 3c further mitigates any such concerns, as it acts as a large (shared) fixed output voltage for the individual MPPT converters.

It should be noted that distributed MPPT architectures themselves are not new, they have in fact successfully been employed in solar PV applications (primarily in residential settings). In these applications, they are often-referred to as module-integrated-converters (MiCs) [19], and typically provide dc-dc module-level MPPT (typically referred to as DC optimizers) or dc-ac power conditioning as well as module-level MPPT (typically referred to as micro-inverters [20]–[22]. Recently, *sub-module* dc-dc MPPT implementations have been demonstrated [12], [23]–[25], where mismatch within the solar PV panel itself can be mitigated. These solutions still operate at substantially higher voltages and power levels than what are presented here, and do not require low-power CMOS control and power devices.

While the I-V characteristics of solar PV modules oftentimes suffer from local maxima in shading scenarios [10], [12], it is important to note that in our application each module only has one global maximum power point. In solar PV applications, bypass diodes are used to prevent excessive power dissipation (and eventual failure) of shaded cells. These are typically placed in parallel to every 18-24 cells, and will conduct when the reverse voltage of the shaded cell exceeds the sum of the forward operating voltages of the unshaded cells. Conducting bypass diodes are what causes the

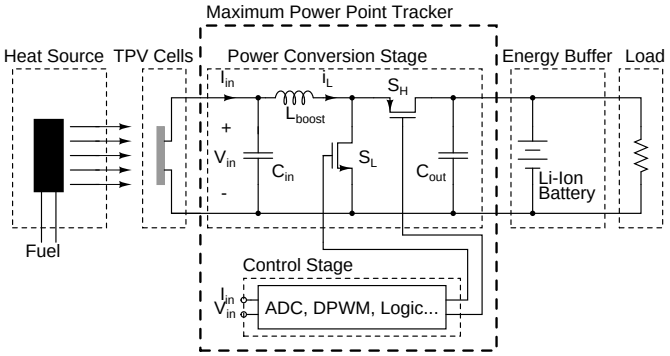

Fig. 4. Schematic drawing of the system architecture. The integrated maximum power point tracker consists of a boost converter power stage and a control stage, all implemented in a 0.35 μm CMOS process.

characteristic local maximum power point in solar modules [12] under shaded operation. In our application, the reverse characteristics of the TPV cells are such that no bypass diodes are required for protection of shaded cells since the cells will not enter reverse breakdown. Thus, unless a large number of cells (much larger than in our system) are connected in series, no local maximas will be observed.

The implementation of a distributed MPPT architecture in such a low power ($<$ 500 mW) and low voltage ($<$ 1.1 V) system presents additional challenges, both from the power converter and control point of view. Low-voltage CMOS energy harvesters for photovoltaic applications have been developed in the past, but typically at much lower power levels [26]–[28] and with lower tracking/conversion efficiencies. Past work has also not discussed the size and efficiency trade-offs in the power stage with respect to passive component selection, something that we address in detail in this work. A more detailed description of the system architecture of the TPV power generator can be found in [2], [29].

III. System Overview

The maximum power point tracker we have developed is illustrated in the schematic drawing of Fig. 4, alongside the other system components. The power tracker consists of two primary structures: the control stage and the power stage.

The power stage comprises a CMOS integrated boost converter with an off-chip inductor and off-chip capacitors. The control stage and gate drivers are all powered from the intermediate energy buffer on the output, which is a lithium-ion battery in Fig. 4, but can be any charge storage device with suitable energy density and voltage range. A detailed description of the power stage and its operation is presented in section V.

The task of the control stage is to provide the duty cycle command to the power devices to ensure that the TPV cell operates at its most efficient point – the maximum power point. Many different techniques [30] have been proposed to implement the maximum power point tracking functionality. In this work, we use Perturb and Observe (P&O) [31]. The synchronous boost converter power stage has an input/output voltage relationship given by:

$$V_{out} = \frac{V_{in}}{1 - D} \tag{1}$$

The boost converter can be controlled to achieve peak power tracking by perturbing the duty cycle (D) in a certain direction (increase or decrease), and observe whether the delivered power increased or decreased due to this perturbation. If the power increased, the controller continues to perturb the duty cycle in the same direction, but if the power decreased, the direction of the perturbation is changed. With this method, the controller eventually settles on the peak power point of Fig. 2, where it oscillates to within the finest resolutions of the duty cycle command and sensors. This method, often called hill climbing, or perturb and observe [31], is one of the most common MPPT algorithms used to date [30]. The P&O technique is well-suited for digital implementation, which we have chosen for our 0.35 μm CMOS design. Digital control was chosen for its flexibility in operating conditions, as we explore switching frequencies over 500 kHz-1.5 MHz, as well as the future possibility of synchronizing the operation of several MPPT converters to achieve ripple reduction through interleaved operation [17], [18]. Moreover, the operating conditions in our intended application are expected to change very slowly with time, enabling very low MPPT update frequencies. A digital solution can retain the MPPT state in logic over an indefinitely long time, which cannot be said for purely analog solutions, which are affected by leakage currents of analog sample-and-hold circuitry. While a digital solution typically will consume more CMOS area, we note that in our fully integrated solution, the area occupied by the MPPT controller itself is quite small compared to that of the power stage. It should be noted that the focus of this work is not the implementation of any new MPPT algorithm, but rather the exploration of CMOS integration of cell-level low-voltage energy harvesting power converters, and their associated design challenges. The implementation details of this control technique in CMOS technology are presented in the next section.

IV. Control

Here we introduce how the controls of our system are realized while achieving the goals of very low sensing and control loss and maximum extraction of available energy from the source.

A. Lossless Current Sensing

While voltage sensing is typically relatively easy to implement, sensing of current in a power converter is often more challenging. The current sensing method used in this work is shown in Fig. 5. It provides lossless sensing of the current by utilizing the parasitic resistance of the power inductor (L_{boost} of Fig. 4). (The approach is "lossless" in the sense that it does not introduce additional loss beyond what is already unavoidably present in the circuit.) This method results in overall increased conversion efficiency, since no additional sense resistors are introduced into the circuit, which would

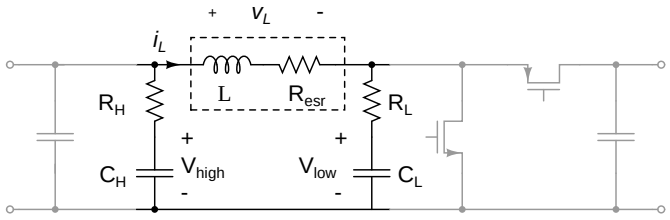

Fig. 5. Schematic drawing of the lossless current sensing implementation. The voltage drop across the inductor parasitic resistance R_{esr} is extracted through low-pass filtering.

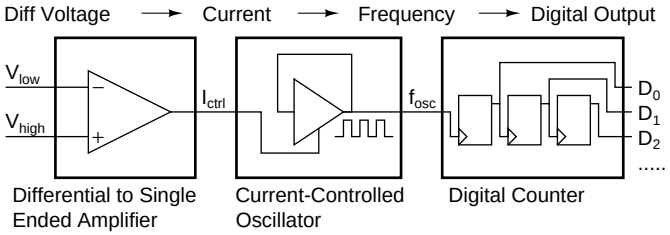

Fig. 6. Block diagram of the differential ADC architecture with inherent low-pass filtering and low power and area requirements.

add power loss to the system. The instantaneous voltage (v_L) across the inductor L of Fig. 5 is given by:

$$v_L = L\frac{di_L}{dt} + i_L R_{esr}, \tag{2}$$

where R_{esr} is the existing parasitic resistance of the inductor, and i_L is the *instantaneous* current through the inductor. Taking the average value of both sides of (2) yields:

$$\langle v_L \rangle = L\langle\frac{di_L}{dt}\rangle + \langle i_L \rangle R_{esr}, \tag{3}$$

where $\langle i_L \rangle$ represents the *average* current through inductor. It is well known [32] that in periodic steady-state, $\langle \frac{di_L}{dt} \rangle$ must be zero, yielding:

$$\langle v_L \rangle = \langle i_L \rangle R_{esr}. \tag{4}$$

The low-pass filtered (averaged) differential voltage v_L can thus be used to measure the average input current. First-order low-pass filtering can be accomplished through the capacitors C_H and C_L together with resistors R_H and R_L of Fig. 5:

$$\langle v_L \rangle = V_{\rm high} - V_{\rm low}. \tag{5}$$

This sensing method is well suited to this application as we only need to know *relative* currents (and powers), not absolute values. Variations in inductor ESR are thus not problematic. Furthermore, the time constant of any temperature-induced variation of the ESR value is much larger than the chosen sampling time, so it does not negatively affect tracking performance. The values of filter capacitors and resistors must be chosen large enough such that the switching ripple is sufficiently attenuated, but as is shown below, the analog-to-digital converter can be designed to provide some of this filtering.

B. Analog to Digital Converter

We implemented the ADC architecture of Fig. 6 to convert the analog low-pass filtered differential voltage of Fig. 5 to a digital value. The architecture provides inherent low-pass filtering through the counting stage, which is beneficial since it reduces the analog filtering requirements of the signal. This directly translates to a reduction in silicon area by the integrated filter resistors and capacitors. Other key characteristics of the architecture of Fig. 6 are low power consumption and very small area. The active area occupied by the two ADCs (for current and voltage measurement) is 0.083 mm^2, and the power consumption for two ADCs at a sampling rate of 100 Hz (much faster than what is required for the application) is 48 μW. Furthermore, the ADC architecture can be implemented as a single-ended ADC by connecting $V_{\rm low}$ to a fixed reference voltage. Since the input stage is implemented with PMOS transistors, it is possible to make this fixed reference voltage equal to ground. By doing so, one can thus realize a single-ended ground-referenced ADC. In our solution, we thus employed two identical ADC converters. The first one was used in differential mode (as shown in Fig. 7) to measure the average input current, while the second was used to measure the input voltage of the MPPT, with $V_{\rm low}$ tied to ground and $V_{\rm high}$ connected to the converter input voltage through a resistor divider.

Here we discuss the operation and design of the components of Fig. 6 in more detail:

1) Differential voltage to single-ended current converter: The conversion from differential voltage to single-ended current is performed by the circuit block shown in Fig. 7, which is a translinear amplifier adapted from [33]. The circuit operation can be analyzed by using the translinear principle [34], [35]:

$$V_{\rm low} - V_{GS1} - V_{GS4} + V_R + V_{GS3} + V_{GS2} = V_{\rm high} \tag{6}$$

Since the current through M2 and M4 is the same, their corresponding V_{GS} must also be the same. A similar argument holds for M1 and M3, resulting in:

$$V_{GS2} = V_{GS4}, \qquad V_{GS1} = V_{GS3} \tag{7}$$

Using the results of Eq. 7 in Eq. 6 gives the result:

$$V_R = V_{\rm high} - V_{\rm low} \tag{8}$$

$$i_R = \frac{V_{\rm high} - V_{\rm low}}{R} \tag{9}$$

The current $I_{\rm bias} + i_r$ is mirrored to the output, and transistor $M_{\rm sub}$ is biased to subtract $I_{\rm bias}$, leading to:

$$I_{\rm ctrl} = i_R = \frac{V_{\rm high} - V_{\rm low}}{R} \tag{10}$$

Shown in Fig. 8 is a plot of simulated performance of the voltage-to-current converter. It shows the output current ($I_{\rm ctrl}$) versus differential input voltage. $V_{\rm low}$ is held at 500 mV while $V_{\rm high}$ is swept from 500 mV to 512 mV, corresponding to the expected maximum average inductor voltage drop of 12 mV in our application. Also shown is a linear least-squares estimate, illustrating the good linearity of the converter. We can characterize the converter by its voltage to current coeffi-

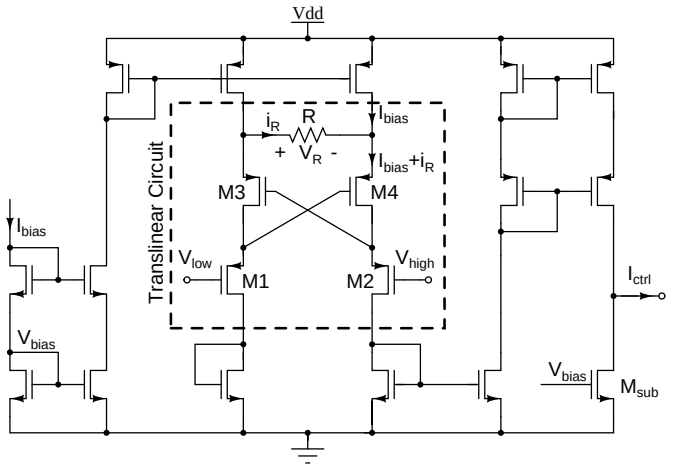

Fig. 7. Schematic diagram of differential voltage to single-ended current converter used as the first stage of the ADC architecture of Fig. 6.

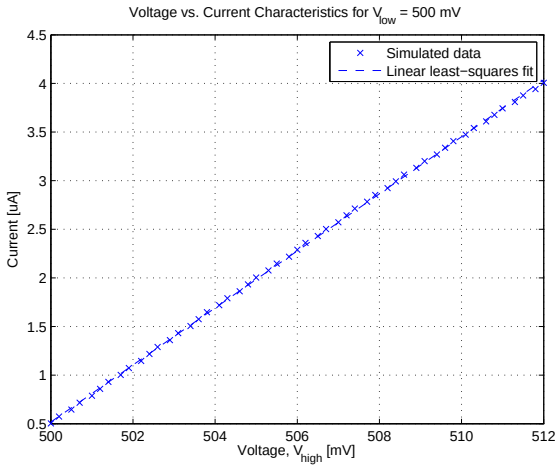

Fig. 8. Plot showing simulated performance of the voltage to current converter of Fig. 7, together with a linear least-squares estimate. $V_{\rm low}$ is held at 500 mV while $V_{\rm high}$ is swept from 500 mV to 512 mV, corresponding to the expected maximum average inductor voltage drop.

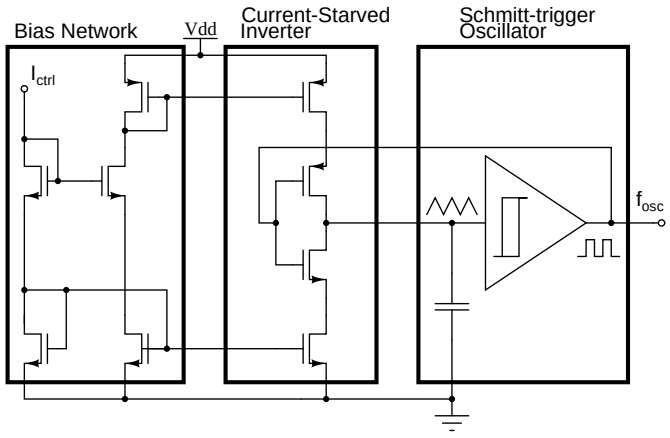

Fig. 9. Schematic diagram of current-controlled oscillator used in ADC architecture of Fig. 6

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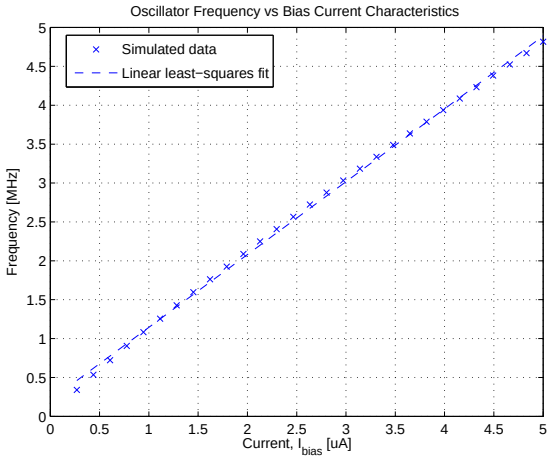

Fig. 10. Plot showing simulated control current to frequency relationship of the Schmitt-trigger-based oscillator of Figure 9. Also shown is a linear approximation for the relationship.

cient, $K_{vi} = \frac{dI}{dV}$. In this example, K_{vi} is approximately 0.293 $\mu A/mV$. Much care was taken in the design of the converter to minimize linearity errors. For this reason, the transistor $M_{\rm sub}$ is not set to subtract the entire 5 μA bias current, but only 4.5 μA to increase linearity, as determined by simulation.

2) Current-controlled oscillator: The output current of the converter of Fig. 7 is used to control the frequency of the current-controlled oscillator of Fig. 9. It comprises a bias network, current-starved inverter, an on-chip capacitor, and a Schmitt trigger to produce a square-wave output voltage whose frequency is dependent on the input current.

The oscillation frequency is given by:

$$f_{osc} = \frac{I_{\rm ctrl}}{2\Delta V_{\rm Schmitt} C_{\rm osc}}, \tag{11}$$

where $\Delta V_{\rm Schmitt}$ is the hysteretic voltage of the Schmitt trigger (which thus sets the amplitude of the triangle waveform), and $C_{\rm osc}$ is the capacitor value. The resulting waveform has a duty cycle of approximately 50%, owing to the fact that the charge and discharge transistors of the current-starved inverter are biased by the same current.

By changing the bias current, the oscillation can thus be controlled in a linear matter. Since $C_{\rm osc}$ and $\Delta V_{\rm Schmitt}$ are determined at design time, they can be combined into a single coefficient, K_{if} yielding the relationship

$$f_{osc} = K_{if} I_{bias}.$$

Figure 10 shows a simulated plot of the frequency versus control current characteristics for the Schmitt trigger oscillator, together with a linear least square error fit. From this, we we can deduce the proportionality constant K_{if} to be approximately 0.94 MHz/μA. We also see from the plot that the frequency and bias current are very well approximated by a linear relationship. In this simulation (and in the experimental prototype), $C_{\rm osc}$ has a value of 273 fF, and the Schmitt trigger oscillator has a hysteretic voltage value of 1 V.

C. Digital Counter

The output of the current-controlled oscillator (f_{osc}) is fed into a digital counter to produce a value proportional to the

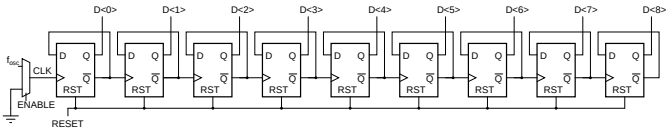

Fig. 11. Schematic diagram of the digital counting stage used in the ADC architecture of Fig. 6.

differential input voltage. A schematic drawing of the 9-bit digital counter is shown in Fig. 11. The counter is resettable via the RESET command, followed by an ENABLE command that begins the counting phase.

The relationship between the count K, and our other parameters is given by:

$$K = (V_{\text{high}} - V_{\text{low}})K_{vi}K_{if}T_{sample},$$

where T_{sample} is the sampling time[1], and the other parameters are as described previously. K_H denotes the count observed for the highest inductor current (400 mA in this application), and K_L by the count corresponding to the lowest inductor current (0 mA). T_{sample} must then be chosen such that $K_H < 512$ (for a 9-bit counter) to prevent counter overflow. To keep the counter (and subsequent logic elements) relatively small, it is also desirable to keep K_H as small as possible, given the constraint above. While it is tempting to try to design the system such that K_H is 512 and K_L is 0, this should typically be avoided, as it implies that the voltage to current converter needs to be linear all the way down to zero current, which is very difficult to achieve in practice.

In the TPV system, the largest expected inductor ESR is 30 mΩ, corresponding to a maximum average expected inductance voltage drop of 12 mV. From Figs. 8 and 10 it can be observed that this corresponds to a maximum expected control current of 4 μA, corresponding to a frequency of 4 MHz. However, since Figs. 8 and 10 were generated from typical transistor models under room temperature conditions, the maximum frequency under 80° C, with fast-fast corner transistors was also determined. Through simulation, a maximum frequency of 4.3 MHz was observed in that case, which will determine the appropriate sample time to ensure that the counter does not overflow. The maximum sample time for a 9-bit counter is thus:

$$T_{sample} = \frac{K_H}{f_{osc,max}} = \frac{512}{4.3} = 119\,\mu s. \qquad (12)$$

A sampling time of 119 μs will correspond to an approximate K_L of 60, giving our ADC an effective resolution of $K_H - K_L = 512 - 60 = 452$. It should be pointed out that it is possible (through careful fine-tuning) to achieve an effective resolution of 9-bit in this ADC, despite the non-zero frequency associated with a zero voltage drop across the inductor. Implementing resistive dividers used to sample V_{high} and V_{low} to provide a slight negative differential voltage would have the effect of decreasing K_L all the way to zero, if desired. While the non-linearity would suffer at very low counts, this may be a desirable trade-off, in particular if high resolution at higher currents is important.

[1]If possible, it would be preferable to make T_{sample} an integer number of switching periods to help cancel out the effect of the residual ripple. This is similar to the 60 Hz noise canceling technique commonly used in dual-slope ADCs. In this work, the sampling times is controlled from off-chip, so the added timing complexity of integer sampling made this a less attractive option.

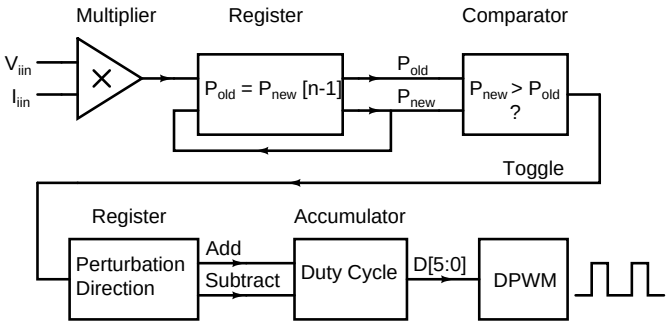

Fig. 12. Block diagram illustrating digital implementation of the Perturb and Observe MPPT algorithm.

In our TPV MPPT experimental prototype, we provide the sampling clock externally, to enable a wide range of tunable ADC resolutions for a variety of inductor ESRs and output powers. The digital counter was implemented using low-voltage transistors in the 0.35 μm process, which can operate at substantially higher frequencies than the maximum 4.3 MHz used here, if desired.

D. Digital Logic

The MPPT algorithm was implemented in digital logic, and Fig. 12 shows a block diagram of the key components. The current and voltage measurements are provided as 9-bit values from the ADC, and the digital multiplier calculates the corresponding input power. This power is then compared to the last power sample, and if it is smaller, the perturbation direction is changed. Depending on the direction, the digitally-stored duty cycle command is either incremented or decremented in the accumulator, and the duty cycle command is translated to a time-domain waveform by the digital pulse-width modulator.

Through appropriate choice of sampling time and resistor dividers, the ADC and digital logic described in this work can be employed in a variety of output power applications. For the parameters calculated here, an expected power converter range of 0-500 mW with an effective sensing resolution higher than 8 bits can be achieved.

E. Digital Pulse Width Modulator

The digital pulse width modulator (DPWM) of Fig. 13 is used to convert the digital code held in the accumulator (of Fig. 12) to a series of pulses of the correct width to drive the gates of the power MOSFETs. The design is a counter-based solution, which ensures monotonicity and achieves good linearity, while keeping the implementation area low. The frequency is controlled by an external bias current, which is fed to a current-to-frequency-converter (using the same design as the current-controlled oscillator of Fig. 9). The resulting high ($\sim$ 128 MHz) frequency clock is fed to a 9-bit counter (using the same design as the digital counting stage for the

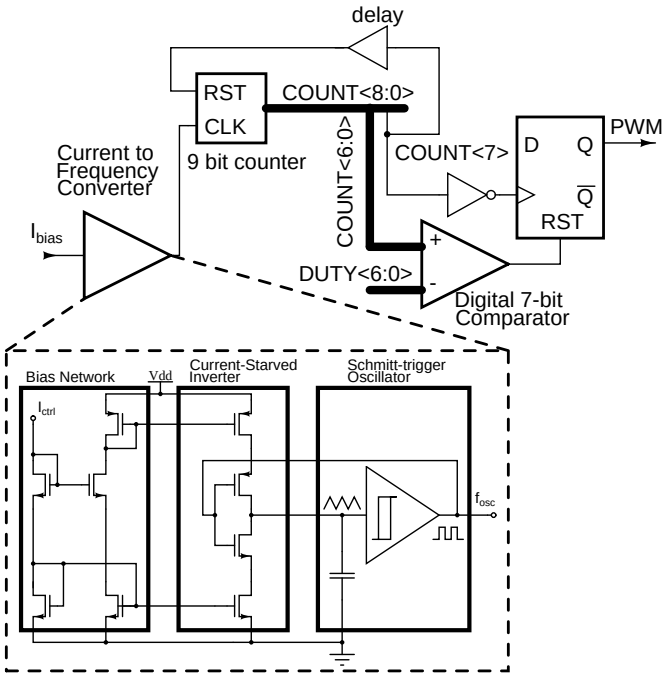

Fig. 13. Schematic drawing of the counter-based digital pulse-width modulator implementation.

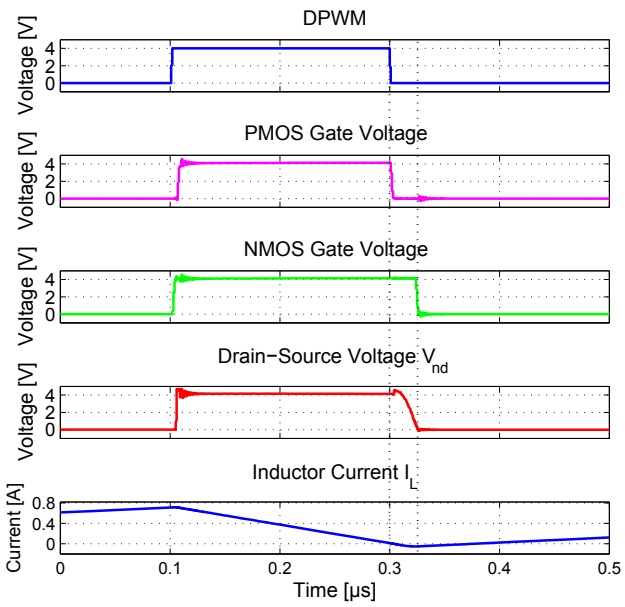

Fig. 14. Simulated waveforms to illustrate soft-switching operation. V_{in} = 0.9 V, V_{out} = 4 V and P_{out} = 300 mW.

ADC, shown in Fig. 11). The 7 lowest order bits from the counter is connected to a 7-bit comparator, which compares the counter output to the 7-bit duty code that the MPPT logic outputs. When the count exceeds the duty value, the output of the comparator is triggered, which resets the flip-flop. Whenever the counter has counted up to 128 (COUNT<7> goes high), the counter is reset, and the edge-triggered flip-flop sets its output (Q) high, so that the PWM output is high until the 7-bit comparator resets it again. Because of the relatively low switching frequency and DPWM resolution (6-bit), the power consumption of the DPWM can be kept low. (Unlike in other applications such as [36]–[38], where a high effective resolution is demanded, the P&O tracking algorithm actually operates based on measurable steps in operation.) At a switching frequency of 1 MHz, the estimated (from simulation) power consumption of the DPWM is 0.45 mW.

V. Power Stage

The power stage of the TPV tracking system is an integrated synchronous dc-dc boost converter. In the maximum power operating condition, it converts 0.8-1.3 V from the output of the TPV cell to 3.6-4.2 V for battery charging. A TSMC 0.35 μm thick oxide device process is used to provide 5 V blocking voltage capability. Since the maximum power output of the TPV cells is approximately 300 mW (as seen in Fig. 2), the device sizes and gate driver taper factor are optimized for this power level, to balance the capacitive switching loss and conduction loss [39]. The IC power stage is designed to be flexible, enabling operation at switching frequencies to beyond 1.5 MHz, and with either hard-switching or high-ripple soft-switching operation [40], [41].

Since the converter will operate at the optimal power output condition of the TPV unit most of the time, the system only needs to operate efficiently over a relatively narrow power range. In other words, while conventional power converters are often tasked with operating over the full range of no-load to full load, our MPPT converter will always operate at or near the peak power of the TPV module. While the power levels of individual TPV modules are expected to differ by as much as 30% due to the non-uniform irradiation, this power range is still sufficiently narrow to explore soft-switching operation, at least for parts of the output power range. This opens up the possibility of using high-ripple zero-voltage-switching (ZVS) soft-switched operation. Figure 14 shows sample soft-switching waveforms of this mode of operation.

If the inductor current i_L has peak-to-peak current ripple over 200% of the average current, soft-switching can be implemented [42]–[44]. After the high-side device is turned off and before the low-side device is turned on, the inductor current will discharge the drain-source capacitance of the low-side device and charge the capacitance of the high-side device. The converse can likewise be made to happen on the other transition. By adjusting the dead-times between the switching of the two devices carefully, ZVS can be achieved at the turn-on transition for both devices.

In this paper, self-adjusted digital dead-time control circuitry is introduced. This self-adjusted dead-time control circuit has several advantages, including simplicity, low power consumption, fast response to changes in operating condition, and the ability to extend the soft-switching operation range as compared to fixed dead-time control. Figure 15 shows a simplified schematic of the dead-time control circuit. The self-adjusted dead-time circuit controls the dead-time based on the voltage level at the drain of the low-side device, V_{nd}. The low-side device will only be turned on once voltage V_{nd} drops below the dead-time logic threshold. Likewise, the high-side device will only be turned on after voltage V_{nd} rises above the dead-time threshold level for the high-side device turn-on.

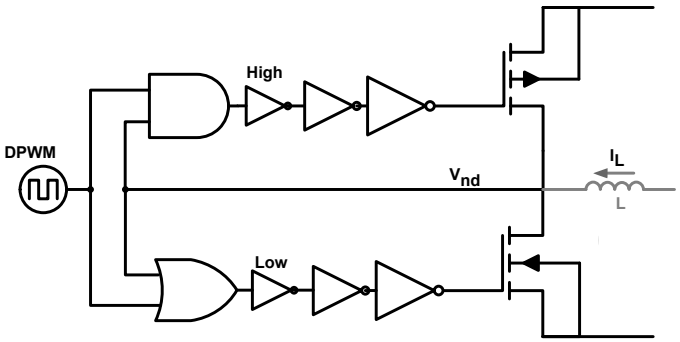

Fig. 15. Simplified schematic drawing of the self-adjusted dead-time control circuit used to achieve ZVS. Additional logic ensures switching even when soft switching is not realized.

A Schmitt trigger is used to set the upper and lower switching threshold voltages and also provide stability improvement.

To address operating conditions when ZVS switching will not occur, an additional 28 ns dead-time limit is set. This enables hard-switching operation to be employed if desired, and also ensures correct operation under conditions (such as transients) that disrupts soft-switching operation. (This window size is determined by the longest required dead-time for ZVS with minimum inductor current ripple.)

The power stage design is compatible with both soft and hard switching operation. The final optimized size (device width) for the NMOS transistors is 118000 μm, and for the PMOS transistor is 121000 μm. A taper factor of 11 is chosen for the gate drivers to balance the gate drive loss and switching loss of the power devices. The dead-time control logic and gate drivers are powered by the output of the converter.

VI. Experimental Results

The TPV tracking system was fabricated in a TSMC 0.35 μm CMOS process and mounted in a QFN40 package. An annotated die photo of the converter is shown in Fig. 16, and approximate silicon area breakdown is presented in Table I. The converter specifications are shown in Table II, and Fig. 17 shows an annotated photograph of the PCB test-board used in this experiment. Note that the micro-controller shown in the photograph was not used for direct control of the CMOS converter, but rather used to load operating parameters, disable/enable signals, as well as provide external timing to the converter over a serial interface. As discussed below, many different inductors were experimentally tested. The photograph of Fig. 17 shows the largest inductor, the SER1360 from Coilcraft. More detailed schematic drawings and component listings for the converter can be found in [29].

A. Power Stage Characterization

Shown in Fig. 18 are experimental waveforms of the converter which illustrate soft-switching operation using a 0.9 μH inductor with 11-120-P material, and operating at an input voltage of 0.9 V, an output voltage of 4 V, and an output power of 300 mW. Hard-switching waveforms are also as would be expected. Measured converter efficiencies for various power and voltage levels are shown in Fig. 19 for one power-stage

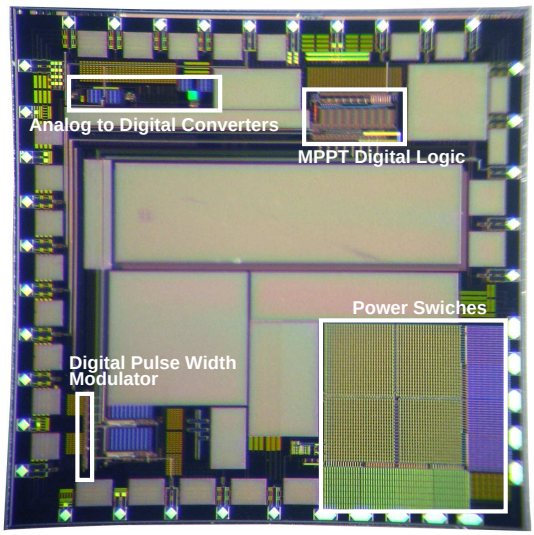

Fig. 16. Annotated die photo of the maximum power point tracker implemented in a 0.35 μm CMOS process. Total die area is 4x4 mm, with approximately 1.16 mm^2 of active area (see Table I for more details regarding area breakdown).

TABLE I
Converter Area Breakdown

Component	Area [mm^2]
ADCs (2)	0.083
Analog Bypass Capacitors (oversized)	0.131
MPPT Logic	0.192
DPWM	0.031
Digital Decoupling Capacitors (oversized)	0.134
Power Devices	0.752
Gate Drives	0.061
Dead-time Control	0.040
Output Capacitor	1.21
Total Active Area	1.159
Total Capacitor Area (oversized)	1.475

implementation under hard-switched conditions. It can be seen that the converter has a peak efficiency of 95.4% with V_{in} = 1.3 V, V_{out} = 4 V and output power of 300 mW. While the main loss components are from switching, conduction, and inductor loss (core and conduction), the control losses are also important to consider, in particular for low power operation. The estimated (from simulation) DPWM power consumption is 0.45 mW/MHz, and the ADC converter power

TABLE II
Converter Specifications

Input Voltage Range	0.8-1.3 V (1 V Nominal)
Output Voltage Range	3.6-4.2 V (4 V Nominal)
Nominal Output Power	300 mW
Switching Frequency	500 kHz
Converter Peak Efficiency	95.4%
Tracking Efficiency	>98%

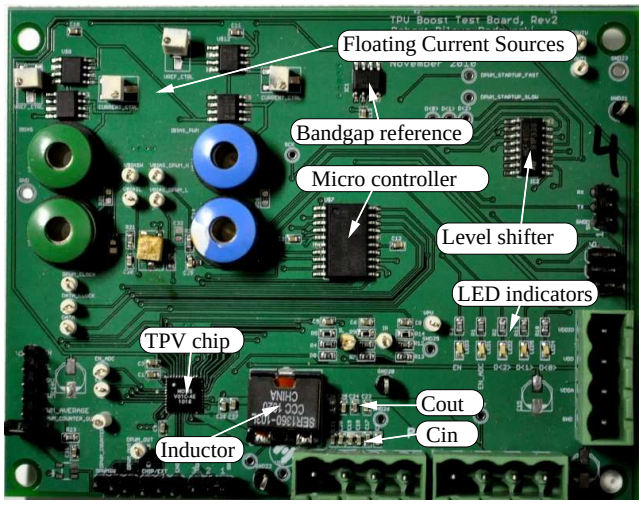

Fig. 17. Annotated photograph of printed circuit board used for testing the MPPT power converter.

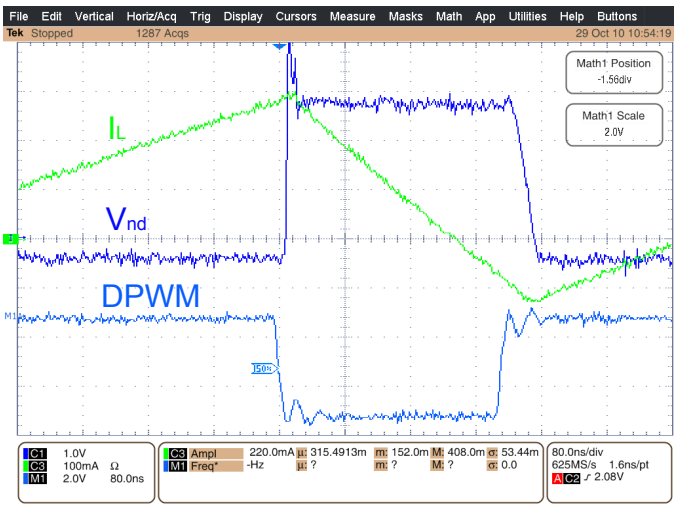

Fig. 18. Experimental waveforms of the power stage drain voltage and inductor current, as well as the DPWM signal. The dead-time control circuitry adjusts the timing of the gate signals to achieve ZVS. In this example, the input voltage is 0.9 V, the output voltage is 4 V, the inductor value is 0.9 μH, and the output power is 300 mW.

losses (current and voltage sensing) are measured to be 1.88 μW at an MPPT update interval of 100 ms.

With the low output power and requirements of small size and high efficiency in this work, inductor size and converter performance trade-offs become important, especially as inductor size dominates the overall size of the converter (for most design conditions). Figure 20 shows the measured converter performance for different frequencies, inductor designs and operating modes with a nominal input voltage of 1 V, output voltage of 4 V and output power of 300 mW. Note that the legend describes whether soft-switching (ss) or hard-switching (hs) mode was employed. A picture of some of the inductors used in the experimental measurements is shown in Fig. 21. For reference, the TPV converter chip and a US penny are also shown in the picture, as well as a cm-scaled ruler.

As part of evaluating our system, we undertook a detailed

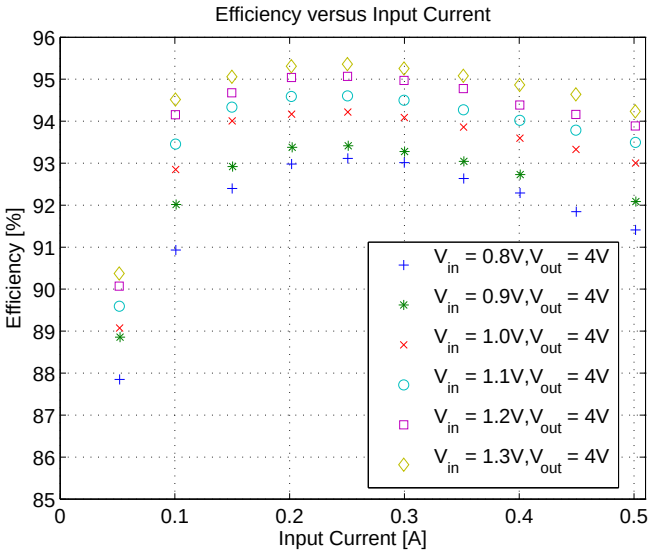

Fig. 19. Plot of measured power stage efficiency in hard-switching operation at f_{sw} = 500 kHz. Input capacitance is 4 μF, output capacitance is 4.8 μF, and the power inductor is 8 μH wound on a P9/5 3F3 core with 3 $\times$ 28 AWG.

study of achievable efficiency as a function of inductor size, switching frequency and operating mode (hard switching vs. soft switching). This included modeling of system losses for numerous designs (using loss models of commercial inductors along with detailed models of our own converter IC) and experimental validation of a subset of designs. We considered operation at frequencies from 500 kHz to 1.5 MHz, with inductance values selected for both soft- and hard-switching operation.

At higher operating frequencies, designs can effectively use either high-permeability core materials or low-permeability core materials. An advantage of some low-permeability materials (e.g., NiZn ferrites) is that the effect of core loss can be reduced to an extent, benefiting the use of high-ripple soft switching. As illustrated in Fig. 20, at the lowest inductor volumes tested ($\approx$ 80 mm^3), the achieved experimental efficiencies with soft switching and hard switching were very close. (The soft-switched design operated at 1.5 MHz, while the hard switching design of comparable efficiency operated at a reduced frequency of 1 MHz; considering only 1.5 MHz operation, soft switching was superior by more than 2% in efficiency.) However, our models suggest that with an appropriate customized low permeability core material (relative permeability of 20-30), a soft-switched implementation could perform significantly better than a hard-switched implementation at frequencies above 1 MHz. (Our experimental results were limited to available commercial cores, and did not include an appropriate custom core material.)

Figure 22 shows calculated converter efficiency as a function of inductor size for a wide variety of commercial cores and inductance values, for both hard and soft switching. Figure 23 overlays these calculated results with the experimental results from Fig. 20. It can be seen that the measured experimental results all fall in to the range expected from

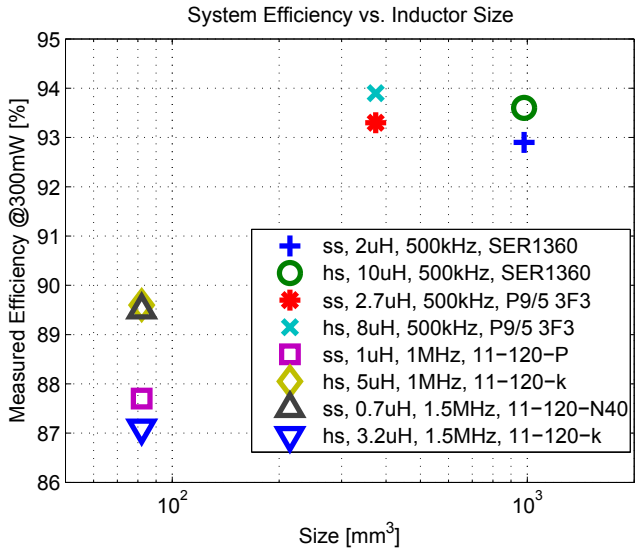

Fig. 20. Measured converter efficiency for various inductor sizes and values. Inductors are wound on selected available cores. "hs" stands for hard-switching and "ss" stands for soft-switching. Operation is for V_{in} = 1 V, V_{out} = 4 V, and P_{out} = 300 mW.

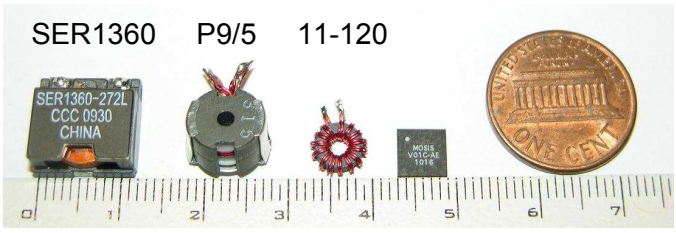

Fig. 21. Picture of some inductors used for the experiment. The packaged TPV converter chip and a US penny are shown for size reference, together with a cm-scale ruler.

model calculations. Consequently, Figs. 20, 22, and 23 show the frontier of inductor size vs. conversion efficiency, at least for the types of core materials and inductor designs evaluated.

B. Tracking Performance

Shown in Fig. 24 is the result of an experimental verification of the digital MPPT implementation and the ADC in isolation, without the power stage considerations. In this experiment, the differential input to the current-sensing ADC was externally generated with a DC bias current through a resistance of value similar to that of the investigated inductors. The resulting voltage drop across the resistor, ΔV, is shown on the y-axis of the bottom plot of Fig. 24. By adjusting the bias current, the performance of the MPPT circuitry and current sensing ADC can be investigated, where the converter duty cycle (shown on the y-axis on the top plot of Fig. 24) should change in accordance with the relative change of sensed current. As can be seen in Fig. 24, the duty cycle code continues to decrease as long as the sensed current (ΔV) increases, up until sample time 5, where the current has been manually decreased. At this time, the MPPT algorithm changes direction of the perturbation, as can be seen by the increase in duty cycle code at this time. Similarly, at sample time 6 the sensed current has decreased further, again initiating a change in the direction of

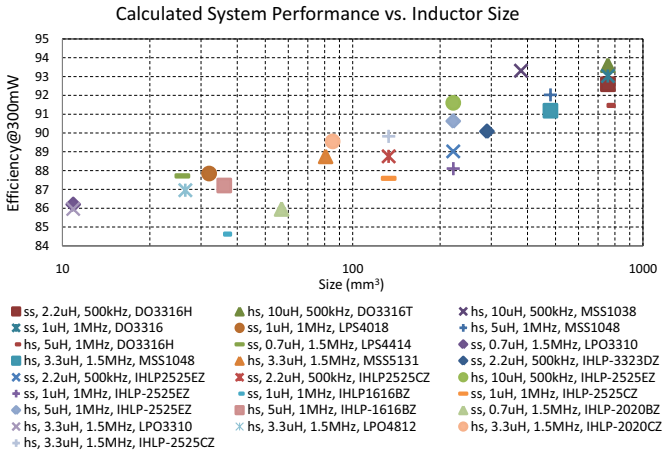

Fig. 22. Calculated converter efficiency versus inductor sizes. All inductors are commercially available from Coilcraft and Vishay. "hs" stands for hard-switching and "ss" stands for soft-switching.

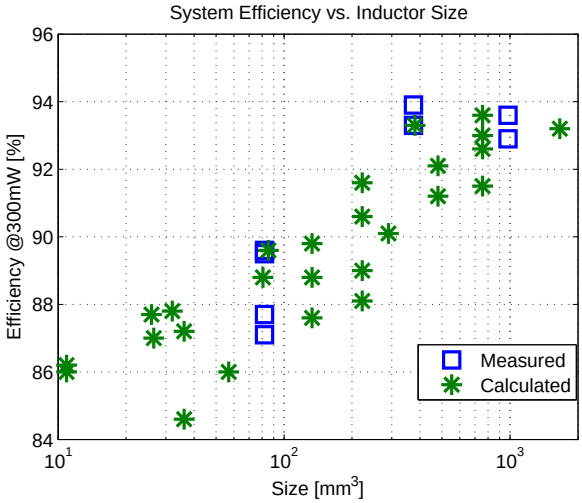

Fig. 23. Measured and calculated converter efficiency versus inductor sizes. The measured results agree well with calculated values. Operation is for V_{in} = 1 V, V_{out} = 4 V, and P_{out} = 300 mW.

perturbation of the MPPT algorithm. For the remaining sample times, the sensed current is continuously increasing, leading to no further changes in duty cycle perturbation direction. It should be noted that the sample times in this experiment were increased to enable accurate voltage sensing by the instruments, as well as duty cycle code read-out from the IC at each interval.

To evaluate the performance of the peak power tracker under repeatable conditions, the converter was attached to two crystalline Silicon series-connected solar cells illuminated by a halogen lamp to produce I-V characteristics similar to that produced by the micro-burner. This enabled characterization of the converter without the added complexity of the micro-reactor dynamics. The micro-reactor hardware is still being refined, and performance depends on several factors which are difficult to control for (e.g., reactor age, fuel contaminants, vacuum quality). In order to ensure repeatable and careful characterization of the MPPT solution alone, we performed all

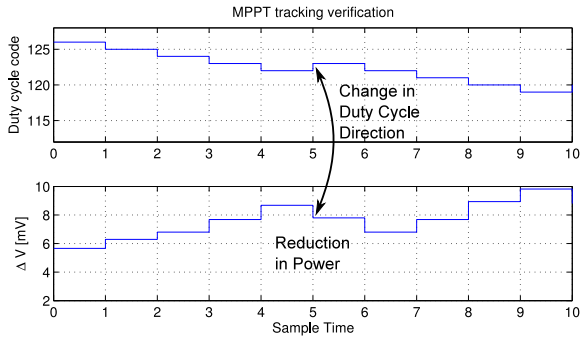

Fig. 24. Experimental verification of the MPPT circuitry and ADC operation, with sensed current adjustment. The duty cycle perturbation changes direction each time the sensed current (ΔV) is decreased.

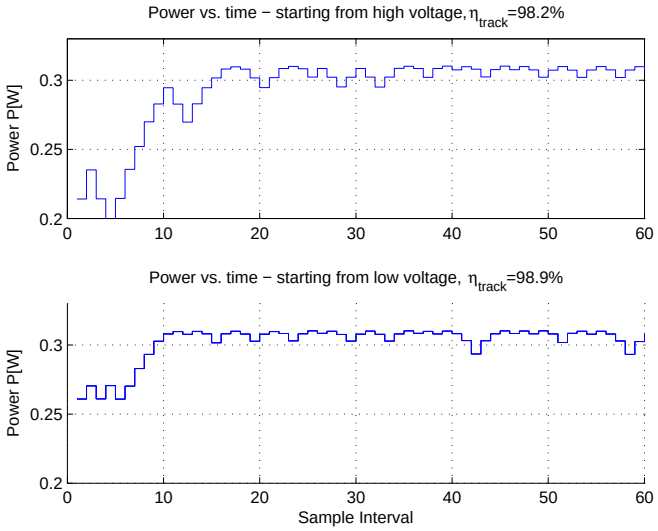

Fig. 25. Time-domain plot of the converter input power, showing maximum power point tracking.

experimental testing on a source with carefully matched characteristics. We note that full experimental testing of a discrete MPPT implementation together with a complete micro-reactor setup has been presented in [7].

Shown in Fig. 25 are plots of power versus time, illustrating the peak power tracker performance. In the top plot, the tracker is started with a duty cycle set to operate at a voltage that is higher than V_{mpp}. The bottom plot shows the corresponding data when the starting voltage is set below V_{mpp}. In both cases, the converter correctly finds the maximum power point and tracks it to within the resolution of the duty cycle command and the noise in the power measurement. The tracking efficiency, η_{track}, is a measure of how precisely the MPP is tracked, and is given by: $\eta_{\text{track}} = \frac{\langle P_{in} \rangle}{P_{MPP}}$, and is above 98% in both cases in Fig. 25. The update interval of the MPPT algorithm was 1 s, which was chosen to allow careful and time-synchronized measurements of all voltages and current with precision instruments (Agilent 34410A). The update interval of the MPPT converter in conventional operation can be chosen to be in the kHz range, and is primarily limited by the ADC conversion time.

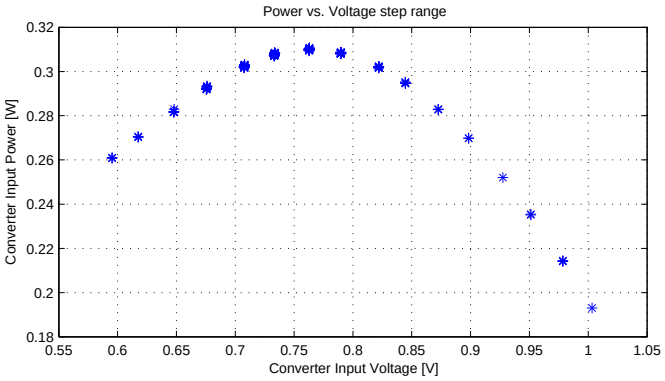

Fig. 26. Plot showing the power and voltage dependence of the experimental power source, using the same data as that which generated Fig. 25. The voltage step-size is limited by the resolution of the digital pulse-width modulator.

Fig. 26 shows a plot of converter input power versus input voltage, which illustrates the I-V characteristics of the source, which is similar to the plot shown in Fig. 2. In addition, the discretization of the input voltage illustrates the finite achievable voltage step-size. The minimum step size is limited by the resolution of the digital pulse-width modulator. The experimentally measured convergence regions of the MPPT converter is V_{in}=0.5-1.4 V, V_{out}=3.0-4.2 V, which is well within the expected operating parameters of both the source (TPV module) and load (Li-Ion battery). This convergence region was determined experimentally with little consideration given to improving upon it. It is, however, possible that the convergence region can be further extended by suitable adjustments of bias currents and sample intervals for the ADC.

C. Tracking Efficiency Analysis

An important consideration for MPPT converters is the tracking efficiency. In practice, one must consider two main sources of errors, static and dynamic.

1) Static Errors: Static errors in turn can be attributed to two causes. The first source is constant errors in current or voltage sensing, which can cause the converter to operate around an incorrect steady-state operating point. These types of errors are most often caused by offsets in voltage or current measurements, but can generally be avoided to a large degree by proper design choices. The other source of static errors is that associated with the resolution of the current/voltage sensing, as well as the pulse-width modulation. While these errors are generally easy to quantify in digital implementation (as quantization noise and DPWM resolution, respectively), it should be noted that they also exist in purely analog implementations, where noise limits of sensing and PWM generation still limits the achievable tracking efficiency.

2) Dynamic Errors: Another important consideration is the dynamic performance of the MPPT converter. In situations where fast transients occur (e.g., solar PV applications) [45], [46], it is important that the converter can quickly converge to the new steady-state operating point. In the application considered here the tracking speed is expected to be less important, considering the relatively static behavior of the radiation source.

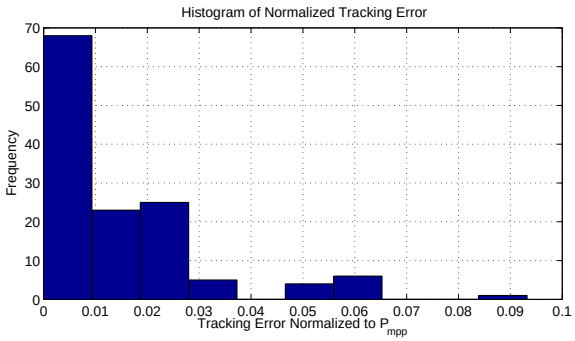

Fig. 27. Histogram of normalized (to P_{MPP}) tracking error, showing the statistical distribution of MPPT operation.

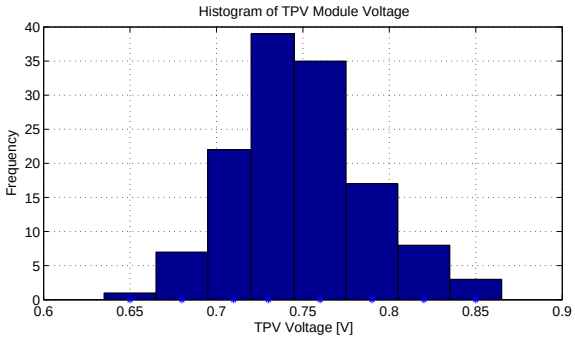

Fig. 28. Histogram of TPV voltage during stead-state MPPT operation. It can be seen that the converter operates around the MPP voltage for the majority of the time, with occasional error-induced operation at voltages further away from the MPP.

In order to better quantify the tracking performance, Figs. 27 and 28 were generated from measured MPPT data. Shown in Fig. 27 is a histogram of normalized (to P_{mpp}) tracking error. For steady-state MPPT operation, the quantity $\frac{P_{MPP}-P_{in}}{P_{MPP}}$ was computed at each MPPT update interval, where P_{in} represents the measured input of the MPPT converter (i.e., the TPV output power), and P_{MPP} represents the measured maximum power point of the TPV cell. For this experiment, the irradiation of the TPV module was held constant. The statistical distribution of Fig. 27 thus captures the static error caused by noise, including quantization (ADC and DPWM) and injected noise by the switching action of the power stage. As can be seen from this plot, the majority of time the MPPT operates with an error of less than 1%, but at times the error can be larger. The larger errors are most likely caused by repeated switching noise injected at the time of ADC sampling, which would cause the MPPT to make repeated incorrect decisions. As can be seen from the distribution, however, this occurs with very low frequency.

Shown in Fig. 28 is a histogram of TPV module voltage, when the MPPT converters are operating in steady-state for the same experiment as that used to generate Fig. 27. Again, the PWM quantization and error induced by ADC quantization errors and switching-induced noise can be observed. However, the majority of time is spent at voltages near V_{MPP}.

D. Performance Comparison

Shown in Table III is a comparative listing of CMOS integrated MPPT converters with similar operating conditions. While the specific application and design considerations for each solution makes it difficult to directly compare the relative performances of these cases, we note that our implementation compares well with existing solutions in terms of MPPT tracking efficiency and power conversion efficiency.

VII. Conclusion

A fully integrated maximum power point tracking system developed in 0.35 μm CMOS is presented. A low power custom-designed ADC suitable for lossless current sensing is utilized to achieve very low control losses, together with a digital implementation of a peak power tracking algorithm. The integrated boost power stage can be configured to employ either soft-switching techniques to achieve high efficiency operation while operating at high switching frequencies, or hard-switching operation for efficient operation at lower switching frequencies. Achievable efficiency versus passive component size is explored; power stage efficiencies above 95% are demonstrated, and MPP tracking efficiency of above 98% is demonstrated.

Acknowledgments

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TABLE III
PERFORMANCE COMPARISON TO OTHER CMOS INTEGRATED MPPT CONVERTERS

Reference	This work	[47]	[48]
CMOS Process	0.35 μm	0.35 μm	0.35 μm
Application	TPV	PV	PV
Input Voltage Range	0.8-1.3 V	0.5-2 V	1.5-5 V
Output Voltage	3.6-4.2 V	4.2 V	0-4 V (buck, below V_{in})
Power Rating	300 mW	500 mW	800 μW
MPPT Algorithm	P&O	Sectored Hill-Climbing	SAR MPPT
MPPT Implementation	Digital	Digital	Analog
MPPT Efficiency	98.9%	N/A	84.3%
Peak Conversion Efficiency	95.4%	89%	N/A
Switching Frequency	500 kHz-1.5 MHz	500 kHz	500 kHz

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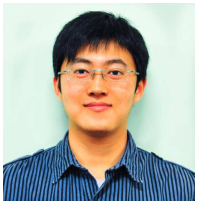

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