Design of Class E Resonant Rectifiers and Diode Evaluation for VHF Power Conversion

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***Abstract*—Resonant rectifiers have important applications in very-high-frequency (VHF) power conversion systems, including dc-dc converters, wireless power transfer systems, and energy recovery circuits for radio-frequency systems. In many of these applications, it is desirable for the rectifier to appear as a resistor at its ac input port. However, for a given dc output voltage, the input impedance of a resonant rectifier varies in magnitude and phase as output power changes. This paper presents a design methodology for class E rectifiers that maintain near-resistive input impedance along with the experimental demonstration of this approach. Resonant rectifiers operating at 30 MHz over 10:1 and 2:1 power ranges are used to validate the design methodology and identify its limits. Furthermore, a number of Si Schottky diodes are experimentally evaluated for VHF rectification and categorized based on performance.**

I. Introduction

Resonant rectifiers have important applications in power conversion systems operating at frequencies above 10 MHz. Applications for these circuits include very-high-frequency dc-dc converters [1-8], wireless power transfer systems [4,9,10], and energy recovery circuits for radio-frequency systems [5,6]. In many of these applications, it is desirable for the rectifier to appear as a resistive load at its ac input port. For example, in some very-high-frequency dc-dc converters, proper operation of the inverter portion of the circuit can depend upon maintaining resistive (but possibly variable) loading in the rectifier stage. In still other applications it is desired to have an input impedance that is resistive and approximately constant across operating conditions [5,6]; this can be achieved by combining a set of resonant rectifiers having variable resistive input impedances with a resistance compression network [5,7-10]. In all these systems, however, it is desirable to maintain resistive input impedance of the rectifier as the operating power varies.

Resonant rectifiers have been explored in a variety of contexts [9-25]. The traditional design of a class E rectifier, or shunt-loaded resonant rectifier, utilizes a (large) choke inductor at its output and does not provide near-resistive input impedance [3,11]. This paper introduces a design method for realizing class E rectifiers that provide near-resistive input impedance over a wide range of output power levels. Experimental validation of the proposed method is also provided along with its limitations. The selection of a diode is also critical in very high frequency (VHF) designs (30-300 MHz), as the performance of many diodes degrades as switching frequency increases [12,26]. This phenomenon is also explored in this paper through evaluation of different commercial diodes.

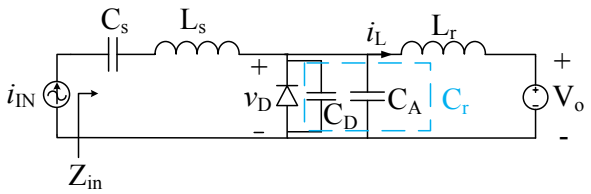


Figure 1. Class E resonant rectifier driven by a current source. In this model, intrinsic capacitance C_D plus external capacitance C_A form a total capacitance C_r.

Section II of the paper presents an analysis of the operation of the resonant class E rectifier. Section III presents a design methodology for class E rectifiers that yields resistive ac input impedance characteristics over a wide operating power range. The design equations are derived and solved numerically and a series of plots are provided that aid in the design process. Section IV demonstrates the application of the design methodology. Section V presents supporting experimental results. Resonant rectifiers operating at 30 MHz over 10:1 and 2:1 power ranges are developed and used to validate and identify the limits of the design methodology. Section VI explores the suitability of a variety of Si Schottky diodes for use in VHF resonant rectifiers. A number of commercially-available Si Schottky diodes are experimentally evaluated for VHF rectification and categorized based on performance. Finally, section VII concludes the paper.

II. Class E Rectifier Operation and Analysis

A class E resonant rectifier driven by a sinusoidal current source is shown in Fig. 1. Modeling the input source as a sinusoidal current source is appropriate for analysis purposes, as in most applications the source feeding the class E resonant rectifier is sinusoidal and/or the rectifier is provided with a high Q (Q > 3) series resonant tank at its input which makes the current nearly sinusoidal. In the proposed design the rectifier input series resonant tank is tuned on resonance at the desired operating frequency, with a sufficiently high loaded quality factor that the input current is substantially sinusoidal. Also, unlike many class E rectifier designs, we consider the case where the dc-side inductor L_r has substantial ac current ripple (and in fact has a carefully selected value as it resonates with the diode capacitance). As will be seen, such operation permits resistive ac-side input characteristics to be achieved over a wide power range. This is similar to the design of class E inverters for variable-load operation as described in [27,28]. Hence, for analysis the input source will be assumed to be of the form $i_{IN}(t) = I_{IN}\sin(\omega t + \phi)$ where I_{IN} is the amplitude of the input current, ω its angular frequency and ϕ its phase. Having a non-zero phase (ϕ) associated with the input current allows us to define the time axis in such a way that time t = 0 corresponds to the instant when the diode turns off.

The operation of the resonant rectifier is illustrated in Fig. 2, where we have assumed the diode to be ideal (excepting the diode capacitance, which is absorbed as part of the circuit operation). The diode capacitance is approximated as a single constant value C_D that is equal to the capacitance of the diode biased at the output dc voltage. We are able to disregard the effect of the input-side resonant tank as the input current is sinusoidal and the input network is tuned on resonance. The diode turns off when the current through it ($i_L - i_{IN}$) reaches zero (at t = 0). At this instant the capacitor across the diode starts charging with zero initial current. As a result the reverse voltage across the diode increases slowly with an initial d*v*/dt equal to zero. The diode turns on when the reverse voltage across it returns to zero at t = (1-D)T, where T = ($2\pi/\omega$) is the period of the ac drive current and D, the duty ratio, is defined as the fraction of the period the diode stays on.

The inductor current (i_L) waveform shown in Fig. 2 (e) differs from that of a traditional class E rectifier. In a traditionally-designed class E rectifier, a large inductor is used at the output so that the inductor current is nearly constant [9]. However, by relaxing this design constraint to allow a substantial ac current component in i_L, we open up the possibility of designing a class E rectifier with near-resistive input impedance. As the input filter network is tuned on resonance, the input impedance of the rectifier at the drive frequency is the ratio of the fundamental component of the diode voltage $v_D(t)$ (and input voltage) to the fundamental component of the input current $i_{IN}(t)$ (which has amplitude I_{IN}). Since v_D is non-sinusoidal, its fundamental component needs to be extracted from its waveform. For this purpose, we develop an analytical expression for the diode voltage waveform v_D. The diode voltage waveform across the full period is given by:

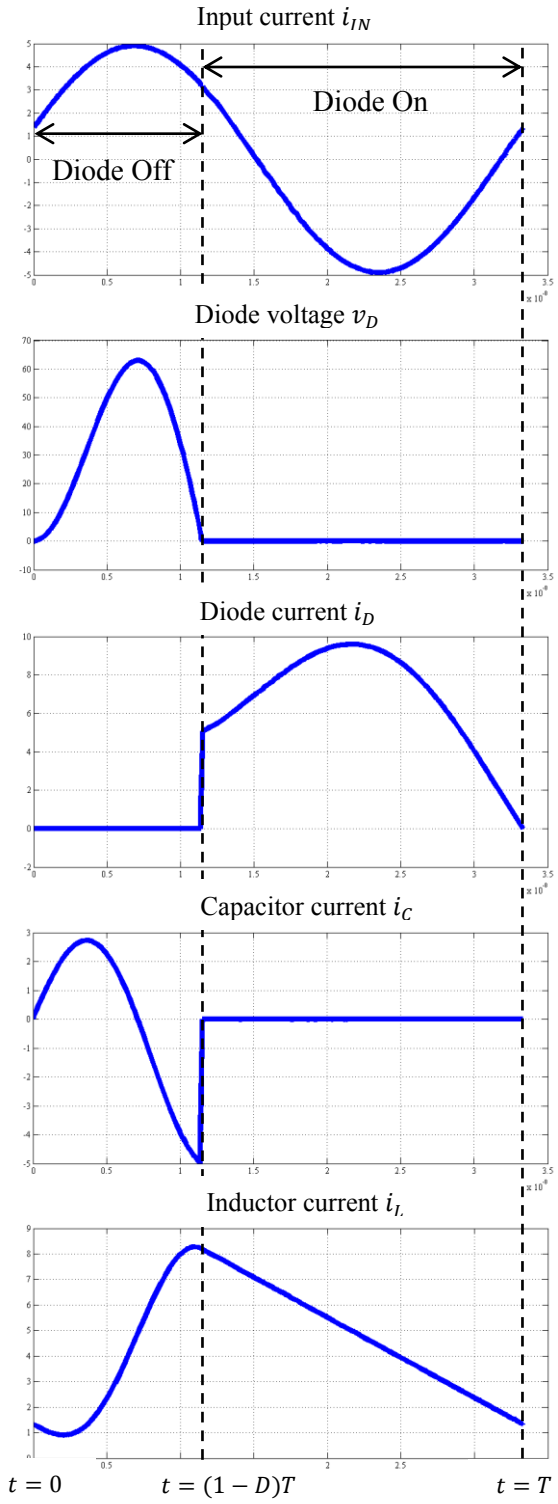


Figure 2. Class E resonant rectifier waveforms; from the top: (a) ac input current through L_s, (b) diode voltage, (c) diode current, (d) capacitor current, and (e) inductor L_r current.

$$v_D(t) = \begin{cases} \frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\Big[\sin(\omega t)\sin(\phi) - \frac{Z_r}{\omega L_r}\sin(\omega_r t)\sin(\phi) + \\ \cos(\omega_r t)\cos(\phi) - \cos(\omega t)\cos(\phi)\Big] - V_O\cos(\omega_r t) \\ -I_{IN}Z_r\sin(\omega_r t)\sin(\phi) + V_O \qquad \text{for } 0 \le \mathrm{t} \le (1-\mathrm{D})\mathrm{T} \\ 0 \qquad\qquad\qquad\qquad\qquad\qquad \text{for } (1-\mathrm{D})\mathrm{T} \le \mathrm{t} \le \mathrm{T}. \end{cases} \quad (1)$$

Here

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (2)$$

is the resonant frequency of the L_r-C_r resonant network and

$$Z_r = \sqrt{\frac{L_r}{C_r}} \quad (3)$$

is the characteristic impedance of the network.

The expression for v_D contains three unknowns: duty ratio[1] D, input current amplitude I_{IN} and input current phase ϕ. The values of these unknowns need to be determined before we can compute the fundamental component of v_D. For this we need to also develop an expression for the current in inductor L_r. To calculate the current, the circuit has to be analyzed in its off and on states. The inductor current i_L when the diode is off is given by:

$$i_{L,off}(t) = \frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}[\cos(\omega_r t)\sin(\phi) - \cos(\omega t)\sin(\phi) + \frac{\omega L_r}{Z_r}\sin(\omega_r t)\cos(\phi) - \sin(\omega t)\cos(\phi)\Big] - \frac{V_O}{Z_r}\sin(\omega_r t) + I_{IN}\cos(\omega_r t)\sin(\phi) \quad \text{for } 0 \le \mathrm{t} \le (1-\mathrm{D})\mathrm{T} \quad (4)$$

and the inductor current when the diode is on is given by:

$$i_{L,on}(t) = -\frac{V_O}{L_r}\left[t - \frac{2\pi(1-D)}{\omega}\right] + i_{L,off}\left(t = \frac{2\pi(1-D)}{\omega}\right) \quad \text{for } (1-\mathrm{D})\mathrm{T} \le \mathrm{t} \le \mathrm{T}. \quad (5)$$

In addition, the class E rectifier circuit of Fig. 1 must satisfy three constraints. The first constraint is that the diode voltage v_D has to be zero when the diode turns on. The second constraint is that the average value of v_D has to be equal to the output voltage V_o. The third constraint is that the average of inductor current i_L has to be equal to the output power P_o divided by the output voltage V_o. In summary:

$$v_D\left(t = \frac{2\pi(1-D)}{\omega}\right) = 0, \quad (6)$$

$$\frac{1}{T}\int_0^T v_D(\mathrm{t})\mathrm{dt} = V_o, \quad (7)$$

$$\frac{1}{T}\int_0^T i_L(\mathrm{t})\,\mathrm{dt} = \frac{P_o}{V_o}. \quad (8)$$

By applying these constraints to (1), (4) and (5), we can derive three independent equations in terms of the three unknowns (D, I_{IN} and ϕ) and ω, P_o, V_o, L_r and C_r[2]:

$$\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\Big[\sin(2\pi(1-D))\sin(\phi) - \frac{Z_r}{\omega L_r}\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + \cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\cos(\phi) - \cos(2\pi(1-D))\cos(\phi)\Big] - V_O\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right) - I_{IN}Z_r\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + V_O = 0, \quad (9)$$

$$\frac{1}{T}\Bigg[\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\Bigg[\frac{-\cos\left(2\pi(1-D)\right)\sin(\phi)}{\omega} + \frac{Z_r}{\omega\omega_r L_r}\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + \frac{\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\cos(\phi)}{w_r} - \frac{\sin(2\pi(1-D))\cos(\phi)}{\omega}\Bigg] - \frac{V_O}{\omega_r}\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right) + \frac{I_{IN}Z_r}{\omega_r}\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + V_O\frac{2\pi(1-D)}{\omega} - \left(\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\frac{-\sin(\phi)}{\omega} + \frac{Z_r\sin(\phi)}{\omega\omega_r L_r}\right] + \frac{I_{IN}Z_r}{\omega_r}\sin(\phi)\right)\Bigg] = V_O, \quad (10)$$

$$\frac{1}{T}\Bigg[\frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\Bigg[\frac{\sin\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\sin(\phi)}{\omega_r} - \frac{\sin\left(2\pi(1-D)\right)\sin(\phi)}{\omega} - \frac{\omega L_r}{\omega_r Z_r}\cos\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\cos(\phi) + \frac{\cos\left(2\pi(1-D)\right)\cos(\phi)}{\omega}\Bigg] + \frac{V_O}{\omega_r Z_r}\cos\left(\omega_r\frac{2\pi(1-D)}{\omega}\right) + \frac{I_{IN}}{\omega_r}\sin\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\sin(\phi) - \left(\frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[-\frac{\omega L_r}{\omega_r Z_r}\cos(\phi) + \frac{\cos(\phi)}{\omega}\right] + \frac{V_O}{\omega_r Z_r}\right) - \frac{V_O}{2L_r}\left[\frac{2\pi D}{\omega}\right]^2 + i_{L,off}\left(t = \frac{2\pi(1-D)}{\omega}\right)\left(\frac{2\pi D}{\omega}\right)\Bigg] = \frac{P_o}{V_o}. \quad (11)$$

These three equations, (9)-(11), can be solved numerically to find D, I_{IN} and ϕ for given values of ω, P_o, V_o, L_r and C_r. These equations were coded in Matlab and solved using the *fsolve* function. This numerical approach is similar to the one used in [29-31]. The magnitude and phase of the input impedance are obtained by numerically extracting the fundamental Fourier series component of v_D and comparing it to the fundamental of i_{IN}.

For a given L_r, C_r pair, the code sweeps power over a given range and calculates the maximum value of phase of the input impedance. This is repeated for a range of values of

[1]The duty ratio is of interest because it determines the limits of integration during fundamental frequency component extraction.

[2] Note that Z_r and ω_r used in (9)-(11) are functions of L_r and C_r.

L_r and C_r to determine the variation in maximum input impedance phase with variations in values of L_r and C_r. This analysis was done for four different power range ratios (2:1, 5:1, 10:1 and 20:1).

These results were used to generate a set of normalized relationships that define the values for L_r and C_r that give the smallest deviation (in phase) from resistive operation over a specified operating power range ratio. This information is plotted in normalized form in three graphs (Figs. 3-5) that aid in the design of resonant class E rectifiers: (i) *maximum absolute value of input impedance phase vs. normalized capacitance*, (ii) *normalized peak diode voltage vs. normalized capacitance*, and (iii) *normalized inductance vs. normalized capacitance*. The next section discusses the design of the rectifier using these plots.

III. Class E Rectifier Design Methodology

Here we introduce a methodology for designing class E rectifiers that maintain resistive input impedance over a wide power range. The design of the class E rectifier begins with its specification of frequency f ($=\omega/2\pi$), dc output voltage V_o and rated output power $P_{o,max}$. These specifications can be used in conjunction with Figs. 3-5 to identify component values that minimize the worst case input impedance phase for a given power range ratio ($P_{o,max}$:$P_{o,min}$) as determined by the numerical investigation of the last section.

Figure 3 shows the absolute value of the maximum input impedance phase vs. normalized capacitance C_n for four different power range ratios (2:1, 5:1, 10:1 and 20:1). The capacitance is normalized as follows:

$$C_n = C_r \frac{2\pi f V_o^2}{P_{o,max}}, \tag{12}$$

where $P_{o,max}$ is the maximum (rated) output power. The plot shows that to minimize the worst case input impedance phase over the specified operating power range, the capacitance should be selected as a minimum within other design constraints (such as device voltage rating, etc.). The value of capacitance obtained with this methodology includes the intrinsic capacitance of the diode, any stray capacitance and any additional external capacitance if needed. Hence, C_r cannot be chosen to be smaller than the intrinsic capacitance of the diode. A value of capacitance above this level should be chosen based on the acceptable value of maximum input impedance phase.

The next step is to select an appropriate diode. The required voltage rating of the diode for the selected normalized capacitance can be determined from Fig. 4. Figure 4 plots the normalized peak diode voltage vs. normalized capacitance. The voltage is normalized to the dc output voltage:

$$V_{D,n} = \frac{V_{D,pk}}{V_o}, \tag{13}$$

where $V_{D,pk}$ is the peak diode voltage. The normalized reverse voltage blocking capability of the diode must be greater than what is indicated by Fig. 4. The voltage stress on the diode reduces as capacitance increases. Hence, Fig. 4 gives a minimum achievable capacitance value for a given peak diode voltage rating. Once the diode is selected, one can check Fig. 3 to ensure that the maximum input phase of the rectifier is within acceptable limits. If not, one might want to change the

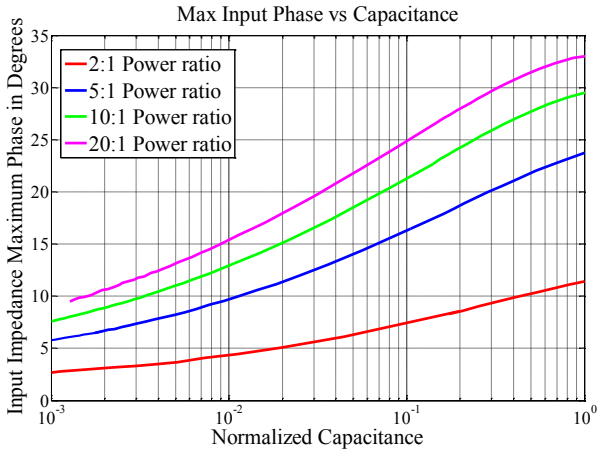


Figure 3. Worst-case phase angle magnitude across the specified operating conditions vs. normalized capacitance for different power ranges ratios ($P_{o,max}$:$P_{o,min}$).

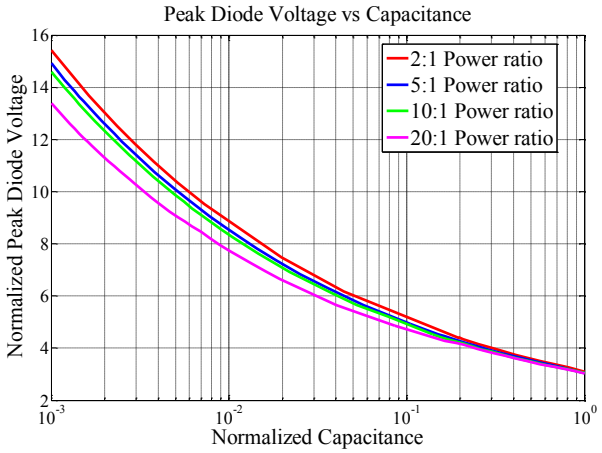


Figure 4. Maximum normalized peak diode voltage vs. normalized capacitance for different power range ratios ($P_{o,max}$:$P_{o,min}$).

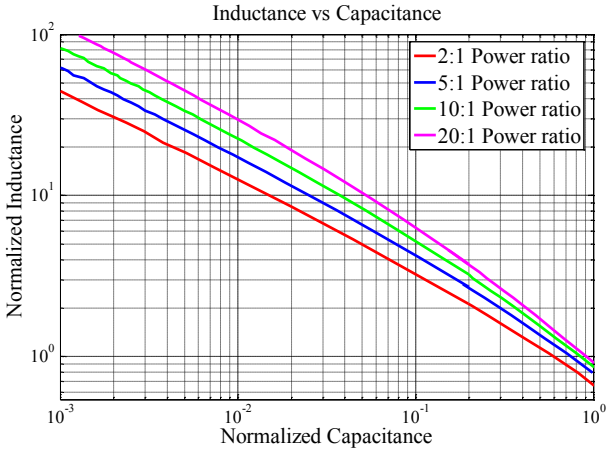


Figure 5. Normalized inductance vs. normalized capacitance for different power ranges ratios ($P_{o,max}$:$P_{o,min}$).

diode for one with a higher voltage rating and/or lower capacitance.

The next step is to select an appropriate value of L_r. Figure 5 shows a plot of normalized inductance vs. normalized capacitance. The inductance is normalized as follows:

$$L_n = L_r \frac{2\pi f P_{o,max}}{V_o^2}. \quad (14)$$

From this chart one determines the appropriate value of inductance L_r that will yield the most resistive input impedance across the specified operating power range for the selected capacitance.

Finally, the input L_s-C_s filter is chosen so that its resonant frequency is equal to the drive frequency f and it provides an adequate Q to achieve the desired spectral purity of the rectifier input waveforms for the application in question. We can quantify the relationship as:

$$\sqrt{\frac{L_s}{C_s}} = QR_{min}, \quad (15)$$

where L_s and C_s are the input filter inductance and capacitance, respectively, Q is the quality factor of the filter and R_{min} is the minimum value (at rated power) of the magnitude of rectifier input impedance Z_{in}. The following section presents a design example using this methodology that validates the approach.

IV. Class E Rectifier Design Example and Simulation

This section demonstrates the use of the design methodology described above in the design of a class E rectifier. The example we consider at first is that of a class E resonant rectifier operating at a frequency of 30 MHz with output voltage of 12 V dc and output power ranging from 18 W down to 1.8 W (i.e., a 10:1 power range ratio). We would like the input impedance of the rectifier to be as resistive as possible (i.e., minimizing the worst-case phase angle amplitude of the input impedance over the entire power range), while using a 60 V diode with nominal capacitance of 80 pF (based on the PMEG6020EPA diode which has a nominal average current rating of 2A). Thus, the normalized peak diode voltage capability is about 4 (assuming we allow only up to around 48 V peak with appropriate margin). From Fig. 4, the corresponding normalized capacitance C_n is 0.2. From Fig. 3 the expected maximum absolute value of input impedance phase angle is about 25°. From Fig. 5 the normalized inductance is 3.5. De-normalizing the L and C values, the inductance L_r comes out to be 149 nH and the capacitance C_r comes out to be 132.6 pF. The value of C_r is greater than the 80 pF intrinsic capacitance of the diode. The input LC filter is designed with a Q of 3 and R_{min} of 19 Ω, leading to a C_s of 93 pF and L_s of 302 nH. We also designed another rectifier with the same specifications except the power range ratio is selected as 2:1. Only the value of L_r changed to 89 nH and the expected maximum value of impedance change is 9°. Table I summarizes the design and parameters for the rectifiers to be simulated.

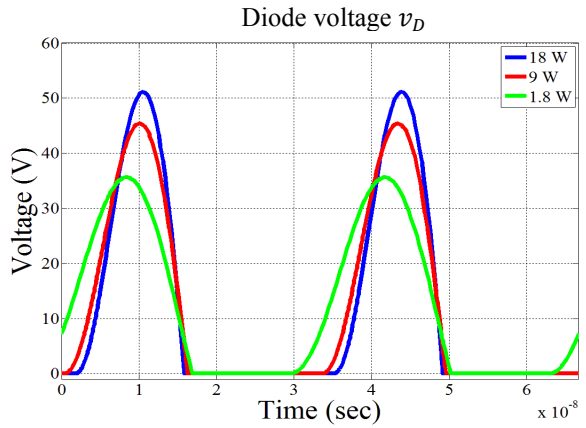


Figure 6. SPICE simulation results. Time-domain simulation of the diode voltage at 18 W, 9 W and 1.8 W of output power.

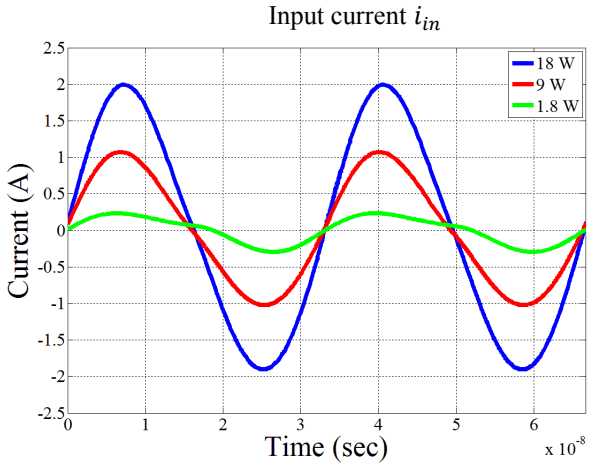


Figure 7. SPICE simulation results. Time-domain simulation of ac input current at 18 W, 9 W and 1.8 W of output power.

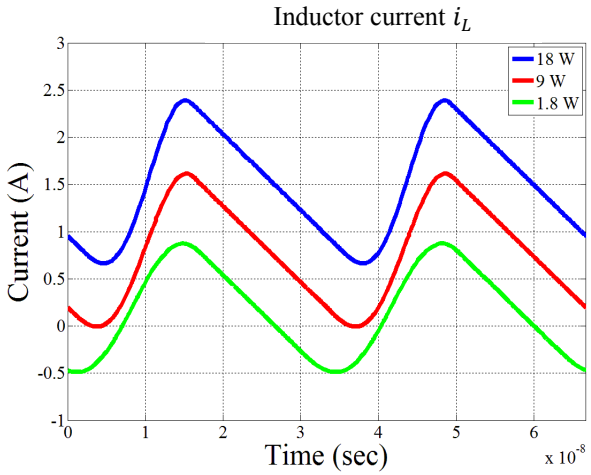


Figure 8. SPICE simulation results. Time-domain simulation of inductor L_r current at 18 W, 9 W and 1.8 W of output power.

Figures 6-8 show the LT SPICE simulation of our designed class E rectifier (based on a diode that is ideal except for a fixed intrinsic capacitance of 80 pF). Figure 6 shows the peak diode voltage to be around 51 volts, which is well within the diode specifications and well matching the predicted peak voltage of 48 V for C_n = 0.2 in this design. Figure 7 shows the input current to the rectifier, which shows

low harmonic content at full power. Figure 8 shows the inductor current with an average of 1.5 amps and substantial ac current.

Figure 9 shows the phase and magnitude of the input impedances (i.e. the based on the fundamental component of input voltage) of the rectifiers designed for 10:1 and 2:1 power range ratios. The impedance magnitude is inversely proportional to output power. The impedance is capacitive at high power and becomes inductive at low power. The maximum input impedance phase amplitude found by time-domain simulations across the specified operating power range is very close to the 22° predicted by the design graph in the 10:1 power range ratio. The 2:1 power range ratio curve has a maximum impedance phase of 10° which is in close agreement with the predicted 9°. The simulated results show that the design procedure works accurately, at least for idealized diode characteristics. It also shows that one can come closer to resistive input impedance behavior for smaller operating power range ratios.

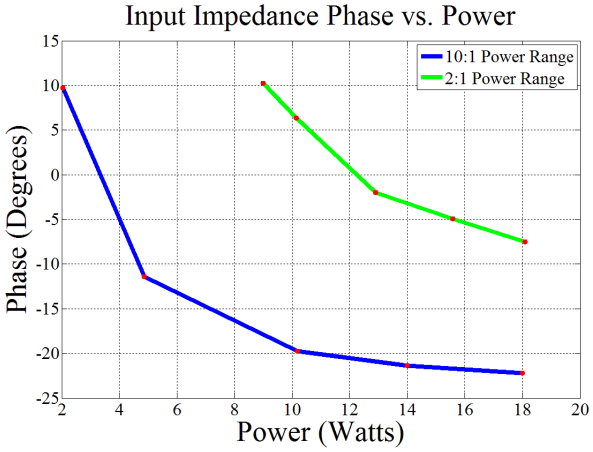
V. Experimental Validation

Figure 10 shows one of the boards used in testing the rectifier performance. The rectifier is driven by a power amplifier (AR 150A100B) with a sinusoidal input from a signal generator (BK Precision 4087). The load of the rectifier is a zener bank that consists of 10 SMBJ5349B diodes connected in parallel and mounted to a heat sink. The output dc voltage and current are measured with multimeters (Agilent U3606A and 34401A), the rectifier voltage is measured with a (10x, 500 MHz) oscilloscope probe model TPP0050, and the rectifier input current is measured with the TCP0030A current probe (120 MHz). The oscilloscope used was the MSO4054B.

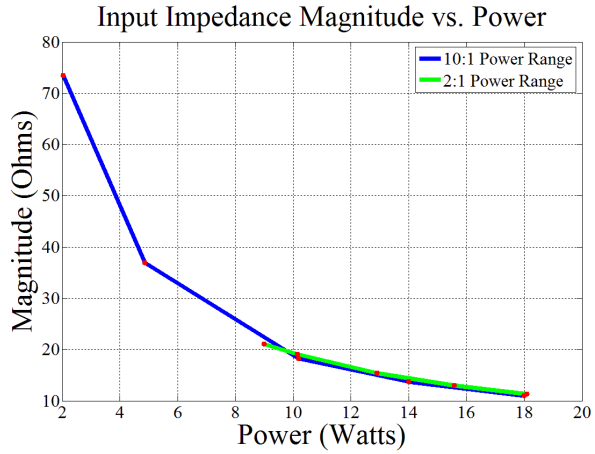
The biggest assumption in the design methodology is that the diode capacitance is constant with voltage (i.e., that the capacitance is linear). Two rectifiers were built to demonstrate the effectiveness of the design methodology. The first rectifier is a high-capacitance design where the additional (highly linear) capacitance C_A is much bigger than the diode capacitance C_D (where C_D is approximated as the diode capacitance when biased at the output voltage as read from the datasheet's C-V curve). This is done by allowing a design having relatively high input impedance phase (big deviation from resistive behavior) as per the curves of Fig. 3. The second rectifier was designed with C_A on the same order as C_D. The first (high capacitance) rectifier was designed for a maximum phase to be around 30° with a predicted peak diode voltage of 38 V over a 10:1 power range ratio. The circuit parameters are shown in Table II. The second (low capacitance) rectifier was designed for a predicted maximum phase shift of 10° and a predicted peak diode voltage of 53 V over a 2:1 power range. Table III shows the circuit parameters of this low capacitance rectifier. Both rectifiers used the SS16 diode from Vishay. Both rectifiers have an output capacitance C_{OUT} that is much higher than C_r and keeps the output voltage steady (low ripple) even in the presence of high ripple current on L_r.

TABLE I. Class E Rectifier Parameter Values Used in the Simulations.

Parameter	Value for 10:1 Power Range	Value for 2:1 Power Range
P_o	18-1.8 W	18-9 W
V_o	12 V	12 V
f	30 MHz	30 MHz
L_s	302 nH	302 nH
C_s	93 pF	93 pF
L_r	149 nH	89 nH
C_r	132.9 pF	132.9 pF
C_D	80 pF	80 pF
C_A	52.9 pF	52.9 pF



(a)



(b)

Figure 9. Resonant rectifier simulated input impedance as a function of output power: for 10:1 and 2:1 power range ratios: (a) input impedance phase angle and (b) input impedance magnitude.

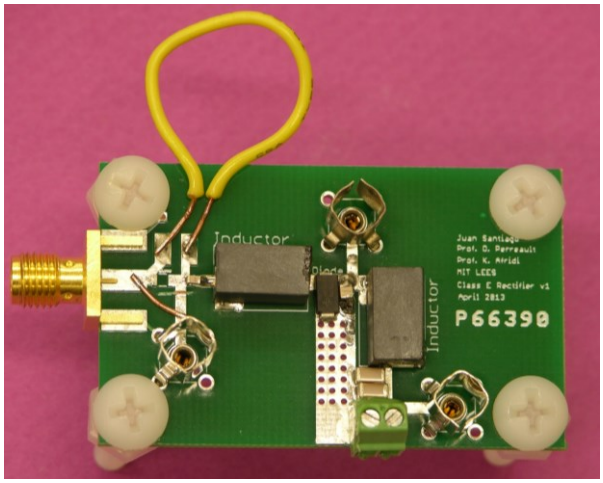


Figure 10. Class E resonant rectifier rated for 12 W, 12 V output voltage and 30 MHz switching frequency.

TABLE II. RECTIFIER CIRCUIT PARAMETERS FOR A DESIGN WITH RELATIVELY LARGE EXTERNAL CAPACITANCE ACROSS THE DIODE, OPTIMIZED FOR A 10:1 POWER RATIO.

Parameter	Design Value	Circuit Implementation
P_O	1.5-15 W	1.5-15 W
V_O	12 V	12-13 V 10x SMBJ5349B in parallel
f	30 MHz	30 MHz
L_S	307 nH	307 nH Coilcraft MAXI Spring
C_S	91 pF	91 pF, 250V ATC 600S910JT250XT
L_r	51 nH	48 nH Coilcraft MIDI Spring
C_r	477 pF	477 pF
C_D	47 pF	47 pF Vishay SS16 biased @ V_O
C_A	430 pF	100 pF, 500V ATC100B101JW 330 pF, 200V ATC100B331JW
C_{OUT}	20 µF	2x 10 µF, 50V, TDK C3225X7S1H106K250AB

The effective rectifier impedance is defined as the complex ratio of rectifier fundamental input voltage v_{IN} to rectifier fundamental input current i_{IN}. The input impedance at a given power level is found by measuring the input voltage and current, extracting the fundamental frequency component of each signal through Fourier analysis in MATLAB, and taking the ratio of the two. (It is noted that the rectifier input voltage and the diode voltage ideally have the same fundamental, as the input tank is tuned on resonance. In some cases input impedance is estimated using measurements of diode fundamental voltage as the "input" voltage. This is done so we can see the peak diode voltage which is more useful than the input voltage). The ratio of the fundamental voltage amplitude to fundamental current amplitude is the magnitude of the impedance and the phase shift between the fundamental voltage and current signals is the impedance phase. In order to measure the phase accurately, it is important that the oscilloscope and its probes are calibrated and deskewed with good precision before each test. The delay between the probes needs to be adjusted (deskewed) to get an accurate phase measurement.

TABLE III. RECTIFIER CIRCUIT PARAMETERS FOR A DESIGN WITH RELATIVELY SMALL EXTERNAL CAPACITANCE ACROSS THE DIODE, OPTIMIZED FOR A 2:1 POWER RANGE RATIO.

Parameter	Design Value	Circuit Implementation
P_O	6-12 W	6-13 W
V_O	12 V	12-12.7 V 10x SMBJ5349B in parallel
f	30 MHz	30 MHz
L_S	307 nH	307 nH Coilcraft MAXI Spring
C_S	91 pF	91 pF, 250V ATC 600S910JT250XT
L_r	133 nH	130 nH Coilcraft MAXI Spring
C_r	88.4 pF	89 pF
C_D	47 pF	47 pF Vishay SS16 biased @ V_O
C_A	41.4 pF	12 pF, 500V ATC100B120JT 30 pF, 500V ATC100B300JT
C_{OUT}	20 µF	2x 10 µF, 50V, TDK C3225X7S1H106K250AB

A circuit that aids in calibrating the oscilloscope was developed. The circuit was built on a similar board to the rectifier and consists of the same input LC filter of the rectifier (including the current probe) with a 50 Ω RF load. The circuit was tuned appropriately at the fundamental switching frequency so that at 30 MHz the impedance seen at the input is a pure 50 Ω resistive load. Figure 11 shows the input voltage and current of the calibration circuit. The calibration circuit is connected to the power amplifier and driven by a small amount of power and the delay on the current and voltage probes is adjusted so that the signals overlap and have zero phase shift between them. This sets the scope to the zero phase or resistive impedance: any variation of the phase will be caused by the rectifier circuit.

Figures 12 and 13 show the experimental results for the high-capacitance rectifier. Simulation results are also plotted; the simulation is ideal, including only a linear device capacitance of 47 pF, and does not include parasitic inductances, diode forward drop, output voltage increase with power due to zener diode impedance or other non-idealities. The plot shows that the max impedance phase

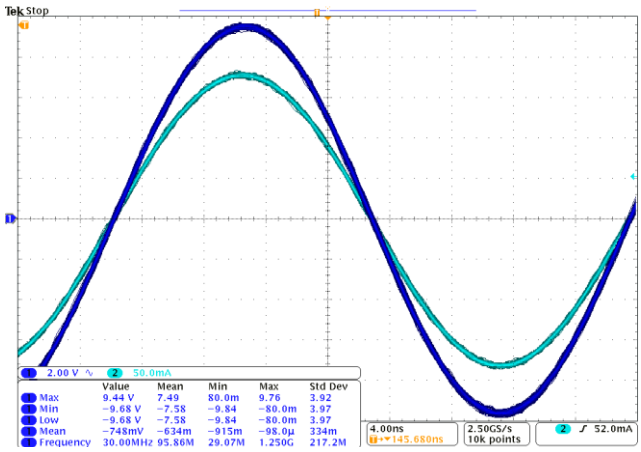


Figure 11. Calibration circuit voltage (dark blue) and current (light blue) waveforms. The oscilloscope is calibrated so that the waveforms are in phase with a 50 Ω load at 30 MHz.

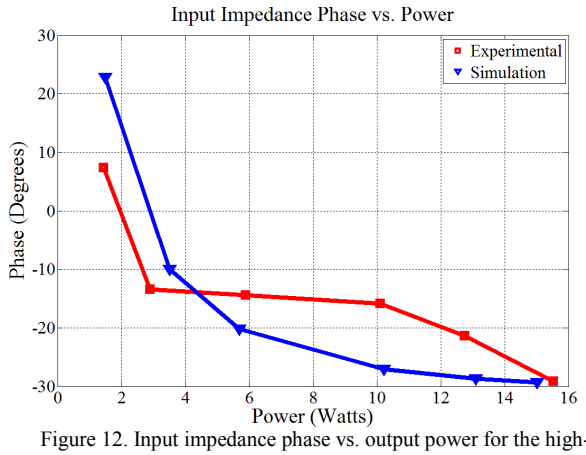


Figure 12. Input impedance phase vs. output power for the high-capacitance rectifier circuit described in Table II. The red curve is the measured experimental data and the blue curve is the simulation data. The maximum absolute phase magnitude over the specified power range is 30°.

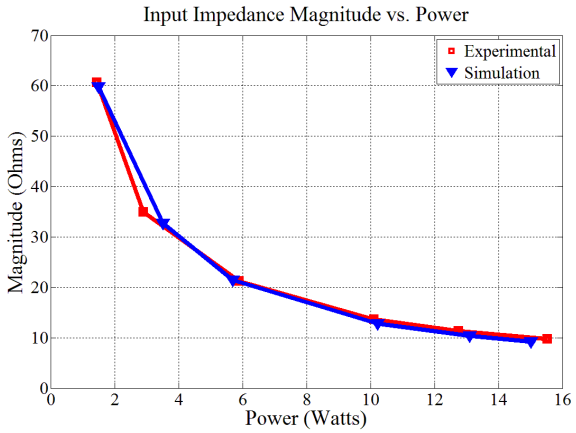


Figure 13. Input impedance magnitude vs. output power for the high-capacitance rectifier circuit described in Table II. The red curve is the measured experimental data and the blue curve is the simulation data.

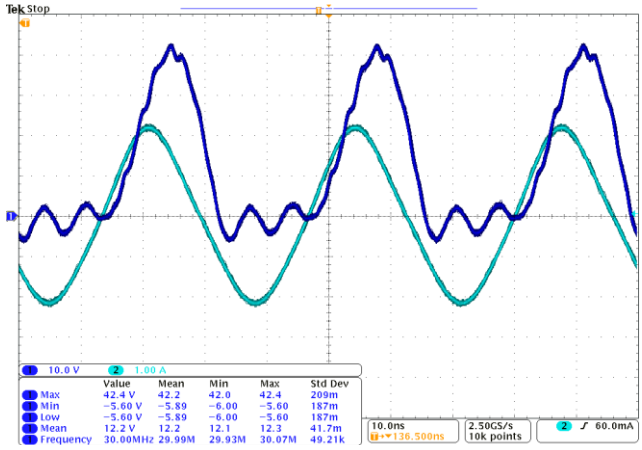


Figure 14. Diode voltage (dark blue) and input current (light blue) at full power, 15.53 W for the circuit of Fig. 10 and values in Table II. The peak diode voltage is 42 V.

is 30°, which confirms our expected value from the design plots in section III (predicted values of 30° for operation from 1.5 W to 15 W). Figure 14 shows the measured diode voltage and input current at full power. The measured peak diode voltage is 42 V, which is very close to the value of 38 V predicted using Fig. 4 for this design. It is suspected that this small deviation is due to the increase in output voltage (above 12 V) owing to the nonzero impedance of the zener bank load. A simulation that includes the output voltage increase to 13 V at full power shows the peak diode voltage is increased to 40 V. This confirms our expected value of peak diode voltage based on the design plots from section III.

Figures 15 and 16 show the experimental results for the low-capacitance design of Table III. Once again, experimental and simulation data is plotted. While there is a reasonable match between simulation and experiment, the match is not nearly as good as in the high-capacitance case (where diode capacitance nonlinearity is not important). In this case, the measured impedance amplitude exceeds that expected by approximately 6-22 % over the operating range and the maximum phase shift exceeds 15° at low power levels, while simulation predicts a worst-case deviation of only 10° from resistive. This shows one of the limitations of the design methodology: the voltage variation of the diode junction capacitance can place a limit on the accuracy of the design methodology.

The design methodology assumes a constant diode capacitance, but this assumption is valid when the external capacitance is considerably higher than the assumed constant value of the diode capacitance or when the actual diode capacitance is nearly constant with voltage. In the diode tested (SS16), the capacitance varies between 210 pF and 19 pF between 0.1 V and 60 V. As the capacitance varies over the switching cycle, the diode voltage waveform varies from that of a system having a constant diode capacitance. A simulation is prepared with C_A = 85.9 pF (additional shunt capacitance), L_r= 89.13 nH, a constant diode capacitance C_D of 47 pF and a variable C_D of $222.95/(1+v_D/0.9511)^{0.5987}$ pF. The variable capacitance model was derived from a curve fitting of the C-V plot on the datasheet of an SS16 diode, while the constant value was taken from the same plot at the average diode voltage. Figure 17 shows the peak diode voltage simulation results for the two diode capacitance models at the same output power (18 W) and output voltage level (12 V). It is clear that the behavior of the circuit changes depending on the capacitance model used.

Moreover, as power varies, the *effective* value of the diode capacitance varies, changing the input impedance from what would be predicted by the design curves (Figs. 3-5). For example, consider the diode in the rectifier discussed above. If the external capacitance is comparable in magnitude to the

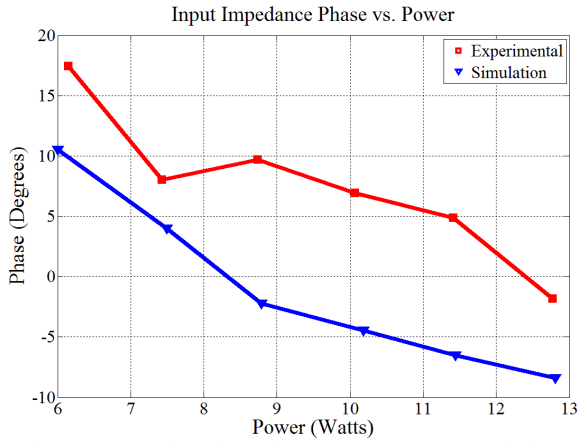


Figure 15. Input impedance phase vs. output power for the low-capacitance rectifier circuit described in Table III. The red curve is the measured experimental data and the blue curve is the simulation data.

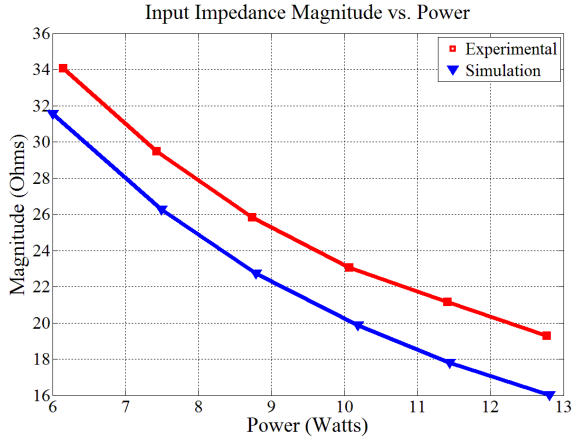


Figure 16. Input impedance magnitude vs. output power for the low-capacitance rectifier circuit described in Table III. The red curve is the measured experimental data and the blue curve is the simulation data.

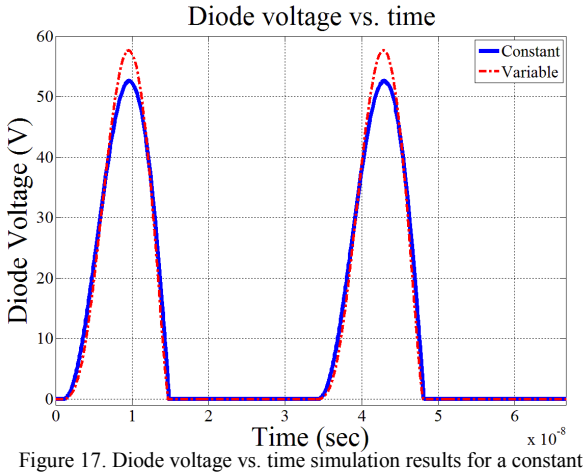


Figure 17. Diode voltage vs. time simulation results for a constant capacitance and for a variable capacitance. For the variable-capacitance case, the range of the diode capacitance is 210 to 19 pF according to instantaneous voltage, while the capacitance for constant-capacitance case is 47 pF. The external capacitance is 86 pF. At higher instantaneous voltage, the variable capacitance is lower and thus the reverse voltage peaks higher.

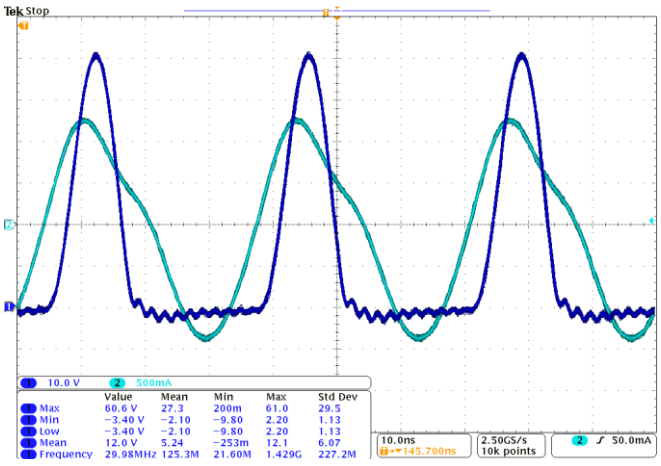


Figure 18. Diode voltage (dark blue) and input current (light blue) at full power, 12.77 W for the circuit of Fig. 3.1 and values in Table III. The peak diode voltage is 60.6 V.

diode capacitance at a dc output voltage of 12 V, the capacitance on the cathode node is dominated by the external capacitance when the instantaneous diode voltage is high. As power goes down, the peak voltage on the diode decreases and the node capacitance increases and is dominated by the diode nonlinear capacitance. This makes it difficult to select an exact equivalent capacitance (to represent the variable diode capacitance), as the correct value varies with input power. The effect can also be seen in Fig. 18. The peak diode voltage at full power was predicted to be 53 V which is acceptable for the SS16 (a 60 V diode), but the experimental value is 60.6 V. The simulation with increased output zener voltage of 12.7 V yielded 54.4 V of peak diode voltage, an increase of 2.64% which is still less than the 14.3% increase present in the experimental data. This increase in peak diode stress is also due to lower node capacitance at high voltages. These phenomena are not present in the high capacitance design seen in previously, as the capacitance was dominated by the linear external capacitance.

In summary, all the predictions by the design methodology are accurate for the case where the total capacitance across the diode (including diode capacitance) does not vary much with voltage (e.g., owing to using substantial external linear capacitance or having a diode with only small capacitance variation). However, accuracy degrades for the case where the effective capacitance across the diode varies substantially with voltage. This presents a limitation in the design method, but iterations on a design starting from design predictions with the proposed method could yield better results.

VI. Diode Performance Evaluation

Some Si Schottky diodes have been found to perform very poorly for resonant rectification at VHF frequencies, exhibiting much higher temperature rises and lower current limits than might be expected from datasheet information [12,22]. To study this issue systematically, fourteen commercially-available Si Schottky diodes were tested at 30 MHz in class E rectifiers. Each rectifier was designed and built using the methodology described above, based on the capacitance of the tested diode. The three best-performing diodes were also tested at 50 MHz.

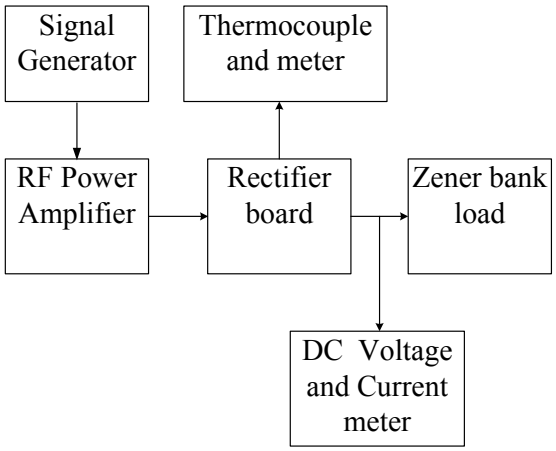


Figure 19. Block diagram of the experimental setup for the diode performance evaluation.

The performance of each diode was assessed by measuring the power dissipation in the diode operating in a class E rectifier. Since determining power through voltage and current measurements is very challenging at VHF, a thermal characterization method was used to simplify the power measurements. First, the diodes were characterized by determining the relationship between their surface temperature and the power dissipated in them using accurate dc measurements. The rectifier board is populated exactly as if used in resonant rectification so that the heat dissipation capability of the system is the same whether the diode carries dc or rf current. The temperature is measured on the board trace (on copper, not on soldermask) close to the anode of the diode using a K-type thermocouple. Because the anode is grounded, the thermocouple will add no significant capacitance to the circuit. Figure 19 shows a block diagram of the experimental setup. The signal generator, rf power amplifier and dc meters are the same used in the previous section. The thermometer is a Digi-Sense Scanning Thermometer. This thermal characterization of the diode was then used to determine the power dissipated in the diode with the rectifier operating at VHF frequencies by measuring diode temperature rise under rf operation.

The diodes selected for testing are shown in Table IV. The diodes can be sorted into seven groups having the same pair of nominal rated peak reverse voltage and nominal rated maximum average forward current (MAFC): {40 V, 1 A}, {40 V, 2 A}, {60 V, 1 A}, {60 V, 2 A}, {60 V, 3 A}, {100 V, 1 A} and {100 V, 2 A}. Thus, seven rectifiers were built to test each group. Each rectifier was designed for a dc output voltage V_0 equal to 20% of its rated diode peak voltage, maximum output power $P_{o,max}$ equal to V_0 times the MAFC of the diode, a 5:1 power range ratio, a maximum voltage stress on the diode of 80% its peak rated voltage, and an operating frequency f of 30 MHz. Using these design rules, reading from Figs. 3-5 we obtain C_n = 0.3 and L_n = 2.0. The expected maximum phase magnitude is 21°. The value of C_D is different for each diode, so we select the value of C_A as appropriate to obtain a constant value of C_r for a given rectifier. Also, some of the 2 A and 3 A diodes were also tested for operation at lower currents of 1 A and 2 A,

TABLE IV. DIODES TESTED FOR USE IN CLASS E RECTIFIERS AT VHF.

Diode	Rated Peak Voltage Vrev,pk	Maximum Average Forward Current MAFC	Capacitance C_D @ 0.2Vrev,pk (pF)
NSR10F40NXT5G	40	1	45
NXP PMEG4010EP	40	1	50
NXP PMEG4020EP	40	2	100
VISHAY SS16	60	1	47
VISHAY MSS1P6	60	1	27
MCC MBRX160	60	1	12
NXP PMEG6020ER	60	2	76
NXP PMEG6020EPA	60	2	80
NXP PMEG6030EP	60	3	105
VISHAY SS3P6L	60	3	110
VISHAY B360B	60	3	130
Fairchild S100	100	1	52
ST STPS1H100A	100	1	28
VISHAY 10MQ100	100	2	17

TABLE V. THE PARAMETERS OF THE SEVEN RECTIFIERS BUILT TO TEST THE DIODES AT 30 MHZ. THE RECTIFIERS WERE OPERATED AT A DC OUTPUT VOLTAGE OF 0.2 TIMES THE PEAK DIODE VOLTAGE RATING.

Diode Group	Cr (pF) (Cn=0.3)	Lr (nH) (Ln=2.0)	Cs (pF)	Ls (nH)
{40 V, 1 A}	199	84.8	74.4	378
{40 V, 2 A}	398	42.4	91	307
{60 V, 1 A}	132.6	127.3	50.5	557
{60 V, 2 A}	266	63.6	91	307
{60 V, 3 A}	398	42.4	91	307
{100 V, 1 A}	80	212.1	44.6	631
{100 V, 2 A}	160	106.1	57	493

respectively. For this reason, 21 tests were performed for the 14 diodes listed in Table IV. Table V shows the component values of the seven different rectifiers designed to test the seven groups of diodes.

During testing, the temperature on the diode was measured in steps of 20% of full diode average current starting from 0 up to 100%. After a step increase in the current, we would wait 5 minutes for the temperature to settle and the system to reach thermal equilibrium before taking a temperature measurement. There were two conditions for which the experiment would be stopped before reaching 100% current to avoid the destruction of the diode: *i*) the temperature of the anode copper trace rises above 90°C, and *ii*) the peak voltage of the diode rises above its rated value. These constraints are imposed to emulate a real application where the diodes are not driven at extreme conditions. Due to these constraints some diodes could not be utilized near their datasheet rated current. Some of these diodes are simply unfit for resonant rectification at VHF frequencies, while others can be derated and considered useful for operation at a fraction of their nominal (datasheet) rated current.

Figure 20 (a) shows the test results for the 40 V diodes. The PMEG4010EP is the diode with the lowest loss. In Fig. 20 (b) the PMEG6020ER and PMEG6020EPA have the least losses. Both are rated for 2 A but operate as 1 A devices in this particular test. Note that one of the diodes could not reach full current and this was due to exceeding temperature limits. Figure 20 (c) shows the 60 V, 2 A test, of which only one diode could be used at full current. The diode with the best performance was the PMEG6030EP, de-rated to 2 A. On the 60 V, 3 A test, Fig. 20 (d), the PMEG6030EP performed the best. None of the diodes could reach rated current. Finally, the 100 V, 1-2 A test is shown in Fig. 20 (e). Here the diode with least losses is the S100, but it was heavily de-rated because of high diode voltage stress. It is important to highlight that the capacitance C_r of the 100V-diode rectifier is comparable in magnitude to the device capacitance as can be seen in Tables IV and V. The resonant capacitance is dominated by the non-linear diode capacitance and, as shown in Fig. 17, this leads to higher voltage stress than predicted.

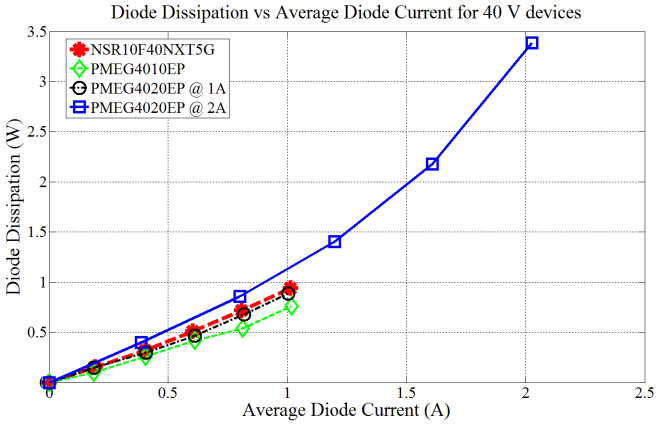
Three diodes with superior performance were chosen and tested in 50 MHz rectifiers. The diodes are the PMEG4010EP (Io = 1A), PMEG6020ER (Io = 1A) and PMEG6030EP (Io = 2A). The rectifiers were designed with the same specifications stated above with the exception of an increase in frequency to 50 MHz. Table VI shows the rectifier parameters and Fig. 21 shows the test results. The power dissipation is slightly higher when operating at 50 MHz but these three diodes are still useful in rectification at VHF frequencies. As frequency increases, the value of C_r decreases and approaches that of C_D, the diode capacitance. In order to keep increasing operating frequency while maintaining resistive behavior, it is important to use diodes with low intrinsic capacitance.

VII. Conclusion

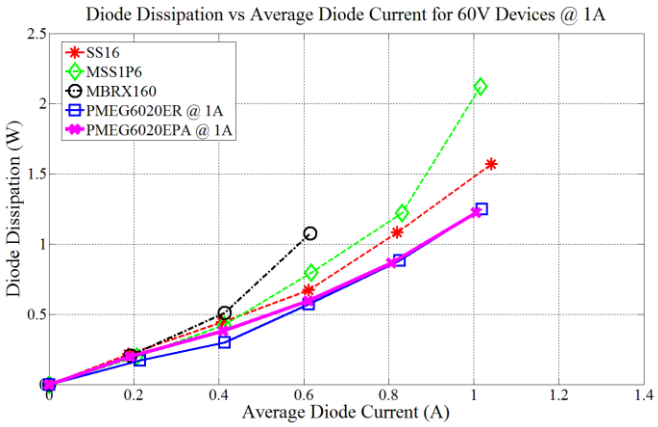
A methodology for designing resonant rectifiers with near-resistive input impedance has been presented in this paper. We develop analytical expressions to model the rectifier, and provide a graphical approach for the design. The methodology is experimentally validated, and its limitations

TABLE VI. The parameters of the rectifiers built to test the diodes at 50 MHz. The rectifiers were operated at a DC output voltage of 0.2 times the peak diode voltage rating.

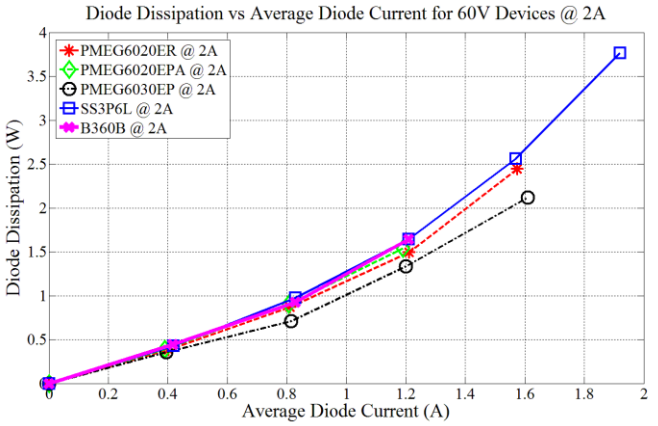
Diode Under Test	Cr (pF) (Cn=0.3)	Lr (nH) (Ln=2.0)	Cs (pF)	Ls (nH)
PMEG4010EP	119	47	47	222
PMEG6020ER	80	82	27	334
PMEG6030EP	160	39	47	206



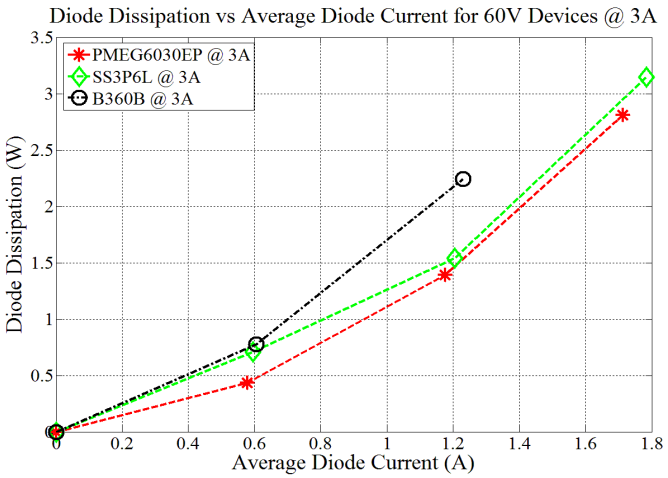
(a)



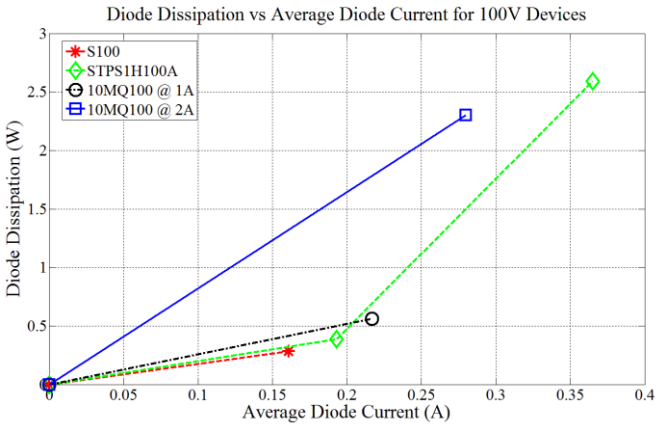
(b)



(c)



(d)



(e)

Figure 20. Diode testing results at 30 MHz. Diode dissipation vs. average current for class E rectification into a dc output voltage of 0.2 times the diode rated voltage. The parameters of the rectifiers are listed in Table V. From top to bottom: (a) 40 V, 1-2 A; (b) 60 V, 1A, (c) 2A, and (d) 3 A; and (e) 100 V, 1-2 A.

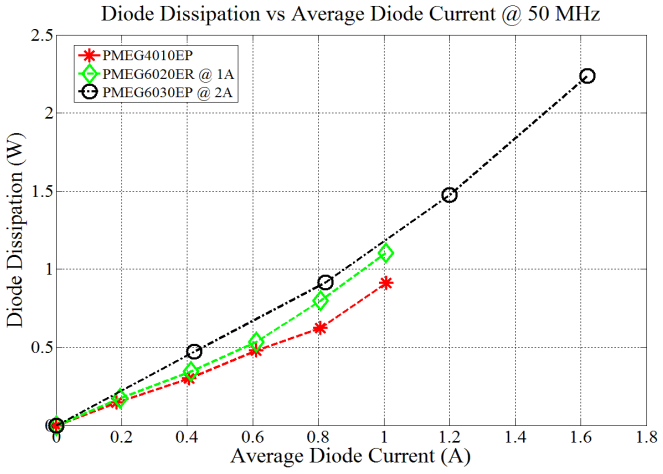


Figure 21. Diode testing results at 50 MHz. Diode dissipation vs. average diode current for class E resonant rectification into a dc output voltage of 0.2 times the diode rated voltage. The parameters of the rectifiers are listed in Table VI.

discussed. Various commercially-available Si Schottky diodes have been tested for their performance in class E resonant rectifiers at VHF frequencies. It is hoped that this design approach, the insights available from the design curves and the experimental evaluation of commercial diodes for VHF rectifiers will prove to be useful in designing resonant rectifiers.

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