A Multilevel Energy Buffer and Voltage Modulator for Grid-Interfaced Micro-Inverters

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***Abstract*—Micro-inverters operating into the single-phase grid from solar photovoltaic (PV) panels or other low-voltage sources must buffer the twice-line-frequency variations between the energy sourced by the PV panel and that required for the grid. Moreover, in addition to operating over wide average power ranges, they inherently operate over a wide range of voltage conversion ratios as the line voltage traverses a cycle. These factors make the design of micro-inverters challenging. This paper presents a Multilevel Energy Buffer and Voltage Modulator (MEB) that significantly reduces the range of voltage conversion ratios that the dc-ac converter portion of the micro-inverter must operate over by stepping its effective input voltage in pace with the line voltage. The MEB partially replaces the original bulk input capacitor, and functions as an active energy buffer to reduce the total size of the twice-line-frequency energy buffering capacitance. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter stage, leading to a higher overall system efficiency. The MEB architecture can be implemented in a variety of manners, allowing different design tradeoffs to be made. A prototype micro-inverter incorporating an MEB, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for a line cycle average power of 70 W, has been built and tested in a grid-connected mode. It is shown that the MEB can successfully enhance the performance of a single-phase grid-interfaced micro-inverter by increasing its efficiency and reducing the total size of the twice-line-frequency energy buffering capacitance.**

***Index Terms*—Switched capacitor circuits, Multilevel systems, Buffer circuits, Photovoltaic power systems, AC-DC power conversion, DC-AC power conversion.**

I. Introduction

In large-scale solar photovoltaic (PV) installations, multiple PV modules (panels) are connected to the electric grid through a single high-power inverter. However, for smaller residential and commercial applications, PV micro-inverters are attractive and are a focus of extensive research in both academia and industry. Each micro-inverter directly connects one PV module to the grid, hence enabling higher overall maximum power point tracking (MPPT) efficiency and improved system reliability by eliminating the potential single point of failure [1]–[8]. Two important considerations in the design of micro-inverters are converter efficiency and size. The size of the micro-inverter can be reduced by increasing its switching frequency. However, to maintain or enhance efficiency at the higher switching frequencies, advanced topologies and control strategies are necessary.

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Recently proposed single-phase micro-inverter architectures have been reviewed in [1]–[4]. Topologies are grouped into single-stage architectures and multi-stage architectures. In a single stage architecture, multiple tasks (e.g. voltage modulation, power modulation and output current shaping) are realized in a single power stage. They have low circuit complexity and simple control, but cannot achieve high performance over a wide operating range. Multi-stage architectures have multiple power conversion stages with each stage performing one or more functions. Each stage can be optimized individually, thus the overall system performance is usually better, while the total component counts and control complexities are usually higher.

One attractive multi-stage architecture for micro-inverters is shown in Fig. 1 [4]–[6]. It comprises a high frequency resonant inverter, a transformer, and a cycloconverter. The resonant inverter is controlled in such a manner that it produces a high-frequency-sinusoidal current with its amplitude modulated at the line frequency (60 Hz in the US). The high frequency transformer steps up the voltage, and the cycloconverter converts the high frequency current into a sinusoidal line-frequency current, which is injected into the grid. Output power can be controlled by a combination of frequency control and phase-shift control. The twice-line-frequency energy buffering in the circuit of Fig. 1 - and in many other micro-inverter architectures - is provided by the input capacitor, C_{IN}, though other methods are possible (e.g., [3], [6]–[9]). Related micro-inverter architectures likewise incorporate a high-frequency inverter and step-up transformation, with subsequent transformation of energy to the line voltage. However, all such architectures must buffer the twice-line-frequency energy and must vary the amplitude of the high frequency output current across a very wide range (e.g., in proportion to the line voltage and the average power delivered by the inverter), posing design and control challenges. For example, if frequency control alone is used to control the amplitude of the output current, the required frequency range can be very wide, reducing efficiency. Hence, there is an evident need for micro-inverter circuit designs and associated controls that can provide improved performance for operating over wide output voltages and power ranges while providing buffering for the twice-line-frequency power variations.

The challenges faced by micro-inverters - wide operating voltage and power ranges and the need to buffer the twice-line-frequency energy - also exist in other single-phase grid-interfaced dc-ac converters. Many approaches have been employed to handle the twice-line-frequency energy concerns, including energy buffers interfaced within the high-frequency portion of the inverter system [6]–[8], "dc" interface energy

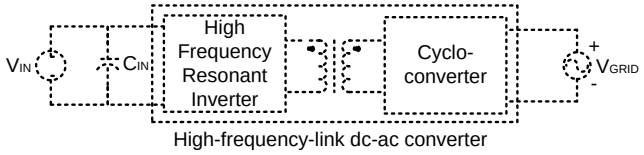


Fig. 1. Architecture of a micro-inverter incorporating a the twice-line-frequency energy buffer capacitance, C_{IN}, a high-frequency resonant inverter, a transformer and cycloconverter.

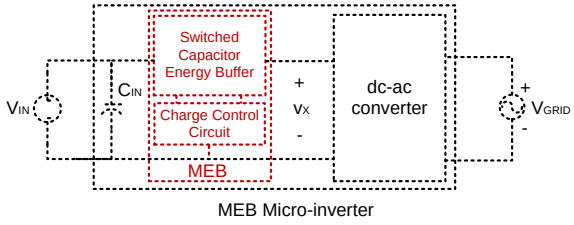


Fig. 2. Architecture of the proposed MEB micro-inverter. It incorporates a MEB and a dc-ac converter. Although here the MEB is shown on the dc side of the micro-inverter, an alternative is to incorporate the MEB function on the ac side of the micro-inverter, as discussed in section IV.

buffers that have wider operating range than simple capacitors placed across the panel or elsewhere [9]–[15], and active power filters placed on the ac side of the system [16], among other approaches. To reduce the required operating ranges of the high-frequency parts of the system, cascaded power stages (such as variable switched-capacitor stages) have sometimes been employed (e.g., [17], [18]). Another approach that has been used is stacking multiple PV modules as part of a multilevel converter to synthesize the ac line voltage [19]. However, this approach is not applicable to single-module micro-inverter systems.

This paper introduces a new technique to address the above-mentioned challenges. The new technique shares some of the benefits of both variable-topology cascade converter structures [18] and switched-capacitor energy buffers [14], [15], while enabling very high efficiency to be maintained. The new power converter architecture incorporates a Multilevel Energy Buffer and Voltage Modulator (MEB) to achieve compression of the high-frequency inverter operating range, thereby improving the efficiency of the high-frequency-link dc-ac converter stage. The MEB also partially replaces the original bulk input capacitor and provides the twice-line-frequency energy buffering between dc and ac. This paper is an expansion on our earlier conference paper [20], and includes alternative implementation methods, updated experimental results and estimates of loss breakdown.

The remainder of this paper is organized as follows: Section II describes the overall architecture of the proposed MEB micro-inverter. A specific implementation of the MEB micro-inverter and its design methodology is described in section III. Section III also explains the expected efficiency benefits of this implementation. Section IV describes alternative implementations of the MEB micro-inverter. The design details of a prototype MEB micro-inverter are given in section V. Section VI presents the experimental results of the MEB micro-inverter tested while connected to the grid, together with estimates of the loss breakdown based on experimental results. Section VII compares the proposed MEB micro-inverter with other recently-proposed micro-inverters to highlight the key contributions of this paper. Finally, conclusions are presented in section VIII.

II. Architecture of the Proposed MEB Micro-inverter

The architecture of the proposed MEB micro-inverter is shown in Fig. 2. The MEB is connected in cascade between the input capacitor and a dc-ac converter block. The MEB comprises a Switched-Capacitor Energy Buffer (SCEB) and an optional Charge Control Circuit (CCC). The SCEB is used to modulate the dc-ac converter block's input voltage, v_X, as the line voltage traverses a cycle to reduce the required amount and variations in voltage conversion ratio of the high-frequency dc-ac converter block over the line cycle. Consequently, the operating range of the high-frequency, high-step-up portion of the micro-inverter is reduced. The SCEB also functions as an active energy buffer and helps to reduce the total energy storage requirement for the twice-line-frequency energy buffering by separating the energy buffer voltage from the input (panel) voltage. Since the capacitor(s) in the SCEB can be charged over a wider range than is permissible for a buffer capacitor across the panel output, the required total energy storage (and capacitor size) can be reduced. This represents a form of third-port energy buffering [2], [3], [6]–[8], providing active control of the energy storage stage, independent of the input and output voltages. The switches in the SCEB switch at low multiples of the line frequency, allowing the SCEB to be highly efficient. The SCEB also steps up the voltage on the primary side of the transformer. Hence, it reduces the transformer primary-side current and the primary-side conduction losses.

The optional CCC provides an additional means to balance the total charge entering and leaving the SCEB over a line cycle, thereby providing greater flexibility in the operation of the SCEB. The power rating of the CCC is a fraction of the power rating of the MEB micro-inverter, and it only operates over part of the line cycle. Hence, it can be small and its losses do not substantially impact the overall efficiency of the micro-inverter. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter block, leading to a higher overall system efficiency.

Although in this paper we present the use of the MEB in the context of a micro-inverter, this MEB based architecture can be applied more broadly to converters interfacing between low-voltage dc and the single-phase ac grid.

III. Design of An Example MEB Micro-inverter

There are many possible implementations of the proposed MEB micro-inverter and the MEB itself, allowing trade-offs to be made between complexity and performance. In this section we describe an example MEB micro-inverter implementation and its design methodology. The full system architecture and some operating waveforms are shown in Fig. 3. The main power path of this architecture consists of two stages: a MEB

stage and a dc-ac converter stage. The MEB stage synthesizes a multilevel voltage $v_{\rm X}$ that is the input voltage of the dc-ac converter. The multilevel voltage $v_{\rm X}$ steps in pace the line voltage, thus reducing the required voltage conversion range of the dc-ac converter. The dc-ac converter is a high-frequency-link resonant converter, incorporating a series resonant inverter, a high-frequency transformer and a cycloconverter. The series resonant inverter creates a high frequency current $i_{\rm S}$ with a line-frequency sinusoidal envelope. The high frequency current $i_{\rm S}$ is then processed by the cycloconverter to generate a line-frequency current that is injected into the grid. Since the dc-ac converter is switching at a high frequency, the high frequency components remaining after the cycloconverter can be filtered by two small output capacitors $\rm C_{o1}$ and $\rm C_{o2}$. The full system also includes a line angle detector circuit and a micro-controller unit (MCU). We first describe the design of the MEB, and then the design of the high-frequency dc-ac converter stage.

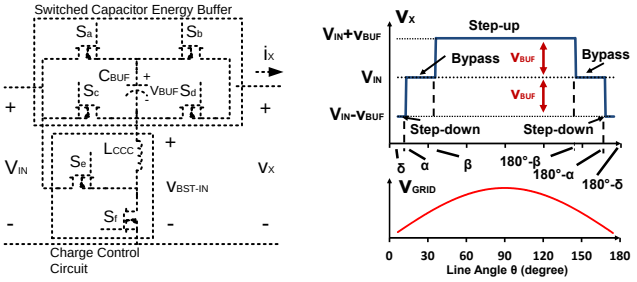
A. Design of the MEB

One implementation of the MEB is shown in Fig. 4a. The MEB has two subsystems: a Switched-Capacitor Energy Buffer (SCEB) and an associated Charge-Control Circuit (CCC). The SCEB comprises four switches, connected as a full bridge, and one buffer capacitor $\rm C_{BUF}$. The switches of the SCEB change state at line angles α, β, $(180^\circ-\beta)$ and $(180^\circ-\alpha)$ to generate the dc-ac converter input voltage $v_{\rm X}$ shown in Fig. 4b. When the magnitude of the line voltage, $|v_{\rm GRID}|$, is low (corresponding to $\theta \in [0^\circ, \alpha] \cup [180^\circ-\alpha, 180^\circ]$, i.e., line angles in the range 0° to α and $180^\circ-\alpha$ to 180°), the SCEB operates in the Step-down Mode with $\rm S_a$ and $\rm S_d$ on ($\rm S_b$ and $\rm S_c$ off) and $v_{\rm X} = V_{\rm IN} - v_{\rm BUF}$; when $|v_{\rm GRID}|$ is in the mid-range ($\theta \in [\alpha, \beta] \cup [180^\circ-\beta, 180^\circ-\alpha]$), the SCEB operates in the Bypass Mode ($\rm S_a$, $\rm S_b$ on) and $v_{\rm X} = V_{\rm IN}$; and when $|v_{\rm GRID}|$ is high ($\theta \in [\beta, 180^\circ-\beta]$), the SCEB operates in the Step-up Mode ($\rm S_b$, $\rm S_c$ on) and $v_{\rm X} = V_{\rm IN} + v_{\rm BUF}$. In Fig. 4b and the following analysis, $\rm C_{BUF}$ is assumed to be large enough that $v_{\rm BUF}$ does not vary significantly over a line cycle. With the SCEB operated in this manner, $v_{\rm X}$ is modulated in pace with the line voltage, yielding a significantly compressed range of voltage conversion ratios for the high-frequency converter. The three SCEB modes repeat periodically every half-line cycle. Each switch changes state twice in each half-line cycle, leading to low switching loss of the SCEB.

Note that in Fig. 4b, $v_{\rm X}$ is not specified for line angles close to the zero crossings of the line. At the zero crossings of the line voltage (i.e., when $\theta = 0^\circ$ and $\theta = 180^\circ$), the output current needs to approach zero in a continuous manner to achieve a perfect power factor. This is practically unachievable under continuous modulation of the converter. To limit the operating frequency range of the dc-ac converter block, a dead-angle, δ, of several degrees is introduced before and after the zero-crossings of the line voltage, during which time the micro-inverter is shut-off and no current is injected into the grid. In this paper, a δ of 6° is selected.

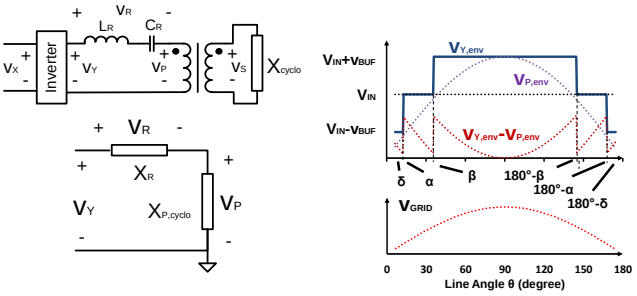
The design of the MEB involves selecting optimal values for the three design parameters: $v_{\rm BUF}$, α and β, so as to achieve the maximum reduction in dc-ac converter block's operating range. To minimize this operating range we must minimize the maximum voltage drop across the resonant tank, $v_{\rm R}$, over the line cycle. This is equivalent to minimizing the difference between the envelope of the high frequency output voltage of the full bridge, $v_{\rm Y,env}$, and the envelope of the voltage across the primary side of the transformer, $v_{\rm P,env}$ (see Fig. 5). Note $v_{\rm P,env}$ is sinusoidal and in phase with $v_{\rm GRID}$. In this work, with δ chosen as 6°, to minimize the operating range of the dc-ac converter, the optimal value of $v_{\rm BUF}$ is $0.6V_{\rm IN}$, α is 12.8°, and β is 40.9°. These control parameters yield a multilevel voltage that optimally approximates a line-synchronized sinusoidal voltage. Detailed derivations of these control parameters are provided in Appendix I.

With these design parameters, a CCC which maintains the charge balance of $\rm C_{BUF}$ (hence maintaining $v_{\rm BUF}$) is needed. An example implementation of the CCC is shown in Fig. 4a, where a modified boost converter connects the negative terminal of $\rm C_{BUF}$ to the MEB input. The output voltage of this boost converter is fixed ($V_{\rm IN}$), while its input voltage is regulated ($v_{\rm BST-IN}$). When $\rm S_a$ is on, regulating $v_{\rm BST-IN}$ effectively regulates $v_{\rm BUF}$. The CCC switches at a higher frequency than the operating frequency of the SCEB, acting as a controlled current source. In the Step-down mode, the CCC and the dc-ac converter charge $\rm C_{BUF}$ adiabatically; in the Bypass mode, the CCC continues to charge $\rm C_{BUF}$ adiabatically; and in the Step-up mode, the CCC is turned off, and $\rm C_{BUF}$ is discharged adiabatically by the dc-ac converter.



(a) (b)

Fig. 4. One embodiment of the proposed MEB: (a) MEB circuit implementation, and (b) waveform of $v_{\rm X}$ relative to $v_{\rm GRID}$ during a half line-cycle.



(a) (b)

Fig. 5. (a) Model of the dc-ac converter stage. Here $\rm X_R$ is the impedance of the resonant tank, $\rm X_{cyclo}$ is the impedance of the cycloconverter (rectifier/unfolder), and $\rm X_{P,cyclo}$ is the impedance of the cycloconverter reflected to the primary side of the transformer. (b) Waveforms of the envelope of $v_{\rm Y}$, $v_{\rm P}$,$v_{\rm Y} - v_{\rm P}$ and $v_{\rm GRID}$ relative to the line voltage during a half line-cycle.

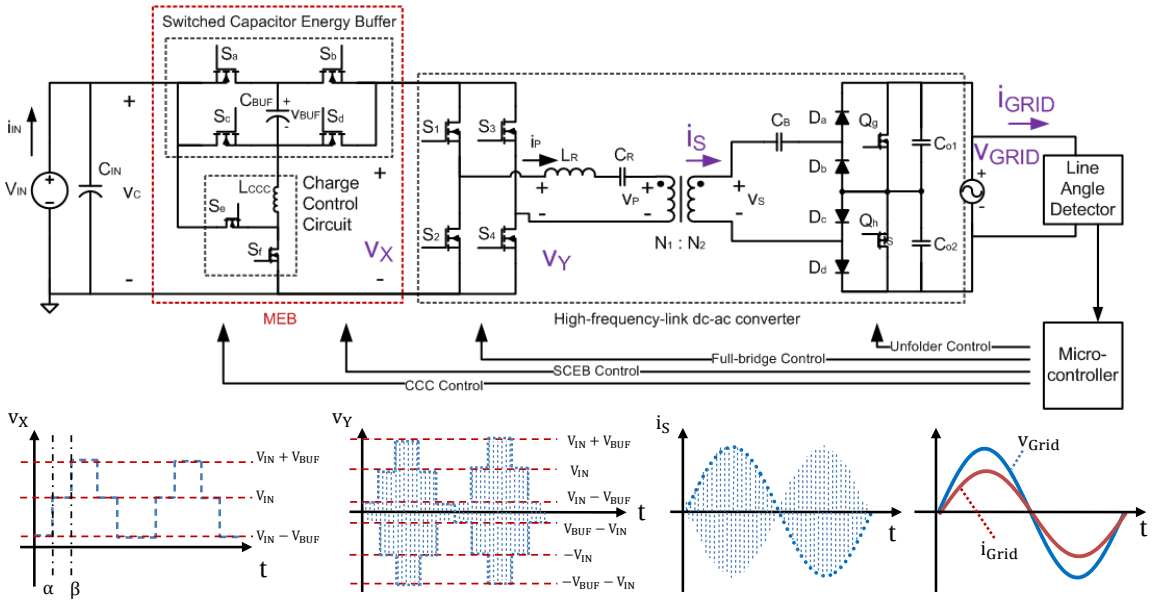


Fig. 3. One implementation of the MEB micro-inverter and its conceptual operating waveforms: $v_{\rm X}$ is the multilevel voltage synthesized by the MEB stage; $v_{\rm Y}$ is a high frequency voltage created by the H-bridge; $i_{\rm S}$ is the current of the resonant tank with a sinusoidal envelope; $v_{\rm GRID}$ and $i_{\rm GRID}$ are the line voltage and the line current.

Figure 6 shows the current flow directions in the MEB during the three operating modes. In this design, the CCC operates in continuous conduction mode (CCM) with the duty-ratio of switch $\rm S_e$ fixed at 0.4. This keeps $v_{\rm BST-IN}$ stable at $0.4V_{\rm IN}$, maintaining $v_{\rm BUF}$ at $0.6V_{\rm IN}$ as required. With this control, $v_{\rm X}$ equals $1.6V_{\rm IN}$ during the Step-up mode, $V_{\rm IN}$ during the Bypass mode, and $0.4V_{\rm IN}$ during the Step-down mode (as shown in Fig. 4b).

In the steady state, the buffer capacitor $\rm C_{BUF}$, is charged when the line voltage is low, and is discharged when the line voltage is high. However, before the system enters periodic steady state operation, $v_{\rm BUF}$ needs to be precharged to $0.6V_{\rm IN}$. The CCC implementation described above has a built-in feedback mechanism which automatically precharges $\rm C_{BUF}$ to this level without the need for additional control. For example, if $v_{\rm BUF}$ is less than $0.6V_{\rm IN}$ either during the startup or because of disturbances, then during the Step-down mode, since $v_{\rm X}$ will be larger than $0.4V_{\rm IN}$, the fixed duty ratio control of the CCC will charge up $\rm C_{BUF}$. Furthermore, during the Step-up mode, since $v_{\rm X}$ will be smaller than the desired value of $1.6V_{\rm IN}$, the dc-ac converter block will have a lower input voltage and thus draw less charge from $\rm C_{BUF}$. As a result, $\rm C_{BUF}$ has a positive net charge during one line cycle and $v_{\rm BUF}$ increases. This process is repeated over a few line cycles until $v_{\rm BUF}$ reaches its steady state value of $0.6V_{\rm IN}$. Note that since the input voltage of the CCC boost converter is regulated, its dynamics are similar to that of a buck converter, which remains stable in the face of disturbances.

The line-synchronized multilevel voltage $v_{\rm x}$ significantly reduces the required voltage conversion range of the dc-ac converter, resulting in higher dc-ac converter efficiency. To achieve high overall system efficiency, the MEB stage itself also needs to be very efficient. The switches of the SCEB are switched at multiples of line frequency and its loss is dominated by conduction loss, which can be kept low by using semiconductor devices with low on-resistance. The CCC is very efficient because of its relatively low voltage rating and fixed voltage conversion ratio. In addition, the average power processed by the CCC circuit is only a fraction of the average output power of the micro-inverter. With the previously-indicated control parameters, only 44.43% of the average output power is processed by the CCC (as shown in Appendix II). As a result, the loss caused by the CCC circuit only penalizes a portion of the total power of the micro-inverter, resulting in high overall system efficiency.

Many micro-inverter topologies require all the twice-line-frequency energy buffering to be done by a capacitor placed across the PV panel (e.g., $\rm C_{IN}$ in Fig. 1) [4], [5]. This makes the size of the energy buffering capacitor large, since there is a limit (of typically 10% peak-to-peak) on the maximum voltage ripple allowed across the PV panel (to ensure it is operating near it maximum power point) resulting in a low utilization of the energy in $\rm C_{IN}$. In the MEB micro-inverter, the buffer capacitor, $\rm C_{BUF}$, absorbs energy when the SCEB is in the Step-down or Bypass mode (i.e., when the power delivered to the grid is low), and delivers energy to the grid when the SCEB is in the Step-up mode (i.e., when the power delivered to the grid is high). In this way, $\rm C_{BUF}$ functions as the storage element of an active energy buffer and can be used to replace the $\rm C_{IN}$ with bulk size. Since $\rm C_{BUF}$ is not across the PV panel, a larger voltage ripple is allowed across it than would otherwise be permissible. This increases the utilization of energy in $\rm C_{BUF}$ and allows a smaller capacitor to be used, creating spaces for the added semiconductor devices in the MEB. As a result, the overall size of the MEB stage (plus a much smaller input capacitor) is demonstrated to be equivalent to the size of the original bulk input capacitor. The size of

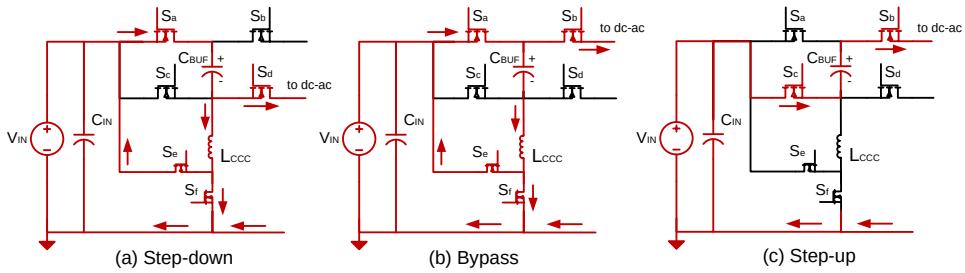


Fig. 6. Current flow directions in the MEB during the three operating modes: (a) Step-down mode, (b) Bypass mode and (c) Step-up mode.

the MEB stage can potentially be further reduced by using a Stacked Switched Capacitor (SSC) energy buffer instead of a single capacitor [14], [15].

B. Design of the dc-ac converter stage

A series-resonant high-frequency-link dc-ac converter is chosen as the dc-ac converter stage. The MEB provides two benefits to the dc-ac converter stage: a reduced transformer turns ratio, and a compressed operation range.

The transformer turns ratio of the dc-ac converter stage needs to satisfy $\frac{N_2}{N_1} > \frac{v_{S,1}(\theta)}{v_{P,1}(\theta)}$, where $v_{P,1}$ and $v_{S,1}$ are the fundamental components of v_P and v_S (Fig. 3). Without the MEB, assuming square-wave switching of a full-bridge, $v_{P,1} = \frac{4}{\pi} V_{IN} \sin(\theta)$, and $v_{S,1} = \frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)$; thus:

$$\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)}{\frac{4}{\pi} V_{IN} \sin(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{2 V_{IN}}. \quad (1)$$

This is a lower bound on the required transformer turns ratio if there is no MEB. With the MEB, as described in Section III-A, $v_{P,1} = \frac{4}{\pi}(V_{IN} + V_{BUF}) \sin(\theta)$, and $v_{S,1} = \frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)$; thus:

$$\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)}{\frac{4}{\pi}(V_{IN} + V_{BUF}) \sin(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{2(V_{IN} + V_{BUF})}. \quad (2)$$

If $v_{BUF} = 0.6 V_{IN}$, then $\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{3.2 V_{IN}}$. In this case, ideally the MEB reduces the transformer turns ratio of the dc-ac converter stage by a factor of 1.6.

The MEB also provides unique opportunities in the control of the dc-ac converter stage. To keep the explanation of this benefit simple, we assume in the following analysis that the dc-ac converter stage is under pure frequency control. In practice, both frequency control and phase-shift control are used. When the micro-inverter has no MEB, and if the resonant inverter is designed to operate at its resonant frequency when the line voltage is at its peak, then its required switching frequency, f_{noMEB}, as function of line angle θ ($0° < \theta < 180°$), is given by:

$$f_{noMEB}(\theta) = \frac{\frac{X_{cyclo} C_R}{N^2} |\cot(\theta)| + \sqrt{(\frac{X_{cyclo} C_R}{N^2} \cot(\theta))^2 + 4 L_R C_R}}{4\pi L_R C_R}. \quad (3)$$

Here, L_R and C_R are the inductance and the capacitance of the resonant tank, respectively, N ($= \frac{N_2}{N_1}$) is the transformer turns ratio, and X_{cyclo} is the impedance of the cycloconverter (or rectifier/unfolder). Under fundamental frequency approximation, for a unity power factor micro-inverter, X_{cyclo} is resistive and given by $\frac{4 V_{IN}^2}{\pi^2 P_{OUT(avg)}}$. When the micro-inverter is designed with the MEB, the required switching frequency, f_{MEB}, as a function of line angle is given by:

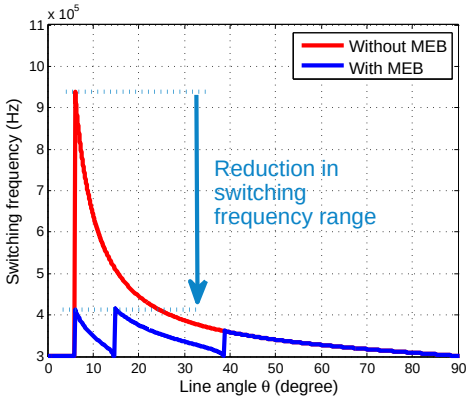


Fig. 7. Calculated switching frequencies of the micro-inverter over a quarter line cycle with and without the MEB with only frequency control, plotted for $P_{OUT(avg)}$ equals 70 W, $C_R = 62$ nF, $L_R = 4.5$ μH, $V_{IN} = 27$ V, $V_{BUF} = 16.2$ V, $V_{GRID} = 230$ V_{rms}. The transformer turns ratio for the micro-inverter with the MEB is 5:28, and the transformer turns ratio for the micro-inverter without the MEB is 4:28. The value of $X_{P,cyclo}$ is 10.7 Ω for the micro-inverter with the MEB, and is 4.22 Ω without the MEB.

$$f_{MEB}(\theta) = \frac{C_R |X_R(\theta)| + \sqrt{C_R^2 X_R(\theta)^2 - 4 L_R C_R}}{4\pi L_R C_R}. \quad (4)$$

Here, $|X_R(\theta)|$ is the magnitude of the impedance of the resonant tank and is given by:

$$|X_R(\theta)| = \sqrt{(\frac{X_{cyclo} v_X(\theta)}{N^2 (V_{IN} + V_{BUF}) \sin(\theta)})^2 - (\frac{X_{cyclo}}{N^2})^2}, \quad (5)$$

where $v_X(\theta)$ is the inverter input voltage as shown in Fig. 4b, and X_{cyclo} equals $\frac{4(V_{IN}+V_{BUF})^2}{\pi^2 P_{OUT(avg)}}$. Figure 7 illustrates the difference in switching frequency operating range across a half-line cycle for the micro-inverter without and with the MEB (computed using (3), (4), respectively). When the resonant frequency of the inverter is chosen to be 300 kHz, the MEB compresses the switching frequency range from 300-950 kHz to 300-410 kHz.

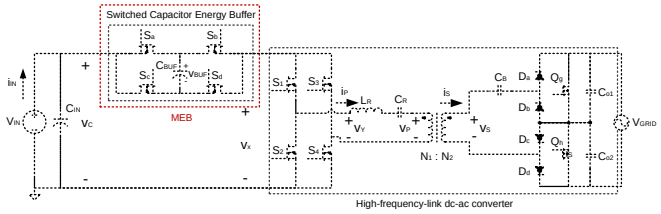


Fig. 8. Schematic of a simplified MEB micro-inverter without the CCC. The charge balance of $C_{\rm BUF}$ is achieved by keeping $cos(\alpha)+cos(\beta)=cos(\delta)$. The SCEB can also be operated in a PWM manner.

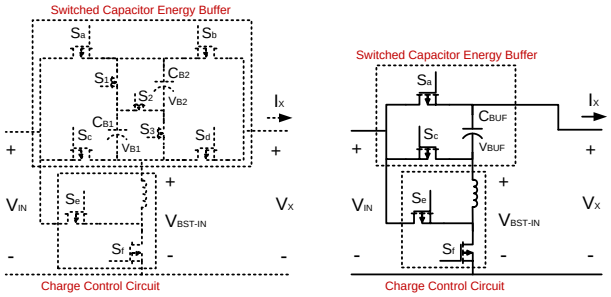


Fig. 9. Topological extensions of the MEB enabling tradeoffs between circuit complexity and performance: (a) A modified MEB stage with seven $v_{\rm x}$ levels: (1) $v_{\rm x}$ equals $V_{\rm IN}-v_{\rm B1}-v_{\rm B2}$ when $\rm S_a$, $\rm S_2$, $\rm S_d$ are on (and other switches in the SCEB are off) ; (2) $v_{\rm x}$ equals $V_{\rm IN}-v_{\rm B1}$ when $\rm S_a$, $\rm S_1$, $\rm S_d$ are on; (3) $v_{\rm x}$ equals $V_{\rm IN}-v_{\rm B2}$ when $\rm S_a$, $\rm S_3$, $\rm S_d$ are on; (4) $v_{\rm x}$ equals $V_{\rm IN}$ when $\rm S_a$, $\rm S_b$ are on; (5) $v_{\rm x}$ equals $V_{\rm IN}+v_{\rm B2}$ when $\rm S_b$, $\rm S_3$, $\rm S_c$ are on; (6) $v_{\rm x}$ equals $V_{\rm IN}+v_{\rm B1}$ when $\rm S_b$, $\rm S_1$, $\rm S_c$ are on; (7) $v_{\rm x}$ equals $V_{\rm IN}+v_{\rm B1}+v_{\rm B2}$ when $\rm S_b$, $\rm S_2$, $\rm S_c$ are on. (b) A modified MEB stage with two $v_{\rm x}$ levels: (1) $v_{\rm x}$ equals $V_{\rm IN}$ when $\rm S_a$ is on; (2) $v_{\rm x}$ equals $V_{\rm IN}+v_{\rm BUF}$ when $\rm S_c$ is on.

IV. Alternative Implementations

The MEB micro-inverter architecture proposed here has many alternative implementations, providing additional design flexibility and tradeoff possibilities. The alternatives are at the level of each sub-block of the architecture, as well as at the overall system level.

Figure 8 shows an alternative MEB micro-inverter architecture with a simplified MEB stage without the CCC. By controlling the switching angles of the SCEB (for example, making the switching angles α, β, and δ satisfy $cos(\alpha)+cos(\beta)=cos(\delta)$ as shown in Appendix III), the charge balance of the $\rm C_{BUF}$ is automatically achieved, thus the CCC can be eliminated, reducing the circuit complexity (while the benefits of the MEB stage to the dc-ac converter are also reduced). Another way is to operate the switches of the SCEB at a higher switching frequency, e.g. in a PWM manner, to synthesize the required voltage difference between a dc voltage and a sinusoidal voltage. The charge balance of $\rm C_{BUF}$ can be obtained by phase-shifting the switches. When the switching frequency of the SCEB is comparable to the switching frequency of the dc-ac converter, the MEB stage can be merged with the inverter switches of the dc-ac converter and becomes a high frequency switched capacitor energy buffer (more closely resembling the system of [6], which has higher switching loss and control complexity). This paper focuses on exploring the concept of combining a low-frequency switched-capacitor stage with a high-frequency dc-ac stage to inherit their strengths in handling different tasks. As a result, a low frequency SCEB with the CCC is selected to minimized the operation range of the dc-ac converter.

In the SCEB, by adding one capacitor and three switches, a modified MEB implementation shown in Fig. 9a can be created. This MEB implementation can produce seven levels of $v_{\rm x}$ and hence synthesizes a voltage that more closely approximates the ac line voltage envelope, leading to further reduction in the operating range of the dc-ac converter. On the other hand, by removing $\rm S_b$ and $\rm S_d$ from the original MEB implementation, the modified implementation shown in Fig. 9b can be created. While this implementation has fewer switches, it only generates a $v_{\rm x}$ having two levels, limiting the compression of the voltage conversion range. To investigate the tradeoff between circuit complexity and performance for the variants of the SCEB, Table I shows and compares the schematics, waveforms, number of switches and frequency modulation ranges of the dc-ac converter if a single capacitor, a two-level SCEB, a three-level SCEB, a five-level SCEB or a seven-level SCEB is used. Increasing $v_{\rm x}$ levels compresses the required frequency modulation range (or, more generally, the operating range) of the dc-ac converter, at the cost of higher circuit complexity.

On the overall system level, an alternative implementation of the MEB micro-inverter is to have the MEB stage on the ac side instead of on the dc side. Instead of synthesizing an approximated replica of the ac line voltage amplitude from the dc input, the MEB stage synthesizes an approximately constant voltage amplitude from the ac line. Hence, it also reduces the voltage conversion range of the high-frequency portion of the system. More details about the operation of the ac side MEB are provided in Appendix IV. Compared to the dc side MEB, the higher operating voltage of the ac side MEB reduces the conduction loss and the total capacitor size (since higher voltage rating capacitors tend to have higher energy density). However, due to the higher operating voltage, the CCC has significantly higher switching loss. Furthermore, since the MEB stage is connected directly to the ac line, this implementation is more complex to drive and control.

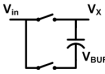
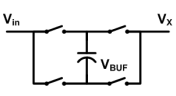
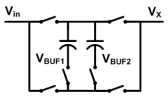
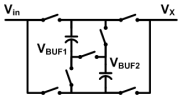
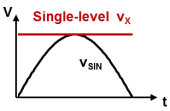
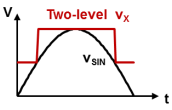
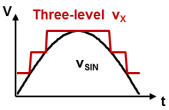
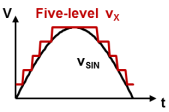
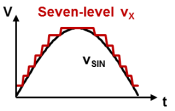
Different alternatives have different advantages and drawbacks in different applications. Since the wide voltage conversion range is a key bottleneck of the micro-inverter incorporating a high-frequency-link resonant dc-ac converter, a MEB that optimally compresses the voltage conversion range of the dc-ac converter is demonstrated in this paper.

V. Prototype Micro-Inverter

To validate the proposed architecture, a prototype MEB micro-inverter, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for 70 W (line cycle average power), has been built, tied to the grid and tested. The peak power rating of the dc-ac converter stage is 140 W, and the peak power rating of the CCC is 68 W. A photograph of the prototype is shown in Fig. 10. Also shown are a pencil and a US quarter to indicate relative size. For comparison purposes, a high-frequency-link micro-inverter without the MEB (and with a different transformer turns ratio) has also been built and

TABLE I

SCHEMATICS, WAVEFORMS, NUMBER OF SWITCHES AND FREQUENCY MODULATION RANGES OF A SINGLE CAPACITOR, A TWO-LEVEL SCEB, A THREE-LEVEL SCEB, A FIVE-LEVEL SCEB AND A SEVEN-LEVEL SCEB. THE FREQUENCY MODULATION RANGE IS CALCULATED FOR THE SAME SETUP AS THAT USED IN FIG. 7.

	Single Capacitor	Two-Level SCEB	Three-Level SCEB	Five-Level SCEB	Seven-Level SCEB
Schematic					
Modulated Multilevel V_X	V_{in}	V_{in} $V_{in} - V_{BUF}$	$V_{in} + V_{BUF}$ V_{in} $V_{in} - V_{BUF}$	$V_{in} + V_{BUF2}$ $V_{in} + V_{BUF1}$ V_{in} $V_{in} - V_{BUF1}$ $V_{in} - V_{BUF2}$	$V_{in} + V_{BUF1} + V_{BUF2}$ $V_{in} + V_{BUF2}$ $V_{in} + V_{BUF1}$ V_{in} $V_{in} - V_{BUF1}$ $V_{in} - V_{BUF2}$ $V_{in} - V_{BUF1} - V_{BUF2}$
Voltage Waveforms					
Complexity	1 Capacitor 0 Switch	1 Capacitor 2 Switches	1 Capacitor 4 Switches	2 Capacitors 6 Switches	2 Capacitors 7 Switches
Frequency Modulation Range	300kHz~950kHz	300kHz~600kHz	300kHz~410kHz	300kHz~350kHz	300kHz~320kHz

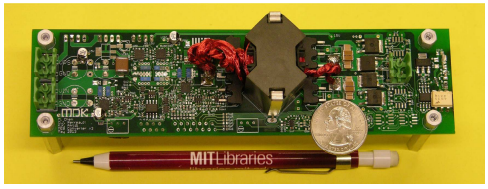


Fig. 10. Photograph of the prototype MEB micro-inverter. Also shown are a pencil and a US quarter to indicate relative size.

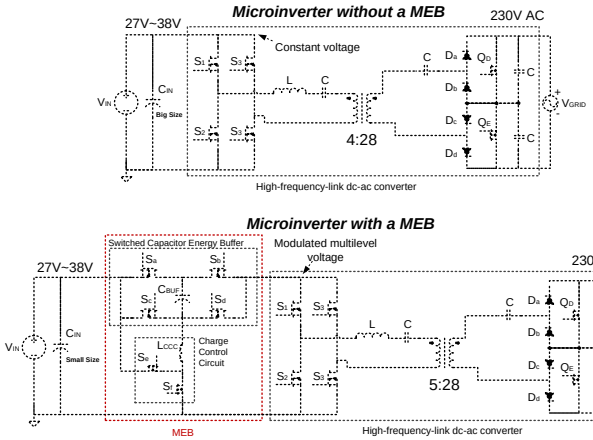


Fig. 11. Schematics of the prototyped micro-inverter without and with the MEB. The MEB stage replaces the original bulk input capacitor. A small C_{IN} is still needed to hold the voltage across the solar panel constant.

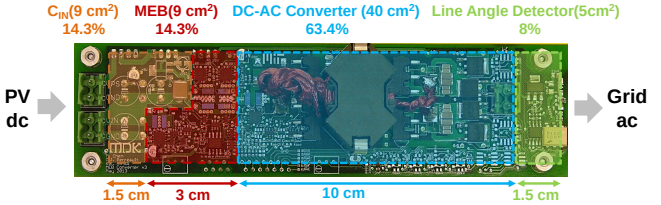


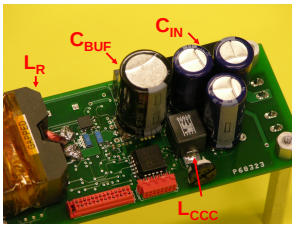
Fig. 12. Board area used by the various functional blocks of the MEB micro-inverter. The micro-inverter without the MEB is implemented on the same board with the space labeled as "MEB" replaced by additional input capacitors. The ac power density is about $1\mathrm{W/cm^3}$.

tested (on the same PCB board with a blank MEB stage). The schematic of these two prototypes are shown in Fig. 11. The components used in these two prototypes are listed in Table II. The board area used by the various functional blocks in the case of the micro-inverter with the MEB is shown in Fig. 12. The MEB stage collectively uses 14.3% of the total board area. The micro-inverter without the MEB is implemented on the same board with the space of the MEB replaced by additional input capacitors. Figure 13a shows the back side of the board where some major passive components - C_{IN}, C_{BUF}, L_{CCC}, and L_R - are placed. The transformer is on the front side of the board and is shown in Fig. 10.

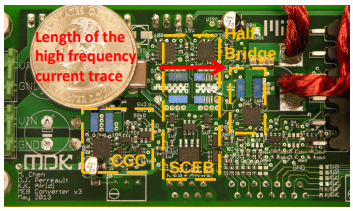
The switch and gate drive implementations of the MEB are shown in Fig. 14. The required voltage and current ratings of the six switches in the MEB stage are listed in Table III. S_a has the highest current rating because it needs to handle the sum of the current of the CCC and the dc-ac converter block. S_b and S_c have higher current ratings than S_d because they are conducting in the step-up mode when the line current is high. Gallium Nitride (GaN) switches manufactured by EPC (a semiconductor company) are selected and intentionally oversized. This improves the transient and fault capability, with negligible increase in overall area. Further optimizations can be made if more advanced GaN switches become available. Three half-bridge gate drives (LM5113) drive these

TABLE II
MICRO-INVERTER COMPONENT LISTS FOR THE SCHEMATIC SHOWN IN FIG. 11.

Name	**With MEB**	**Without MEB**
C_{IN}	3 × 1 mF, 50 V, Panasonic ECA-1HM102 (3.4 cm^3 each)	5 × 1 mF, 50 V, ECA-1HM102 (3.4 cm^3 each)
C_{BUF}	5.6 mF, 25 V, Panasonic EEU-HD1E562 (5.4 cm^3)	Not required
C_{o1} & C_{o2}	Two EPCOS film capacitors, 0.2 uF, 630 V, 2 cm^3	
Total Cap Size	15.6 cm^3	17 cm^3
$S_{b,d}$	EPC2016 100 V 11 A GaN FETs	
$S_{a,c,e,f,1,2,3,4}$	EPC2001 100 V 25 A GaN FETs	
$Q_{g,h}$	Infineon IPD65R380C6 CoolMOS MOSFETs	
$D_{a,b,c,d}$	CREE CSD01060 SiC Schottky diodes	
L_R	4.3 uH, R_{dc} smaller than 4mΩ, size: 15.75 cm^3; Core area: 3 cm^2	
L_{CCC}	10 uH, R_{dc} smaller than 10 mΩ, size: 1 cm^3	Not needed
C_R	60 nF (10nF × 6) 100 V 1206 C0G Ceramic	
Transformer	RM12-3F3, Primary: 5 turns, Secondary: 28 turns	RM12-3F3, Primary: 4 turns, Secondary: 28 turns
CCC control	fixed duty ratio control with LTC6992 VCO	Not Needed
Full bridge timing	LTC6990 VCO with LTC6994 time delay block	
Gate drive ICs for Ss	TI LM5113; Five half-bridge pairs: (S_a-S_c), (S_b-S_d), (S_e-S_f), (S_1-S_2), (S_3-S_4)	
Gate Drive ICs for Qs	Silicon labs Si8420 digital isolator	
Optocoupler	Fairchild 4N35 optocoupler	



(a)



(b)

Fig. 13. (a) Photograph of the back side of the board showing: C_{IN}, C_{BUF}, L_{CCC}, and L_R. (b) PCB layout of the MEB comparing the size of the MEB and a US quarter. The area of the high-frequency current loop is minimized.

six switches. The gate drive IC for S_e and S_f is referenced to ground. The gate drive ICs for S_a, S_b, S_c, and S_d are referenced to the negative terminal of C_{BUF}, and can be powered by v_{BUF} through a 5V linear regulator when v_{BUF} is larger than 5 V. In the precharge period, S_a conducts in reverse to charge C_{BUF} when v_{BUF} is smaller than 5 V. As a result, no isolated power supply for the gate drive is needed. The high-frequency-current ripple created by the full bridge passes through the SCEB and is buffered by C_{IN}. The size of the MEB stage is compared to a US quarter in Fig. 13b.

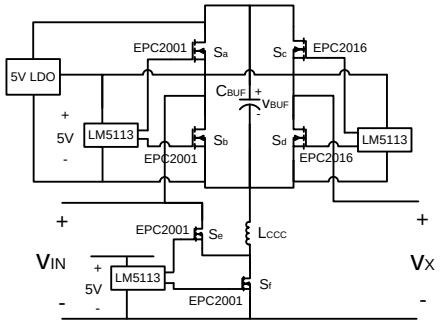


Fig. 14. Switch and gate drive implementation of the MEB.

Figure 13b also shows the length of the high frequency current path through the SCEB switches. The extremely small size of the GaN switches and careful PCB layout enables low parasitic inductances and mitigates possible parasitic effects. The CCC is designed to switch at 500 kHz.

The four switches in the full-bridge inverter (S_1-S_4) are also GaN switches. Their low output capacitance enables high-frequency switching, and helps to reduce any loss caused by the stepped waveform of v_X. A 4.5 μH inductor and a 60 nF (6 × 10nF) NP0/C0G ceramic capacitor (with low equivalent series resistance) form the series resonant tank of the inverter, with a resonant frequency of 300 kHz. The dc-ac converter stage is operated above the resonant frequency to achieve ZVS soft switching. The MEB increases the input voltage of the dc-ac converter stage during a portion of the line cycle. As a result, the peak voltage stress of the switches in the full-bridge is higher than in the micro-inverter without a

TABLE III
REQUIRED VOLTAGE RATINGS (MAXIMUM BLOCKING VOLTAGE) AND CURRENT RATINGS (MAXIMUM RMS CURRENT) OF THE POWER SWITCHES IN THE MEB STAGE. $V_{\mathrm{IN(max)}}$ IS THE MAXIMUM INPUT VOLTAGE (38 V). $V_{\mathrm{IN(min)}}$ IS THE MINIMUM INPUT VOLTAGE (27 V). $P_{\mathrm{OUT(avg,max)}}$ IS THE MAXIMUM LINE CYCLE AVERAGE OUTPUT POWER (70 W). $\alpha = 12.8°$ AND $\beta = 40.9°$. D IS THE DUTY RATIO OF $\mathrm{S_e}$ (0.4). γ_{CCC} IS THE FRACTION OF LINE CYCLE AVERAGE OUTPUT POWER PROCESSED BY THE CCC (44.43%). THE PEAK POWER RATING OF THE PROTOTYPE MICRO-INVERTER IS 140 W.

Switch	Required voltage rating	Required current rating
$\mathrm{S_a}$	23 V [$=(1-D)\ V_{\mathrm{IN(max)}}$]	7.40 A [$=\frac{90°\gamma_{\mathrm{CCC}}P_{\mathrm{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\mathrm{IN(min)}}} + \frac{2P_{\mathrm{OUT(avg,max)}}}{(1+D)V_{\mathrm{IN(min)}}}\sin(\beta)$]
$\mathrm{S_b}$	23 V [$=(1-D)\ V_{\mathrm{IN(max)}}$]	3.24 A [$=\frac{2P_{\mathrm{OUT(avg,max)}}}{(1+D)V_{\mathrm{IN(min)}}}$]
$\mathrm{S_c}$	23 V [$=(1-D)\ V_{\mathrm{IN(max)}}$]	3.24 A [$=\frac{2P_{\mathrm{OUT(avg,max)}}}{(1+D)V_{\mathrm{IN(min)}}}$]
$\mathrm{S_d}$	23 V [$=(1-D)\ V_{\mathrm{IN(max)}}$]	0.72 A [$=\frac{2P_{\mathrm{OUT(avg,max)}}}{(1+D)V_{\mathrm{IN(min)}}}\sin(\alpha)$]
$\mathrm{S_e}$	38 V [$=V_{\mathrm{IN(max)}}$]	2.11 A [$=(1-D)\frac{90°\gamma_{\mathrm{CCC}}P_{\mathrm{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\mathrm{IN(min)}}}$]
$\mathrm{S_f}$	38 V [$=V_{\mathrm{IN(max)}}$]	3.16 A [$=D\frac{90°\gamma_{\mathrm{CCC}}P_{\mathrm{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\mathrm{IN(min)}}}$]

MEB. However, the current stress of the full-bridge switches is reduced with the MEB present.

The MEB reduces the transformer turns ratio. However, since the transformer volt-seconds and the number of turns on the secondary are the same with or without the MEB, the MEB converter has more primary side turns. The transformer turns ratio is 4:28 in the converter without the MEB, and 5:28 in the MEB converter.

Four Cree CSD01060 Silicon Carbide (SiC) diodes and two Infineon IPD65R380C6 power transistors are used for the combined rectifier and unfolder stage (cycloconverter). While using diodes increases the losses in the cycloconverter stage, it avoids the control complexity of synchronous conversion. To further improve efficiency, synchronous cycloconverter designs similar to those in [5], [6] can be used. If a synchronous cycloconverter is implemented, power can be controlled by phase shifting the full-bridge inverter relative to the cycloconverter in addition to frequency control, full-bridge phase-shift control, and burst-mode control of the inverter (e.g., [5], [6], [21]–[24]).

An opto-isolated line angle detector is implemented to synchronize the micro-inverter with the grid. It senses the zero crossing and the polarity of the line voltage, and computes the line angle. A state machine triggered by the line angle detector is implemented in a micro-controller (MCU). The state machine uses the line angle and a look-up table to control all switches in the system. It controls the output power, and modulates the output current to be sinusoidal in phase with the line voltage. The look-up table for the state machine over a quarter line cycle at full power operation is shown in Table IV. This pattern is repeated in the remaining portions of the line cycle. Considering an inverter phase-shift range of up to 20 degrees (each half-bridge goes positive or negative 10 degrees from center), it is experimentally verified that the MEB helps to compress the frequency control range of the dc-ac converter block from 310-500 kHz to 310-368 kHz when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W (see Fig. 15).

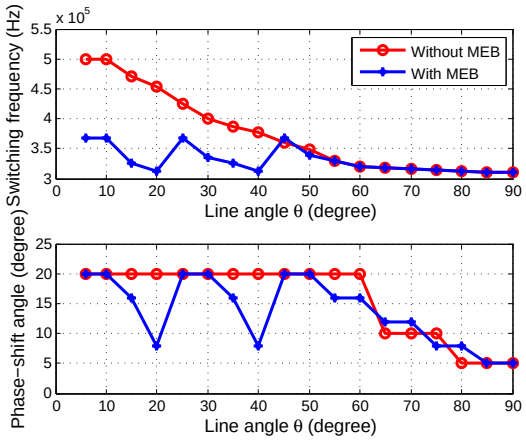


Fig. 15. Frequency and phase modulation range of the micro-inverter without and with the MEB. Range plotted for $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W.

VI. EXPERIMENTAL RESULTS

The prototype MEB micro-inverter described in the previous section has been tested in both islanded and grid-connected mode. Figure 16 shows the waveforms of the MEB micro-inverter when it is delivering full power (line cycle average output power, $P_{\mathrm{OUT(avg)}}$, of 70 W) from a 27 V dc input into a 230 $\mathrm{V_{rms}}$ (60 Hz) ac mains. The output current, i_{GRID}, has a sinusoidal shape and is in phase with the line voltage. EMI filter is not included. A small EMI filter can further null the switching noise. The input voltage of the dc-ac converter stage, v_{X}, is also shown in Fig. 16. As expected it follows a staircase pattern, synchronized with the line voltage, similar to the idealized waveform of Fig. 4b. However, unlike in the idealized waveform there is an expected droop of about 4 V in v_{X} during the Step-up mode as the finite sized buffer capacitor, $\mathrm{C_{BUF}}$, is being discharged. To maintain high efficiency, all the switches in the full-bridge inverter of the dc-ac converter stage are soft-switched by operating the inverter at switching frequencies above resonance. Figure 17 illustrates the soft-switching of switch $\mathrm{S_1}$, when the MEB micro-inverter has an input voltage of 27 V and an average output power of 48 W while switching at 312 kHz. In Fig. 17 the inverter output current, i_{P}, is negative when $\mathrm{S_1}$ turns on, ensuring that the current is flowing through its anti-parallel diode and holding its voltage near zero volts during switch turn-on.

The expected advantages of the MEB micro-inverter com-

TABLE IV
LOOK-UP TABLE FOR THE MICRO-CONTROLLER OF THE MICRO-INVERTER WITHOUT AND WITH THE MEB WHEN $V_{\rm IN} = 30$ V AND $P_{\rm OUT(avg)} = 70$ W.

	Without MEB		**With MEB**				
Line angle θ	$f_{\rm FM}$(kHz)	$\delta_{PM}(^\circ)$	**SCEB Mode**	**CCC**	$f_{\rm FM}$(kHz)	$\delta_{PM}(^\circ)$	**Cycloconverter**
$0^\circ \rightarrow 6^\circ$	dead-angle (Micro-inverter off)						
$6^\circ \rightarrow 15^\circ$	500	20	Step-down	On	368	20	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$15^\circ \rightarrow 20^\circ$	470	20	Bypass	On	325	16	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$20^\circ \rightarrow 25^\circ$	454	20	Bypass	On	312	8	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$25^\circ \rightarrow 30^\circ$	425	20	Bypass	On	368	20	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$30^\circ \rightarrow 35^\circ$	400	20	Bypass	On	335	20	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$35^\circ \rightarrow 40^\circ$	386	20	Bypass	On	325	16	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$40^\circ \rightarrow 45^\circ$	378	20	Step-up	Off	312	8	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$45^\circ \rightarrow 50^\circ$	360	20	Step-up	Off	368	20	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$50^\circ \rightarrow 55^\circ$	348	20	Step-up	Off	340	20	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$55^\circ \rightarrow 60^\circ$	330	20	Step-up	Off	330	16	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$60^\circ \rightarrow 65^\circ$	320	20	Step-up	Off	320	16	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$65^\circ \rightarrow 70^\circ$	318	10	Step-up	Off	318	12	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$70^\circ \rightarrow 75^\circ$	316	10	Step-up	Off	316	12	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$75^\circ \rightarrow 80^\circ$	314	10	Step-up	Off	314	8	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$80^\circ \rightarrow 85^\circ$	312	5	Step-up	Off	312	8	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$85^\circ \rightarrow 90^\circ$	311	5	Step-up	Off	311	5	$Q_{\rm h}$ on, $Q_{\rm g}$ off
$90^\circ \rightarrow 180^\circ$	Same as $90^\circ \rightarrow 0^\circ$						$Q_{\rm h}$ on, $Q_{\rm g}$ off
$180^\circ \rightarrow 270^\circ$	Same as $0^\circ \rightarrow 90^\circ$						$Q_{\rm h}$ off, $Q_{\rm g}$ on
$270^\circ \rightarrow 360^\circ$	Same as $90^\circ \rightarrow 0^\circ$						$Q_{\rm h}$ off, $Q_{\rm g}$ on

TABLE V
PROTOTYPE SPECIFICATIONS

Input voltage range	27 V to 38 V dc
Output voltage	230 V rms ac
Line cycle average power	70 W (peak power: 140 W)

pared to the one without the MEB are in terms of efficiency and the total size of the twice-line-frequency buffering capacitors. To confirm these advantages, the performance of the prototype MEB micro-inverter is compared with the performance of the prototype micro-inverter without the MEB. Both micro-inverters have been designed for the same specifications as shown in Table V. The maximum line cycle average power delivery capability of the two prototypes has been confirmed by running them into the ac mains, and their instantaneous peak power capability has been confirmed by operating them in islanded mode into a resistive load. Figure 18 shows the measured waveforms for the two prototype micro-inverters while delivering power into the 230 $V_{\rm rms}$ (60 Hz) mains. Note the difference in the waveform of the input voltage of the dc-ac converter stage, $v_{\rm X}$, for the two prototypes. This voltage ($v_{\rm X}$) is modulated into staircase pattern in the micro-inverter with the MEB (Fig. 18a), but is constant in the micro-inverter without the MEB (Fig. 18b).

Since the MEB stage is isolated from the line by the dc-ac converter stage, the MEB stage has no impacts on the power factor and THD. Due to the high switching frequency of the dc-ac converter stage, even without the EMI filter, the prototype maintains the power factor between 98% and 99.5%, and THD between 15% and 23% in repeating measurements.

System startup waveforms of the MEB micro-inverter are

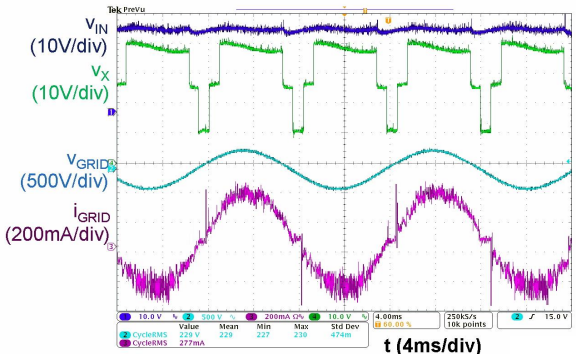


Fig. 16. Waveforms of the MEB micro-inverter, when $V_{\rm IN} = 27$ V, $V_{\rm GRID} = 230 V_{\rm rms}$ and $P_{\rm OUT(avg)} = 70$ W. The power factor in this measurement is 98.2% and the THD is 23% (without the EMI filter).

shown in Fig. 19a. It takes about 400 ms to charge up $C_{\rm IN}$ and $C_{\rm BUF}$. Figure 19b shows the converter waveforms as the load steps from 25 W to 35 W. The ripple in $v_{\rm X}$ is slightly larger after the load step because $C_{\rm BUF}$ is being discharged by a larger output current. Both the startup and the load-step-up were commanded near a zero-crossing of the line voltage to minimize the transient impacts.

A. *Efficiency Comparison*

The line cycle average efficiency of the two prototypes is measured across a range of line cycle average power levels while the micro-inverters were operating in grid-connected mode. The measured efficiency for the micro-inverter with and without the MEB is plotted in Fig. 20 for two different input voltages levels: 30 V and 33 V. At both input voltages, the micro-inverter with the MEB has a higher efficiency across the

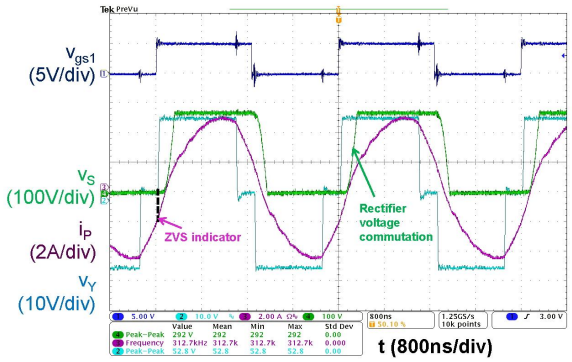
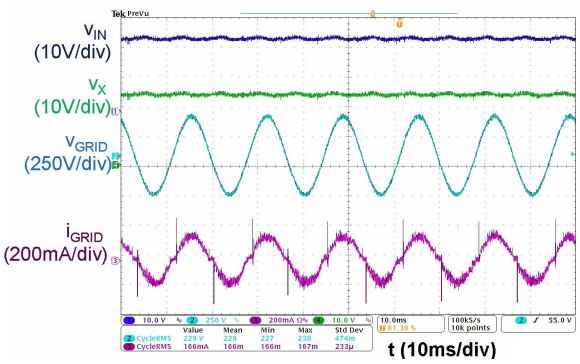
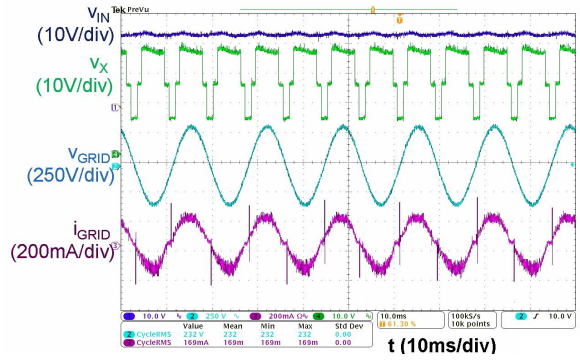


Fig. 17. Waveforms of the MEB micro-inverter showing soft-switching of the full bridge when the switching frequency is 312 kHz, $V_{\rm IN} = 27$ V, $V_{\rm GRID} = 230$ $\rm V_{rms}$ and $P_{\rm OUT(avg)} = 48$ W. $v_{\rm gs1}$ is the gate signal of $\rm S_1$; $v_{\rm S}$ is the voltage at the switching node of the rectifier; $i_{\rm P}$ is the inverter resonant current; and $v_{\rm Y}$ is the voltage generated by the full bridge.

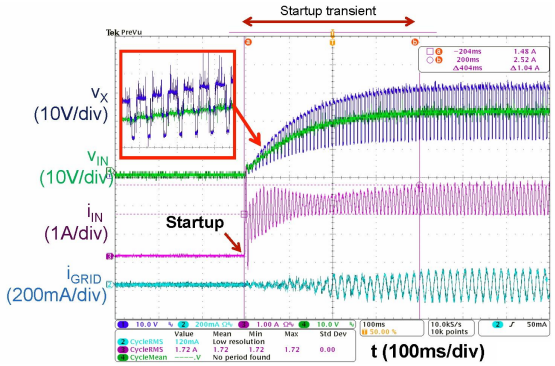


(a)

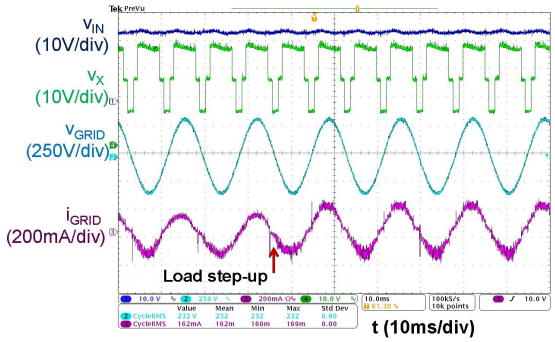


(b)

Fig. 18. Waveforms of the micro-inverter (a) without the MEB (power factor of 99.1% and THD of 19%), and (b) with the MEB (power factor of 98.4% and THD of 23%) without EMI filters. Both figures are measured under the same set-up: $V_{\rm IN} = 27$ V, $V_{\rm GRID} = 230$ $\rm V_{rms}$, $P_{\rm OUT(avg)} = 38.4$ W. Note: the power factors and THDs provided here are calculated from the example measurements shown in the figure. The power factors of two prototype are both maintained between 98% and 99.5%, and the THDs are both maintained between 15% and 23% in all measurements.



(a)



(b)

Fig. 19. (a) System start-up waveforms of the MEB micro-inverter when $V_{\rm IN} = 27$ V, $V_{\rm GRID} = 230$ $\rm V_{rms}$, and $P_{\rm OUT(avg)} = 38.4$ W; (b) Load step-up waveforms of the MEB micro-inverter when $V_{\rm IN} = 27$ V, $V_{\rm GRID} = 230$ $\rm V_{rms}$, and $P_{\rm OUT(avg)}$ steps from 25 W to 35 W.

measured power range of 15 W to 70 W. Although the MEB introduces small additional losses, it significantly reduces the losses in the dc-ac converter stage by compressing its operating range. Hence, resulting in an overall higher system efficiency. The MEB is more effective at improving converter efficiency in the low power range, when the switching frequency without its presence is very high. It is less effective in improving efficiency at the high power range since both micro-inverters are already operating close to the resonant frequency. For both micro-inverters, a higher input voltage results in lower efficiency. This is because a higher input voltage requires a larger voltage to be dropped across the resonant tank of the inverter, meaning that the inverter must be operated at a higher switching frequency and leading to higher losses.

The efficiency of a micro-inverter system can be evaluated either by the California Energy Commission (CEC) efficiency weighting (Table VI), or by the European Efficiency weighting (Table VII). The CEC efficiency places more weight on high power operation, and the European Efficiency places more weight on low power operation. The measured CEC efficiency of the micro-inverter increased from 91.1% to 92.4% by adding the MEB stage, and the measured European Efficiency increased from 85.7% to 89.4% by adding the MEB stage. Table VIII summarizes the measured efficiency of the two prototype micro-inverters, together with the average power factors and THDs when doing these measurements (power factor $> 98\%$ and $15\% <$ THD $< 23\%$). The efficiency of the two micro-inverters can be further enhanced by using a synchronous cycloconverter (e.g. [5], [6]) instead of the diode-based rectifier/unfolder utilized here.

To better understand the tradeoffs of adding a MEB stage to the micro-inverter, a loss breakdown analysis of the micro-inverter with and without the MEB is necessary. To investigate the loss breakdown percentage, the efficiencies of each func-

TABLE VIII
EFFICIENCIES, POWER FACTORS AND THDS OF THE MICRO-CONVERTER WITH AND WITHOUT THE MEB FOR DIFFERENT OUTPUT POWERS (AVERAGE OF FIVE MEASUREMENTS). NOTE: $V_{\rm in} = 30$ V. THE MICRO-INVERTER HAS NO LINE-FREQUENCY EMI FILTER.

	Efficiency		**Power Factor**		**THD**	
	Without MEB	**With MEB**	**Without MEB**	**With MEB**	**Without MEB**	**With MEB**
20% output power (14W)	79.2%	85.3%	98.1%	98.2%	21%	19%
40% output power (28W)	84.9%	88.2%	98.6%	98.4%	17%	15%
60% output power (42W)	89.3%	92.1%	98.4%	99.1%	19%	23%
80% output power (56W)	93.1%	94.1%	98.8%	98.9%	18%	20%
100% output power (70W)	93.9%	94.2%	99.1%	99.2%	17%	15%
CEC efficiency	91.1%	92.4%	-	-	-	-
European efficiency	85.7%	89.4%	-	-	-	-

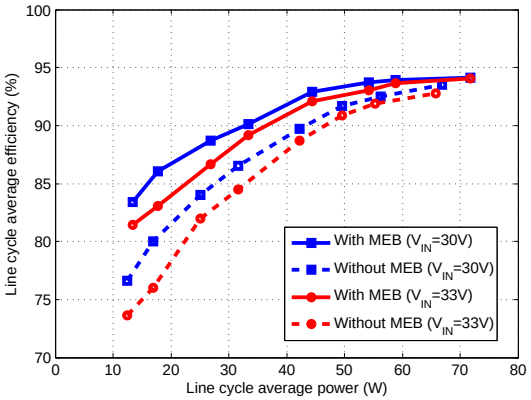


Fig. 20. Line cycle average efficiency of the micro-inverter with and without the MEB, with $V_{\rm GRID} = 230$ $\rm V_{rms}$, and $V_{\rm IN} = 30$ V or 33 V. The efficiency when $V_{\rm IN} = 33V$ is lower because more voltage is dropped on the resonant tank, yield higher circulating current loss.

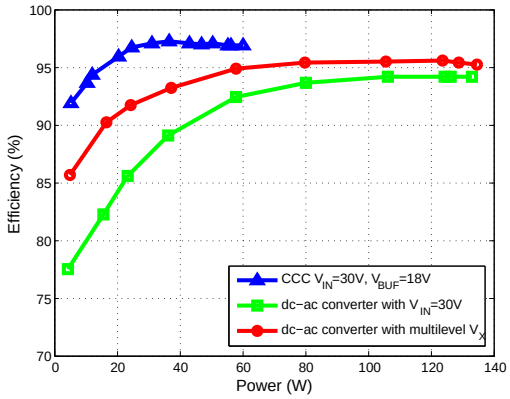


Fig. 21. Measured efficiency of the CCC, the dc-ac converter block with a fixed input voltage, and the dc-ac converter block with a multilevel input voltage when $V_{\rm IN} = 30$ V and $P_{\rm OUT(avg)} = 70$ W. The peak power rating of the dc-ac converter block is 140 W, and the peak power rating of the CCC is 68 W.

TABLE VI
CEC EFFICIENCY WEIGHTING [25].

Output Power	**100%**	**75%**	**50%**	**30%**	**20%**	**10%**
Weight	0.05	0.53	0.21	0.12	0.05	0.04

TABLE VII
EUROPEAN EFFICIENCY WEIGHTING [26].

Output Power	**100%**	**50%**	**30%**	**20%**	**10%**	**5%**
Weight	0.20	0.48	0.10	0.13	0.06	0.03

tion block (MEB, dc-ac converter) are separately measured. To measure the efficiency of the MEB, switch $\rm S_a$ is kept on, while switches $\rm S_b$, $\rm S_c$ and $\rm S_d$ are kept off. A variable resistive load is placed across the buffer capacitor, $\rm C_{BUF}$, to vary the power drawn by the CCC from close to 0 W to 60 W. The efficiency of the dc-ac converter block is measured under conditions mimicking its operation without and with the MEB. First its efficiency is measured with a fixed input voltage, $V_{\rm IN}$, of 30 V and with frequency control similar to that used in the micro-inverter without the MEB, as given by (3). Next its efficiency is measured with a multilevel input voltage (mimicking the output of the MEB) created by externally adjusting the voltage of a dc voltage source. When doing these measurements, the input current flows through $\rm S_a$ and $\rm S_c$ to imitate the conduction loss of the SCEB. The output power is controlled using frequency control similar to that used in the micro-inverter with the MEB, as given by (4). In both cases the efficiency of the dc-ac converter block is measured across its full instantaneous power range (0 V to 140 W). The results of these efficiency measurements are shown in Fig. 21. These results are used to identify the power losses in each of the micro-inverter function blocks.

The results of a loss breakdown analysis for the micro-inverter with and without the MEB are shown in Fig. 22. This loss breakdown analysis is done for an input voltage of 30 V and average output power in the range of 10 W to 70 W. The MEB stage introduces additional loss, but significantly improves the efficiency of the dc-ac converter block. The increased input voltage reduces the inverter current, thus reduces the conduction loss in the switches, the resonant tank and the primary side winding of the transformer. The compressed frequency range not only reduces the magnetic core losses, but also limits the ac resistance of the winding and reduces its conduction losses. For example, when $\rm P_{OUT(avg)} = 70$ W, the conduction loss in the dc-ac converter is reduced by 0.4 W, the inductor core loss is reduced by 0.6 W, and the transformer

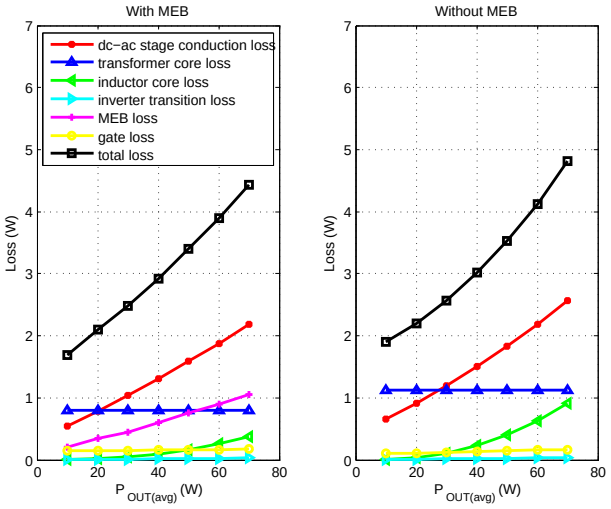


Fig. 22. Loss break-down comparison between the micro-inverter with and without the MEB, when $V_{\rm IN} = 30$ V and $P_{\rm OUT(avg)}$ sweep between 10 W and 70 W.

core loss is reduced by 0.4 W. Hence, even with the additional 1 W loss in the MEB stage, the system with the MEB has about 0.4 W less loss than the system without the MEB.

B. Capacitor Size Comparison

In the MEB micro-inverter the twice-line-frequency energy buffering is provided by both $\rm C_{IN}$ and $\rm C_{BUF}$. Since there is no strict voltage ripple constraint for $\rm C_{BUF}$, moving some buffering capacitance from $\rm C_{IN}$ to $\rm C_{BUF}$ reduces the total size of the capacitors. Selecting the relative sizes of $\rm C_{IN}$ and $\rm C_{BUF}$ requires a trade-off. Buffering more energy in $\rm C_{BUF}$ reduces the total capacitor size, but introduces more ripple in the dc-ac converter block's input voltage, $v_{\rm X}$. A larger variation in $v_{\rm X}$ complicates the control of the dc-ac converter block and increases the peak voltage stress on the full-bridge switches. The potential for capacitor size reduction also depends on the allowed voltage ripple across the PV panel. As the voltage ripple allowance at the output of the solar panel becomes smaller, the amount of total capacitor size reduction possible with the MEB becomes larger.

In the prototype MEB micro-inverter, three 1 mF, 50 V capacitors (Panasonic ECA-1HM102) serve as $\rm C_{IN}$, while one 5.6 mF, 25 V capacitor (Panasonic EEU-HD1E562) serves as the $\rm C_{BUF}$. The total volume of these capacitors is 15.6 $\rm cm^3$. It is experimentally verified that with an input voltage of 27 V and an average output power of 70 W (worst case), the MEB micro-inverter has a 7% peak-to-peak voltage ripple across $\rm C_{IN}$ (and a 4 V peak-to-peak voltage ripple across $\rm C_{BUF}$). To achieve the same voltage ripple across $\rm C_{IN}$ without the MEB, five 1 mF, 50 V capacitors (Panasonic ECA-1HM102) must serve as $\rm C_{IN}$. The total volume of these capacitors is 17 $\rm cm^3$, which is 9% larger than the total capacitor volume in the MEB micro-inverter. This volume reduction creates spaces for the additional semiconductor devices in the MEB stage. The volume of the MEB stage can be further reduced if a narrower ripple is allowed at the micro-inverter input and/or a larger ripple on $\rm C_{BUF}$ can be managed.

VII. Comparisons and Discussions

Table IX compares the figure-of-merit (FOM) of some recently proposed multiple-stage micro-inverter topologies with the micro-inverters (with and without the MEB, Fig. 11) prototyped in this work. Compared to [13], [26], [27], the prototyped MEB micro-inverter achieves higher efficiency and eliminates the need for a bulky line frequency filter. Compared to the topology proposed in [5], the prototyped micro-inverters have similar high-frequency-link dc-ac stage. As a benefit of the MEB stage, the high-frequency-link dc-ac stage in the MEB micro-inverter achieves higher efficiency at a higher switching frequency. The overall system efficiencies are comparable, but the MEB micro-inverter is switching at a higher frequency, resulting in higher power density. It also reduces the twice-line-frequency energy buffering capacitance. Compared to [28], the prototyped MEB micro-inverter achieves comparable CEC efficiency at a lower power rating, and eliminates the need for a bulky line frequency filter. Compared to the prototyped micro-inverter without the MEB, the MEB micro-inverter achieves higher CEC and European efficiencies without increasing the system size. The additional switches in the MEB have low power ratings, small foot prints, and are easy to drive and control. These advantages will be further enhanced by the continued evolution of semiconductor technologies.

The MEB architecture represents a new concept which integrates low frequency switched capacitor circuits with high-frequency-link dc-ac converters. It inherits the advantages of switched capacitor circuits in handling wide voltage conversion range, and the advantages of high-frequency-link dc-ac converters in achieving high power density and high efficiency for grid interfacing (without line frequency filtering).

VIII. Conclusions

This paper introduces a MEB stage for grid-interfaced micro-inverters. The MEB significantly reduces the voltage conversion range that the high-frequency dc-ac converter portion of the micro-inverter must operate over by stepping its input voltage in pace with the line voltage. This enables the dc-ac converter stage to operate over a narrower operating range and achieve higher efficiency. The MEB also functions as an active energy buffer, which helps to reduce the total size of the twice-line-frequency energy buffering capacitance, creating space for the additional components in the MEB. A prototype 70 W MEB micro-inverter, designed for 27 V to 38 V dc input and 230 V rms ac output, has been built, and used to validate the operational principles and performance advantages of the MEB micro-inverter. This MEB based architecture can be applied more broadly to converters interfacing between low-voltage dc and the single-phase ac grid.

Acknowledgment

The authors gratefully acknowledge the support provided for this work by Enphase Energy.

TABLE IX
FOM OF MANY RECENTLY PUBLISHED MICRO-INVERTERS AND THE MEB MICRO-INVERTER ARCHITECTURE.

	[13]	[27]	[26]	[5]	[28]	**Prototype without MEB**	**Prototype with MEB**
Topology	dc-dc-ac	dc-dc-ac	dc-ac-dc-ac	dc-ac-ac	dc-dc-ac-dc-ac	dc-ac-ac	dc-multilevel dc-ac-ac
Year	2006	2007	2008	2010	2013	2013	2013
Peak Power	100W	500W	150W	100W	250W	70W	70W
Grid Voltage rms ac	120V	100V	250V	240V	110V/220V	230V	230V
Input Voltage	35V	30V	36V	25V-40V	22V-40V	27V-38V	27V-38V
Switching Frequency	50kHz	20kHz	200kHz	45kHz-350kHz	-	310kHz-500kHz	310kHz-368kHz
PK: peak efficiency, EU: European efficiency, CEC: CEC effciency	70%PK	85%CEC	87%PK 85%EU	96%PK	93%CEC 94%PK	91%CEC 94%PK 86%EU	92%CEC 94%PK 89%EU
Power Factor	-	99%	-	-	-	99%	99%
THD	5% with line frequency filter	4.2% with line frequency filter	1.50% with line frequency filter	-	-	15%-25% without line frequency filter	15%-25% without line frequency filter
Num. of switches and diodes (FR: fully rated, PR: partially rated)	4 FR switches, 3 FR diodes	4 FR switches, 4 FR diodes	9 FR switches, 9 FR diodes	8 FR switches	7 FR switches, 3 FR diodes	6 FR switches, 4 FR diodes	6 FR switches, 4 FR diodes, 6 PR switches
Reduced twice-line-frequency energy buffer	Yes	Yes	Yes	No	Yes	No	Yes
Grid Interfacing	Line frequency unfolder and filter	Line frequency unfolder and filter	Line frequency unfolder and filter	High frequency cyclocon-verter	Line frequency unfolder and filter	High frequency cyclocon-verter	High frequency cyclocon-verter

APPENDIX I: OPTIMALLY SELECT THE SWITCHING ANGLES OF THE SCEB

The switching angles of the SCEB can be optimized for different design considerations. If a minimized voltage conversion range of the dc-ac converter is the goal, the $v_{\rm x}$ needs to step in pase with the line voltage as shown in Fig. 4b. Since we are using a series resonant converter, the amplitude $v_{\rm P,env}$, is limited to $V_{\rm IN}+v_{\rm BUF}$. Therefore, if $v_{\rm P,env}$ is modulated to be $v_{\rm P,env}(\theta)=(V_{\rm IN}+v_{\rm BUF})\sin(\theta)$, the difference between $v_{\rm Y,env}(\theta)$ and $v_{\rm P,env}(\theta)$ will be minimized, as shown in Fig. 5b. Furthermore, we can minimize this difference by making $v_{\rm Y,env}(\theta)$ and $v_{\rm P,env}(\theta)$ equal at $\theta=\alpha$ and at $\theta=\beta$. Hence, $v_{\rm BUF}$, α and β satisfy the following two constraints:

$$\begin{cases}(V_{\rm IN}+v_{\rm BUF})\sin(\alpha)=V_{\rm IN}-v_{\rm BUF}\\(V_{\rm IN}+v_{\rm BUF})\sin(\beta)=V_{\rm IN}\end{cases} \tag{6}$$

The normalized difference between $v_{\rm Y,env}(\theta)$ and $v_{\rm P,env}(\theta)$, which must be minimized, can be quantified as $\frac{v_{\rm Y,env}(\theta)-v_{\rm P,env}(\theta)}{v_{\rm P,env}(\theta)}$. From Fig. 5b it is easy to see that the maximum of this normalized difference can only occur at one of the following line angles: δ, α or β. Hence, the optimization target, C, that needs to be minimized is given by:

$$C=\max[\frac{V_{\rm IN}-v_{\rm BUF}-(V_{\rm IN}+v_{\rm BUF})\sin(\delta)}{(V_{\rm IN}+v_{\rm BUF})\sin(\delta)},\frac{v_{\rm BUF}}{(V_{\rm IN}+v_{\rm BUF})\sin(\alpha)},\frac{v_{\rm BUF}}{(V_{\rm IN}+v_{\rm BUF})\sin(\beta)}]. \tag{7}$$

Since $\alpha<\beta<\pi/2$, the second argument of (7) is greater than its third argument, i.e., $\frac{v_{\rm BUF}}{(v_{\rm IN}+v_{\rm BUF})\sin(\alpha)}>\frac{v_{\rm BUF}}{(v_{\rm IN}+v_{\rm BUF})\sin(\beta)}$. Hence, the normalized difference will be minimized when the first argument of (7) is equal to its second argument, i.e., when $\frac{V_{\rm IN}-v_{\rm BUF}-(V_{\rm IN}+v_{\rm BUF})\sin(\delta)}{(V_{\rm IN}+v_{\rm BUF})\sin(\delta)}=\frac{v_{\rm BUF}}{(V_{\rm IN}+v_{\rm BUF})\sin(\alpha)}$. Using (6) to eliminate α from this equation yields:

$$v_{\rm BUF}^2-[2+\sin(\delta)]V_{\rm IN}v_{\rm BUF}+[1-\sin(\delta)]V_{\rm IN}^2=0, \tag{8}$$

which can be solved for the optimal value of $v_{\rm BUF}$:

$$v_{\rm BUF}=\frac{V_{\rm IN}[2+\sin(\delta)]+V_{\rm IN}\sqrt{[2+\sin(\delta)]^2-4[1-\sin(\delta)]}}{2}. \tag{9}$$

The optimal values of α and β can now be determined using (6), rewritten explicitly below:

$$\begin{cases}\alpha=\sin^{-1}(\frac{V_{\rm IN}-v_{\rm BUF}}{V_{\rm IN}+v_{\rm BUF}})\\\beta=\sin^{-1}(\frac{V_{\rm IN}}{V_{\rm IN}+v_{\rm BUF}}).\end{cases} \tag{10}$$

With δ chosen as $6°$, the optimal value of $v_{\rm BUF}$ is $0.6V_{\rm IN}$, α is $12.8°$, and β is $40.9°$.

Appendix II: Calculate the Percentages of the Power Processed by the CCC.

The average power over a line cycle processed by the CCC ($P_{\rm CCC}$) can be calculated from the extra energy that must be delivered to $\rm C_{BUF}$ to maintain its charge balance:

$$P_{\rm CCC} = \frac{\int_{\beta}^{\pi-\beta} V_{\rm BUF} I_{\rm IN} \sin(\theta) d\theta - 2\int_{\delta}^{\alpha} V_{\rm BUF} I_{\rm IN} \sin(\theta) d\theta}{\pi} = \frac{2V_{\rm BUF} I_{\rm IN}[\cos(\alpha) + \cos(\beta) - \cos(\delta)]}{\pi}. \quad (11)$$

Here $I_{\rm IN}$ is the amplitude of the envelope of the input current of the dc-ac converter block. The fraction of line cycle average output power ($P_{\rm OUT(avg)} = \frac{2V_{\rm IN} I_{\rm IN}\cos(\delta)}{\pi}$) processed by the CCC is given by:

$$\gamma_{\rm CCC} = \frac{P_{\rm CCC}}{P_{\rm OUT(avg)}} = \frac{V_{\rm BUF}[\cos(\alpha) + \cos(\beta) - \cos(\delta)]}{V_{\rm IN}\cos(\delta)}. \quad (12)$$

With $v_{\rm BUF} = 0.6V_{\rm IN}$, $\delta = 6°$, $\alpha = 12.8°$, and $\beta = 40.9°$, $\gamma_{\rm CCC}$ equals 44.43%. Hence, only 44.43% of the average output power is processed by the CCC. Since the SCEB is switching at a low frequency (240 Hz), its switching loss is negligible compared to that of the CCC. Therefore, assuming the efficiency of the CCC circuit is $\eta_{\rm CCC}$, and neglecting the losses in the SCEB, the efficiency of the MEB architecture can be estimated as:

$$\eta_{\rm MEB} = \frac{P_{\rm OUT(avg)}}{P_{\rm OUT(avg)} + P_{\rm Loss,CCC}} = \frac{1}{1 + \gamma_{\rm CCC}(1-\eta_{\rm CCC})}. \quad (13)$$

This shows that the loss caused by the CCC circuit only penalizes the energy passing through the CCC in the MEB architecture. This, together with the high efficiency of the SCEB, allows the MEB based micro-inverter architecture to have a higher efficiency than conventional two stage architectures.

With the SCEB controlled as described above, the peak power rating of the CCC, $P_{\rm CCC,peak}$, is 97.7% of the line cycle average output power of the micro-inverter, $P_{\rm OUT(avg)}$. Hence, the peak power rating of the CCC is only 48.8% of the peak power rating of the micro-inverter ($2P_{\rm OUT(avg)}$). The CCC can be made extremely small and highly efficient since it has a fixed and reasonably small input to output voltage conversion ratio ($0.4:1$), processes a portion of the total energy and can be switched at a relatively high switching frequency.

Appendix III: Operation of the MEB Stage without the CCC.

To eliminate the requirement of the CCC, the average current of $\rm C_{BUF}$ needs to be zero over the line cycle. $\rm C_{BUF}$ is charged when the line voltage is low ($\theta \in [0°, \alpha] \cup [180° - \alpha, 180°]$), and is discharged when the line voltage in high ($\theta \in [\beta, 180° - \beta]$). Assume the dc-ac converter draws sinusoidal input current, the charge balance relationship of $\rm C_{BUF}$ can be written as Eq. 14:

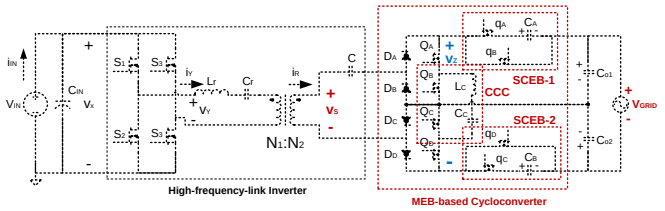


Fig. 23. A MEB micro-inverter with an ac-side MEB. The MEB stage in this implementation is combined with the cycloconverter. When $v_{\rm GRID}$ is in the positive half cycle, $\rm Q_C$ and $\rm Q_D$ are kept on. In this condition, if $v_{\rm GRID}$ is low, $\rm q_A$ and $\rm q_D$ are turned on to step-up the voltage seen by the rectifier; $\rm Q_A$, $\rm Q_B$ and $\rm L_C$ charge $\rm C_C$ to reduce the current flow into the grid. If $v_{\rm GRID}$ is moderate, $\rm q_B$ and $\rm q_D$ are turned on to bypass $\rm C_A$ and $\rm C_B$, and $\rm Q_A$ and $\rm Q_B$ are kept off. If $v_{\rm GRID}$ is high, $\rm q_B$ and $\rm q_C$ are switched on to step-down the voltage seen by the rectifier; $\rm Q_A$, $\rm Q_B$ and $\rm L_C$ discharge $\rm C_C$ to inject more current into the grid. When $v_{\rm GRID}$ is in the negative half cycle, $\rm Q_A$ and $\rm Q_B$ are kept on, and the circuit operates in a symmetric manner to the one described above.

$$\int_{\delta}^{\alpha} \mathrm{I_{GRID}} sin(\theta)\,\mathrm{d}(\theta) = \int_{\beta}^{\frac{\pi}{2}} \mathrm{I_{GRID}} sin(\theta)\,\mathrm{d}(\theta) \quad (14)$$

thus:

$$cos(\alpha) + cos(\beta) = cos(\delta) \quad (15)$$

Appendix IV: Operation of the MEB Stage on the AC Side of the Converter.

At the overall system level, an alternative implementation of the MEB micro-inverter can have the MEB stage on the ac side instead of the dc side. An example schematic of this implementation is shown in Fig. 23. The MEB stage of this implementation also has SCEB and CCC. The difference is that the SCEB is spitted into two parts to make ease connection with the grid. In this implementation, instead of synthesizing an approximated replica of the ac line voltage amplitude from the dc input, the MEB stage synthesizes an approximately constant voltage amplitude from the ac line. Hence, it also reduces the voltage conversion range of the high-frequency portion of the system. An example implementation with an ac-side MEB is shown in Fig. 23. In this implementation, the MEB stage is combined with the cycloconverter. The full-bridge SCEB is split into two half-bridge versions for ease of interfacing with the ac line. the twice-line-frequency energy is now substantially buffered by $\rm C_A$ and $\rm C_B$, allowing the use of a much smaller $\rm C_{IN}$. In each half-line-cycle, $\rm L_C$, $\rm C_C$, and two MOSFETs ($\rm Q_A$&$\rm Q_B$, or $\rm Q_C$&$\rm Q_D$, depending on the half-line-cycle) function as the CCC, maintaining the voltage across $\rm C_A$ and $\rm C_B$. Figure 24 shows the simulated waveforms of the MEB micro-inverter with the MEB stage on the ac side. Owing to the MEB stage, the amplitude variation of $v_{\rm Z}$ and $v_{\rm S}$ are significantly reduced, compressing the operation range of the high-frequency portion of the converter. In other words, the resonant inverter sees load voltage with relatively constant amplitude.

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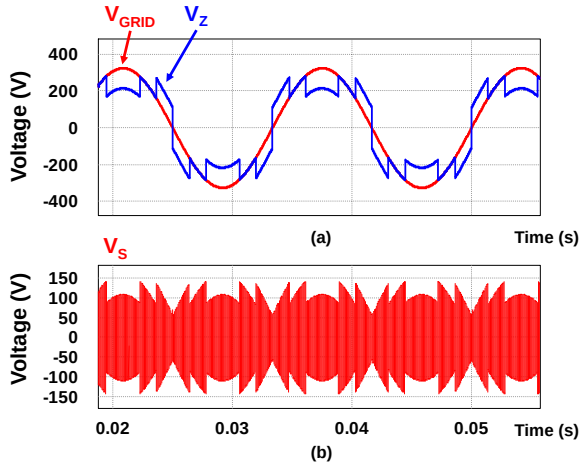

Fig. 24. Simulated waveforms for the MEB micro-inverter with the MEB stage on the ac side for $V_{\rm GRID}$ = 230 V rms and $V_{\rm BUF}$ = 106 V. (a) Line voltage $V_{\rm GRID}$ and the synthesized voltage $v_{\rm Z}$. (b) the voltage at the transformer secondary, $v_{\rm S}$. The amplitude variation of $v_{\rm S}$ over the line cycle has been significantly reduced.

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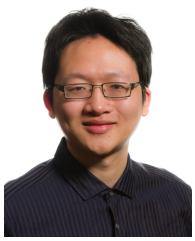

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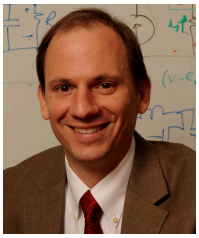

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