A Very High Frequency DC–DC Converter Based on a Class Φ_2 Resonant Inverter

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***Abstract*—This paper introduces a new dc–dc converter suitable for operation at very high frequencies (VHF) under on–off control. The converter power stage is based on a resonant inverter (the Φ_2 inverter) providing low switch voltage stress and fast settling time compared to other resonant topologies. A new multistage resonant gate driver suited for driving large, high-voltage RF MOSFET at VHF frequencies is also introduced. Experimental results are presented from a prototype dc–dc converter operating at 30 MHz at input voltages up to 200 V and power levels above 200 W under closed-loop control. These results demonstrate the high performance achievable with the proposed design.**

***Index Terms*—Burst-mode control, class Φ inverter, class E inverter, class F power amplifier, class phi inverter, cycle skipping control, harmonic peaking, on–off control, resonant dc–dc converter, resonant gate drive, resonant rectifier, very high frequency (VHF).**

I. Introduction

POWER density and response speed are important performance metrics in dc–dc power converters. Increases in switching frequency potentially enable improvement of both of these metrics: higher switching frequencies permit the use of smaller valued (and often physically smaller) passive components having reduced energy storage requirements. Reduced intermediate energy storage, coupled with a shorter switching period, permits more agile response to changes in operating condition. There is, thus, strong motivation to move to greatly increased switching frequencies if losses, switch driving, control, and other design challenges can be addressed.

Zero-voltage-switching (ZVS) resonant dc–dc converters offer the opportunity to operate at higher frequencies, but pose a number of design challenges [1]. First, designs of this type often suffer from high device voltage stress [2]–[12]. Driving of transistors also becomes a challenge as frequencies are increased, due to both loss considerations and the difficulty of achieving sufficiently fast switching transitions. Moreover, it is often difficult to achieve efficient operation of ZVS resonant converters across a wide load range, owing to resonating losses (for ZVS operation) that do not scale with output power delivery [13].

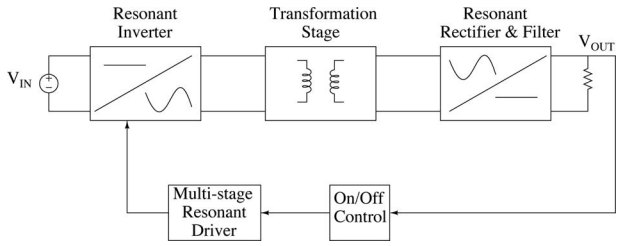

Fig. 1. General structure of the proposed dc–dc converter.

This paper introduces a new resonant dc–dc converter and associated driving and control methods that address the aforesaid challenges. The converter power stage is based on a resonant inverter (the Φ_2 inverter) that provides low switch voltage stress and fast settling time compared to other resonant inverter topologies. The proposed power stage is operated at fixed switching frequency and duty ratio. To achieve output control and high efficiency across a wide load range, we adopt on/off control [9]–[12], [14]–[17]. We also introduce a new multistage resonant gate drive that provides low-loss driving of high-voltage MOSFETS at very high frequency (VHF), and is well suited to the implemented on/off control. Together, these circuit designs and methods yield high efficiency across a wide load range as well as the ability to respond rapidly to load steps without voltage deviation.

Section II of the paper introduces the system structure and control approach. Detailed descriptions of the proposed converter and its constituent elements are also presented. The new multistage resonant gate drive system is treated in Section III. Closed-loop voltage control of the converter is discussed in Section IV. The results presented throughout this document demonstrate the efficacy of the proposed approach. Finally, Section V concludes the paper.

II. Proposed Converter System

A. System Structure

Fig. 1 shows the general structure of the proposed dc–dc converter. The converter power stage comprises a resonant inverter, a transformation stage, and a resonant rectifier. The resonant inverter accepts a dc input voltage, and generates VHF ac, which

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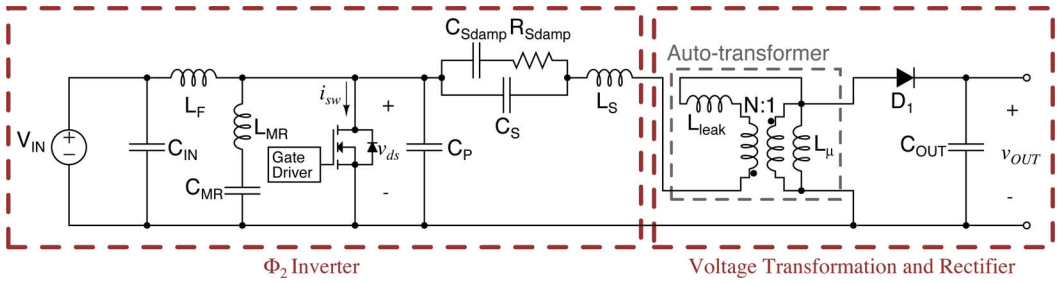


Fig. 2. DC–DC converter as implemented with an autotransformer.

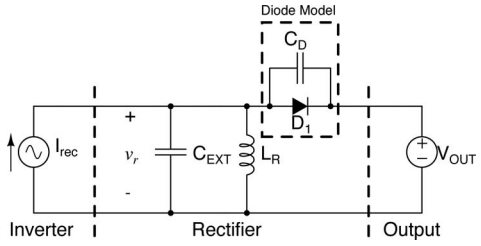


Fig. 3. Resonant rectifier. In this implementation, $C_{\rm EXT} = 0$ and L_R is provided by L_μ, the magnetizing inductance of the autotransformer (see Fig. 2).

is processed through the transformation stage to produce different ac voltage and current levels. The resonant rectifier then converts the transformed ac power back to dc. A multistage resonant gate drive is employed to drive the inverter switch, enabling efficient operation at much higher frequencies than would otherwise be possible.

Regulation of the converter output voltage can be achieved through on/off control of the inverter [9]–[12], [14]–[17]. In this approach, the power stage is gated on and off at a modulation frequency that is far lower than the inverter switching frequency. By controlling the fraction of time that the inverter stage runs (and delivers power to the output) the output voltage can be regulated to a desired reference level.

Key advances in the system developed here are in the design of the power stage and the gate drive, and in how these elements are specifically optimized to achieve high performance under on/off control. We focus on each of the subsystems in turn and describe the design procedure of a 200-W dc–dc converter operating at 30 MHz with an input voltage range of 160 to 200 V and output voltage of 33 V.

B. Rectification and Voltage Transformation

Fig. 2 shows the schematic of the Φ_2-based dc–dc converter introduced here. The figure outlines the different stages of the converter corresponding to the general structure shown in Fig. 1. We begin by considering how the rectifier and voltage transformation stages of the converter may be designed. For design purposes, the resonant rectifier can simply be modeled as illustrated in Fig. 3, which shows the resonant rectifier driven from a sinusoidal current source and loaded with a constant voltage at the output. Together, the large energy storage at the output and the on–off scheme regulating the output voltage of the converter allow us to treat the output voltage of the rectifier as constant for design purposes. In the figure, the rectifier is modeled as being driven by a sinusoidal current source of magnitude $I_{\rm rec}$. The resonant inductor L_R provides a path for the dc current and resonates with the capacitances C_D and $C_{\rm EXT}$ shown in the figure. C_D represents the diode nonlinear capacitance while $C_{\rm EXT}$ accounts for external capacitance added plus the parasitic interwinding capacitance of inductor L_R.

It is possible to describe the voltage-current relationship of a resonant rectifier in terms of an equivalent input impedance in a describing function sense [10], [18]. In our design, the resonant elements were tuned to make the input look nearly resistive at the fundamental frequency (that is, the fundamental of the voltage v_r is in phase with the drive current $i_{\rm rec}$). Alternatively, if the rectifier is tuned to appear appropriately reactive at the switching frequency, resonance between the interconnect network and the rectifier network can be used to provide voltage gain from the input to the output.

The input current amplitude is selected to provide the desired output power. The amplitude and conduction angle of the diode current depend on the component values. By adjusting the net capacitance ($C_D \parallel C_{\rm EXT}$) in parallel with the resonant inductor, we can shorten the length of the conduction interval by allowing a larger peak reverse voltage across the diode. In some implementations it is convenient to have a conduction angle close to 50%, as this provides a good tradeoff between peak diode forward current and reverse voltage. If additional capacitance is required, this can either be added externally or can be solely provided by additional diode area, which can have the added benefit of reducing the overall conduction loss in the rectifier.

The dependence of the length of the conduction interval of the rectifier on the nonlinear diode capacitance makes it difficult to find equations describing the amplitude and phase of the fundamental component of the rectifier voltage for the simplified circuit of Fig. 3. The authors have used time-domain SPICE simulators to determine the effective impedance at the switching frequency as the rectifier parameters are changed.

A starting value for the rectifier circuit parameters is as follows. Diode current rating and thermal considerations of the system will determine the size and selection of diodes in the resonant rectifier. The main rectifier capacitance C_D is the total diode capacitance when biased at the output voltage. An inductance value L_R that resonates at the switching frequency with the capacitance C_D has been found to provide a good starting value; however, this value of L_R is unlikely to lead to simulated waveforms for which the fundamental component of $V_{\rm rec}$ and

$I_{\rm rec}$ are in phase. By simulating the circuit for different values of L_R, while adjusting the amplitude of $I_{\rm rec}$ to maintain the desired output power, the value of L_R to be implemented in the prototype was found.

Larger values of C_D and correspondingly smaller L_R values result in a lower equivalent resistance of the rectifier. The designer should avoid values of L_R too small to be practically implemented. If extra capacitance is needed, the authors suggest the use of larger diodes, or paralleled diodes where possible, which results in lower conduction losses in the diodes and makes it easier to dissipate the resulting power loss due to the extra area spreading.

For the 200-W design presented here we use a pair of silicon carbide Schottky diodes (Cree CSD10030) in parallel.[1] In the design presented here, the corresponding resonant capacitance ($C_D \| C_{\rm EXT}$) of Fig. 3 is only provided by the nonlinear capacitance of the diodes.

The tuning of the rectifier stage was done numerically in SPICE, which required an accurate diode model. Parameters for the nonlinear diode capacitance were obtained by measuring the diode capacitance ($C_{\rm KA}$ = 548 pF, 163 pF, and 119 pF, at f_S = 1 MHz) at three different bias voltages ($V_{\rm KA}$ = 0, 11 V, and 23 V, respectively) and solving for V_J and m in the equation $C_{\rm KA} = C_{j0}/(1 + (v_{KA}/V_J))^m$. For the CSD10030 diode: $C_{j0} = 548.3$ pF, $V_J = 0.78$ V, and $m = 0.45$ for $0 \le v_{\rm KA} < 100$ V. The CSD10030 datasheet indicates that for $v_{\rm KA} > 100$ V the diode capacitance is approximately constant ($C_{\rm KA} = 62.6$ pF). In addition to the capacitance, the SPICE model of the diode incorporates 6 nH of lead inductance (between lead and the back of the TO-220 package), and 0.15 Ω of equivalent series resistance. The forward characteristic of each diode is modeled as a constant forward drop ($V_{d,\rm ON} = 507$ mV) in series with a resistor (R_S = 89.7 mΩ). With the appropriate model of the diodes, we proceeded to iteratively adjust the value of L_R and $I_{\rm rec}$ in SPICE and look for the values at which the fundamental of v_r and $i_{\rm rec}$ were in phase, and for which the rectifier delivered sufficient output power.

Fig. 4 (a) shows a SPICE simulation of the rectifier shown in Fig. 3, tuned to appear resistive at the fundamental frequency. For the conditions shown in the figure, $L_{\rm R}$ = 75 nH, $f_s = 30$ MHz and $|I_{\rm rec}| = 7.15$ A. The output power $P_{\rm OUT}$ delivered to the 33-V load is 200 W. Fig. 4(b) shows the sinusoidal input current, and the fundamental component of the input voltage, from which an equivalent resistance of approximately 8.4 Ω can be extracted.

Generally, the equivalent rectifier resistance will not correspond to the load resistance value at which a given power will be delivered by the Φ_2 inverter with greatest efficiency. Hence, there is a need to provide some sort of impedance transformation between the inverter and rectifier (e.g., by using a matching network [19], [20] and/or a transformer). For the dc–dc converter design presented here, a 4 to 1 impedance transformation is realized using a 1:1 autotransformer, with the transformer parasitics absorbed into the resonant tank of the inverter and the rectifier network. As will be discussed in subsequent sections, the optimal value for the equivalent resistance for the rectifier as seen at the input of the auto-transformer is a tradeoff between the resonating currents circulating within the inverter and the maximum power that can be delivered.

[1]These devices have a positive forward conduction thermal coefficient, which allows the paralleling of multiple devices.

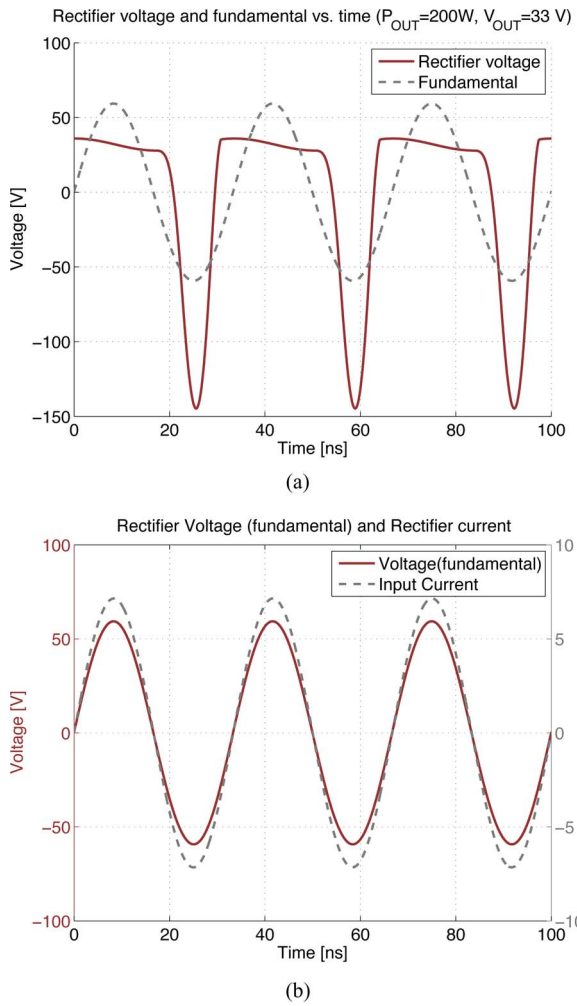


Fig. 4. (a) Rectifier voltage and its fundamental component. (b) Fundamental component of the input voltage and input current. $P_{\rm OUT}$ = 200 W, f_s = 30 MHz, L_R = 75 nH, and Q_L = 160. The equivalent resistance of the rectifier under this condition is 8.4 Ω.

Notice that in the schematic of Fig. 2 the magnetizing inductance of the autotransformer functions as the rectifier's resonant inductance (see L_R in Fig. 3). Designing an autotransformer with a coupling coefficient close to unity is desirable in order to achieve an accurate 4 to 1 impedance transformation, but this may be hard to achieve in practice. As an inspection of Fig. 2 will show, the autotransformer leakage inductance $L_{\rm leak}$ can be absorbed by the inverter's inductor L_S. Although parasitic capacitance between the autotransformer windings and the converter ground can be absorbed by the rectifier capacitances, care should be taken to minimize parasitic capacitances across the windings.

C. Φ_2 Resonant Inverter Design

When operating at very high frequencies, it becomes difficult to implement gate drives for switching elements having

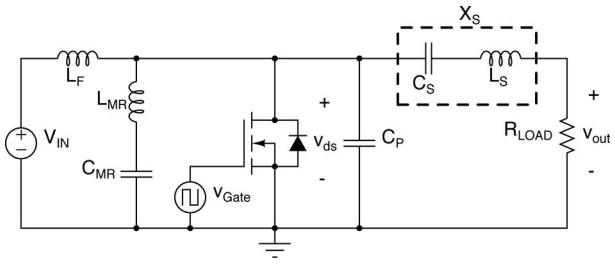


Fig. 5. Φ_2 resonant inverter.

floating sources (owing to capacitive currents) so designs having switches with their control ports referenced to constant potentials are often preferred. Likewise, it is often preferable to design inverters using only one semiconductor switch because of the difficulty of accurately commutating among multiple devices in this frequency range. Furthermore, switching high voltage at very high frequencies requires designs that realize ZVS to minimize switching losses. Finally, inverters that absorb switch parasitic capacitance and are tolerant of relatively slow gating waveforms are advantageous.

Unfortunately, many inverter designs that meet the aforementioned requirements suffer from extremely high voltage stress. For example, the widely used class E inverter [21], [22] meets all of these requirements, but results in voltage stresses across the switch that can reach over four times the input voltage [23] when the nonlinear capacitance of the device is considered. Other limitations of many inverter topologies appropriate to VHF operation include the use of bulk "RF choke" inductors (which is disadvantageous for rapid transient response and on–off control), and a tight tie between device parasitic capacitance and achievable output power and frequency [11], [15].

In this paper, we use a recently developed single-switch ZVS inverter topology that overcomes the aforementioned limitations. The so-called Φ_2 inverter (shown in Fig. 5) introduced in [16], [24]– [26] is a highly simplified variant of the class Φ inverter [27]–[29]. It operates with a much reduced voltage stress across the switch (slightly over twice the input voltage) and breaks the tight link between semiconductor capacitance, output power, and frequency found in many high-frequency resonant designs. Furthermore, the Φ_2 inverter only uses resonant elements (no input choke inductor) thus reducing the energy storage requirements of the converter and providing an inherently faster response. The benefits of this are twofold: it allows a reduction in the overall size of the converter (by reducing input and output bulk capacitance requirements), and improves the control bandwidth.

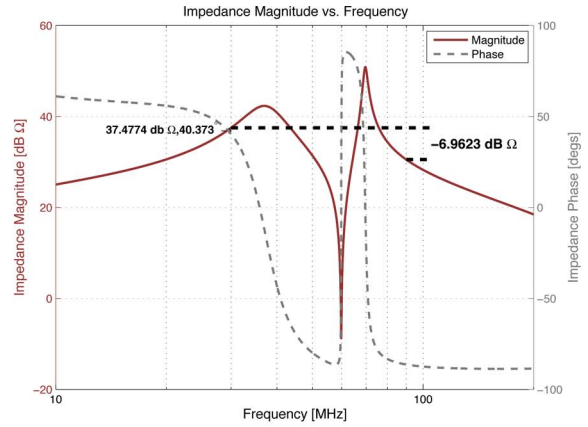
As introduced in [24]–[26], the resonant components of the Φ_2 inverter are selected to achieve shaping of the switch drain voltage into a trapezoidal waveform by controlling the impedance characteristics at the switch drain. Specifically, the design procedure detailed there calls for certain characteristics in the magnitude and phase of the impedance seen looking into the drain to source port of the MOSFET during its off state. These requirements include the following.

1) The impedance at the fundamental switching frequency is 30°–60° inductive.
2) The impedance at the second harmonic is small due to the series resonance between $L_{\rm MR}$ and $C_{\rm MR}$.
3) The impedance at the third harmonic is capacitive in phase and its magnitude is several dB (between 4 and 8) below the impedance magnitude at the fundamental.
4) The values of $X_{\rm S}$ and $R_{\rm LOAD}$ are selected to achieve the desired power transfer based on the voltage division from the trapezoidal operating waveforms of the inverter.

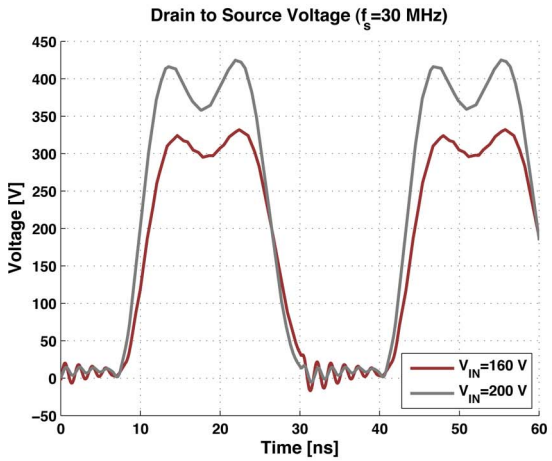
The inverter design starts by obtaining values for components L_S and C_S forming the reactance X_S in Fig. 5. Here, X_S was designed to look inductive at the fundamental frequency (30 MHz). Assuming the drain to source voltage of the MOSFET resembles a trapezoid going from zero to an amplitude of twice the input voltage, we can determine the value of inductor L_S by assuming all power will be delivered at the fundamental frequency. Moreover, we know that $R_{\rm LOAD} = 33\ \Omega$ in Fig. 5 (the equivalent resistance, at the fundamental, of the rectifier as seen at the input of the autotransformer: $4 \times 8.2\ \Omega$). By solving the equation of the reactive voltage divider formed by the series combination of L_S and $R_{\rm LOAD}$ with a fundamental voltage at the drain node of $\approx(4/\pi)V_{\rm IN}$ (by further approximating the drain to source trapezoid as a square wave) we find that with $L_S =$ 256 nH we can deliver approximately 200 W when $V_{\rm IN} = 160$ V. In practice, the output power of the inverter will be somewhat smaller than predicted because of the lower amplitude of fundamental component of the trapezoidal waveform at the drain node. Here, capacitor $C_S = 4$ nF and only provides dc blocking and presents a relatively low impedance at 30 MHz.

We then proceed to find values for resonant components $L_{\rm MR}$, $C_{\rm MR}$, L_F, C_P following the guidelines outlined in [24]–[26]. As described in the references, starting values of these components can be found using $L_{\rm MR}=1/15\pi^2 f_s^2 C_F$, $C_{\rm MR}=15C_F/16$, and $L_F=1/9\pi^2 f_s^2 C_F$, where C_F is a fraction of the total capacitance formed by the switch capacitance and the external capacitance C_P. To minimize conduction losses in the resonant components of the inverter, it is desirable to have relatively high- impedance levels at the fundamental and third harmonic while allowing for realizable inductor and capacitor values.

Starting with $C_F = 20$ pF (less than half the $C_{\rm ds} = 55.47$ pF of the ARF521 MOSFET when $V_{\rm IN} = 160$ V) we find $L_{\rm MR} =$ 375 nH, $C_{\rm MR}$ = 18.75 pF, $L_F = 625$ nH, as starting values for the resonant components of the inverter. The resonant element L_F has to be further adjusted to a value of 345 nH and an external capacitance $C_P = 30$ pF has to be added to the drain node (making the total drain to source capacitance equal to 88.5 pF when $V_{\rm IN} = 160$ V) to achieve the impedance characteristics at the fundamental, second, and third harmonic of the switching frequency that will result in a trapezoidal $v_{ds}(t)$ waveform with ZVS and with low dv/dt at switch turn on. A Bode plot of the Φ_2 inverter drain to source impedance $Z_{\rm DS}(f)$ is shown in Fig. 6(a) when the inverter is loaded with the equivalent rectifier resistance. Here, $|Z_{\rm DS}|=$ 37.5 dBΩ and $\angle\ Z_{\rm DS} = 40°$ at the fundamental frequency (30 MHz). Moreover, the impedance magnitude at the fundamental is 7 dB above the impedance at the third harmonic. Notice, the notch at 60 MHz. Fig. 6(b) shows



(a)



(b)

Fig. 6. (a) Drain to source impedance of the Φ_2 inverter design. Here, $L_F = 345$ nH, $L_{\rm MR} = 375$ nH,$C_{\rm MR} = 18.75$ pF, $C_P = 30$ pF, $C_S = 4$ nF, $L_S = 256$ nH, and $R_{\rm LOAD} = 33\ \Omega$. At the fundamental, $|Z_{\rm DS}| = 37.5$ dBΩ and $\angle Z_{\rm DS} = 40°$. The impedance magnitude at the fundamental is 7 dB above the impedance at the third harmonic. Notice the notch at 60 MHz ($Z_{\rm DS}(f)$). (b) Drain to source voltage of the Φ_2 inverter when $V_{\rm IN} = 160$ and 200 V (transient simulation). The waveform shows the drain node achieves ZVS and approximately zero dv/dt at switch turn-on. The simulation accounts for the nonlinear capacitance behavior of the ARF521 and of relevant parasitics. ($v_{\rm ds}(t)$).

a transient simulation of the drain to source voltage for the same parameters. Under these conditions, the load power is $P_{R\rm load} = 174$ W when $V_{\rm IN} = 160$ V and $P_{R\rm load} = 277$ W when $V_{\rm IN} = 200$ V.

D. DC–DC Converter Implementation

It should now be clear that implementation of the proposed Φ_2-based dc–dc converter requires careful design and placement of the various resonant elements which are tuned to achieve precise waveform characteristics. The printed circuit board (PCB) prototype was designed to minimize parasitic impedances, especially where these could not be absorbed into nearby lumped components. As inductance was found to provide more difficulty than capacitance, this indicated a tight layout with wide traces. In part because of these parasitic impedances, the authors found it convenient to characterize each element's impedance as it was placed on the PCB and then measure the impedance at the drain-source port. During the tuning process, the component values in the simulation were continually updated to maintain good agreement between the measured values on the prototype and the simulation. This step was made to verify and account for as many parasitics as was deemed possible.

The nonlinear dependency with voltage of both the MOSFET and diode capacitances required impedance measurements throughout the tuning process having both semiconductors properly biased at their respective operating voltages ($V_{\rm DS} = 160$ V for the MOSFET and $V_{\rm KA} = 33$ V for the diode). A 250 V 10 μF ceramic capacitor was placed between the measurement device (Agilent 4395 Impedance Analyzer) and the drain node of the converter to protect the analyzer from potentially destructive voltages. The introduction of the blocking capacitor contributed 6 nH of series inductance between the impedance analyzer and the drain node that had to be accounted for in our simulations.

The implementation of the prototype started with placement of the elements forming the rectifier described in Section II-B. The autotransformer was built on a Teflon rod (9/16 in. diameter, with 12 turns/in threads). The primary winding consists of three turns of AWG16 magnet wire, while the secondary has two turns. The secondary winding was placed on top of the primary to maximize coupling. Parameter extraction was performed by standard short- and open-circuit impedance measurements. These measurements were made with the autotransformer placed on the PCB to account for board parasitic inductances. We used a cantilever model for the transformer as illustrated in Fig. 2. The measured value of $L_{\rm leak} = 84.8$ nH, $L_\mu = 78.5$ nH, and the effective turns ratio is $N = 0.83$. The leakage $L_{\rm leak}$ contributes part of the 257 nH needed by the inverter's reactive interconnect X_S.

The reader should keep in mind that the resistive behavior of the rectifier is a modeling strategy valid only when the rectifier is in operation. During construction of the prototype, impedance measurements were done under small signal conditions. This means that the impedance looking into the autotransformer and toward the rectifier will not look resistive but will exhibit the parallel resonance formed by L_μ and the diode capacitance under bias.

We proceeded to place the inverter's components on the board, starting with $C_{\rm MR}$ and $L_{\rm MR}$. These elements are responsible for introducing a null at the second harmonic of the switching frequency. $L_{\rm MR}$ was constructed by winding 9 turns of AWG16 magnet wire on a $3/8$-in diameter Teflon rod (with 14 turns/in threads). $C_{\rm MR}$ was implemented by connecting 3 (two 56 pF and one 39 pF) porcelain capacitors in series. A measurement of drain impedance[2] placed the resonant frequency of the $L_{\rm MR}$–$C_{\rm MR}$ combination at 61 MHz. We then put the ARF521 MOSFET in place and continued by adding L_S (with a value of 175 nH that when adding $L_{\rm leak}$ of the autotransformer makes the total value of the branch inductance 259 nH). The last component to be placed was L_F. The designed value of L_F had to be slightly adjusted to precisely achieve ZVS and zero dv/dt in simulation. L_F was made of nine turns of AWG 16 wire on a

[2]All small-signal impedance measurements were performed using the Agilent 4395A impedance analyzer.

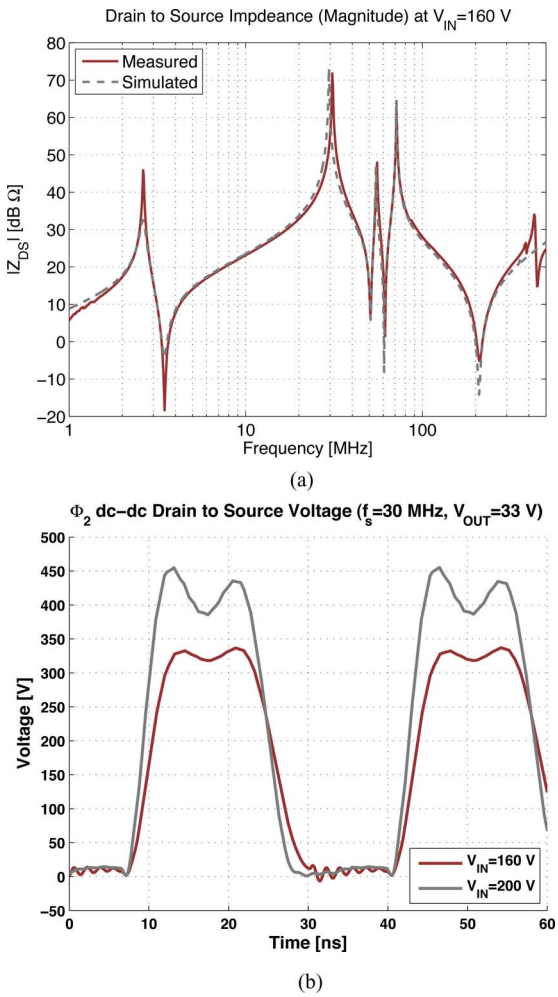


Fig. 7. (a) Comparison between measured and simulated drain to source impedance of the Φ_2 dc–dc converter prototype when $V_{\rm IN} = 160$ V and $V_{\rm OUT} = 33$ V. The differences between this and the plot shown in Fig. 6(a) are explained by accounting for the small-signal impedance of the resonant rectifier (biased to 33 V) during prototype implementation ($Z_{\rm DS}(f)$). (b) Drain to source voltage of the Φ_2 dc–dc converter when $V_{\rm IN} = 160$ and 200 V (transient simulation). The waveforms show almost identical dynamic behavior to the simulated drain to source voltage waveforms of the inverter shown in Fig. 6 ($v_{\rm ds}(t)$).

3/8-in diameter Teflon rod (14 turns/in threads) with an off-board value of 384 nH.

With all the components in place, we measured the impedance looking into the drain port. Fig. 7(a) shows the measured $Z_{\rm DS}(f)$ and compares it with a SPICE simulation in which the parameters were extracted from measurements on the PCB when $V_{\rm IN} = 160$ V and $V_{\rm OUT} = 33$ V. Fig. 7(b) shows the $v_{\rm ds}(t)$ of a transient simulation of the expected behavior of the dc–dc converter operating at both extremes of the input voltage range. Table I shows measured values of the components in the prototype.

E. Experimental Performance of the Φ_2 DC–DC Converter

Fig. 8 displays a photograph of the prototype power stage. Details of the mounting and cooling of the power stage may be found in [26].

TABLE I
LIST OF COMPONENTS FOR THE 30 MHz, 160– 200 V INPUT 33 V OUTPUT Φ_2 PROTOTYPE DC–DC CONVERTER

Part	Measured Value	Q	Part number
$C_{\rm IN}$	4 μF (250 V Ceramic)		4x CKG57NX7R2E105M
$L_{\rm F}$	384 nH (off-board measurement)	197	9 turns of AWG 16 wire on a 3/8 in. diam. Teflon® rod with 14 turns/in. threads
MOSFET	ARF521		APT Inc.
$L_{\rm MR}$	414 nH	185	9 turns AWG 16 wire on a 3/8 in. diam. Teflon® rod with 14 turns/in. threads
$C_{\rm MR}$	16.3 pF (porcelain)	10 K 10 K	2x56 pF ATC100B560JW 1x39 pF ATC100B390JW
$C_{\rm P}$ $C_{\rm S}$	28 pF 4 nF	 3 K	Parasitic drain capacitance 4x1 nF MC22FD102J-F
$C_{\rm Sdamp}$	10 nF		15 nF C3225C0G2E153J
$R_{\rm Sdamp}$	10 Ω		(SMD1012) ERJ-S14F10R0U
$L_{\rm S}$	175 nH	195	5 turns AWG 16 wire on a 3/8 in. diam. Teflon® rod with 14 turns/in. threads
Auto-transformer	N=0.83 $L_{\rm LEAK}$=84.8 nH L_{μ}=78.5 nH		Primary: 2 turns AWG 16 wire Secondary: 3 turns AWG 16 wire on a 9/16 in. diam. Teflon® rod with 12 turns/in. threads
Diode	2x CSD10030		Cree Inc.
$C_{\rm OUT}$	4 μF (250 V Ceramic)		4x CKG57NX7R2E105M

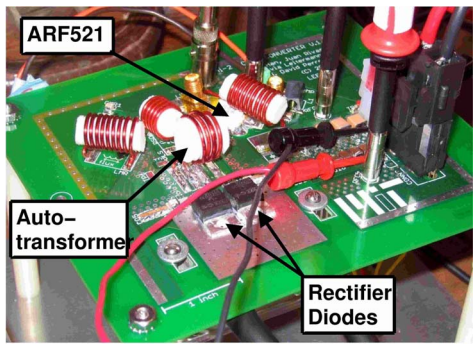


Fig. 8. Prototype Φ_2 dc–dc Converter.

To evaluate and measure the steady-state performance of the converter, a 33-V dc load was constructed by paralleling 14 50-W Zener diodes (NTE5269A).

To test the power stage of the converter prior to development of a complete gate drive, the gate was driven from a 50 Ω power amplifier. In order to reduce the impact of the 50 Ω output impedance of the power amplifier (Amplifier Research 150A100B) used, a 4:1 (in impedance) bifilar RF transformer (Pulse Engineering p/n CX2024) was connected as a transmission-line transformer (autotransformer) to the input of the gate drive.

Fig. 9 shows the drain voltage $v_{\rm ds}(t)$ and the gate voltage $v_{\rm gs}(t)$ of the MOSFET when $V_{\rm IN} = 160$ V. Waveforms are measured with high-voltage (PMK PHV621 1.5 kV) probes and a Tektronix 2.5-GHz (TDS7254B) oscilloscope. The desired trapezoidal drain waveforms with ZVS switching are achieved [cf., 6(b)]. The drain-gate capacitance $C_{\rm rss}$ is responsible for the distortion in the gate waveform. This issue is addressed by the improved gate driver described in the following section.

Experimental measurements of $v_{\rm ds}(t)$ over the entire operating input voltage range (160–200 V), portrayed in Fig. 10, demonstrate that the peak voltage across the power MOSFET is at most 2.35 times the input voltage.

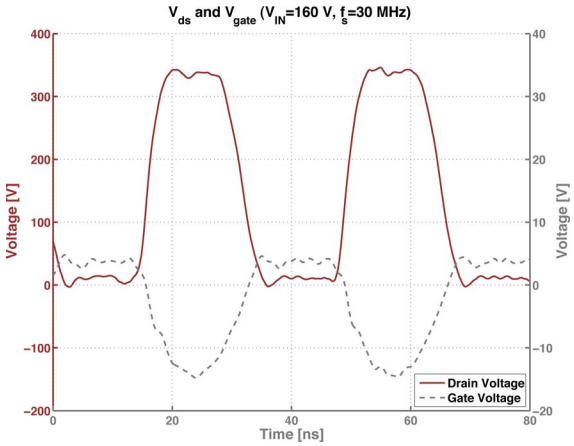


Fig. 9. Experimental MOSFET drain to source and gate voltage at $V_{\rm IN} = 160$ V. The gate is driven from a 50 Ω power amplifier through a CX2024 transmission-line transformer.

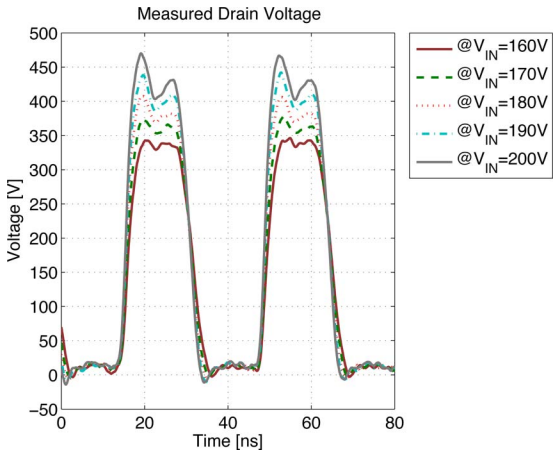


Fig. 10. Experimental drain-to-source voltage $v_{\rm ds}$ for 160 V $\leq V_{\rm IN} \leq$ 200 V. The peak drain voltage to input voltage ratio is ≃2.35.

The output power and the drain efficiency, defined as the efficiency when gate and control power are neglected, of the converter are presented in Fig. 11 over the input voltage range. The input and output power and efficiency are measured by sensing the voltage and current at the input and output of the converter with digital multimeters[3] (4 × Agilent 34401A) read using a LabView interface. The figure demonstrates that the Φ_2 dc–dc converter can achieve high drain efficiency over the entire input range (82.5–87.5%).

III. MULTISTAGE RESONANT GATE DRIVE

In VHF power conversion, driving the switching device(s) fast enough and hard enough is a significant challenge. For example, the large gate capacitances of high-power vertical MOSFETS require high currents to switch fast enough. Further complicating the drive is the substantial feedback from the drain voltage through the gate-drain capacitance, especially in high-voltage

[3]A current shunt (Agilent 34330A) was required for sensing the output current when using this 3 A meter.

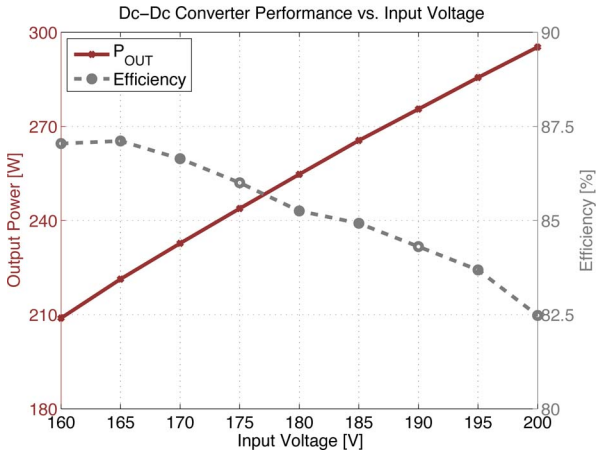


Fig. 11. Experimental output power and drain efficiency (i.e., efficiency when gate and control power are neglected) versus input voltage for the prototype dc–dc converter driven with the power amplifier.

TABLE II
SUMMARY OF GATE DRIVE PERFORMANCE REQUIREMENTS

Attribute	Value
Switching Time	$<< 33ns; \approx 1ns$
Threshold Voltage	$\approx 2.5V$
Target On-state Gate Voltage	$8V$
Gate Voltage Limits	$\pm 30V$
Target Duty Cycle	0.3

designs. Additionally, the nonlinearities of all the device capacitances constrain the design of the gate drive. Finally, all these problems must be solved while driving the gate with a total power that is small compared to the output power in order to keep efficiency high.

The specific targets for the prototype device and power converter are summarized in Table II.

The majority of standard gate drive techniques are not well suited to this problem. For example, the power dissipation of a commercial hard-switched RF driver such as the IXYS DEIC420 is prohibitively large (>50 W) for a 200-W dc–dc converter [30]. While resonant gate drives are attractive at these frequencies, a single-stage resonant drive such as those in [9]–[11], [15], [16] would be difficult to realize. In many fields, including RF amplifiers and digital drives, the use of multistage amplifiers or drives is a standard technique to deliver additional power gain, and it is useful for achieving the current gain necessary here. Thus, a multistage gate drive was implemented here.

In this driver, a small, hard-switching tapered inverter (the "hard-switching inverter") drives a larger resonant inverter (the "resonant drive inverter"), which in turn drives the gate of the main inverter switch via a matching network. Schematics for the hard-switching inverter are shown in Fig. 12, while schematics for the resonant drive inverter are shown in Fig. 13. As will be shown, this structure is suitable for efficiently developing the required drive waveforms.

Use of a hard-switched inverter as a first driver stage is attractive because the resonant drive inverter it feeds operates at substantially lower voltage and power levels and has much smaller capacitances than the main resonant inverter. As

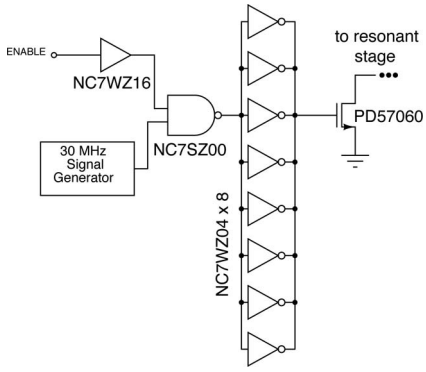


Fig. 12. Auxiliary hard-switched driver. Logic parts include Fairchild NC7WZ16, NC7SZ00, and NC7WZ04 driving the ST PD57060 MOSFET.

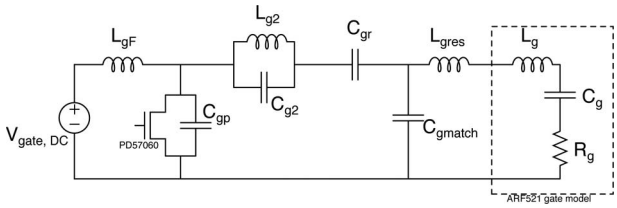


Fig. 13. Resonant second harmonic class E gate driver. $V_{\mathrm{gate,DC}} = 12$ V, gate bias voltage $V_{\mathrm{bias}} = -3.75$ V.

illustrated in Fig. 12, the first stage drive includes a 30-MHz clock signal feeding a single CMOS gate whose output is modulated by an enable signal (providing a means for on–off control). This single gate in turn drives a stack of eight CMOS inverters in parallel, providing a tapered drive.

The CMOS hard-switched inverter drives the gate of the resonant drive inverter (see Fig. 13), which is a second-harmonic class E inverter [31]. The second harmonic class E inverter is well suited to the gate drive problem. The inverter contains only resonant components and requires no bulk inductor. This provides fast transient response, which is necessary for fast startup and shutdown of the gate drive under on–off control. The second harmonic class E topology is also well suited to driving low impedances, which is helpful given the low gate impedance to be driven.

To further provide good matching to the very low gate (load) impedance, an *L*-section matching network was used. This serves to raise the effective load resistance seen by the inverter, thereby reducing resonant losses and improving the sizing of resonant component values in the inverter. Because a dc-pass matching network is used, the resonant tank inductance is in series with both the matching inductance and the parasitic gate inductance, enabling these resonant components to be lumped together in one physical inductor that absorbs the parasitic gate inductance. Moreover, this structure allows a dc bias V_{bias} (not shown) to be applied to the gate in order to control switch duty cycle. The dc bias shifts the entire gate drive waveform up or down in voltage, which allows small changes in the duty cycle of the power stage.

Table III contains the values and part numbers of the parts used. The PCB prototype board design again requires close attention to parasitic impedances, especially inductance in series with capacitive branches. The total power dissipation of the gate drive was approximately 2.4 W when the drive was running and approximately 22 mW static power when the drive was powered but not running. This amounts to less than 1.5% of the total output power.

TABLE III
COMPONENTS USED IN GATE DRIVE

Device	Manufacturer	Part No.
NAND Gate	Fairchild	NC7SZ00M
Hard-switching Inverters	Fairchild	NC7WZ04
Auxiliary Switch	ST Micro	PD57060

Component	Value	Part No.
L_{gF}	68 nH	1812SMS-68N
L_{g2}	16 nH	2508-16NJL
C_{g2}	417 pF	GRM1885C2A391JA01D + GRM1885C2A270JA01D
C_{gr}	220 pF	C1608C0G2A221J
L_{gres}	30 nH	Custom 1812SMS-33N
C_{gmatch}	3 x 1 nF	3 x ATC100B102KW

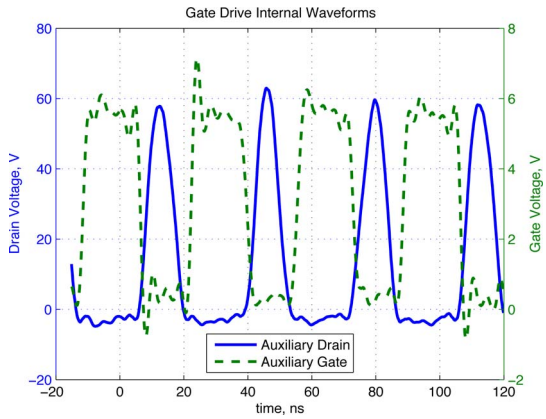


Fig. 14. Experimental internal gate drive waveforms. $V_{\mathrm{IN}} = 180$ V, $V_{\mathrm{bias}} = -3$ V.

Fig. 14 shows the output of the hard-switched first stage and the drain waveforms of the auxiliary second harmonic class E gate drive inverter.[4] Note that the second harmonic class E waveforms look like standard class E drain waveforms, switching at approximately zero voltage and low dv/dt.

The gate and drain waveforms of the power stage are shown in Fig. 15. As can be seen from the low drain voltage during on state, the switch is fully enhanced. Note the rapid switching times and the substantial gate voltage in the middle of the on state. Fig. 16 compares the performance of the system, in terms of total efficiency and output power, running with the gate drive as described here. A photograph of the gate drive board mounted on the converter is included as Fig. 17. Further details of the implementation of the gate drive are available in [32].

An advantage of this gate drive design is the speed with which the entire system may be turned on or off. As can be seen in Fig. 18, the full system is approximately in steady state

[4]Waveforms were sensed using the same Tektronix TDS7254B oscilloscope (with Tektronix P6139A probes).

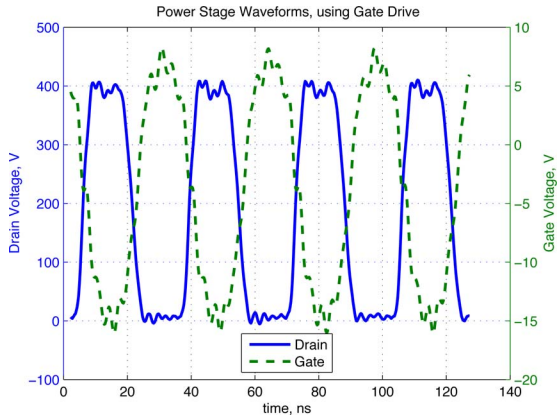


Fig. 15. Experimental power stage waveforms using multistage resonant gate driver. $V_{\rm IN} = 180\,{\rm V}, V_{\rm bias} = -3.75\,{\rm V}$.

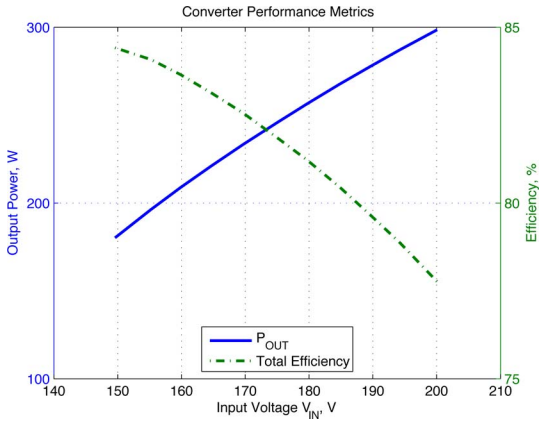


Fig. 16. Experimental open-loop performance of the dc–dc converter as measured using the described gate drive. $V_{\rm bias} = -3.75$ V.

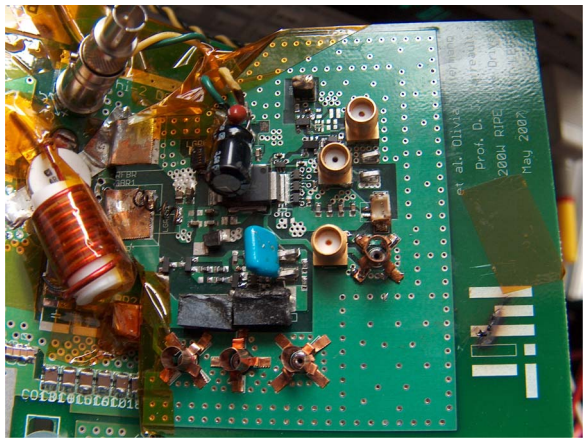


Fig. 17. Photograph of the gate drive board.

within about 500–1000 ns after an enable command. Since there is very little stored energy, the turn-off is very rapid as well. Fig. 19 shows the turn-off transient. Note that the drain voltage is substantially decayed within 500 ns after disable and that only small oscillations remain beyond $1\,\mu$s. This response speed is certainly adequate to implement on–off control as described in [9]–[12], [14]–[16].

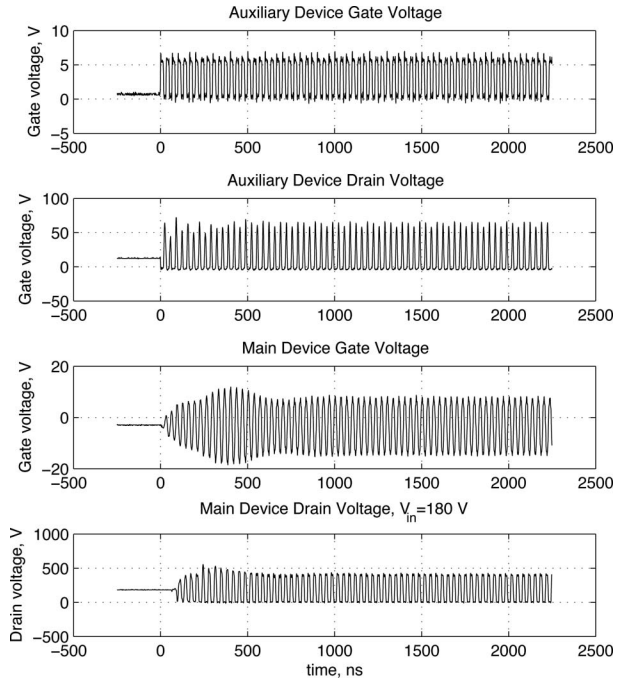


Fig. 18. Experimental turn-on transient with gate drive. $V_{\rm IN} = 180\,{\rm V}, V_{\rm bias} = -3\,{\rm V}$, load at or above 31 V.

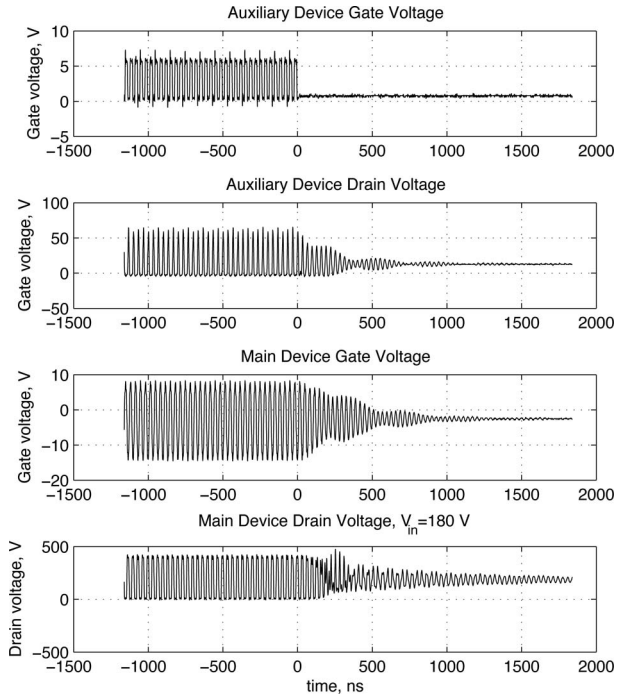


Fig. 19. Experimental turn-off transient with gate drive. $V_{\rm IN} = 180\,{\rm V}, V_{\rm bias} = -3\,{\rm V}$.

IV. Closed-Loop Control

In order to provide regulation with this converter, the whole power stage is switched on and off at a speed much slower than the switching frequency. This is known as burst mode control, on–off control, or bang–bang control [11], [14], [33].

One way to achieve closed-loop on–off regulation is to implement a hysteretic control, as in [16]. In this scheme, the

TABLE IV
THE COMPONENTS USED IN THE HYSTERETIC CONTROLLER BOARD

Component	Value
R_H	300 Ω
R_F	220 kΩ
R_1	1.5 kΩ
R_2	10.4 kΩ
C_{LP}	33 pF

Further data may be found in [1], [16], [35].

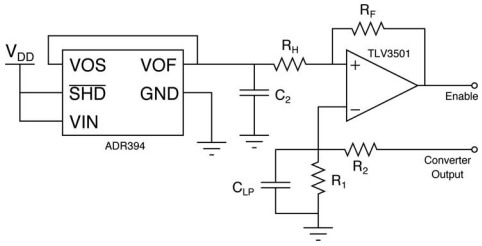


Fig. 20. Schematic of the controller board used for the closed-loop control. Adapted from [35].

controller monitors the output voltage. It then switches the converter on if the voltage drops below a preset "low" value and off if the voltage rises above a preset "high" value. In this way, the peak to peak ripple is essentially fixed, while the (relatively low) modulation frequency and modulation duty cycle vary with the load.

The output capacitance is sized based on ripple considerations, taking into account this lower modulation frequency. In contrast, the power stage passive components are sized according to the much higher internal switching frequency. However, it is notable that because the dynamics of the converter are much faster than the modulation frequency, the converter can respond very quickly to changes in load. Thus, the output capacitance need not be increased to mitigate the effects of converter dynamic response [16], [34].

For this project, the closed-loop control hardware was a board designed for control of a similar converter at a different power and frequency level [16], [35]. A schematic of the controller is shown in Fig. 20, and Table IV lists the passive component values used. The board senses the output voltage, and provides an on/off signal for the power stage. This on/off signal is connected to the "enable" input on the auxiliary gate driver, which is designed to modulate the gate drive (and from there the entire converter) on and off. The board also includes a 12 V to 5 V prepackaged buck converter which can serve as the 5 V (logic) supply to the gate drive.

A. Experimental Setup

The inputs to the converter include a 12 V gate drive power supply, the −3.75 V gate bias supply, and a 30 MHz clock signal in addition to the main input voltage of 150–200 V.

The converter is run into an electronic load acting as a resistive load in order to measure the performance at different output power levels. In addition to the on-board capacitance at the output of the converter, a 2200 μF U767D electrolytic capacitor (United Chemi-con, 026L61) was added at the electronic load to accept the modulating ripple. The capacitor was selected for its ripple current rating of approximately 6 A, as well as for its immediate availability. In order to have acceptable modulation frequencies, a smaller capacitance (down to 200–300 μF) could be used if the high ripple current rating could be preserved.

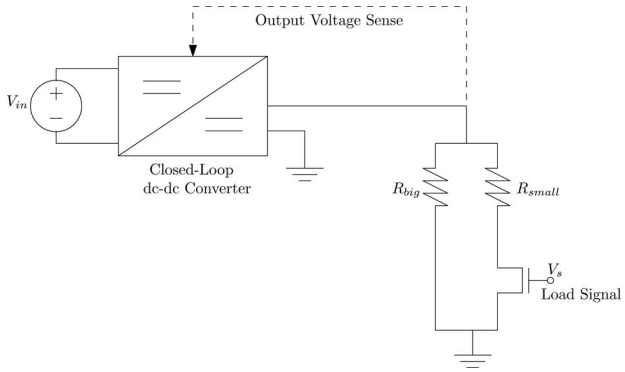


Fig. 21. Block diagram of the load step setup.

While the electronic load was also capable of generating a load step, it was found that the slew rate of the load was slower than was desirable for demonstration of the capabilities of the converter. To generate a faster load demand, a switched-resistor load was constructed. The larger resistance of 57 Ω[5] was permanently connected across the load, and a smaller second resistance was connected in series with the output port of an Infineon IPW60R045CP MOSFET. The second resistance included a wound-wire rheostat[6] which was adjusted to provide 6 Ω across the load when the MOSFET was on. The 2200 μF capacitor was retained across the resistive load. This setup is illustrated in Fig. 21. In this way, by switching the gate of the MOSFET, it was possible to create a load step on the inverter of approximately 10–90%.

B. Results

Measurements of the dc–dc converter under closed-loop control are displayed in Figs. 22–28. Figs. 22 and 23 display the very fast transient response of the complete system. The ac component of the output voltage ripple at 50% load is pictured in Fig. 24. Plots of the performance under a load step, Figs. 25 and 26, illustrate the performance advantage of this very fast response.[7] The converter output does not leave the ripple band when the load is stepped. As may be seen in Figs. 27 and 28, the system maintains high efficiency across the power and input voltage range. In particular, because the whole converter is operated under on–off control, the efficiency at light load drops off only slightly from that at heavy load. This drop off is due to the larger portion of time that the converter is starting up and shutting down under light load conditions. This startup and shutdown are associated with somewhat larger losses than steady state operation.

The system exhibited an audible buzz at some load levels. The precise source of this is as yet unknown. However, with more

[5] 5 × Barry 100 Ω RA1000–150–4X resistors, $133\Omega \| 100\Omega$.
[6] Jagabri "Lubri-tack" 5.5 A 52 Ω.
[7] The input and output current were measured using Tektronix current probes (A6302 and AM503 with TTCP202, respectively).

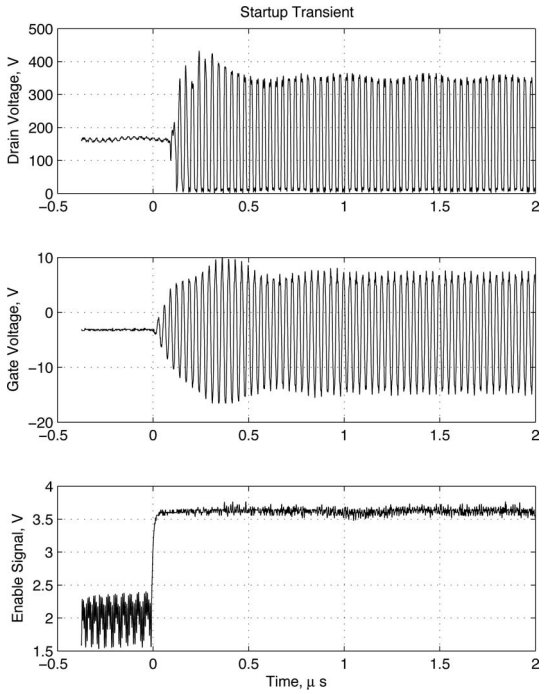


Fig. 22. Startup response of the converter. $V_{\rm IN} = 160$ V, $R_{\rm load} = 11\,\Omega$ (electronic load).

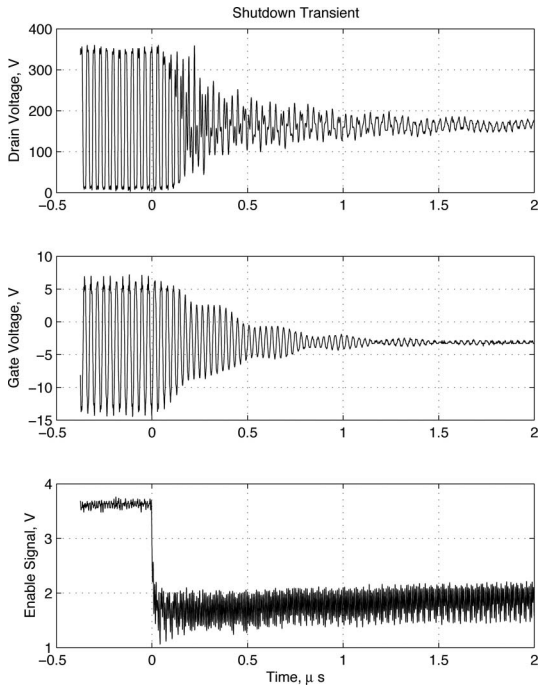


Fig. 23. Shutdown response of the converter. $V_{\rm IN} = 160$ V, $R_{\rm load} = 11\ \Omega$ (electronic load).

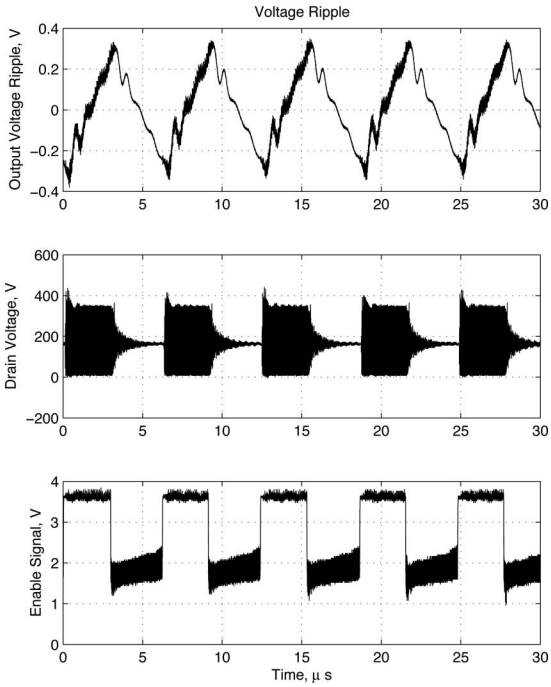


Fig. 24. AC component of the output voltage ripple on the converter. $V_{\rm IN} = 160$ V, $R_{\rm load} = 11\,\Omega, C_{\rm OUT} = 2200\,\mu$F (electronic load).

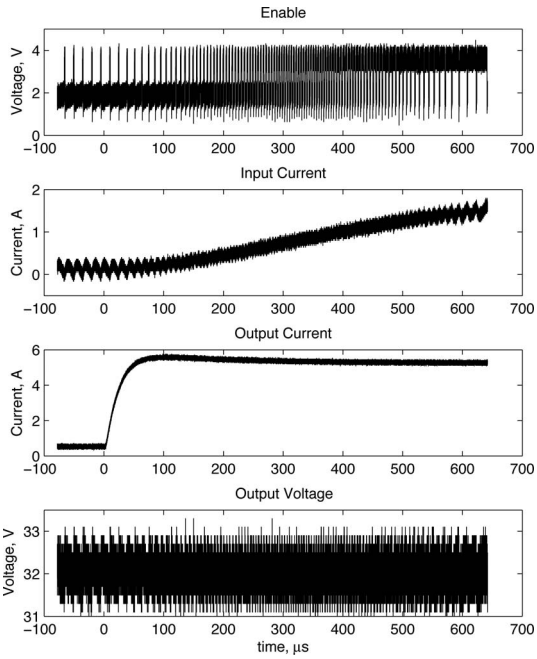


Fig. 25. Converter under a load step of approximately 10–90% of full load, or 18–176 W. $V_{\rm IN} = 170$ V, $R_{\rm load} = 57$–$6\,\Omega$.

careful control of the inverter, it should be possible to avoid any frequency content in the audio band (see, e.g., [34]).

C. Discussion

As can be seen from the results in the previous section, the converter provides good regulation at reasonable efficiencies. The ripple band on the output voltage is somewhat larger than might be desirable for some applications; however, this is not fundamental to converter operation but is rather a result of the design of the controller board only. By adjusting the hysteresis controller or by implementing a different controller type, it should be possible to reduce the ripple band. It should also be noted that the converter transient in response to changes in load

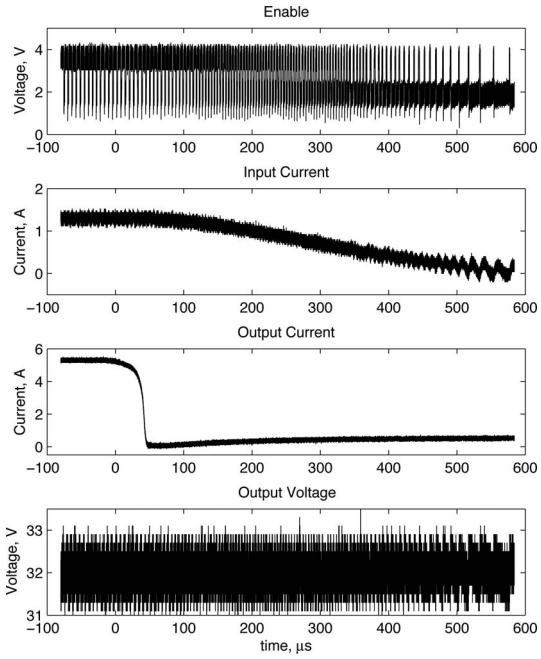


Fig. 26. Converter under a load step of approximately 90–10% of full load, or 175–18 W. $V_{\rm IN} = 170$ V, $R_{\rm load} = 6$–$57\,\Omega$.

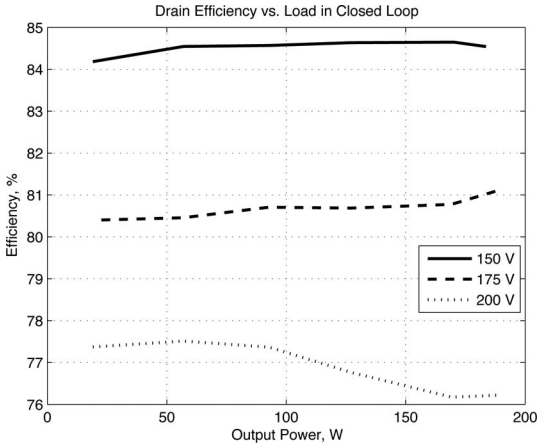


Fig. 27. Closed-loop drain efficiency, i.e., efficiency when gating and control losses are neglected, of the converter at three different input voltages.

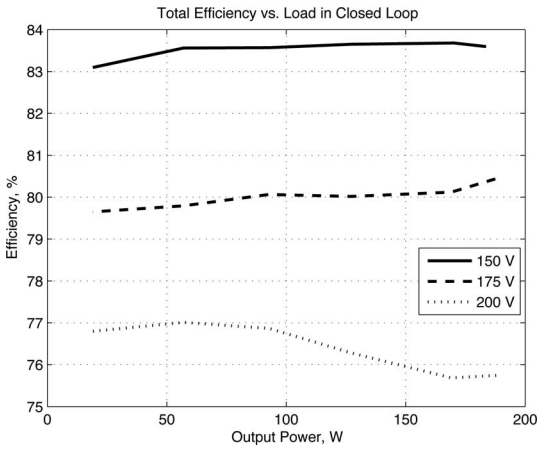


Fig. 28. Closed-loop total efficiency of the converter at three different input voltages. Includes power delivered to the gate and control circuitry.

consists only of changes in modulation frequency and that the output voltage does not leave the ripple band during the load step. In this sense, the converter transient response is "fast," in that it can respond to any load step without voltage excursions outside the ripple band. This behavior is contrasted with that of a traditional pulse width modulated converter requiring additional output filtering to handle rapid changes in load in [1].

Upon measuring the converter transient response, it was found that the peak drain voltage on the main switching device exceeds that device's 500 V rating at input voltages of approximately 180 V and above. This peaking during the startup transient is evident in Fig. 22. The drain voltage exceeds the rated voltage for only one to three cycles each time the converter is turned on. Additionally, this voltage peak takes place when there is no current through the device. It was found that the device withstood the peaks in drain voltage at least long enough for the data in this report to be acquired. It may be that long term operation of the device under overvoltage conditions would cause premature device failure, but this has not been explored.

V. Conclusion

The dc–dc converter presented here offers significant advantages over previous VHF designs. The power stage, based on the Φ_2 inverter, provides efficient dc–dc conversion at VHF with low device stresses. The converter power stage includes only small-valued passive components, and the output capacitance is sized based on ripple considerations rather than on transient performance, which can result in smaller capacitor values [1]. The multistage resonant gate driver developed here provides high-speed, low-loss driving of the inverter. Due to the small values and energy storage of the passive components in both the power stage and gate driver, the transient response can be very fast compared to conventional designs, and the converter is especially well suited to on–off control. Experimental results from a prototype design operating in closed loop at 30 MHz and up to 190 W output and 200 V input demonstrate the effectiveness of the proposed design approach.

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