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Merged Two-Stage Power Converter with Soft Charging Switched-Capacitor Stage in 180 nm CMOS

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***Abstract*—In this paper, we introduce a merged two-stage dc-dc power converter for low-voltage power delivery. By separating the transformation and regulation function of a dc-dc power converter into two stages, both large voltage transformation and high control bandwidth can be achieved. We show how the switched-capacitor stage can operate under *soft charging* conditions by suitable control and integration (merging) of the two stages. This mode of operation enables improved efficiency and/or power density in the switched-capacitor stage. A 5-to-1 V, 0.8 W integrated dc-dc converter has been developed in 180 nm CMOS. The converter achieves a peak efficiency of 81%, with a regulation stage switching frequency of 10 MHz.**

I. INTRODUCTION

The continued downward scaling of the operating voltage of CMOS circuitry has created a demand for dc-dc converters with improved size and performance. There is a need for dc-dc converters with the ability to deliver power at low output voltage (< 2 V) with high bandwidth regulation, while drawing power from a higher input voltage (5-12 V).

Switched-mode magnetics-based power converters (e.g, synchronous buck, three-level buck converter [1]–[3]) operating at low input voltages are able operate at very high switching frequencies when fast low-voltage CMOS transistors are used. The passive components (i.e. inductors and capacitors) can thus be made very small, and the converter can regulate the load at a high control bandwidth. At higher input voltages, however, much lower switching frequencies (a few MHz and below) are used, due to the need to use slow extended-voltage transistors (on die) or discrete high-voltage transistors (off die), resulting in large passive components. Here we demonstrate for the first time an integrated power converter realizing an architecture that bypasses these constraints.

II. ARCHITECTURE

Shown in Fig. 1 is a two-stage architecture that combines a high efficiency switched-capacitor (SC) transformation stage with a high-frequency regulation stage. The architecture, first introduced in [4], achieves both large voltage step-down and high bandwidth regulation across a wide output and input voltage range. The architecture makes use of the transistors typically available in a CMOS process: slow, moderate blocking voltage devices (e.g. thick gate oxide and/or extended drain transistors) and fast, low-voltage transistors. The SC transformation stage, employing slow-switching moderate voltage devices and off-chip capacitors, can be designed for very high power density and efficiency. The intermediate voltage, V_{unreg}, can be made sufficiently low such that the regulation stage can utilize low-voltage, fast-switching transistors that enable high switching frequency with correspondingly high bandwidth regulation and small passive components. The separation of the transformation (step-down) and regulation functionality of the converter into two stages provides substantial advantage: the architecture makes use of the inherent advantages of SC power converters (high voltage step-down, high efficiency), while not tasking it with regulation, which SC converters cannot do efficiently. The regulation functionality is performed by the low-voltage synchronous buck converter, and since that stage operates at low voltage and transformation ratio, it can operate at high frequency with small magnetics size.

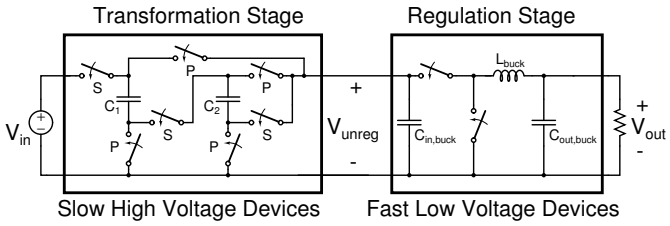
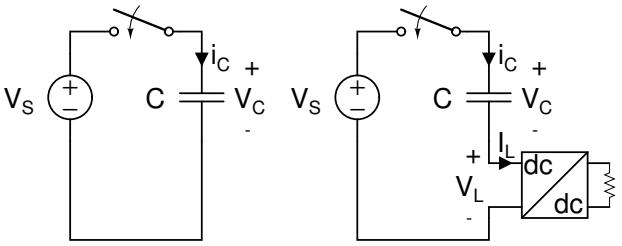


Fig. 1. Block diagram illustrating the two-stage architecture, which enables large voltage step down and high frequency operation on the same die.

A. Soft Charging

The architecture of Fig. 1 can provide yet another attractive benefit if designed and operated in a specific manner ("merging" of the two stages). In this case, the regulation stage can provide *soft charging* of the SC stage, a mode of operation that provides increased efficiency and power density of the SC converter as compared to conventional designs. In a conventional SC power converter, the capacitor size and switching frequency are constrained by the requirement to keep the voltage ripple of the capacitors low to achieve high efficiency [5]. This constraint restricts the designer of SC power converters to either use large capacitors (with corresponding low power density) or operate at a high switching frequency (with attendant increases in switching losses). For a given switch and capacitor technology implementation, conventional SC dc-dc converters are thus limited in terms of their achievable power density and efficiency. Soft charging operation, however, enables an increased capacitor ripple while maintaining low-loss operation.

The circuits shown in Fig. 2 help illustrate the loss mechanism in SC dc-dc power converters, and the role that soft charging can play to decrease power losses. Fig. 2a shows an example of hard charging (sometimes also referred to as impulse charging), which happens at each switching interval



(a) Hard charging. (b) Soft charging.

Fig. 2. Simplified circuits for illustrating capacitor charging in a switched capacitor system. (a) Hard charging in a conventional SC system. (b) Soft charging with energy recovery.

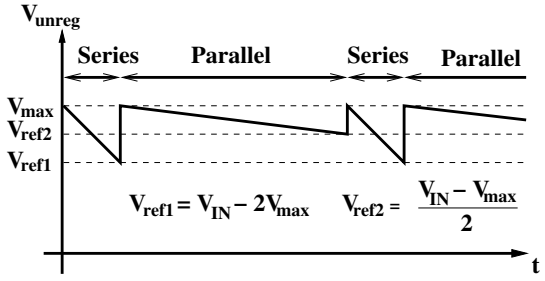


Fig. 3. Ideal waveforms illustrating the switched-capacitor control strategy to maintain the SC stage output voltage below $V_{\max}$, thus enabling the use of low-voltage devices in the regulation stage.

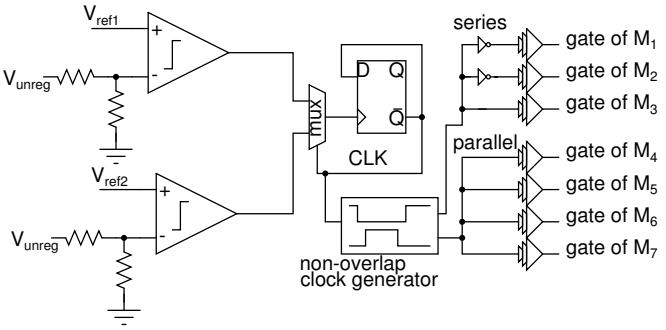


Fig. 4. The control strategy of Fig 3 is implemented using dual comparators and a flip-flop to keep state between series and parallel operation. The 5 V power mosfets (shown in the schematic of Fig. 6) are driven by level-shifted tapered gate drivers.

in conventional SC converters. The capacitor has an initial voltage of $V_C(t<0) = V_S - \Delta V$, and the switch is closed at time $t = 0$. After a sufficiently long time, the capacitor voltage will charge up to V_S. During the charging period, however, $\frac{1}{2}C(\Delta V)^2$ of energy is dissipated as heat in the switch resistance. It should be noted that this energy dissipation is independent of the value of switch resistance, and cannot be reduced by employing a switch with lower on-state resistance. In order to reduce the power loss in conventional SC power converters, one typically attempts to minimize ΔV, either by using large capacitors or by operating at high switching frequency. In doing so, the capacitors are not utilized well from an energy storage perspective, as the ratio of energy transferred in a cycle to energy stored in each capacitor is kept low.

The circuit of Fig. 2b illustrates the soft charging concept. In this circuit, a dc-dc converter is placed in series with the voltage source and capacitor. The dc-dc converter is designed to operate at a much higher switching frequency than the SC stage, so that it appears as a constant power load. The system is designed such that during charging, the majority of the voltage difference between the capacitor and the voltage source appears across the input of the dc-dc converter, instead of the switch resistance, reducing the $\frac{1}{2}C(\Delta V)^2$ energy that would be lost in the hard charging circuit. The important thing to note is that a SC converter operating with soft charging is no longer restricted to keep the capacitor voltage ripple small for efficiency reasons, and can more effectively utilize the energy stored on the capacitors (enabling reduced switching frequency or capacitor size).

In the circuit of Fig. 1, the high frequency regulation stage (a synchronous buck converter) provides soft charging for the series-parallel SC transformation stage. When the SC stage is configured to charge capacitors C_1 and C_2 in series (switches S closed), the capacitors are charged at a rate determined by the power drawn from the regulating stage, ensuring soft charging operation. When the SC stage is configured to discharge C_1 and C_2 in parallel (switches P closed), the capacitor voltages appear directly across the input terminal of the regulating stage, providing soft discharging of the capacitors. It should be noted that the input capacitor of the buck converter, $C_{in,buck}$ is considerably smaller than C_1 and C_2, as it serves only to filter the high frequency ripple of the buck converter.

III. Control

In this section, we present soft charging control techniques suitable for implementation in a CMOS process.

A. Switched Capacitor Stage Control

Conventional SC power converters are often controlled with a simple two-phase clock to alternate between two switch configurations. The soft charging technique presented in this work requires a more sophisticated control implementation to ensure that the SC output voltage stays within a suitable range. Fig. 3 shows a hysteretic control strategy that ensures that the input voltage to the regulation stage is maintained below a maximum value ($V_{\max}$). The value of $V_{\max}$ is chosen to be below the maximum operating voltage of the (low-voltage) transistors of the regulation stage.

Fig 4 shows the on-chip circuitry implementing the control strategy of Fig. 3. The comparators and digital logic are implemented with 2 V, 180 nm CMOS transistors, while the tapered gate drivers use 5 V transistors.

B. Regulation Stage Control

While the SC stage operates with significant output voltage ripple (as seen in Fig. 3), the frequency of this ripple is substantially lower than the control bandwidth of the regulation

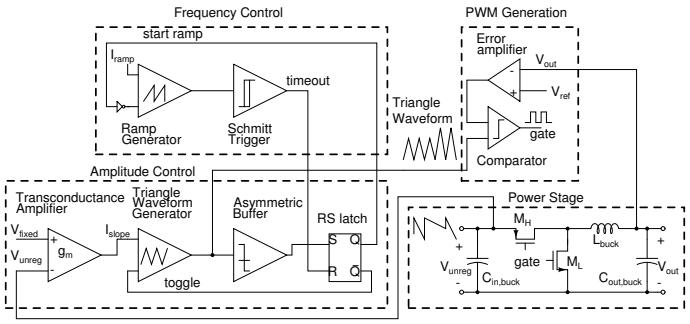


Fig. 5. Block diagram illustrating feed-forward control. The height of the triangle waveform is proportional to the regulation stage input voltage (V_{unreg}).

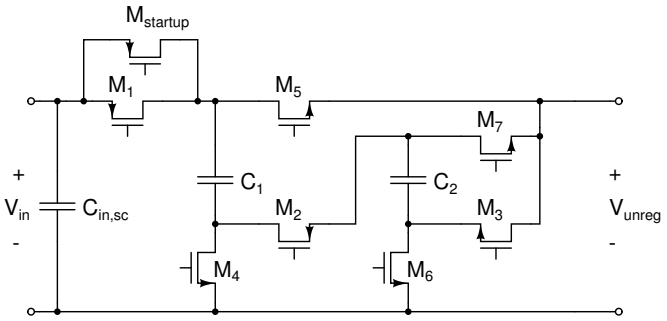


Fig. 6. Schematic drawing of switched-capacitor transformation stage. The capacitors are off-chip, and the transistors are 5 V triple-well thick-oxide devices available in the 180 nm CMOS process.

TABLE I
CONVERTER SPECIFICATIONS

Input Voltage Range	4.5-5 V
Output Voltage Range	1-1.3 V
Output Power Range	0.3-0.8 W
SC Switching Frequency	2-100 kHz (load dependent)
Buck Switching Frequency	10 MHz
Peak Efficiency	81%

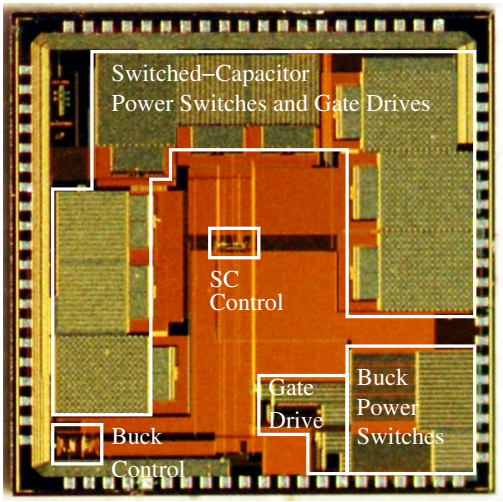


Fig. 7. Die photograph of the converter implemented in 180 nm CMOS technology. The total die area is 5x5 mm, although much of that area is not used.

stage (this is possible because the switching frequency of the regulation stage is many times higher than the switching frequency of the SC stage). However, the transitions at the switching intervals nevertheless present a problem to a regular feedback controller, and the sharp edges can appear at the output (audio susceptibility). In order to maintain the output voltage steady despite the sharp voltage transitions at its input terminals, the regulation stage employs feed-forward control, as shown in Fig. 5. The feed-forward control is accomplished by making the amplitude of the triangle wave reference proportional to the buck converter input voltage (V_{unreg}). With this method, any sharp edges in the input voltage will immediately appear as an increased triangle amplitude at the input of the comparator, which controls the PWM signal to the gate. The overall feedback loop (controlled by the compensation network of the error amplifier) can still be kept slow enough to ensure stability. Meanwhile, the response of the feed-forward control can be made very fast, and is only limited by the speed of the transconductance amplifier which controls the triangle waveform amplitude. The feed-forward circuitry of Fig 5 was implemented on-die, using 180 nm core transistors and on-chip capacitors and resistors for compensation networks, and off-chip controllable bias currents to accommodate a wide switching frequency range of the regulation stage.

IV. CMOS IMPLEMENTATION

The soft charging two-stage architecture of Fig 1 with the control circuitry described in section 3 has been implemented in a 180 nm CMOS process. Table I lists the specifications of the converter.

A schematic drawing of the SC transformation stage is shown in Figure 6. The transistors in the SC stage are 5 V isolated triple-well thick-oxide devices with extended drain regions. The capacitors C_1 and C_2 are 22 μF off-chip ceramic (X5R) capacitors, and the transistor $\mathrm{M_{startup}}$ is activated during startup (by the on-chip control circuitry) to ensure that the SC output voltage never rises above 2 V (the maximum working voltage of the regulation stage transistors) by slowly charging capacitors C_1 and C_2. During regular operation, $\mathrm{M_{startup}}$ remains off.

Shown in Fig. 7 is an annotated die photo of the converter. It can be seen that the majority of the die area is taken up by the SC power transistors, as they are high voltage devices switching at low frequency. It should be noted that the design was not optimized for die area but was instead driven by the required number of I/O pins for power delivery, control, and testing. This resulted in a IC package size that was larger than the required active die area of the converter.

The 10 MHz regulation stage switching frequency enables the use of a very small output inductor (28 nH Coilcraft air-

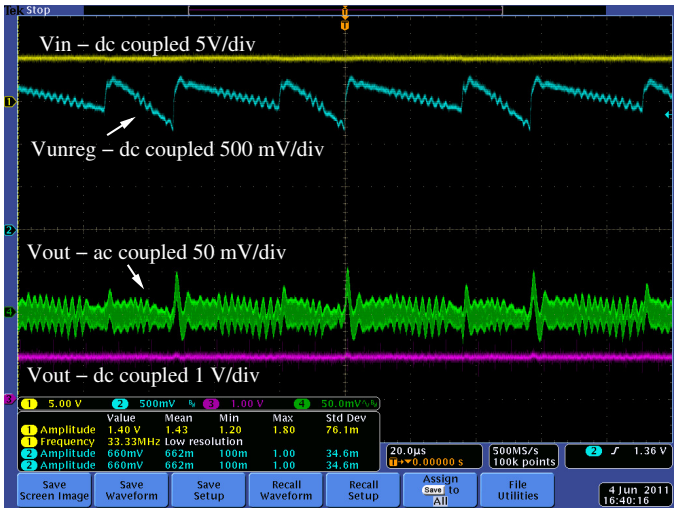


Fig. 8. Experimental waveforms showing converter operation. Note that the input voltage is 4.5 V, and the output voltage is steady at 1 V, despite the large voltage swings at the input of the buck converter (V_{unreg}).

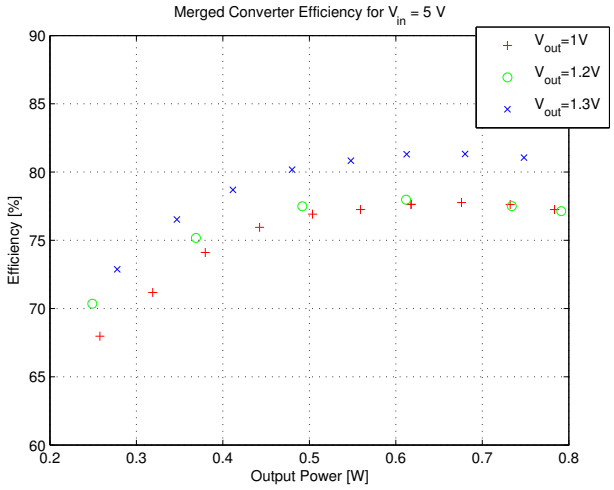


Fig. 9. Plot showing measured efficiency for the prototype merged two-stage converter across output power range. All control and gate drive losses are included in the efficiency measurement.

core) and capacitors (2 and 4.7 μF for $C_{in,buck}$ and $C_{out,buck}$, respectively). As a comparison, a single-stage conventional buck converter tasked with operating at an input voltage of 5 V would not be able to operate at 10 MHz with low loss, owing to the large parasitic losses associated with 5 V devices operated at high frequency, and would therefore have significantly larger passive components.

V. Experimental Results

Shown in Fig. 8 are experimental waveforms of the converter. The input voltage in this plot is 4.5 V, and the output is regulated to 1 V. Note that despite the large voltage ripple at the input of the regulation stage (V_{unreg}), the feed-forward control maintains a steady output voltage.

Measured efficiency for for a few different output voltages are shown in Fig. 9. The efficiency measurement includes all power losses associated with the control circuitry, as well as gating losses. The decrease in efficiency at low input power is almost entirely due to the regulation stage, which was operated at a fixed frequency (10 MHz) at all times. Efficiency at low power levels can be increased with suitable light-load control schemes such as pulse-frequency modulation (PFM), if desired. The SC stage is inherently light-load efficient due to the hysteretic controller, which automatically operates at a lower switching frequency at low output power.

Table II shows an estimated breakdown of losses. A significant portion of the losses come from bond-wire resistance and on-chip metallization resistance, owing to the package used. There are well-known techniques to mitigate these losses (e.g thick top layer metallization, flip-chip technology). It is therefore expected that the overall converter efficiency can be significantly improved through appropriate packaging techniques.

TABLE II
Estimated Converter Loss Breakdown at P_{out}=0.8 W

Bond-wire conduction loss	60 mW
Transistor gating loss	45 mW
On-die metallization conduction loss	40 mW
Transistor conduction loss	11 mW
Inductor loss	5 mW
Control losses	2 mW

VI. Conclusion

An integrated 5-to-1 V merged two-stage converter has been developed, which enables both large voltage step-down and high frequency operation. Through appropriate control and coupling between the transformation and regulation stages, soft charging of the switched-capacitor stage is achieved. On-chip control circuitry to enable this mode of operation is presented, along with the power stage implementation. Experimental results show good efficiency, as well as stable operation over the entire input and output voltage range.

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