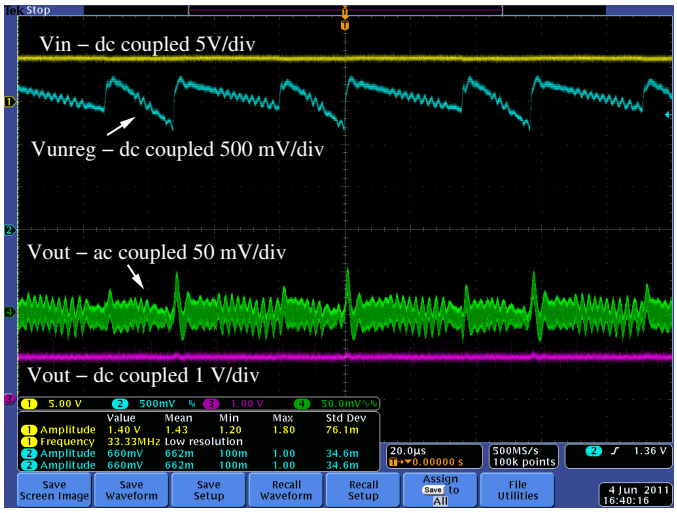

Fig. 8. Experimental waveforms showing converter operation. Note that the input voltage is 4.5 V, and the output voltage is steady at 1 V, despite the large voltage swings at the input of the buck converter (V_{unreg}).

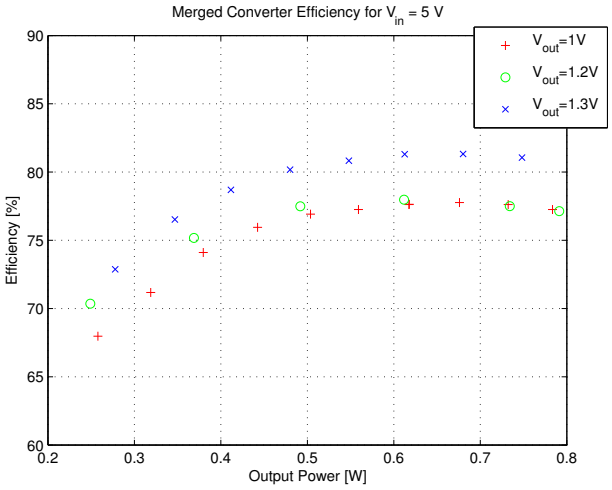

Fig. 9. Plot showing measured efficiency for the prototype merged two-stage converter across output power range. All control and gate drive losses are included in the efficiency measurement.

core) and capacitors (2 and 4.7 μF for $C_{in,buck}$ and $C_{out,buck}$, respectively). As a comparison, a single-stage conventional buck converter tasked with operating at an input voltage of 5 V would not be able to operate at 10 MHz with low loss, owing to the large parasitic losses associated with 5 V devices operated at high frequency, and would therefore have significantly larger passive components.

V. Experimental Results

Shown in Fig. 8 are experimental waveforms of the converter. The input voltage in this plot is 4.5 V, and the output is regulated to 1 V. Note that despite the large voltage ripple at the input of the regulation stage (V_{unreg}), the feed-forward control maintains a steady output voltage.

Measured efficiency for for a few different output voltages are shown in Fig. 9. The efficiency measurement includes all power losses associated with the control circuitry, as well as gating losses. The decrease in efficiency at low input power is almost entirely due to the regulation stage, which was operated at a fixed frequency (10 MHz) at all times. Efficiency at low power levels can be increased with suitable light-load control schemes such as pulse-frequency modulation (PFM), if desired. The SC stage is inherently light-load efficient due to the hysteretic controller, which automatically operates at a lower switching frequency at low output power.

Table II shows an estimated breakdown of losses. A significant portion of the losses come from bond-wire resistance and on-chip metallization resistance, owing to the package used. There are well-known techniques to mitigate these losses (e.g thick top layer metallization, flip-chip technology). It is therefore expected that the overall converter efficiency can be significantly improved through appropriate packaging techniques.

TABLE II
Estimated Converter Loss Breakdown at P_{out}=0.8 W

Bond-wire conduction loss	60 mW
Transistor gating loss	45 mW
On-die metallization conduction loss	40 mW
Transistor conduction loss	11 mW
Inductor loss	5 mW
Control losses	2 mW

VI. Conclusion

An integrated 5-to-1 V merged two-stage converter has been developed, which enables both large voltage step-down and high frequency operation. Through appropriate control and coupling between the transformation and regulation stages, soft charging of the switched-capacitor stage is achieved. On-chip control circuitry to enable this mode of operation is presented, along with the power stage implementation. Experimental results show good efficiency, as well as stable operation over the entire input and output voltage range.

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