Design Methodology for a Very High Frequency Resonant Boost Converter

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Abstract—**This document introduces a design methodology for a resonant boost converter topology that is suitable for operation at very high frequencies. The topology we examine features a low parts count and fast transient response but suffers from higher device stresses compared to other topologies that use a larger number of passive components. A numerical design procedure is developed for this topology that does not rely on time-domain simulation sweeps across parameters. This allows the optimal converter design to be found for a particular main semiconductor switch. If an integrated power process is used where the designer has control over layout of the semiconductor switch, the optimal combination of converter design and semiconductor layout can be found. To validate the proposed converter topology and design approach, a 75 MHz prototype converter is designed and experimentally demonstrated. The performance of the prototype closely matches that predicted by the design procedure, and achieves good efficiency over a wide input voltage range.**

I. INTRODUCTION

Increasing the switching frequency of DC/DC converters has the benefits of requiring less passive energy storage and providing improved transient performance. Since passive components typically dominate converter size, increasing the switching frequency is a crucial step in the development of a fully integrated or co-packaged power converter. Among the challenges standing in the way of such developments, however, are loss mechanisms that grow with switching frequency [1], [13]. Switching loss can be mitigated by using a circuit topology that operates with soft-switching to avoid both capacitive discharge and the overlap of voltage and current at the switching instants. Gating loss that arises from charging and discharging the gate capacitor each cycle can be reduced by using a resonant gate driver to recover a portion of the energy stored in the gate [1],[3]-[5], and/or through transistor layout optimization [16]. With these frequency dependent device losses minimized, the converter can be operated at a frequency high enough to use air core or low permeability RF core inductors to avoid the losses from high permeability magnetic materials.

This concept has been successfully demonstrated for boost conversion at frequencies up to 110MHz using a resonant boost Φ_2 converter topology in [5],[7], and [10]. This topology uses a multi-resonant network to shape the switch's drain-to-source voltage waveform to approximate a square wave with a peak value of about $2V_{IN}$ (under ideal conditions). In this paper an alternative resonant boost converter topology is explored that uses fewer passive components but suffers from a higher peak drain-to-source voltage. We develop a design procedure for this topology that readily yields necessary component values. This procedure — unlike previous design methodologies for similar topologies [11],[12] — is based on direct analysis of the topology and does not rely on lengthy time-domain simulation sweeps across circuit parameters to identify desirable design points.

Section II of the paper presents an overview of the topology and how it relates to previous RF converter designs. Section III of the paper details the proposed design method and illustrates how it is applied to design a converter. Section IV validates the proposed design methodology and presents experimental results from a 75 MHz converter. The performance of the prototype design is shown to closely match that predicted by the design procedure. Finally, section V concludes the paper.

II. RESONANT BOOST CONVERTER TOPOLOGY

A schematic of the power stage of the proposed converter is shown in Figure 1. This converter topology operates with zero voltage switching by tuning the resonant elements (L_F, L_R, C_E, and C_R) such that when the switch is opened, the drain-to-source voltage of the switch will naturally ring up and then back to zero half of a switching period later.

It should be noted that aside from the important aspects of component values and control, the circuit of Figure 1 is topologically equivalent to the ZVS multiresonant boost converter of [14] and to the resonant boost converter of [13]. The difference in design between the converter of [14] and here is quite large owing to major differences in control (constant on-time variable frequency vs. burst mode control) and the resulting difference in the choice of component values. The design here is more similar to that of [13], but differs substantially from both [14] and [13] in that the inductor L_F in Figure 1 is a resonant inductor rather than a simple choke as in [14] and [13]. This design choice provides much

faster response under on-off control than is achievable with a choke inductor and results in different design considerations and component selections.
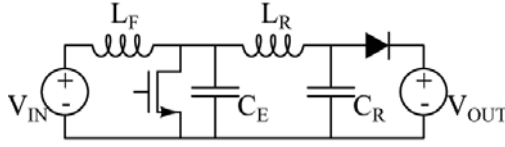

Fig. 1.   Power section schematic of the proposed boost converter.

The converter is designed to operate with fixed switching frequency and duty cycle. This makes available the use of highly efficient resonant gate drivers when desired. While varying the frequency or duty cycle is not used for control, an on-off modulation scheme can be employed where the entire converter is switched on and off at a modulation frequency much less than the switching frequency of the converter [3]-[7],[11],[12],[13].

III. DESIGN METHODOLOGY

Here we develop a design procedure for the proposed converter circuit that both provides insight into the converter's operation and is straight-forward to use. Single-switch resonant power converters have often been designed through an iterative modeling approach, in which one starts from some approximate component values and searches for good designs through a series of time-domain simulations sweeping parameters (e.g. using SPICE simulations [12],[13]). This approach is workable, especially for an experienced designer with good knowledge of a particular topology. However, due to the large number of parameters that can be varied, it is difficult for the designer to know if they have reached the optimal design. We seek to remedy this issue here. Additionally, when designing a converter where the main switching device will be fabricated from an integrated power process, the designer has the ability to change the layout of the device to vary the parasitics. Methods have been developed to find the optimal device layout for a particular converter design [16]. However, previous design methods for such circuits have not been sufficiently simple that one can easily vary both the device layout and the converter design to find the best possible combination. Enabled by the simplicity of this converter topology, a design procedure is developed here that aims to address these challenges.

With four energy storage elements, the converter is described by fourth order differential equations. Additionally, since the converter contains two switching devices, there are a four different circuit configurations possible. Thus, a comprehensive mathematical description of the converter requires four sets of fourth order differential equations. This is further complicated by the fact that the switching times of the diode are unknown. Clearly, deriving a complete set of closed form equations to directly describe the converter is a cumbersome and unfruitful task. For this reason, the simplifying assumption is made that the rectifier's LC tank, formed by L_R and C_R,

is high Q, and the current in inductor L_R, labeled I_{RECT}, is sinusoidal with a DC offset.

$$I_{RECT} = I_{AC} \sin{(\omega_s t + \phi_1)} + \frac{P_{OUT}}{V_{OUT}} \quad (1)$$

This allows the inverter and rectifier to be separated for analysis. The inverter design is then found by replacing the rectifier with a sinusoidal current source. Similarly, the rectifier design can then be found by replacing the inverter with a sinusoidal voltage source. Making this assumption simplifies the problem to the point where a converter solution is readily obtained, but at the cost of the accuracy. Since the current I_{RECT} is actually not purely sinusoidal, there will be some error in the solution. Typically the rectifier has a modest loaded Q, and the error is small enough such that the designer can easily make small corrections to the resulting component values when simulating the converter in SPICE.
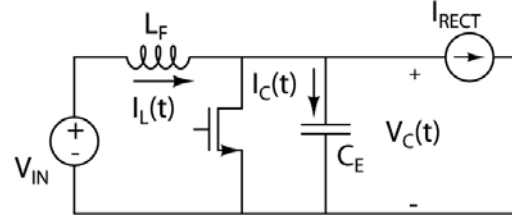

Fig. 2.   Schematic of the inverter used for analysis with the rectifier modeled as a current source labeled I_{RECT}.

A. Inverter Analysis

In this analysis, the duty cycle of the inverter is set to 50%. While this is not a fundamental limit, it is a good design choice to ease the use of a resonant gate driver. With the duty cycle of a half, the time period $0 \le t < T_S/2$ is defined as period with the switch turned off, and $T_S/2 \le t < T_S$ as the period with the switch on.

The analysis starts at $t = 0$, when the switch has just turned off. The node equations in this time period (with the switch off) form a second order differential equation for the voltage $V_C(t)$.

$$L_F C_E \frac{d^2 V_C(t)}{dt^2} + V_C(t) = V_{IN} - \omega_s I_{AC} L_F \cos{(\omega_s t + \phi_1)} \quad (2)$$

The general solution to this equation is:

$$V_C(t) = \frac{\omega_s L_F I_{AC}}{\omega_s^2 L_F C_E - 1} \cos{(\omega_s t + \phi_1)} \\ + C_1 e^{-jt/\sqrt{L_F C_E}} + C_2 e^{jt/\sqrt{L_F C_E}} + V_{IN} \quad (3)$$

where C_1 and C_2 are constants. To solve for these constants, two initial conditions are required. The capacitor voltage at $t = 0^+$ is known to be 0 since the switch was turned on at $t = 0^-$. The initial inductor current is not known, and the constants are found in terms of the initial inductor current, $I_L(0)$, resulting in the following equation:

$$V_C(t) = Z_o \left[(r_o - 1) I_{AC} \sin \phi_1 + I_L(0) - \frac{P_{OUT}}{V_{OUT}} \right] \sin(\omega_o t)$$
$$- \left[\frac{Z_o \omega_s}{\omega_o} r_o I_{AC} \cos \phi_1 + V_{IN} \right] \cos(\omega_o t)$$
$$+ \frac{Z_o \omega_s}{\omega_o} r_o I_{AC} \cos(\omega_s t + \phi_1) + V_{IN}$$
$$\text{for } 0 \le t \le T_S/2$$
$$(4)$$

where

$$\omega_o = \frac{1}{\sqrt{L_F C_E}}, \quad Z_o = \sqrt{\frac{L_F}{C_E}}, \quad \text{and} \quad r_o = \frac{(\omega_s/\omega_o)^2}{(\omega_s/\omega_o)^2 - 1}.$$

From Equation 4 we see that there are five unknown quantities that must be found: the resonant frequency and characteristic impedance of L_F and C_E (ω_o and Z_o), the magnitude and phase of the rectifier current (I_{AC} and ϕ_1), and the initial current in $L_F(I_L(0))$. To solve for these unknowns, design constraints are applied to the system:

1) Since average power is only delivered by DC current from the source, the DC current in L_F is constrained by conservation of energy.

$$\langle I_L(t) \rangle = \frac{P_{OUT}}{V_{IN}} \qquad (5)$$

where

$$I_L(t) = \frac{1}{L_F} \int_0^t (V_{IN} - V_C(t)) \, dt + I_L(0) \qquad (6)$$

2) The inverter must operate in periodic-steady-state:

- The average voltage across L_F must be 0.

$$\langle V_C(t) \rangle = V_{IN} \qquad (7)$$

- The average current through C_E must be 0.

$$\langle I_C(t) \rangle = 0 \qquad (8)$$

where

$$I_C(t) = \begin{cases} I_L(t) - I_{RECT} & 0 \le t < T_S/2 \\ 0 & T_S/2 \le t < T_S \end{cases} \qquad (9)$$

Since the capacitor does not conduct any current when the switch is on and had an initial voltage of 0, this constraint is equivalent to setting the capacitor voltage to 0 at the switching instant. Thus, a separate constraint for zero-voltage-switching is not required.

3) It is chosen to constrain the switch voltage to have zero slope at the turn-on switching instant. This ensures that there is no current in C_E at the switching instant and results in the least amount of ringing in the circuit.

$$\left. \frac{dV_C(t)}{dt} \right|_{t=T_s/2} = 0 \qquad (10)$$

Application of these constraints to the circuit node equations results in four non-linear equations. Since there are five

unknown quantities and only four constraints, the system has one free variable. In this development, it is chosen to use this free variable to leave ω_o unconstrained. This allows the designer to trade additional circulating resonant currents in the inverter for smaller values of L_F and larger values of C_E.

Additionally, to aid in matching the inverter solution to a rectifier solution, it is desirable to leave the rectifier's current (I_{RECT}) phase ϕ_1 unconstrained. This is obtained by loosening the constraint that the switch's drain voltage must have zero derivative at the turn-on switching instant. Rather than constraining the derivative to be zero, it can instead be held to a small value. This gives the designer some choice of ϕ_1.

The resulting non-linear equations are solved numerically in MATLAB. The solution for the inverter is shown in Figure 3 where the inductance and capacitance of L_F and C_E are plotted versus switching frequency and rectifier phase, ϕ_1 (as specified in (1)). The solution describes a converter with an input and output voltage of 12 and 30 Volts and an output power of 7 Watts.
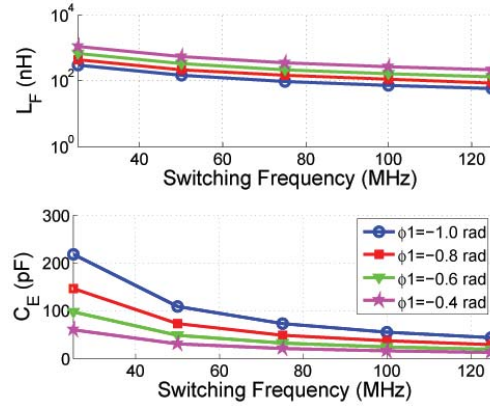

Fig. 3. Numerical solution to the inverter. Solution assumes an input and output voltage of 12 and 30 Volts and an output power of 7 Watts. ϕ_1 is the rectifier's current phase, as specified in (1).

B. Rectifier Analysis

Similar to the approach taken for the inverter, the rectifier design is determined by replacing the inverter with a sinusoidal voltage source with a DC component, labeled V_{INV} and shown in Figure 4.

$$V_{INV} = V_{AC} \sin(\omega_s t + \phi) + V_{IN} \qquad (11)$$

V_{AC} and ϕ are the fundamental component and phase of $V_C(t)$ (the drain to source voltage of the inverter).

Unlike the inverter, the rectifier's duty cycle is unknown. When the diode turns on, the voltage $V_D(t)$ is held at V_{OUT}, and there is no current in the capacitor C_R. The diode turns off when $I_R(t)$ crosses zero, reversing the direction of current in the diode. While the diode is off the resonant circuit rings until $V_D(t)$ reaches V_{OUT} again and the diode turns back on. For analysis the times that the diode turns on and off in a cycle are labeled t_{on} and t_{off}.
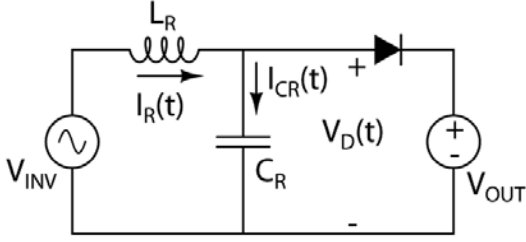
Fig. 4. Schematic of the rectifier used for analysis with the inverter modeled as a voltage source, labeled V_{INV}.

The following differential equation describes the rectifier voltage, $V_D(t)$, for the time period with the diode off, $t_{off} \leq t < t_{on} + T_S$:

$$L_R C_R \frac{d^2 V_D(t)}{dt^2} + V_D(t) = V_{IN} + V_{AC} \sin(\omega_s t + \phi) \quad (12)$$

The general solution to this differential equation is:

$$V_D(t) = \frac{V_{AC}}{1 - (\omega_s/\omega_r)^2} \sin(\omega_s t + \phi) \\ + C_1 e^{(-j\omega_r t)} + C_2 e^{(j\omega_r t)} + V_{IN} \quad (13)$$

where C_1 and C_2 are constants. With the rectifier, there are two known initial conditions that occur when the diode turns off.

$$V_D(t_{off}) = V_{OUT} \quad (14)$$

$$I_R(t_{off}) = 0 \quad (15)$$

Upon applying these initial conditions the rectifier voltage becomes:

$$V_D(t) = (rV_{AC} \sin(\omega_s t_{off} + \phi) + V_{OUT} - V_{IN}) \cos(\omega_r(t - t_{off})) \\ + r(\omega_s/\omega_r) V_{AC} \cos(\omega_s t_{off} + \phi) \sin(\omega_r(t - t_{off})) \\ - rV_{AC} \sin(\omega_s t + \phi) + V_{IN} \\ \text{for} \quad t_{off} \leq t < t_{on} + T_S \quad (16)$$

where

$$\omega_r = \frac{1}{\sqrt{L_R C_R}}, \quad Z_R = \sqrt{\frac{L_R}{C_R}}, \quad \text{and} \quad r = \frac{1}{(\omega_s/\omega_r)^2 - 1} .$$

From equation 16 it is found that the rectifier has four unknown quantities: the resonant frequency and characteristic impedance of L_R and C_R (ω_r and Z_R), and the times that the diode turns on and off (t_{on} and t_{off}). As with the inverter, design constraints are applied to the voltages and currents in the circuit to solve for the unknown values.

1) Since average power is only delivered to the load by DC current, the DC current in L_R is constrained by conservation of energy.

$$\langle I_R(t) \rangle = \frac{P_{OUT}}{V_{OUT}} \quad (17)$$

where

$$I_R(t) = \frac{1}{L_R} \int_{t_{off}}^{t} (V_{AC} - V_D(t)) \, dt \quad (18)$$
$$\text{for} \quad t_{off} < t < t_{off} + T_S$$

2) The rectifier must operate in periodic-steady-state:
   - The average inductor voltage must be 0.

$$\langle V_D(t) \rangle = V_{IN} \quad (19)$$

   - The average capacitor current must be 0.

$$\langle I_{CR}(t) \rangle = 0 \quad (20)$$

where

$$I_{CR}(t) = C_R \frac{d}{dt} V_D(t) \quad (21)$$

3) The phase of the fundamental component of $I_R(t)$ is constrained by the inverter.

Application of these constraints results with four non-linear equations that are solved numerically in MATLAB. Figure 5 shows the solution in terms of the inductance and capacitance of L_R and C_R versus switching frequency and the phase of the fundamental component of the rectifier current, ϕ_1.
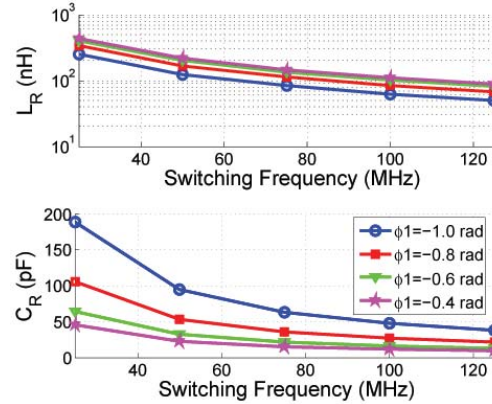

Fig. 5. Numerical solution to the rectifier. Solution assumes an input and output voltage of 12 and 30 Volts and an output power of 7 Watts. ϕ_1 is phase of the fundumental component of $I_R(t)$.

C. Converter Loss Analysis and Device Layout Optimization

Additionally, with all of the converter's voltage and current waveforms described mathematically, it is possible to estimate the losses in the circuit. To do this, the loss mechanisms of all of the components must be modeled. For all of the components except possibly the main semiconductor switch, the loss mechanisms can be determined from datasheets. Layout of the semiconductor switch can be optimized for the particular converter design. Thus, it is not necessary to use only a single switch design to calculate loss. Rather, for each design point, the optimal switch layout can be calculated, and then the converter losses evaluated.
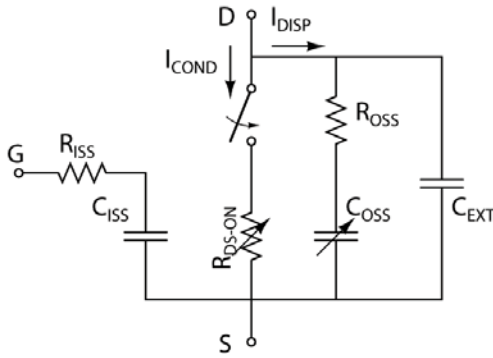
Fig. 6. Simplified MOSFET model showing device parasitics that are important to converter operation at RF.

A model of the switch that includes the parasitic components that are important to RF operation is shown in Figure 6.

These parasitic components are parameterized by the switch geometry, and then the space bounded by the process design rules and the available chip area is searched to find the device layout that results in the least amount of loss, using an approach similar to that of [16]. When varying the device size, three primary device losses trade with each other: gating loss, conduction loss, and displacement loss (the loss in the device output capacitance). For sinusoidal resonant gating, the total device loss is given by:

$$P_{TOT} = 2R_{ISS}(\pi V_{G,AC} f_{SW} C_{ISS})^2$$
$$+ \left(\frac{I_{DISP,RMS}}{C_{TOT}}\right)^2 C_{OSS}^2 R_{OSS} + I_{COND,RMS}^2 R_{DS-ON} \qquad (22)$$

where $V_{G,AC}$ is the amplitude of the sinusoid driving the transistor gate, f_{SW} is the switching frequency of the converter, C_{TOT} is the total drain-to-source capacitance ($C_{OSS} + C_{EXT}$), $I_{COND,RMS}$ and $I_{DISP,RMS}$ are RMS converter operating currents, and the remaining variables are parasitic elements shown in Figure 6.

Thus, by increasing the size of the device, the conduction loss is reduced, but the gating loss and displacement loss are increased. When designing a converter using the typical iterative modeling approach in which converter designs are found using time-domain simulations sweeping parameters, the designer would use values of $I_{DISP,RMS}$ and $I_{COND,RMS}$ that were found from simulation for the device optimization. With the design methodology proposed here, $I_{DISP,RMS}$ and $I_{COND,RMS}$ are described mathematically. This enables the design optimization to be run for each design point with little added effort. Figure 7 shows the result of such an optimization by plotting normalized converter losses versus switching frequency and rectifier current phase for the design target considered previously and switch parameters from an integrated power process having LDMOS transistors. The figure shows the size of the optimal device to illustrate how the

same device is not optimal for all designs (the design sweep further assumes inductor Q of 120 @ 120 MHz and a simple diode loss model based on the S310 Schottky diode).
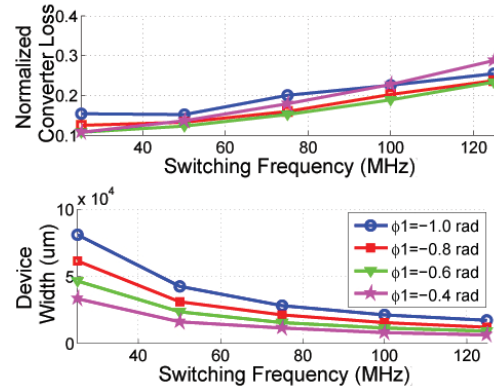

Fig. 7. The upper figure shows total converter loss estimated by the numerical converter solution, and the lower figure is the the optimal transistor size at each frequency and design point. The normalization is to converter output power.

D. Design Example

In this section, the proposed design methodology is used to design a converter to boost 12 Volts to 30 Volts with a peak power of 7 Watts. It is important to note that device parasitics greatly constrain the available design space. It is chosen to use the S310 silicon Schottky diode which has an equivalent reverse biased junction capacitance of approximately 55 pF. Additionally, a custom LDMOS device fabricated from an integrated power process is used as the main switch, which has an equivalent C_{OSS} of approximately 34 pF. From Figure 7 it is chosen to operate the converter at 75 MHz for an efficiency of about 85%. With the switching frequency now chosen, the converter solutions are re-plotted to show more of the available design space, shown in Figures 8 and 9. From Figure 8 we see that to accommodate the diode's parasitic capacitance ϕ_1 must be less than about -1 radian. Figure 10 shows that tuning ϕ_1 further out of phase results in more loss. Thus, it is chosen to design the converter with $\phi_1 = -1$ radian to achieve the best efficiency. From Figure 8 it is found the $L_R = 83.5nH$ and $C_R = 62.6pF$. Finaly, the last design choice is ω_o, the resonant frequency of the inverter. Choosing a small ω_o results in a large value of L_F slowing the transient response of the converter. Since the converter is intended to be operated with on-off modulation, fast transient response is a necessity. Thus ω_o must be chosen high enough to achieve a fast enough response. Choosing ω_o higher than is required results in circulating extra current in the inverter leading to lower efficiency. Based on these criterea, it is chosen to set $\omega_o = 0.85\omega_s$. Referencing Figure 9, we find that $L_F = 80.3nH$ and $C_E = 77.4pF$.

To verify the solution, the converter is simulated in SPICE. From the simulation output, shown in Figure 11, one can observe the error produced by the design methodology (e.g.
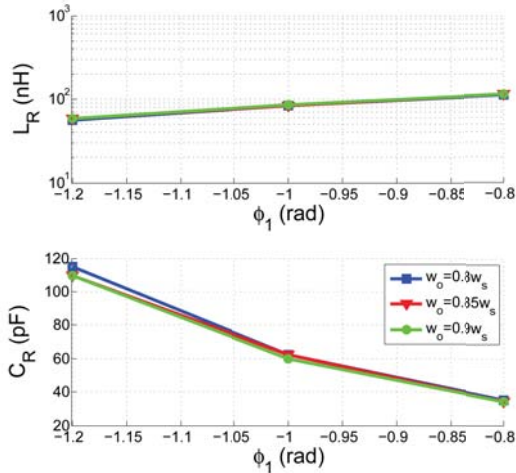
Fig. 8. Numerical solution to the rectifier with the selected frequency (75 MHz). Solution assumes an input and output voltage of 12 and 30 Volts and an output power of 7 Watts. ϕ_1 is the rectifier's current phase, and ω_o is the resonant frequency of the inverter.
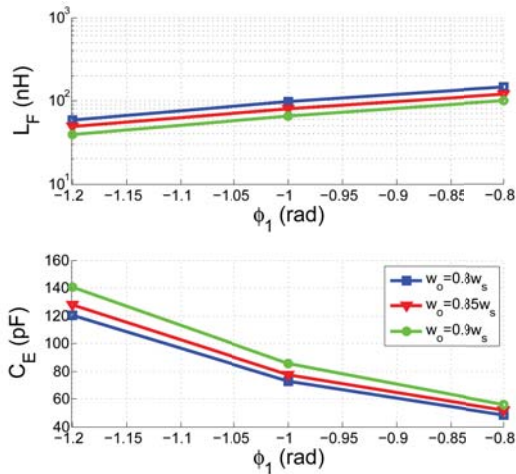

Fig. 9. Numerical solution to the inverter with the selected frequency (75 MHz). Solution assumes an input and output voltage of 12 and 30 Volts and an output power of 7 Watts. ϕ_1 is the rectifier's current phase, and ω_o is the resonant frequency of the inverter.

owing to the sinusoidal current approximation). This error is easily corrected, however. First both inductors are adjusted to standard value of 82 nH, and the rectifier capacitance C_R is set to 55pF such that no additional capacitance is required beyond the diode's junction capacitance. From Figure 11, we observe that $V_C(t)$ crosses zero too soon; thus, C_E is increased to 86 pF by adding additional (external) capacitance to achieve zero-voltage-switching.

IV. EXPERIMENTAL RESULTS

To evaluate this converter topology and design approach, a prototype power stage was constructed. Aiming to validate the design methodology, the prototype converter was constructed
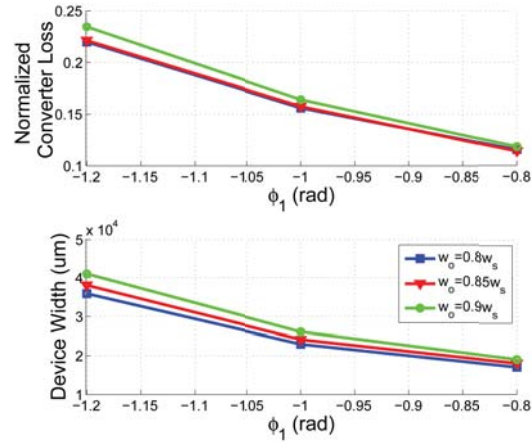

Fig. 10. With the selected frequency (75 MHz), the upper figure shows total converter loss estimated by the numerical converter solution, and the lower figure is the the optimal transistor size. ϕ_1 is the rectifier's current phase, and ω_o is the resonant frequency of the inverter.
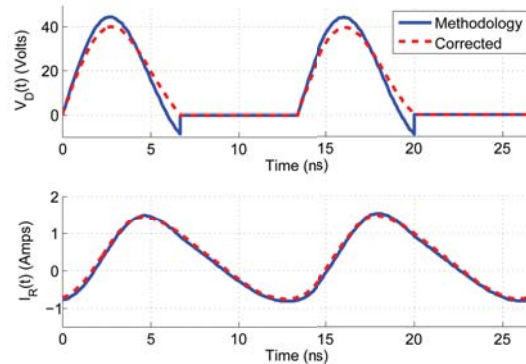

Fig. 11. Simulated converter waveforms using component values found from the design methodology, and after making small adjustments to compensate for the error.

with the same specifications used in the design example of the previous section, summarized in Table I.

Vin	Vout	Pout	Fs
12V	30V	7W	75MHz

TABLE I
TARGET CONVERTER SPECIFICATIONS FOR THE EXPERIMENTAL IMPLEMENTATION.

A schematic of the converter is shown in Figure 12, and a photograph of the converter is shown in Figure 13. The rectifier capacitor C_R is entirely composed by the diode parasitic junction capacitance. This allows parasitic inductance in the rectifier to be absorbed into L_R, leading to more optimal performance. The capacitor C_E is made up of the parallel combination of the transistor output capacitance (34pF) and a discrete 51.7pF capacitor. Figure 14 shows measured converter waveforms and a comparison to simulated SPICE waveforms.

The close agreement of the waveforms validates the operation of the prototype. Efficiency over the input voltage range for two specified output power levels are presented in Figure 15. Based on these results, one can observe that the proposed topology and design approach lead to good performance at very high frequencies.
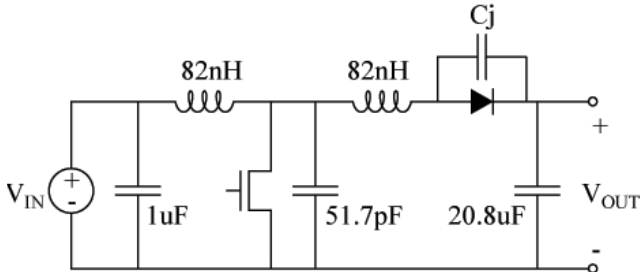

Fig. 12. Schematic of the experimental implementation. The inductors are from the midi-spring family from Coilcraft, and the Diode is an S310 Schottky diode from Comchip Technology. The MOSFET is a LDMOS device fabricated from an integrated power process. The converter operates at 75MHz with a 50% duty cycle.

Fig. 13. Photograph of the converter prototype PCB.

V. CONCLUSION

This document presents a resonant boost converter topology that is suitable for operation at very high frequencies. The topology uses a small number of passive components. Moreover, only small-valued resonant inductors are used, enabling fast response under on-off control.

The paper further introduces a procedure to design the proposed resonant boost converter. Unlike some previous design methods for similar converter types, the method here does not require extensive time-domain simulation sweeps across circuit parameters. Rather, the procedure is based on numerical solutions to closed-form circuit equations. This enables the designer to rapidly find the optimal converter design given a particular semiconductor switch, or the optimal combination
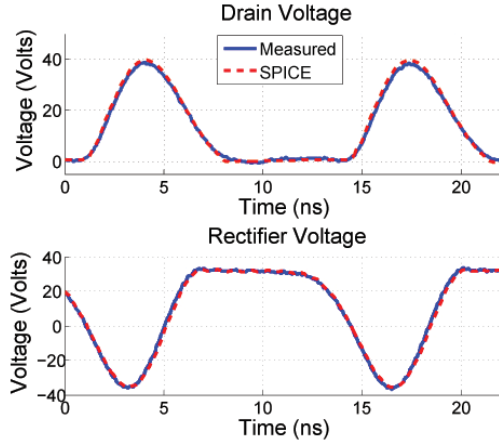

Fig. 14. Measured converter waveforms compared so simulated waveforms in SPICE.
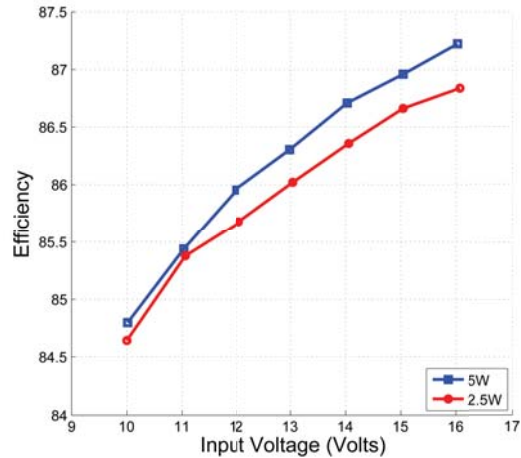

Fig. 15. Measured efficiency (not including gate drive loss) vs. input voltage for two specified output power levels. Output power is controlled by on-off modulating the converter with a PWM signal at 1 MHz.

of converter design and switch layout if an integrated power process is used.

To validate the converter topology and design procedure, an experimental implementation has been constructed. Measured waveforms from the prototype are in close agreement to simulated waveforms, and the converter achieves good efficiency over a wide input voltage range. It may be concluded that the proposed converter topology and design method yields effective converter designs at VHF frequencies.

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