Design of Resistive-Input Class E Resonant Rectifiers for Variable-Power Operation

Juan A. Santiago-González, Khurram K. Afridi and David J. Perreault

Dept. of Electrical Engineering and Computer Science

Massachusetts Institute of Technology

Cambridge, MA, USA

juansant@mit.edu, afridi@mit.edu and djperrea@mit.edu

Abstract—**Resonant rectifiers have important application in very-high-frequency power conversion systems, including dc-dc converters, wireless power transfer systems, and energy recovery circuits for radio-frequency systems. In many of these applications, it is desirable for the rectifier to appear as a resistor at its ac input port. However, for a given dc output voltage, the input impedance of a resonant rectifier varies in magnitude and phase as output power changes. A design method is introduced for realizing single-diode "shunt-loaded" resonant rectifiers, or class E rectifiers, that provide near-resistive input impedance over a wide range of output power levels. The proposed methodology is demonstrated in simulation for a 10:1 power range.**

I. INTRODUCTION

Resonant rectifiers have important application in power conversion systems operating at frequencies above 10 MHz. Applications for these circuits include very-high-frequency dc-dc converters [1-8], wireless power transfer systems [4], and energy recovery circuits for radio-frequency systems [5,6]. In many of these applications, it is desirable for the rectifier to appear as a resistive load at its ac input port. For example, in some very-high-frequency dc-dc converters, proper operation of the inverter portion of the circuit can depend upon maintaining resistive (but possibly variable) loading in the rectifier stage. In still other applications it is desired to have an input impedance that is resistive and approximately constant across operating conditions [5,6]; this can be achieved by combining a set of resonant rectifiers having variable resistive input impedances with a resistance compression network [5,7,8]. In all these systems, however, it is desirable to maintain resistive input impedance of the rectifier as the operating power varies.

The traditional design of a class E rectifier, or shunt-loaded resonant rectifier, utilizes a (large) choke inductor at its output and does not provide near-resistive input impedance [1,9]. This paper introduces a design method for realizing class E rectifiers that provide near-resistive input impedance over a wide range of output power levels.
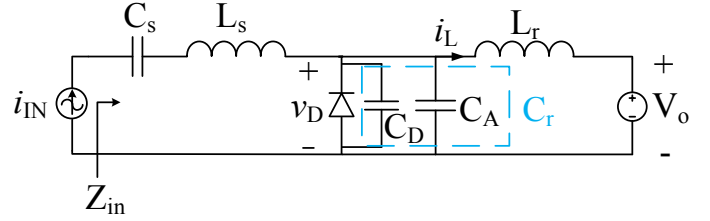

Figure 1.   Class E resonant rectifier driven by a current source.

II. CLASS E RECTIFIER OPERATION AND ANALYSIS

A class E resonant rectifier driven by a sinusoidal current source is shown in Fig. 1. Modeling the input source as a sinusoidal current source is appropriate for analysis purposes, as in most applications the source feeding the class E resonant rectifier is sinusoidal and/or the rectifier is provided with a high Q (Q > 3) series resonant tank at its input which makes the current nearly sinusoidal. In the proposed design the rectifier input series resonant tank is tuned on resonance at the desired operating frequency, with a sufficiently high loaded quality factor that the input current is substantially sinusoidal. This is similar to the design of class E inverters for variable-load operation as described in [10]. Hence, for analysis the input source will be assumed to be of the form $i_{IN} = I_{IN}\sin(\omega t + \phi)$ where I_{IN} is the amplitude of the input current, ω its angular frequency and ϕ its phase. Having a non-zero phase (ϕ) associated with the input current allows us to define the time axis in such a way that time t = 0 corresponds to the instant when the diode turns off.

The operation of the resonant rectifier is illustrated in Fig. 2, where we have assumed the diode to be ideal (excepting the diode capacitance, which is absorbed as part of the circuit operation). We are able to disregard the effect of the input-side resonant tank as the input current is sinusoidal and the input network is tuned on resonance. The diode turns off when the current through it ($i_L - i_{IN}$) reaches zero (at t = 0). At this instant the capacitor across the diode starts charging

with zero initial current. As a result the reverse voltage across the diode increases slowly with an initial dv/dt equal to zero. The diode turns on when the reverse voltage across it returns to zero at t = (1-D)T, where T = (2π/ω) is the period of the drive current and D, the duty ratio, is defined as the fraction of the period the diode stays on.

The inductor current (i_L) waveform shown in Fig. 2 differs from that of a traditional class E rectifier. In a traditionally-designed class E rectifier, a large inductor is used at the output so that the inductor current is nearly constant. However, by relaxing this design constraint to allow a substantial ac current component in i_L, we open up the possibility of designing a class E rectifier with near-resistive input impedance. As the input filter network is tuned on resonance, the input impedance of the rectifier at the drive frequency is the ratio of the fundamental component of the diode voltage $v_D(t)$ (and input voltage) to the fundamental component of the input current $i_{IN}(t)$ (which has amplitude I_{IN}). Since v_D is non-sinusoidal, its fundamental component needs to be extracted from its waveform. For this purpose, we develop an analytical expression for the waveform of v_D. The reverse diode voltage waveform across the full period is given by:

$$v_D(t) =$$
$$\begin{cases} \dfrac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\sin(\omega t)\sin(\phi) - \dfrac{Z_r}{\omega L_r}\sin(\omega_r t)\sin(\phi) + \right. \\ \left. \cos(\omega_r t)\cos(\phi) - \cos(\omega t)\cos(\phi)\right] - V_O\cos(\omega_r t) \\ -I_{IN}Z_r\sin(\omega_r t)\sin(\phi) + V_O \qquad \text{for } 0 \le t \le (1-D)T \\ \\ 0 \qquad\qquad\qquad\qquad\quad \text{for } (1-D)T \le t \le T. \end{cases}$$
(1)

Here

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$
(2)

is the resonant frequency of the L_r-C_r resonant network and

$$Z_r = \sqrt{\frac{L_r}{C_r}}$$
(3)

is the characteristic impedance of the network.

The expression for v_D contains three unknowns: duty ratio[1] D, input current amplitude I_{IN} and input current phase ϕ. The values of these unknowns need to be determined before we can compute the fundamental component of v_D. For this we need to also develop an expression for the current in inductor L_r. To calculate the current, the circuit has to be analyzed in its off and on states. The inductor current i_L when the diode is off is given by:

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[1]The duty ratio is of interest because it determines the limits of integration during fundamental frequency component extraction.

Input current i_{IN}

Diode On

Diode Off

Diode voltage v_D

Diode current i_D

Capacitor current i_C

Inductor current i_L

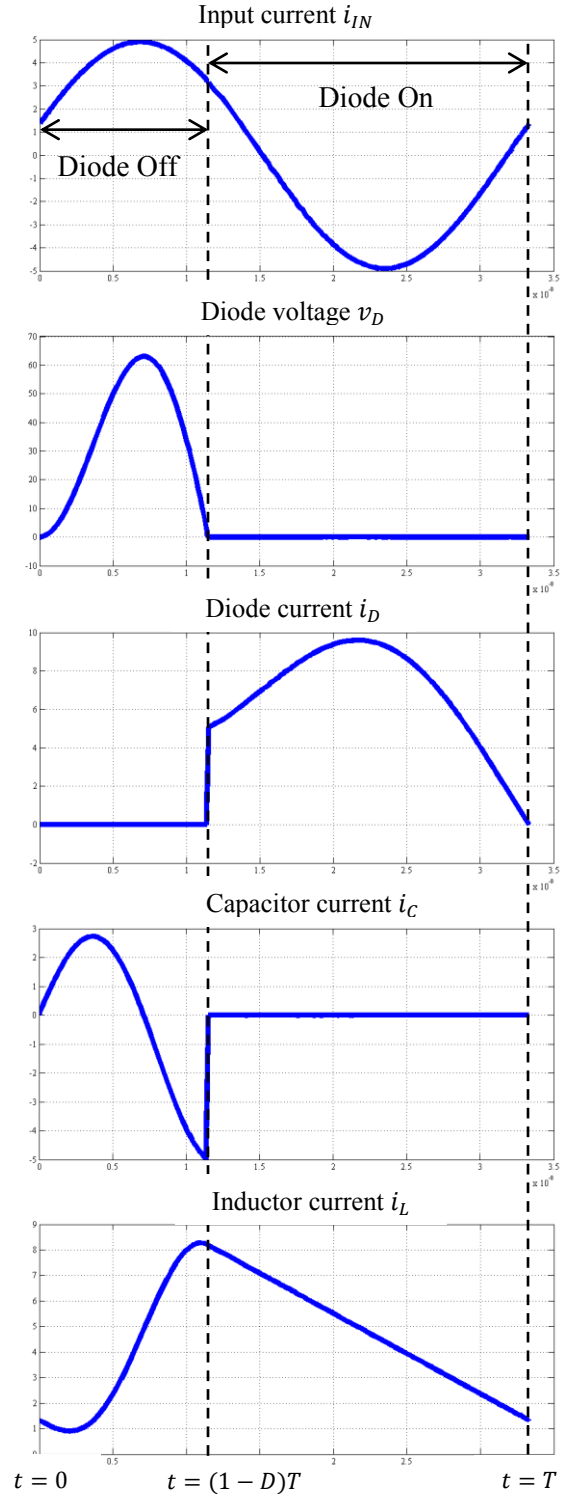$t = 0$ $\qquad\qquad t = (1-D)T \qquad\qquad t = T$

Figure 2. Class E resonant rectifier waveforms; from the top: (a) Input current, (b) diode voltage, (c) diode current, (d) capacitor current, and (e) inductor current

$$i_{L,off}(t) = \frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\cos(\omega_r t)\sin(\phi) - \cos(\omega t)\sin(\phi)\right.$$
$$\left. + \frac{\omega L_r}{Z_r}\sin(\omega_r t)\cos(\phi) - \sin(\omega t)\cos(\phi)\right] - \frac{V_O}{Z_r}\sin(\omega_r t)$$
$$+ I_{IN}\cos(\omega_r t)\sin(\phi) \quad \text{for } 0 \le t \le (1-D)T$$
(4)

and the inductor current when the diode is on is given by:

$$i_{L,on}(t) = -\frac{V_O}{L_r}\left[t - \frac{2\pi(1-D)}{\omega}\right]$$
$$+ i_{L,off}\left(t = \frac{2\pi(1-D)}{\omega}\right) \quad for \ (1-D)T \le t \le T. \quad (5)$$

In addition, the class E rectifier circuit of Fig. 1 must satisfy three constraints. The first constraint is that the diode voltage v_D has to be zero when the diode turns on. The second constraint is that the average value of v_D has to be equal to the output voltage V_o. The third constraint is that the average of inductor current i_L has to be equal to the output power P_o divided by the output voltage. In summary:

$$v_D\left(t = \frac{2\pi(1-D)}{\omega}\right) = 0, \quad (6)$$

$$\frac{1}{T}\int_0^T v_D(t)dt = V_o, \quad (7)$$

$$\frac{1}{T}\int_0^T i_L(t)\,dt = \frac{P_o}{V_o}. \quad (8)$$

By applying these constraints to (1), (4) and (5), we can derive three independent equations in terms of the three unknowns (D, I_{IN} and ϕ) and ω, P_o, V_o, L_r and C_r[2]:

$$\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\sin(2\pi(1-D))\sin(\phi) - \frac{Z_r}{\omega L_r}\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\right.$$
$$\left. \sin(\phi) + \cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\cos(\phi) - \cos(2\pi(1-D))\cos(\phi)\right]$$
$$- V_O\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right) - I_{IN}Z_r\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi)$$
$$+ V_O = 0 \quad (9)$$

$$\frac{1}{T}\left[\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\frac{-\cos(2\pi(1-D))\sin(\phi)}{\omega} + \right.\right.$$
$$\frac{Z_r}{\omega\omega_r L_r}\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + \frac{\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\cos(\phi)}{w_r}$$
$$\left. - \frac{\sin(2\pi(1-D))\cos(\phi)}{\omega}\right] - \frac{V_O}{\omega_r}\sin\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)$$
$$+ \frac{I_{IN}Z_r}{\omega_r}\cos\left(\frac{\omega_r}{\omega}2\pi(1-D)\right)\sin(\phi) + V_O\frac{2\pi(1-D)}{\omega}$$
$$\left. - \left(\frac{I_{IN}\omega L_r}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\frac{-\sin(\phi)}{\omega} + \frac{Z_r\sin(\phi)}{\omega\omega_r L_r}\right] + \frac{I_{IN}Z_r}{\omega_r}\sin(\phi)\right)\right] = V_O \quad (10)$$

$$\frac{1}{T}\left[\frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[\frac{\sin\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\sin(\phi)}{\omega_r} - \right.\right.$$
$$\frac{\sin(2\pi(1-D))\sin(\phi)}{\omega} - \frac{\omega L_r}{\omega_r Z_r}\cos\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\cos(\phi)$$
$$\left. + \frac{\cos(2\pi(1-D))\cos(\phi)}{\omega}\right] + \frac{V_O}{\omega_r Z_r}\cos\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)$$
$$+ \frac{I_{IN}}{\omega_r}\sin\left(\omega_r\frac{2\pi(1-D)}{\omega}\right)\sin(\phi)$$
$$- \left(\frac{I_{IN}}{\left(\frac{\omega}{\omega_r}\right)^2 - 1}\left[-\frac{\omega L_r}{\omega_r Z_r}\cos(\phi) + \frac{\cos(\phi)}{\omega}\right] + \frac{V_O}{\omega_r Z_r}\right)$$
$$\left. - \frac{V_O}{2L_r}\left[\frac{2\pi D}{\omega}\right]^2 + i_{L,off}\left(t = \frac{2\pi(1-D)}{\omega}\right)\left(\frac{2\pi D}{\omega}\right)\right] = \frac{P_o}{V_o} \quad (11)$$

These three equations, (9)-(11), can be solved numerically to find D, I_{IN} and ϕ for given values of ω, P_o, V_o, L_r and C_r. These equations were coded in Matlab and solved using the *fsolve* function. This numerical approach is similar to the one used in [11-13]. The magnitude and phase of the input impedance are obtained by numerically extracting the fundamental Fourier series component of v_D and comparing it to the fundamental of i_{IN}.

For a given L_r, C_r pair, the code sweeps power over a given range and calculates the maximum value of phase of the input impedance. This is repeated for a range of values of L_r and C_r to determine the variation in maximum input impedance phase with variations in values of L_r and C_r. This analysis was done for four different power range ratios (2:1, 5:1, 10:1 and 20:1).

These results were used to generate a set of normalized relationships that define the values for L_r and C_r that give the smallest deviation (in phase) from resistive operation over a specified operating power range ratio. This information is plotted in normalized form in three graphs (Figs. 3-5) that aid in the design of resonant class E rectifiers: (i) *maximum absolute value of input impedance phase vs. normalized capacitance*, (ii) *normalized peak diode reverse voltage vs. normalized capacitance*, and (iii) *normalized inductance vs. normalized capacitance*. The next section discusses the design of the rectifier using these plots.

III. CLASS E RECTIFIER DESIGN METHODOLOGY

The design of the class E rectifier begins with its frequency $f (= \omega/2\pi)$, dc output voltage V_o and output power P_o specifications. These specifications can be used in conjunction with Figs. 3-5 to identify component values that minimize the worst case input impedance phase for a given power range ratio ($P_{max}:P_{min}$).

Figure 3 shows the absolute value of the maximum input impedance phase vs. normalized capacitance, for four different power range ratios (2:1, 5:1, 10:1 and 20:1). The capacitance is normalized as follows:

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[2] Note that Z_r and ω_r used in (10)-(12) are functions of L_r and C_r.

$$C_n = C_r \frac{2\pi f V_o^2}{P_{o,max}},\qquad(12)$$

where $P_{o,max}$ is the maximum (rated) output power. The plot shows that to minimize the input impedance phase, the capacitance should be selected as a minimum within other design constraints (such as device voltage rating, etc.). The value of capacitance obtained with this methodology includes the intrinsic capacitance of the diode, any stray capacitance and any additional capacitance if needed. Hence, C_r cannot be chosen to be smaller than the intrinsic capacitance of the diode. A value of capacitance above this level should be chosen based on the acceptable value of maximum input impedance phase.

The next step is to select an appropriate diode. The required voltage rating of the diode for the selected normalized capacitance can be determined from Fig. 4. Figure 4 plots the normalized diode peak reverse voltage vs. normalized capacitance. The voltage is normalized to the dc output voltage:

$$V_{D,n} = \frac{V_{D,pk}}{V_o},\qquad(13)$$

where $V_{D,pk}$ is the diode peak reverse voltage. The normalized reverse voltage blocking capability must be greater than what is indicated by Fig. 4. The voltage stress on the diode is reduced as capacitance increases. Hence, Fig. 4 gives a minimum achievable capacitance value for a given diode peak reverse voltage rating. Once the diode is selected, one can check Fig. 3 to ensure that the maximum input phase of the rectifier is within acceptable limits. If not, one might want to change the diode for one with a higher voltage rating and/or lower capacitance.

The next step is to select an appropriate value of L_r. Figure 5 shows a plot of normalized inductance vs. normalized capacitance. The inductance is normalized as follows:

$$L_n = L_r \frac{2\pi f P_{o,max}}{V_o^2}.\qquad(14)$$

From this chart one determines the appropriate value of inductance L_r that will yield the most resistive input impedance across operating power for the selected capacitance.

Finally, the input L_s-C_s filter is chosen so that the resonant frequency is equal to f and it provides an adequate Q to achieve the desired spectral purity of the rectifier input waveforms for the application in question. We can quantify the relationship as:

$$\sqrt{\frac{L_s}{C_s}} = QR_{min},\qquad(15)$$

where L_s and C_s are the input filter inductance and capacitance, respectively, Q is the quality factor of the filter and R_{min} is the minimum value (at rated power) of the magnitude of rectifier input impedance Z_{in}. The following section has a design example using this methodology that validates the approach.
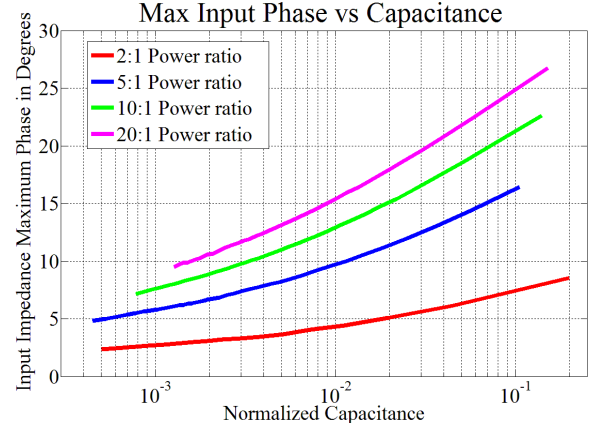

Figure 3. Worst-case phase angle magnitude across the specified operating conditions vs. normalized capacitance for different power ranges ratios (P_{max}:P_{min}).
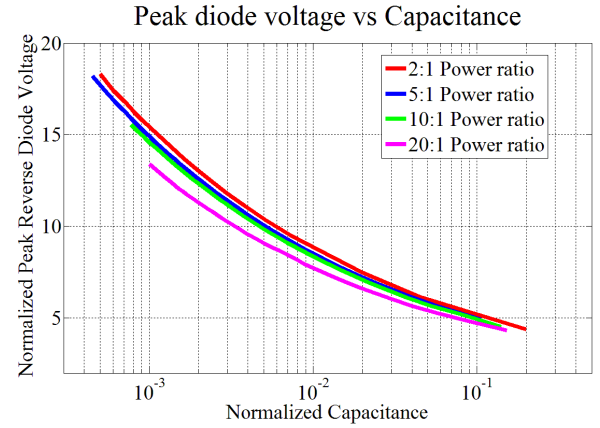

Figure 4. Maximum normalized peak reverse diode voltage vs. normalized capacitance for different power ranges (P_{max}:P_{min}).
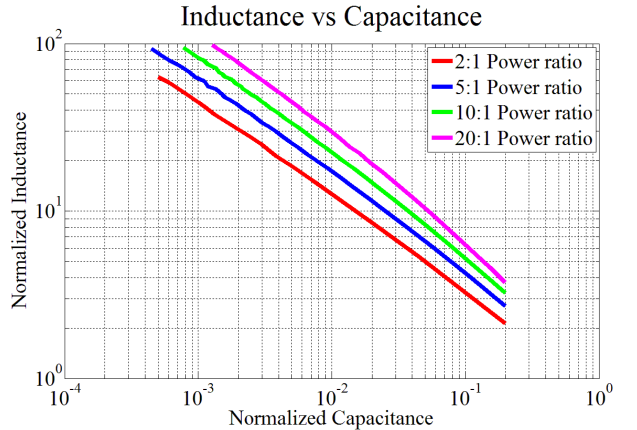

Figure 5. Normalized inductance vs. normalized capacitance for different power ranges ratios (P_{max}:P_{min}).

IV. CLASS E RECTIFIER DESIGN EXAMPLE AND SIMULATION

This section demonstrates the use of the design methodology described above in the design of a class E rectifier. The example we consider is that of a class E resonant rectifier operating at a frequency of 30 MHz with output voltage of 12 V dc and output power ranging from 18 W down to 1.8 W (i.e., a 10:1 power range ratio). We would like the input impedance of the rectifier to be as resistive as possible (i.e., minimize the worst-case phase angle of the input impedance) over the entire power range, while using a 60 V diode with nominal capacitance of 50 pF (based on the PMEG6030EP diode which has average current rating of 3A). Thus, the normalized peak diode voltage capability is about 4 (assuming we allow only up to around 48 V peak with appropriate margin). From Fig. 4, the corresponding normalized capacitance C_n is 0.2. From Fig. 3 the expected maximum absolute value of input impedance phase angle is about 25 degrees. From Fig. 5 the normalized inductance is 3.5. De-normalizing the L and C values, the inductance L_r comes out to be 149 nH and the capacitance C_r comes out to be 132.6 pF. The value of C_r is greater than the 50 pF intrinsic capacitance of the diode. The input LC filter was designed with a Q of 3 and R_{min} of 19 Ω, leading to a C_s of 93 pF and L_s of 302 nH. Table 1 summarizes the design and parameters for the rectifier to be simulated.

Figures 6-8 show the SPICE simulation of our designed class E rectifier. Figure 6 shows the peak diode voltage to be around 51 volts, which is well within the diode specifications and well matching the predicted peak voltage of 48 V for C_n = 0.2 in this design. Figure 7 shows the input current to the rectifier, which shows low harmonic content at full power. Figure 8 shows the inductor current with an average of 1.5 amps and substantial ac current.

Figure 9 shows the phase and magnitude of the input impedance of the rectifier. The impedance magnitude is inversely proportional to output power. The impedance is capacitive at high power and becomes inductive at low power. The maximum input impedance phase amplitude found by time-domain simulations across the specified operating power range is very close to the 22 degrees predicted by the design graph.

The simulated results show that our design procedure works accurately, at least for idealized diode characteristics.
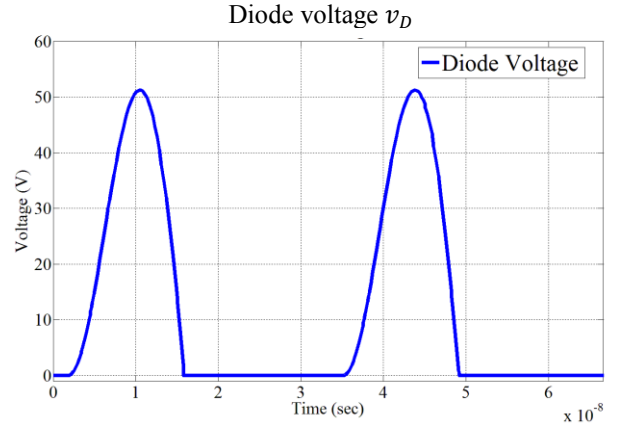

Figure 6. SPICE simulation results. Time-domain simulation of the diode voltage at the full power of 18 W.
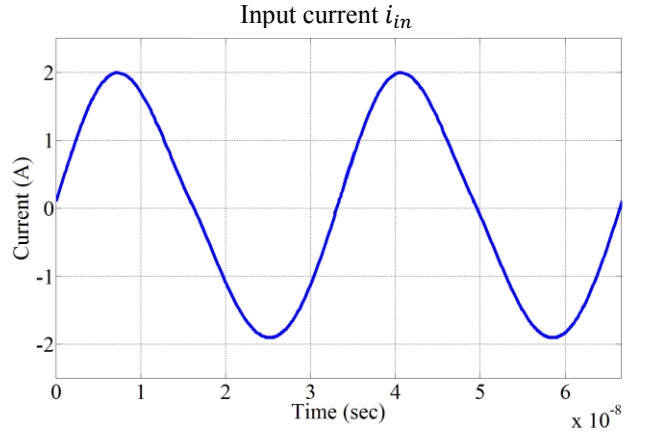

Figure 7. SPICE simulation results. Time-domain simulation of input current at the full power of 18 W.
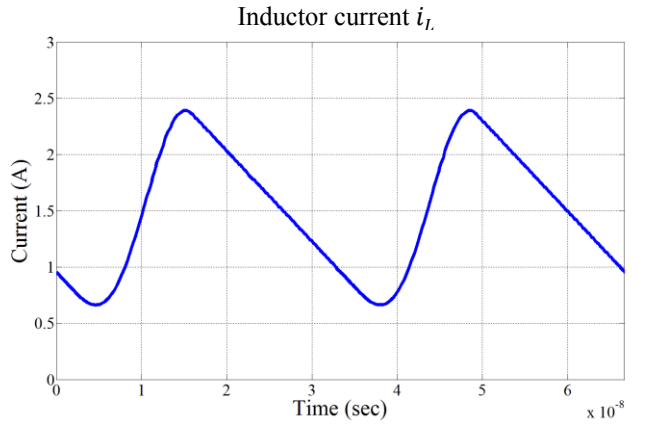

Figure 8. SPICE simulation results. Time-domain simulation of inductor current at the full power of 18 W.

TABLE I.   CLASS E RECTIFIER PARAMETER VALUES USED IN THE SIMULATION

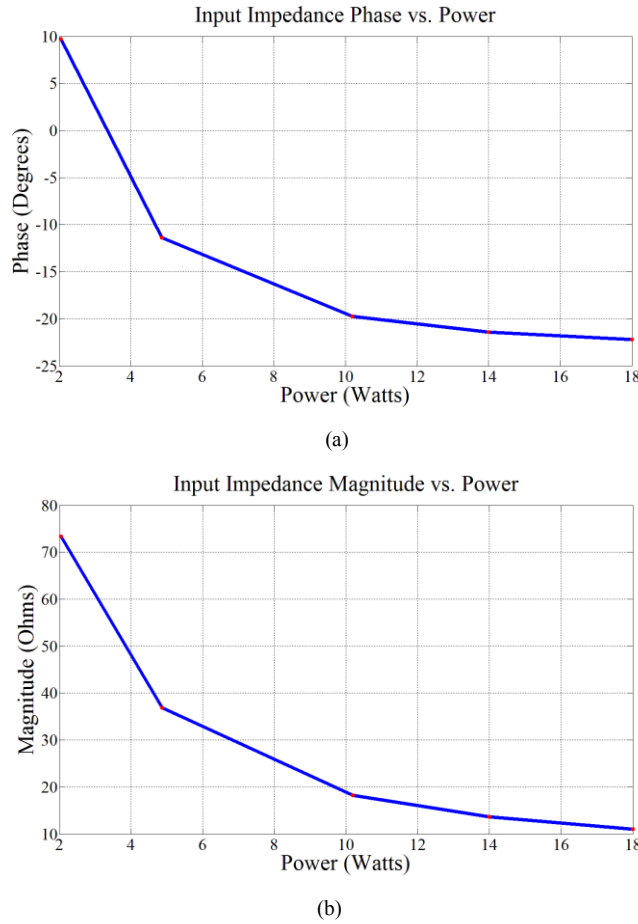| Parameter	Value
P_o	18-1.8 W
V_o	12 V
f	30 MHz
L_s	302 nH
C_s	93 pF
L_r	149 nH
C_r	132.9 pF
C_D	50 pF
C_A	82.9 pF

(a)

(b)

Figure 9. Resonant rectifier's input impedance as a function of output power: (a) phase angle and (b) magnitude.

V. CONCLUSION

A methodology for designing resonant rectifiers with near resistive input impedance has been presented in this paper. We develop analytical expressions to model the rectifier, and provide a graphical approach for the design. The design method is validated in simulation. It is hoped that this design approach and the insights available from the design curves will prove to be useful in designing resonant rectifiers in applications that require resistive rectifier loads.

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