A Single-Phase Photovoltaic Inverter Topology with a Series-Connected Power Buffer

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***Abstract*— Module integrated converters (MICs) have been under rapid developement for single-phase grid-tied photovoltaic applications. The capacitive energy storage implementation for the double-line-frequency power variation represents a differentiating factor among existing designs. This paper introduces a new topology that places the energy storage block in a series-connected path with the line interface block. This design provides independent control over the capacitor voltage, soft-switching for all semiconductor devices, and full four-quadrant operation with the grid. The proposed approach is analyzed and experimentally demonstrated.**

I. Introduction

Grid-tied inverters for photovoltaic systems represent a rapidly developing area. Microinverters, also known as module-integrated converters (MICs), are designed to interface a single, low-voltage (25–50 v, typically) panel to the AC grid [1]–[5]. Such converters provide a number of benefits: ease of installation, system redundancy, and increased energy capture in partially shaded conditions [6].

Module integrated converters typically target single-phase electrical systems [7] (e.g. at 240 V). Therefore, the converter must deliver average power plus a sinusoidally varying power component at twice the line frequency, while drawing a constant power from the PV module. Fig. 1 illustrates the power transfer versus time for the grid and the PV module, with the shaded area between the curves indicating the temporal energy storage required for the inverter. To model this transfer of energy through the converter, a generalized three port system can be used. The constant power source of the PV and the sinusoidal power load of the grid are illustrated in Fig. 2, and can be written as

$$P_{\mathrm{PV}} = P_{avg}, \tag{1}$$

$$P_{\mathrm{Line}} = -P_{avg}(1 - cos(2\omega_l t)). \tag{2}$$

The energy storage buffer must absorb and deliver the difference in power between these two ports, specifically

$$P_{\mathrm{Buf}} = -P_{avg}\cos(2\omega_l t). \tag{3}$$

Inverters investigated in the past (see literature reviews [4], [5]) can be classified by the location and operation of the energy storage buffer within the converter. Most single-stage topologies, such as flyback and ac-link converters, place capacitance in parallel with the PV panel [8]. This is an effective low-complexity implementation, but in order to avoid interfering with the peak-power tracking efficiency, substantial

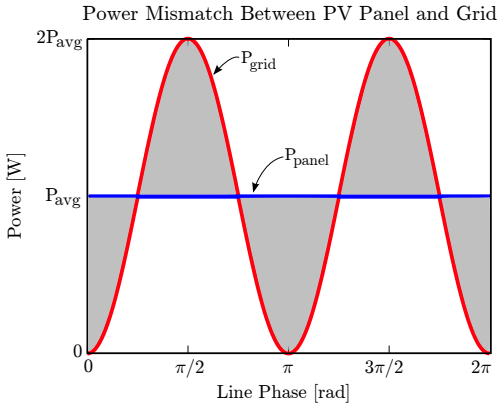

Fig. 1: The power flow mismatch between the grid and a constant power source results in the shaded area, representing the required energy storage.

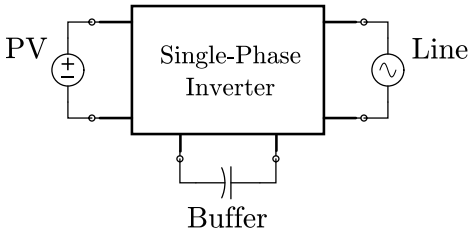

Fig. 2: A generalized grid-connected power converter, visualized as a three-port system.

energy storage is required to keep the voltage ripple extremely low across the panel. A common second method involves two cascaded conversion stages, providing energy storage at an intermediate dc bus. This arrangement can be implemented with less energy storage than the previous method, as a much larger voltage fluctuation on the intermediate bus can be tolerated.

One drawback common to both of the energy storage methods described involves the near exclusive use of electrolytic capacitors for the dc energy storage. They are traditionally selected due to their high energy density, but suffer from the stigma of long-term failure rates. Recent developments have investigated "third-port" topologies (e.g. [9], [10]), which can control the voltage on the energy storage capacitor independent of the input and output voltages. This permits the use of much lower total energy storage, along with the possibility of using more reliable but less energy dense capacitors. The

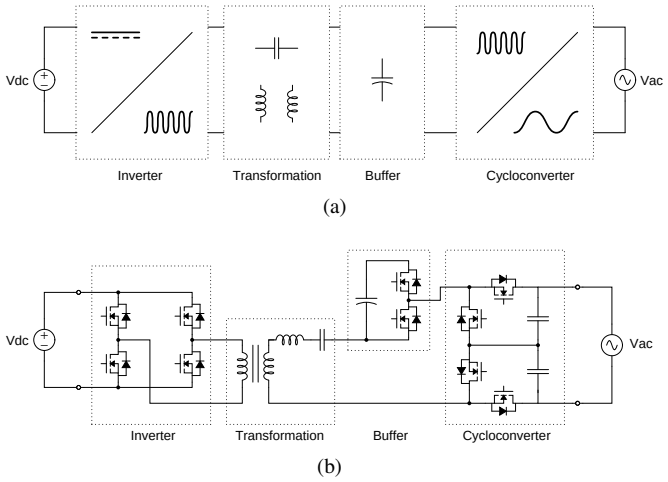

Fig. 3: The (a) block diagram and (b) schematic of proposed photovoltaic module-integrated converter.

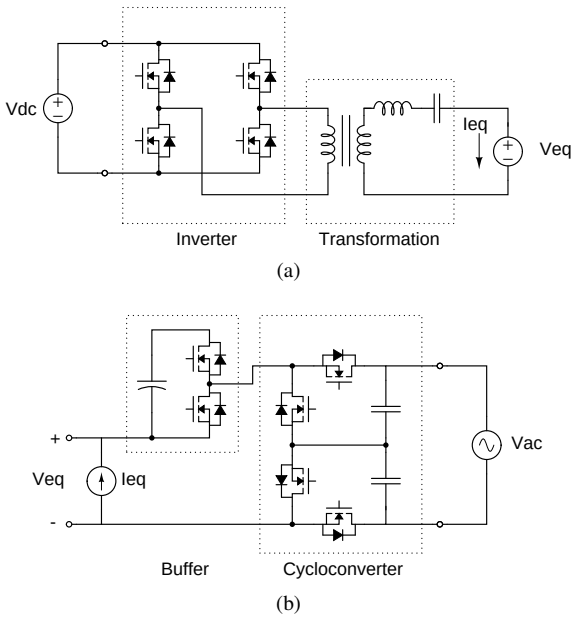

Fig. 4: Equivalent circuits representing the (a) primary and (b) secondary sides, decoupled by approximating the transformation stage as a current source.

topology presented in this paper implements a type of third-port storage, placing the energy storage (buffer) block "in series" with the line voltage interface. This topology reduces the effective voltage transformation ratio that is required, provides zero-voltage soft-switching (ZVS) for all devices, scales with improvements in semiconductor technology, allows independent control over energy storage voltage, and enables full four-quadrant operation.

II. Proposed Solution

Considering the circuit in Fig. 3, the placement of all three blocks in a series path — linked by a high-frequency resonant current — seems, at first glance, to impose a conduction loss penalty. However, the proposed approach provides means to mitigate this loss, in addition to presenting opportunities not found in previous designs. Using unipolar devices such as MOSFETs for the primary switches allows the semiconductor area to be scaled to reduce conduction loss; devices such as IGBTs, SCRs, and diodes allow current flow in a single direction and impose a fixed on-state voltage drop, which is not scalable. The switching losses associated with large MOSFET devices can be greatly reduced through soft-switching techniques and device improvements [11]. Additionally, the resistive channel structure allows current to flow both directions through the device, allowing for bidirectional power flow in each block of the converter.

MOSFET device figure-of-merit values have improved steadily since their introduction, and the recent use of charge-compensation principles has allowed high-voltage silicon MOSFETs to surpass the "silicon limit" [12]–[14] and become viable for voltage ranges once relegated to IGBT devices alone. Additionally, the emergence of wide-bandgap based devices, implemented in SiC and GaN, have the potential to dramatically reduce the on-state resistance of devices even further while reducing undesirable parasitics [15], [16]. This historical semiconductor device progress, combined with these and other anticipated future improvements, are a motivating factor in the elimination of p-n junction devices with this topology development. Our work shows that this approach provides high efficiency with presently-available devices, and may be anticipated to improve as device technology evolves.

III. Topology Operation and Analysis

In the general form, operation of this converter requires control over the output waveforms of each block relative to others. The combined voltage pattern imposed across the transformation stage is responsible for generating the resonant current that links the three blocks of the converter. In turn, the switching pattern of each block relative to this resonant current is what determines the average power delivery for that block. Unfortunately, this results in a highly-coupled non-linear relationship between the output voltage waveform of each block and their respective power deliveries.

Given these complications, an initial analysis is performed with the following simplifying approximations: (1) The quality factor of the series resonant circuit is sufficiently high to approximate it as a sinusoidal current source operating at the switching frequency, and (2) The voltage at each terminal of the converter (PV, buffer, and line) changes slowly enough, relative to the switching frequency, that they can be approximated as constant over a switching cycle. The first approximation is referred to as the sinusoidal approximation, and allows the converter to be analyzed using phasors and equivalent impedances when appropriate. The second approximation allows the voltages on the panel, line, and buffer capacitor to be modeled as dc voltage sources, with values set by operating conditions at a particular point in a line cycle. Using these approximations, the converter can be divided into the two subcircuits shown in Fig. 4.

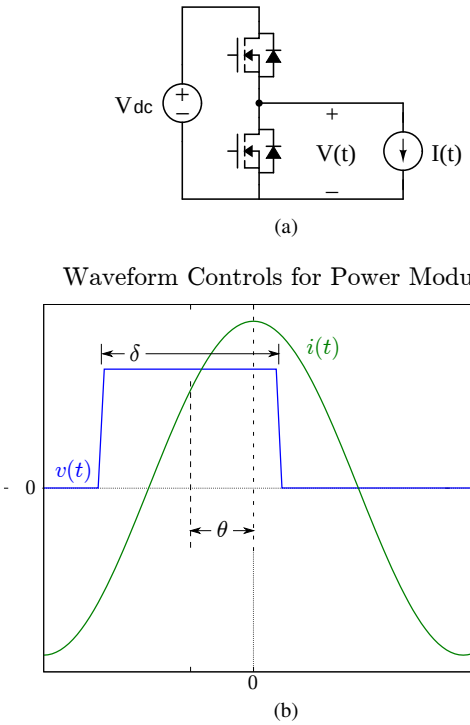

Fig. 5: The relationship between the series-path current and switching function determines the transfer of energy through the converter.

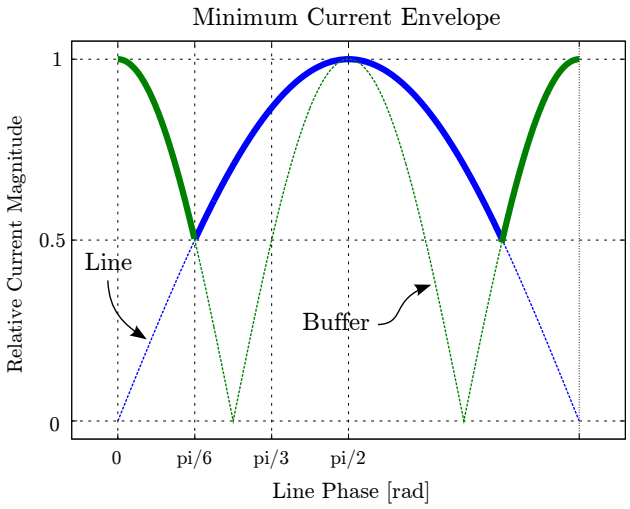

Fig. 6: This illustrates the minimum resonant current magnitude requirements for the buffer-block and line-connected cycloconverter, including the emboldened line indicating the envelope of current to meet both constraints.

A. Power Modulation

The modulation of power through the buffer and cycloconverter blocks in the converter is accomplished by controlling the switching function of that block relative to the series resonant current. The switch control is most easily illustrated by Fig. 5 where a half-bridge is fed by a sinusoidal current source. The on time of the high side switch directs the current though the dc voltage source, while the low side switch acts effectively a bypass. The average power delivered over a switching cycle can the be expressed as a function of the pulse width, δ, and the phase shift, θ, by

$$\begin{aligned}\langle P\rangle &= \frac{1}{T}\int_0^T i(t)v(t)\mathrm{d}t \\ &= \frac{VI}{\pi}\cos(\theta)\sin(\delta/2),\end{aligned} \tag{4}$$

where δ and θ are expressed in radians and shown in Fig. 4b.

To address the continuum of parameter combinations, two specific switch modulation cases are considered: phase-shift, and PWM. The basis for the phase-shift modulation is to maintain a fixed pulse width, δ, and shift the phase of the half-bridge switching function, θ, relative to the resonant current. Alternatively, in the PWM method, the pulse width, δ, is controlled such that the high side switch remains on for the duration required to obtain the required energy transfer. In both cases, the turn-on and turn-off transitions for all devices can be selected such that they occur under zero-voltage conditions.

The primary side full-bridge inverter is controlled by phase-shifting the two halves of the bridge relative to each other with each operating at a fixed 0.5 duty cycle. The phase shift is what controls the pulse width seen at the output. The average power transfer over a switching cycle can be found, using the same method in (4), to be

$$\langle P\rangle = 2\frac{VI}{\pi}\cos(\theta)\sin(\delta/4), \tag{5}$$

where δ denotes the pulse width, expressed in radians, and the phase θ denotes the difference in phase between the output voltage waveform and the series resonant current.

For a given power transfer constraint in either the buffer-block or cycloconverter, (4) can be used to determine the minimum magnitude of current required to satisfy it. The constraints in (2) and (3) vary over the line cycle, and when both requirements are combined, a minimum current magnitude can be found. An example of the constraints over a line cycle can be seen in Fig. 6, which plots both blocks' minimum current magnitude, and the resulting envelope. A less complex alternative to tracking the minimum current is to select a constant resonant current magnitude to maintain over a line cycle, where its value is large enough to satisfy the worst case requirement (e.g. a value of one for the example in Fig. 6).

An evaluation of the differences between the two resonant current magnitude options can be seen by considering Fig. 7, where the buffer-block and cycloconverter combination are approximated as load impedance (i.e. using the fundamental components in a describing function approach). This load impedance has a direct effect on the design constraints of the the full-bridge inverter and transformation network that are used to drive it. If the equivalent circuit impedance of the constant- and minimum-current profiles are evaluated, Fig. 8 present their variation over a line cycle.

With a chosen current drive mode, consideration must be given to the ability of this current to be generated with realistic converter control parameters. Closer analysis of the converter

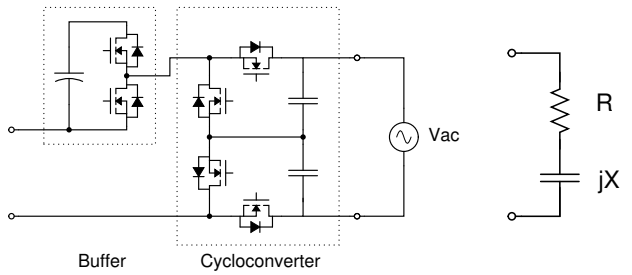

Fig. 7: The buffer-block and cycloconverter in (a) can be approximated as the complex load impedance in (b).

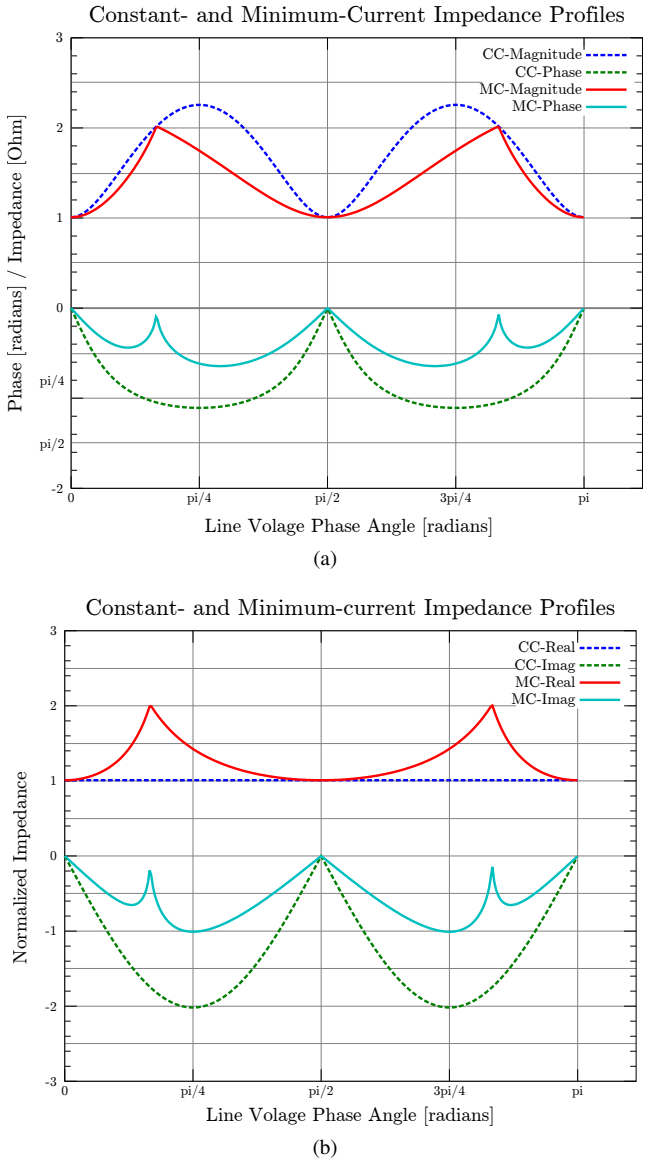

Fig. 8: The complex impedance of the buffer-block and cycloconverter are shown to vary over a line cycle based on the constant- or minimum-current drive method. Both the (a) magnitude/phase and (b) real/reactive relationships are presented.

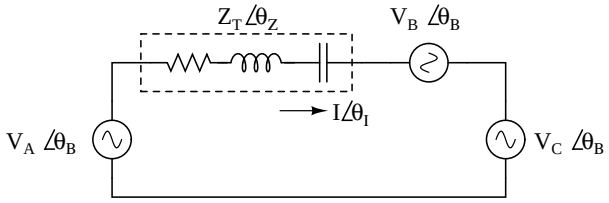

Fig. 9: The converter shown in Fig. 3, approximated using sinusoidal sources for each block.

operation shows that the resonant tank impedance, transformer turns ratio, and applied terminal voltages each influence the converter's power transfer capability.

Of particular interest is the

B. Modeling Converter Operation

If the sinusoidal approximation of the current is expanded to include the synthesized voltages of each block, the converter operation can be investigated with simple phasor analysis. In this case, the transformation stage is lumped into a single series reactive element $z_T = R + jX_T$, where the reactive impedance is implicitly dependent on the switching frequency. Fig. 9 illustrates the new equivalent circuit, where each block has been replaced by its phasor equivalent.

If the resonant current is defined in terms of the circuit voltages and tank impedance, then

$$\bar{I} = \frac{1}{Z_T e^{j\theta_Z}} \left(V_A e^{j\theta_A} + V_B e^{j\theta_B} + V_C e^{j\theta_C} \right), \qquad (6)$$

and the power through series-connected source k is

$$\begin{aligned} P_k &= \frac{1}{2} Re\left\{ \bar{V}_k \bar{I}^* \right\} \\ &= \frac{1}{2} Re\left\{ V_k e^{j\theta_k} \frac{\left(V_A e^{-j\theta_A} + V_B e^{-j\theta_B} + V_C e^{-j\theta_C} \right)}{\left(Z e^{-j\theta_Z} \right)} \right\}. \end{aligned} \qquad (7)$$

In this formulation, it is clear that the voltage of each block influences both the magnitude and phase of the current, resulting in a coupled non-linear system of equations for power modulation. The power transfer for a single block, as defined by (7), requires seven parameters: the operating frequency, and the magnitude and phase for the three voltage sources. This set can be reduced by applying the external terminal voltages, power transfer requirements, and the selection of control constraints. Implementing phase-shift power modulation for the buffer and cycloconverter, in combination with the known terminal voltages, results in known voltage magnitudes for V_B and V_C. By choosing to define θ_A as the phase reference, it can be removed as an unknown. The remaining number of unknowns has been reduced to four: the switching frequency ω_{sw}, phase shifts θ_B and θ_C, and full-bridge voltage V_A.

The power transfer requirements for the three ports of the converter, given in (1)–(3), only contain two independent constraints; this leaves need for an additional two. The phase-shift angles θ_B and θ_C have mathematically enforced bounds, whereas the bounds on switching frequency ω_{sw} and full-bridge pulse-width δ_A (for control of V_A) are loosely defined

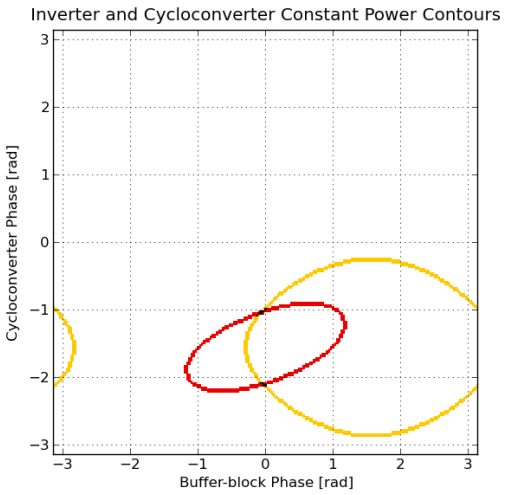

Fig. 10: Contour plots for the valid solution sets of two power transfer constraints over the (θ_B, θ_C) phase space. The intersection of the two contours yields a set of solutions that meet both of these requirements.

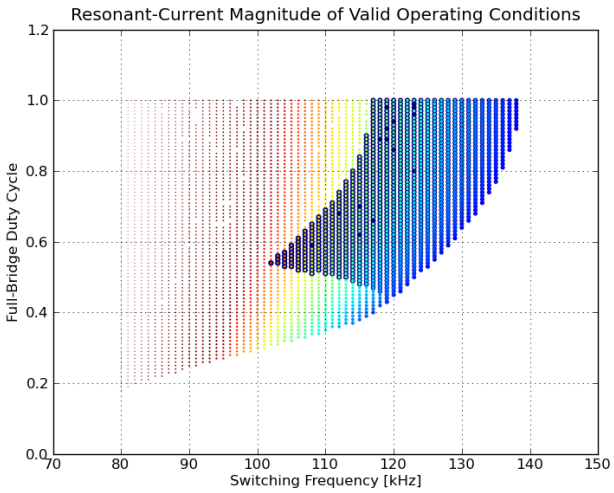

Fig. 11: A map of valid solutions for varying combinations of switching frequency and full-bridge inverter duty-ratio. The larger blue points indicate low resonant current magnitude, with smaller red dots indicating larger currents.

by the physical operation of the converter. Given this, the frequency and and full-bridge pulse width are selected to be free variables.

One method to understand the solution(s) for the unknown angles is to consider each power transfer constraint from (7) separately. To calculate a valid set of solutions for each, a simple brute-force map of the phase-space (θ_B, θ_C) is performed to determine the resulting power transfer at each phase pair; the contour corresponding to the constraints of desired power transfer among the three ports provides the valid set. The intersection of these sets provides solutions to meet both sets of constraints. To visualize the valid-set intersections, Fig. 10 presents two contours in the phase-space that corresponds to P_{PV} and P_{Line} valid sets. In this example, the intersection results in two solutions.

With a procedure in place for finding the unknown phase angles, it is repeated for additional combinations of the free variables, ω_{sw} and δ_A, until a solution map emerges. An example solution map is shown in Fig. 11, which has been limited to include only solutions that provide zero-voltage switching transitions for all devices; the large blue dots indicate the lowest resonant current magnitude relative to the small red points which are the largest. A number of the points contain two valid solutions, each with a different (θ_B, θ_C) pair, and different resonant currents. The solution map presented is valid for the single operating condition defined by the applied terminal voltages and power transfer constraints, and therefore the process must be repeated for each operating condition of interest.

C. Parameter Selection

Reducing the possible solution space generated in the previous section is important to limit the complexity of real-time operation. For a given solution map of ω_{sw} and δ_A combinations, an objective function can be used to find an optimal parameter pair for that given operating condition.

By selecting a single element from each solution map, the dimensionality of the solution space is greatly reduced, and the relationship of operating conditions and corresponding operating parameters can be investigated in a tractable manner.

TABLE I: Prototype converter target requirements.

Parameter	Value	
Input Voltage	25–40	$\mathrm{V_{DC}}$
Output Voltage	240 $\pm$ 10%	$\mathrm{V_{AC}}$
Input Power	0–200	W
Line Frequency	50–60	Hz

IV. Proof-of-Concept Implementation

To illustrate the performance and functionality of the series connected buffer-block topology described in this paper, the prototype platform shown in Fig. 12 has been designed and built for input from a single 72-cell photovoltaic module, and output to a single-phase 240 V residential service. The operating requirements for the inverter are outlined in Table I.

A. Converter Design

The converter's primary power-stage topology follows directly the circuit shown in Fig. 3, with the addition of the required gate-drive, isolation, and digital communication hardware. For all three blocks' gate drive power and digital signals are independently isolated, then connected externally a to common voltage source and FPGA development board. The power stage specifications, including the resonant tank and magnetics, are included in Table II.

The design of the transformer is one key element that benefits from the presence and operation of the buffer-block;

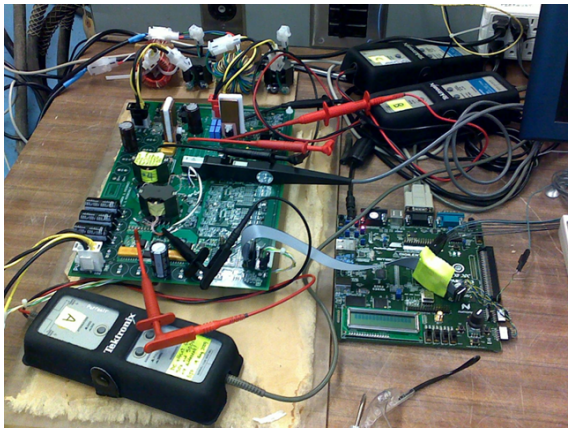

Fig. 12: Photograph of the proof-of-concept implementation for the series buffer-block topology, including measurement probes and digital control board.

TABLE II: Operating range and Component listing for proof-of-concept converter implementation. The resonant component values are listed as the values measured in-circuit.

Component	Description
Switching Frequency	100–400 kHz
Buffer-block Voltage	170 V_{DC}
Resonant Inductor	158.2 μH[1]
Resonant Capacitance	24.5 nF
Transformer	1:6[2]
Full-bridge MOSFETs	STMicro STB160N75F3 75 V, 3.5 mΩ
Cycloconverter and Buffer-block MOSFETs	Infineon IPP60R250CP 650 V, 250 mΩ

[1] 36 turns, 270 strand 44 AWG litz; RM14-3F3 core, 3.25 mm center-post gap.
[2] Primary: 5 turns, 300 strand 40 AWG litz; Secondary: 30 turns, 100 strand 40 AWG litz; RM14-3F3 core, ungapped.

the turns ratio and secondary side volt-seconds are both reduced. In a directly comparable topology [8], implemented without the use of the series buffer, a turns ratio of 1:7.5 (of an ideal minimum 1:6.8) was used, while the implementation here uses a 1:6.0 ratio, with a lower limit below 1:5.3, depending on the switching modulation and current drive method selected.

The resonant inductor value and transformer turns ratio were selected such that the full-bridge was presented with a low enough impedance to meet the highest power transfer requirement at the lowest input voltage, while also providing enough inductive energy to provide ZVS transitions at low loads. The resonant inductance of the circuit includes both the discrete inductor and the leakage inductance of the transformer, totaling 170.3 μH. The resonant capacitance was selected such that its impedance was less than half of the impedance of inductance at the minimum frequency range (100 kHz). This placed the series resonant frequency at 78 kHz.

The large operating frequency range specified in Table II describes the bounds for which valid solutions exist for the specification ranges given in Table I, and not the range where typical operation would occur. The following results were run between 110–170 kHz

In determining the control parameters for the converter demonstration, the direct search method outlined in Section III-C was implemented for a set of predetermined conditions. An objective function was selected to minimize the magnitude of the series-resonant current, while providing adequate margin for zero-voltage commutation time.

Each set of operating condition constraints describe a static dc operating point that would be seen over the course of a line cycle. Operation at dc requires the buffer-block to continually sink or source power for the converter. This is remedied with an additional power supply having a parallel ballast resistor.

B. Experimental Results

Three waveform captures are used to illustrate the operation of the converter at different points in the line cycle. In this setup, a constant power of 150 W from an input source of 32 V is drawn by the converter for each demonstrated operation.

Starting at the zero crossing of the line, a line phase of zero degrees, Fig. 13a shows the buffer-block absorbing power. The switching waveform is nearly in-phase with the negative portion of the resonant current. The second point occurs at a line phase of 30 degrees (170 V), where the buffer-block and cycloconverter are each absorbing 75 W from the source. This can be seen in Fig.13b, where the voltage waveforms are switching complimentary to each other. In the final line phase of 90 degrees (340 V) shown in Fig. 13c, the buffer and source are each providing 150 W to the cycloconverter, which is providing 300 W out.

Using the same input conditions as the scope captures, the power transfer between ports was experimentally measured over a one-quarter line-cycle set of points. The power transfer relationships can be found in Fig 14, which clearly shows the constant power to the input port, the bidirectional energy transfer through the buffer-bock, and the sinusoidal power delivery to the line.

The efficiency of the power conversion was also investigated for the same 150 W average power, but two additional input voltages were investigated: 25, and 40 V. These results are show in Fig. 15, where the power-stage efficiency is above 90% for all points, and peaks at 98%. The power supplied to the gate drives was not included in these measurements.

V. Conclusions

The converter design and implementation presented in this paper has outlined a new topology with an energy-storage buffer in the series-connected path with the line interface. The benefits of this design have been enumerated, and the bench prototype operation presented with verification of the functionality and performance.

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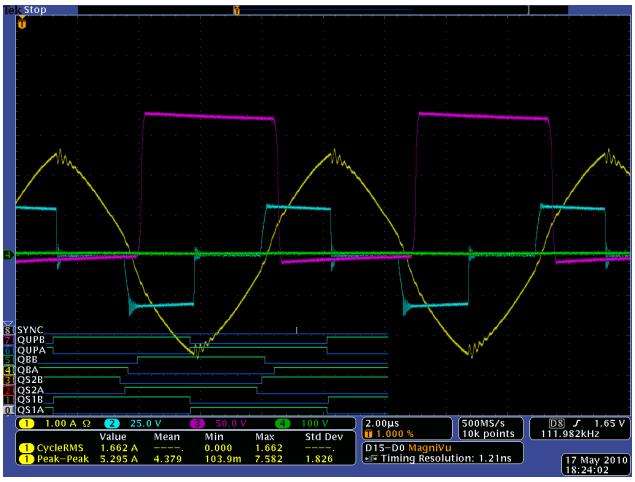
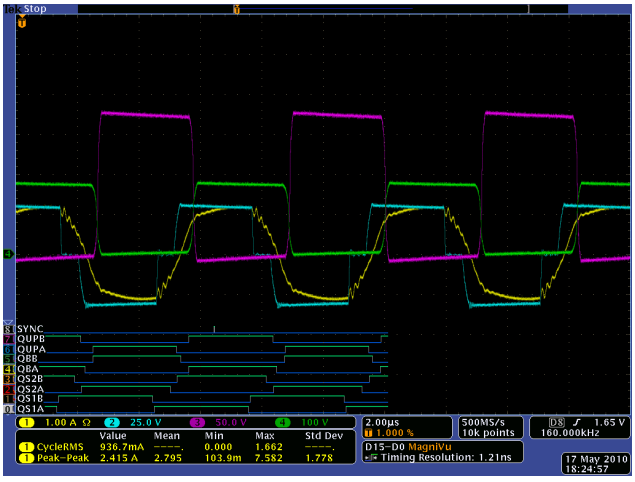


(a)



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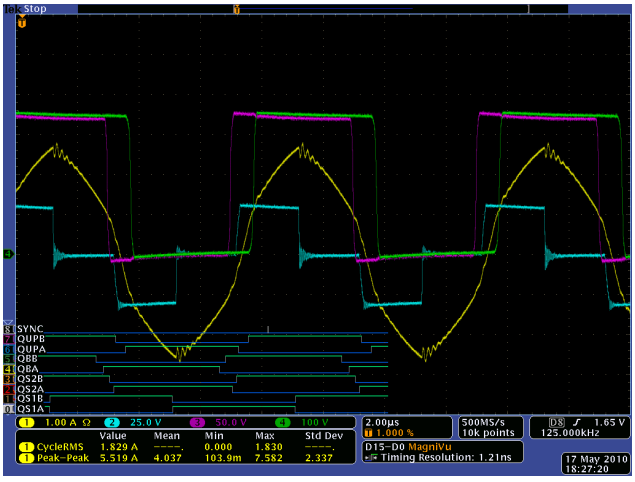

(c)

Fig. 13: Converter operation at a line phase of (a) zero degrees: 0 V, (b) 30 degrees: 170 V, and (c) 90 degrees: 340 V. Waveform color key; yellow: current, cyan: full-bridge, magenta: buffer-block, green: cycloconverter.

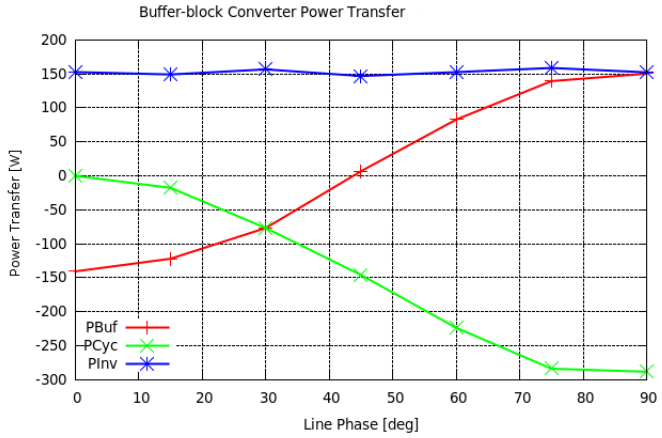

Fig. 14: Experimentally obtained power transfer measurements for each of the three converter blocks. The operation of the buffer-block's bidirectional energy transfer clearly illustrated.

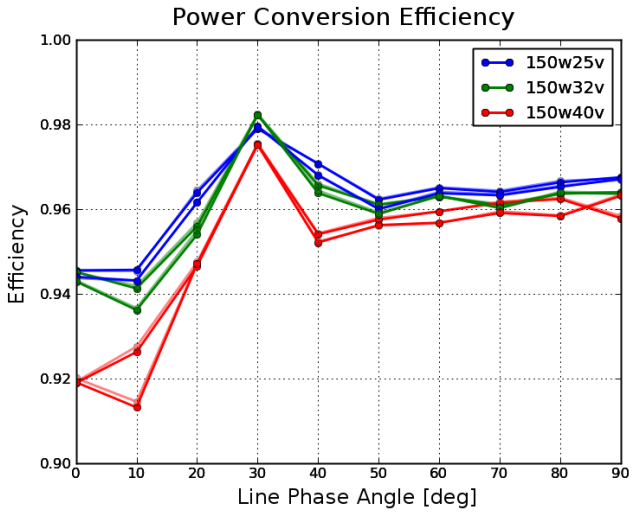

Fig. 15: Experimentally obtained power-stage conversion efficiency for the prototype converter, at an input power of 150 W, operated over a quarter line-cycle. Two data sets are drawn for each of three input voltages: an initial cold-start efficiency measurement, and a thermal steady-state measurement.

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