Power Conversion Architecture for Grid Interface at High Switching Frequency

Seungbum Lim, David M. Otten, and David J. Perreault
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139-4307
Email: sblim@mit.edu

Abstract—This paper presents a new power conversion architecture for single-phase grid interface. The proposed architecture is suitable for realizing miniaturized ac-dc converters operating at high frequencies (HF, above 3 MHz) and high power factor, without the need for electrolytic capacitors. It comprises of a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter (or set of power combining converters). The regulating converters have inputs connected to capacitors on the capacitor stack, and provide regulated outputs while also achieving high power factor, with twice-line-frequency energy buffered on the capacitor stack. The power combining converter combines power from the individual regulated outputs to a single output, and may also provide isolation. While this architecture can be utilized with a variety of circuit topologies, it is especially suited for systems operating at HF (above 3 MHz), and we introduce circuit implementations that enable efficient operation in this range. The proposed approach is demonstrated for an LED driver operating from 120 V_{ac}, and supplying a 35 V, 30 W output. The prototype converter operates at a (variable) switching frequency of 5–10 MHz and an efficiency of $> 93\%$. The converter achieves a displacement power density of 130 W/in^3, while providing a 0.89 power factor, without the use of electrolytic capacitors.

I. INTRODUCTION

For an ac-dc converter, high power factor is desirable to best convey real power from the ac grid to a dc load [1]. One common method to achieve high power factor is to cascade a "Power Factor Correction (PFC)" circuit and a dc-dc converter, where the PFC circuit shapes sinusoidal input current and buffers twice-line-frequency ac energy to a capacitor with a certain (usually high) dc voltage. The following dc-dc converter then regulates the load voltage from the voltage of energy buffer capacitor.

The boost converter is often selected for PFC circuit because of its filtered input current, high efficiency, and high power factor capability [1], [2]. However, in the case of low dc voltage load applications, the subsequent dc-dc converter needs a large step-down voltage conversion ratio; this imposes large voltage stress on the second stage and makes it difficult to design the second stage to operate at high frequency and high efficiency (especially for low output powers).

Instead of a boost converter, one alternative for the PFC circuit is a buck converter, which draws a clipped-sinusoidal current waveform with 0.9−0.95 power factor [3]–[5]. In the low load voltage applications, the benefit of the buck PFC is the reduced voltage stress and the voltage conversion ratio for the following dc-dc converter. However, the active components in the buck PFC circuit still need to be operated directly from the ac line voltage, and thus the buck PFC should be designed with high voltage active devices. This high voltage requirement for grid interface also results in large parasitic capacitance, low achievable switching frequencies, and large passive components, and consequently in low power density.

Here we propose a new grid-interface power conversion architecture that addresses these problems. It can achieve reasonably high power factor (e.g., about 0.9, which is sufficient for many applications such as LED driver circuits), while dynamically buffering twice-line frequency energy using small capacitors operating at moderate voltages and voltage swings. The proposed converter thus shares the benefits of some "third port" architectures for buffering line frequency energy (e.g., [6]–[12]), in that it can achieve high energy storage density without the need for electrolytic capacitors. Moreover, it enables high switching frequencies to be achieved (above 3 MHz) with relatively low voltage components, yielding high efficiency and high power density. Section II of the paper describes the structure and operation of the proposed grid interface architecture, and illustrates its characteristics with simulations. Section III of the paper presents a circuit implementation that leverages the advantages of the proposed architecture to operate efficiently at 5–10 MHz, and presents experimental results demonstrating the proposed system. Finally, Section IV concludes the paper.

II. SYSTEM ARCHITECTURE AND CHARACTERISTICS

The proposed architecture is illustrated in Fig. 1. It comprises a line-frequency rectifier, a stack of capacitors across the rectifier output, a set of regulating converters having inputs connected to capacitors on the capacitor stack and outputs that are regulated to a desired level, and a power-combining converter (or set of power combining converters) that combines the power from the outputs of the regulating converters to provide a single output.

The line-frequency rectifier draws current from the grid during a portion of the cycle, with a waveform controlled by the operation of the regulating converters. The capacitor stack provides most or all of the twice-line-frequency energy buffering, such that the converter can provide high power factor without buffering energy at the system output. One or
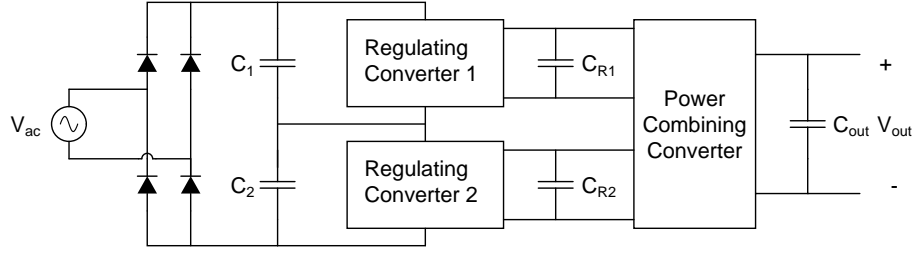
Fig. 1. The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter.
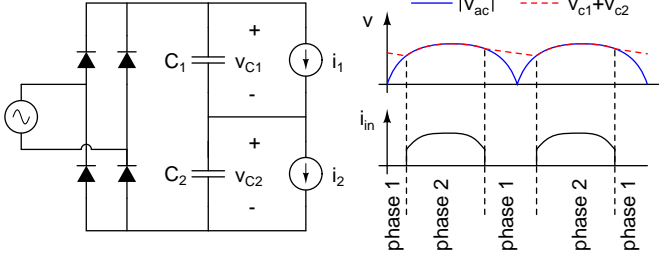

Fig. 2. The simplified front-end circuit model of the proposed architecture with example voltage and current waveforms. The currents i_1 and i_2 models the average current (averaged over a switching cycle of the regulating converters) drawn by regulating converter 1 and regulating converter 2, respectively. The regulating converters modulate their current draw over the line cycle and result in an input current waveform with high power factor.

more of the capacitors in the capacitor stack is relatively small, such that the total capacitor stack voltage can vary over a wide range as the line voltage varies over the line cycle. The input ac current waveform may approximate a clipped sine waveform or a similar waveform providing high power factor, while the total capacitor stack voltage closely follows the amplitude of the line voltage over the portion of the line cycle for which the rectifier conducts.

A set of regulating converters, which have their inputs connected to capacitors of the stack of capacitors, provide regulated outputs. The currents drawn by the (at least) two regulating converters are modulated to draw energy from the capacitors, such that the currents drawn from the capacitor stack results in an input current waveform to the rectifier that provide both high power factor and the total needed energy transfer to support the output. Because the regulating converters operate from voltages that are much smaller than the total line voltage, they can be designed to switch at much higher frequencies and can be operated at smaller character-istic impedance levels than could a single converter rated at line voltage (e.g., as described in [13] [14]). Many converter topologies can be considered as a regulating converter of the proposed architecture. For example, as described later, the regulating converters may be very effectively implemented using resonant-transition discontinuous-mode inverted buck converters [14]. This topology enables high-frequency op-eration of the regulating converters (3–30 MHz) with high efficiency, low device voltage stress, small component size, and good control capability.

The power-combining converter has a plurality of inputs connected to the regulating converter outputs, wherein the power-combining converter draws energy from the regulat-ing converter outputs and delivers the combined power to the converter system output. The power-combining converter may provide one or more of: voltage balancing among the regulating converter outputs, isolation, voltage transformation, a portion of twice-line-frequency energy buffering, and addi-tional regulation of the output. The power-combining converter may be designed as a multi-input converter, or as a set of single-input converters which take inputs connected to ones of the regulating converter outputs and supply a single output. Because the power combining converter operates from a low, narrow-range input voltage, and needn't (in many designs) provide regulation, it can be designed to be very compact. One possibility in this case is to design it for operation at HF or VHF [15]. Another possibility (when isolation is not required) is to design it using switched-capacitor techniques, as demonstrated here.

A. Line-Frequency Energy Buffering

Before introducing an example implementation with a spe-cific regulating and power combining circuit topology, we show how the stacked converter structure (i.e., stack of capac-itors and regulating converters) can be used to buffer twice-line-frequency energy and provide high power factor.

Fig. 2 shows a simplified model of the front end of the proposed grid interface architecture along with example oper-ating waveforms. The two current sources (i_1 and i_2) model the currents drawn by the regulating converters. The circuit cycles in two phases across a half line cycle. During phase 1, the input ac voltage amplitude is lower than the total voltage of the stacked capacitors; the full-bridge rectifier is off and there is no current drawn from the grid. During this phase, capacitors C_1 and C_2 are discharged by the regulating converters and the voltage across the capacitor stack decreases. When the input ac voltage amplitude reaches the total capacitor stack voltage, the full-bridge turns on and the circuit enters phase 2.

During phase 2, the total voltage of stack capacitors tracks the rectified ac input voltage, and the input current follows the sum of the currents into C_1 and regulating converter 1 (as well as tracking the sum of the currents into C_2 and regulating converter 2). When the regulating converters no longer discharge the capacitor stack voltage fast enough to

- phase 1 – full-bridge is off and conducts zero input current

$$i_{ac}(t) = 0 \tag{1}$$

$$P_o(t) = v_{c1}(t) \, i_1(t) + v_{c2}(t) \, i_2(t) \tag{2}$$

- phase 2 – full-bridge is on and conducts $i_{ac}(t)$ input current

$$v_{ac}(t) = V sin\omega t = v_{c1}(t) + v_{c2}(t) \tag{5}$$

$$i_{ac}(t) = i_{c1}(t) + i_1(t) = i_{c2}(t) + i_2(t) \tag{6}$$

$$P_o(t) = v_{c1}(t) \, i_1(t) + v_{c2}(t) \, i_2(t) \tag{7}$$

$$i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} = -i_1(t) \tag{3}$$

$$i_{c2}(t) = C_2 \frac{dv_{c2}(t)}{dt} = -i_2(t) \tag{4}$$

$$i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} \tag{8}$$

$$i_{c2}(t) = C_2 \frac{dv_{c2}(t)}{dt} \tag{9}$$

$$i_1(t) = \frac{C_1 \, C_2 \, v_{c2}(t)}{C_2 \, v_{c2}(t) - C_1 \, v_{c1}(t)} \left\{ \left(\frac{1}{C_1} + \frac{1}{C_2} \right) i_{in}(t) - \omega V cos \, \omega t - \frac{P_o(t)}{C_2 \, v_{c2}(t)} \right\} \tag{10}$$

$$i_2(t) = \frac{1}{v_{c2}(t)} \, (P_o(t) - v_{c1}(t) \, i_1(t)) \tag{11}$$

follow the decrease in line voltage, the full-bridge turns off and the circuit enters phase 1.

Assuming that the regulating converters draw currents (averaged over a switching cycle of the regulating converters) $i_1(t)$ and $i_2(t)$, and that the power combining converter combines power (from the two regulating converters) without loss and continuously supplies the required output power $P_o(t)$, the mathematical expressions for each phase are as shown in equations (1)–(11).

It should be noted that during phase 2 equations (10) and (11) are calculated from equations (5)–(8), and the $i_1(t)$ and $i_2(t)$ currents result in the pre-defined input current of the system over the line cycle providing good power factor. There are many relations among the stack capacitor values, power level, capacitor voltage variation, regulating converter operating range, and power factor. Thus, selecting appropriate topologies, design values and operating waveforms is essential.

A key design consideration is selection of the capacitor values C_1 and C_2. The capacitors are typically sized asymmetrically (one large, one small), such that one can both buffer the twice-line-frequency energy with reasonable voltage swing and provide a desired line-current pattern for high power factor.

Another key consideration in controlling the converter is to follow the desired input current waveform (and capacitor stack voltage pattern) over a line cycle. These patterns may be pre-computed as a function of desired output power P_o and/or output voltage, and applied to both maintain the desired output and input waveforms across operating condition. Waveform selection is accomplished by iteratively selecting waveform shapes and numerically calculating performance over a half line cycle using (1)–(11), with the requirement that the system both operate in periodic steady state over this interval and remain within the operating constraints of the regulating converters.

B. Circuit Simulation

To demonstrate the operation of the proposed architecture and illustrate how it achieves high power factor and buffers ac energy, we present time-domain simulations of the system front-end using the model of Fig. 2.

We illustrate how the currents of each regulating converter are calculated and how the capacitor stack voltage varies for a particular set of design parameters. We consider an ac-dc converter operating from 60 Hz, 120 V_{ac} and supplying 30 W of output power; this example matches the experimental system described in the following section. The stack capacitors are picked as $C_1 = 1\mu F$ and $C_2 = 50\mu F$. In addition, each regulating converter is assumed to be able to operate across a 35–100 V input voltage range and to be able to deliver power unidirectionally from its input to the power combining circuit (with the power combining converter assumed to combine powers from the regulating converters without loss).

For the proposed design and operating point, the initial voltages on capacitors C_1 and C_2 (at the line zero crossing) are 35 V and 70 V, respectively. Figs. 3–8 show the simulation results for this case. Fig. 3 shows the input current waveform programmed to be drawn from the ac line for this design at the specified 30 W output operating condition. From numerous iterative simulations, a folded-clipped-sinusoidal input current waveform is selected as a good operating waveform providing high power factor (about 0.9) and satisfying the system design constraints (That is, the input current waveform is selected as zero for part of the cycle, as a sinusoidal signal for part of the cycle, and as a constant minus the sinusoidal signal during part of the waveform.)

With the specified input current waveform and design parameters, the average currents of each regulating converter and stack capacitor voltages are calculated from equations (1)-(11) and plotted as shown in Figs. 4 and 5. As can be seen in Fig. 4, the current drawn by each regulating converter is always positive. Moreover, as shown in Fig. 5, the voltages of the two "stack" capacitors vary over the line cycle as
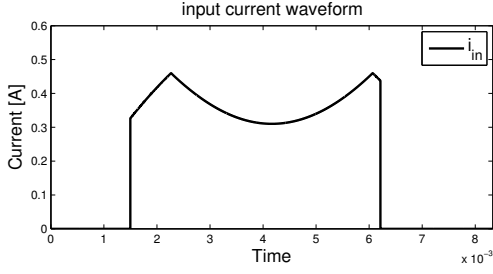
Fig. 3. This figure shows the simulated example input current waveform over a half line cycle. The example is for a system drawing 30 W from 120 Vrms, 60 Hz ac, and employing stack capacitors of $C_1 = 1$ μF and $C_2 = 50$ μF, respectively. Based on iterative numerical simulations to determine the desired operating waveforms, a folded-clipped sinusoidal current waveform is selected, which is nonzero only when the full-bridge rectifier is turned on.
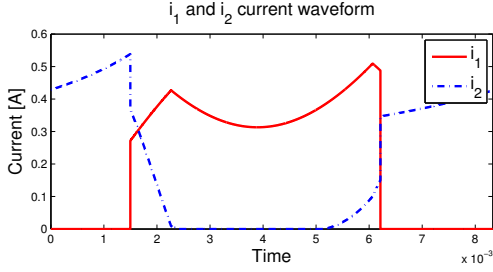

Fig. 4. The currents i_1 and i_2 (average currents drawn by the regulating converters) are numerically calculated over a half line cycle, for a design and operating point of $C_1 = 1$ μF, $C_2 = 50$ μF, $P_o = 30$ W, and line current of Fig. 3.
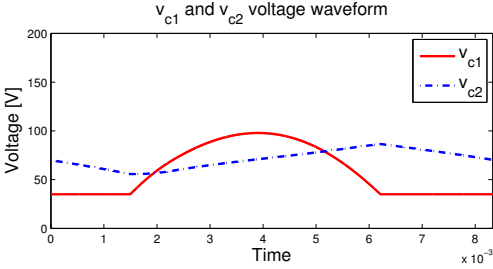

Fig. 5. The capacitor voltages v_{c1} and v_{c2} are numerically calculated over a half line cycle, for the case of $C_1 = 1$ μF, $C_2 = 50$ μF, and $P_o = 30$ W with the input current of Fig. 3 and regulating converter input currents of Fig. 4. In this simulation, $v_{c1,i} = 35$ V, $v_{c2,i} = 70$ V.

Fig. 6. Input sinusoidal voltage v_{in} and capacitor stack voltage $v_{c1} + v_{c2}$ plotted over a half line cycle for the example of Figs. 3-5. The line frequency rectifier turns on when the ac line voltage reaches the capacitor stack voltage, and turns off when ac line voltage falls below the capacitor stack voltage.

Fig. 7. Input power P_{in} (drawn from the line) and output power P_{out} (total of power delivered by the regulating converters) plotted over a half line cycle for the example of Figs. 3-6. In this example simulation, the stack of capacitors can dynamically buffer the twice-line-frequency energy through modulation of the current drawn by the regulating converters such that the net output power is approximately constant over the line cycle.

Fig. 8. The power drawn by regulating converters 1 and 2 plotted over a half line cycle for the example of Figs. 3-7. The power combining converter combines the powers from regulating converters to supply a single load. Each of the regulating converters is rated for the (line-cycle-average) output power of the system.

they are dynamically charged and discharged by the regulating converters, remaining within the specified operating range. The input voltage of the regulating converters varies over 35–100 V (operating range of the regulating converter), and the system operates in periodic steady state over the line cycle (i.e., the capacitor voltages are the same at the beginning and end of the half line cycle.)

Fig. 6 shows the line voltage and total capacitor stack voltage over a half line cycle. When the full bridge rectifier conducts, the capacitor stack voltage tracks the line voltage. Once the line voltage falls below the total capacitor stack voltage, the rectifier ceases to conduct, as illustrated in Fig. 2 and described in section II-A. From Figs. 5 and 6 it can be seen that the asymmetric sizing of the stack capacitors enables the
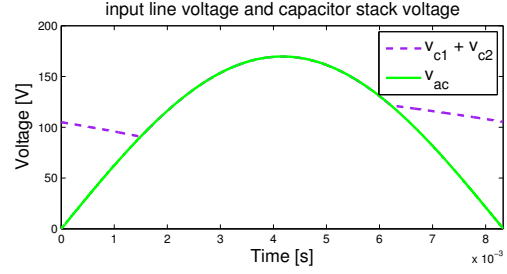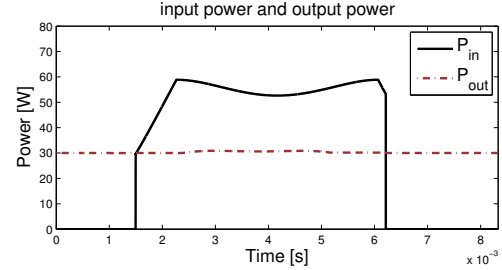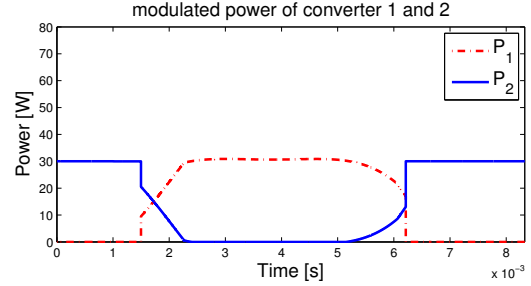
stack voltage to track the line voltage (and draw line current) over a large portion of the line cycle, while also buffering the twice-line-frequency energy.

The input power P_{in} is drawn from the line and the output power (total of the powers drawn from the capacitor stack by the regulating converters) are shown in Fig. 7. The proposed architecture controls the regulating converters to buffer the twice-line-frequency energy on the stack capacitors such that the total output power from the two regulating converters is almost constant. As illustrated in Fig. 8, the two regulating converters split the total power over the line cycle, and each regulating converter is rated for the total (line-cycle-average) output power of the system.

As illustrated in the above example, the front-end of the proposed architecture accomplishes three functions: First, it draws power from the line at high power factor. Second, it buffers twice-line-frequency energy from the line on the capacitor stack, such that constant power can be delivered to the system output. Lastly, while it is not explicitly shown above, the front end steps down the large input voltage, and provides narrow-range regulated outputs for the power combining stage.

C. Design Tradeoffs

There are several trade-offs among the design parameters to be considered in realizing a design. The first is the relation between capacitor stack size and the operating voltage of regulating converters. Usually as one uses smaller stack capacitors (C_1 and C_2), the capacitor voltages vary across wider voltage ranges over the line cycle to buffer the twice-line-frequency energy. The regulating converters then needs to be operated over this wider voltage range, which can degrade the size and performance of the regulating converters. Another design consideration is between power factor and the operating voltage range of the regulating converters. As the regulating converter are operated across wider voltage ranges, the proposed ac-dc architecture can conduct current for a longer conduction time over the line cycle, providing higher power factor. However, again, the burden on the regulating converters increases. Lastly, bi-directional converter capability could improve the achievable power factor of the system and required buffer capacitance size, but makes the design of the regulating converters much more challenging.

It should be noted that in some cases (or for some power levels), high power factor and twice-line-frequency energy buffering cannot be met simultaneously with a given set of capacitor vlaues. In such cases, the power combining converter may then needs to buffer some portion of twice-line-frequency energy to supply constant power to the load. Overall, the trade-offs are mainly restricted by the topology of the regulating converter.

D. System Characteristics

The proposed grid interface architecture we adopt has several advantages. One apparent benefit is the decreased voltage stress to the components in the regulating converters and the power combining converter relative to the line voltage. In comparison to common grid interface converter which must be rated for the grid voltage, each regulating converter of the proposed architecture instead operates up to about half of the grid voltage because of the stacked capacitor structure (with an increased number of "stack" capacitors and regulating converters, this voltage stress may be further reduced as illustrated in Fig. 9.) Moreover, the power combining converter, tied to the regulated outputs of the regulating converters, operates at both low voltage and narrow input voltage range. Large step down conversions are also more readily achieved, aided by the stacked nature of the front end conversion system and -
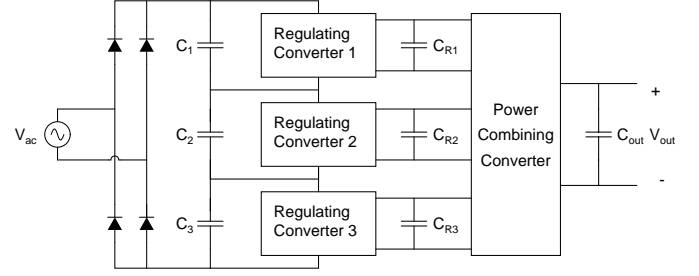

Fig. 9. The proposed architecture can be extended with more than two capacitors in the capacitor stack and correspondingly other system blocks for the universal ac line interface. Moreover, the number of capacitors and sub-regulating converter may be allowed to vary dynamically depending upon whether the circuit is connected to 120 or 240 V_{ac}.

in some cases - supplemented by further step down from the power combining converter.

It should be noted that with certain power combining topologies (e.g. the SC charge balance circuit as shown in Fig. 10 and described hereinafter), one of the two regulating converters can directly supply the system output, and the combining converter only need process a portion of the power. This can be regarded as reducing the redundant processing power in the converter, and contributes to improved efficiency [16].

Converters operating at high voltages and low currents operate at high impedance levels, and consequently utilize relatively large inductors and small capacitors (e.g., characteristic impedance $Z_0 = \sqrt{L/C}$ scales as V/I). Furthermore, inductor and capacitor values scale down with increasing resonant frequency (e.g., $f = 1/\sqrt{LC}$). Thus, for a given topology, increasing frequency beyond a certain point may lead to capacitance values that are too small to be practically achievable (e.g., given parasitics), placing a practical bound on frequency and miniaturization. For miniaturization of converters at high voltage and low power, it is preferable to select system architectures and circuit topologies that require relatively low characteristic impedance values (i.e., small inductances and large capacitances) to reduce constraints on scaling up in frequency. The proposed architecture roughly divides the input voltage range of each regulating converter by two, by stacking two regulating converters, and thus decreases the required inductance and increases the allowable capacitance. Higher switching frequencies (bounded by practically achievable capacitance levels) are thus enabled by this approach. This consideration is further associated with converter topology selection, as described in Section III.

The difference between instantaneous input power from the line and output power (twice-line-frequency energy) should be buffered inside of the converter so that it needn't be buffered at the system output. This twice-line-frequency energy ($E_b = P_o$ / ω_{line}) is not related to the switching frequency of the converter, but to the power level and the ac line frequency. By utilizing a relatively large voltage swing on the storage capacitors C_1 and/or C_2, small-valued capacitors can be employed (i.e., $\frac{1}{2} C(V+\Delta V)^2 - \frac{1}{2} CV^2$ = buffered energy). This
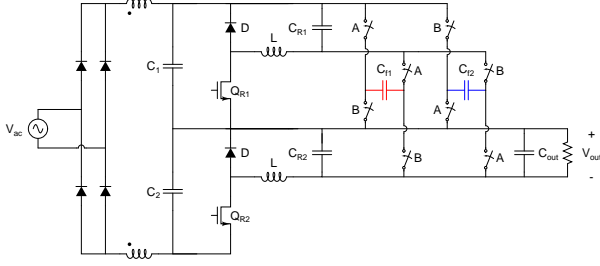
Fig. 10. This figure shows the implementation of the proposed grid interface architecture. The regulating converters are designed as resonant-transition inverted buck converters operating at high frequency (3–30 MHz). The power combining converter is a switched-capacitor converter operating at moderate frequency (about 30 kHz). An implementation of this system is illustrated in Fig. 12.

TABLE I
COMPONENTS OF THE PROPOSED ARCHITECTURE

Stack of Capacitors	
C_1	1 μF X7R Ceramic 100 V
C_2	225 μF X7S Ceramic 100 V
Regulating Converter	
Q_{R1}, Q_{R2}	GaN switch EPC 2012
D	Schottky diode STPS30120DJF
L	800 nH 10 turns on a Micrometal P68-106
Power Combining Converter	
switch	GaN switch EPC 2012
C_{f1}, C_{f2}	20 μF X7R Ceramic 100 V
Control	
Microcontroller	Atmel ATtiny 1634

enables film or ceramic capacitors to be employed instead of electrolytic capacitors, which can benefit lifetime, temperature rating, and reliability of the system.

The proposed architecture can be extended with many variations and many options of converter topologies. For example, as shown in Fig. 9, the architecture may provide an interface to universal ac grid voltage with an increased number of capacitors and subsystem blocks. Moreover, the number of capacitors and regulating converters that are used at a given time may be allowed to vary dynamically (e.g., depending upon whether the circuit is connected to 120 or 240 V_{rms}.) This enables greater flexibility of operation, and narrower component operating ranges than could otherwise be achieved.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Topololgy Selection

The proposed architecture enables substantial miniaturization through adoption of greatly increased switching frequencies for the regulating converters. To attain greater miniaturization, increases in switching frequency are necessary because the values of inductors and capacitors vary inversely with switching frequency. However, the sizes of passive components do not necessarily decrease monotonically with frequency, owing to magnetic-core loss, voltage breakdown, and heat transfer limits. In addition to loss considerations,

the practical values of required components can also limit switching frequency (i.e., yielding impractical values compared to inherent parasitics as frequency is increased). This is a particular challenges in converter operating at high voltage and low current. Consequently, achieving substantial miniaturization through high frequency operation further relies upon appropriate passives design and careful selection of circuit topology to minimize the demands placed upon the passive components, especially the magnetic components.

To address the considerations and achieve high efficiency and high power density, the regulating converters are designed as inverted resonant buck converter and the power combining converter is designed as a switched capacitor circuit as shown in Fig. 10. The regulating converter is designed with single switch, diode, and small inductor, and operates at HF (3–30 MHz) similar to the regulation-stage design illustrated in [13], [14]. It is an "inverted" circuit in the sense that it is designed with "common positives." Besides control methods, for much of its operating range, the topology acts like a quasi-square-wave ZVS buck converter with a low ratio of switching to resonant frequency [17]. Each regulating converter takes as an input one of the capacitor voltages (from the stack of capacitors) and provides a regulated voltage across its output capacitor. This regulating converter design has several benefits. First, it operates with ZVS or near-ZVS soft switching across the 35–100 V wide input voltage range. The single common-referenced switch (referenced to a slowly-moving potential) makes it suitable for operation at HF (3–30 MHz). Second, it requires only a single, small-valued inductor. Furthermore, it has very fast response (near single cycle) to input voltage transients and changes in the output current command. Finally, for a given input voltage, the output current is roughly proportional to transistor on-time, allowing a variety of control schemes to be employed.

We selected an interleaved switched-capacitor (SC) circuit for the power combining converter. This is an effective choice for high efficiency and power density, as the converter needn't provide regulation [18]. The SC circuit draws energy from the two regulating converter outputs and supplies the single system output (which is also the output of one of the regulating converters). Because the switched capacitor circuit transfers charge without voltage regulation, and is designed with switches and capacitors, it can be operated high efficiency at low frequency with small converter size. In the proposed SC circuit, the capacitors C_{f1} and C_{f2} transfer charge from capacitor C_{R1} to capacitor C_{R2} and supply the combined power to the load. Since in this prototype the load is connected across the output of one of the regulating converter, the SC circuit only processes a portion of overall system energy. Moreover, if C_{f1} and C_{f2} are selected as much larger than C_{R1} and C_{R2}, partial "soft charging" of the energy transfer capacitors can be achieved [19].

B. Implementation

To test the proposed architecture, we implemented an example system based on the topology describe above. The system
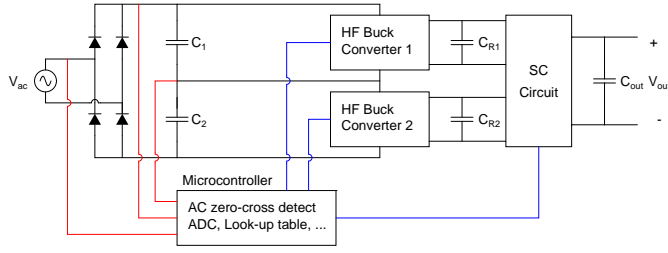
Fig. 11. Block diagram showing the converter and control system. The microcontroller detects the zero crossing event of ac line voltage and resets the time state. The microcontroller monitors the capacitor stack voltage (the input voltage of each regulating converter) via a voltage divider and ADC, and sends updated switch-turn-on duration information to each regulating converter every $\sim$80 μs. The turn-on durations used over the line cycle are predetermined for the desired output power and input voltage and stored in a lookup table. In addition, the microcontroller generates the 30 kHz 50 % duty ratio switching signals (with dead time) for the SC circuit.
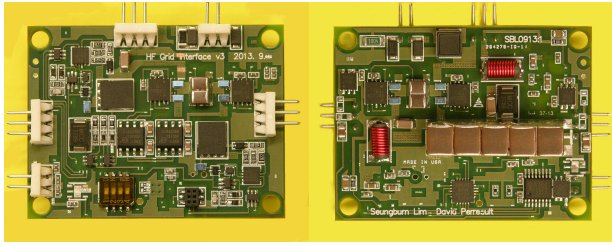

Fig. 12. The prototype converter, implemented in a 1.9 in x 1.4 in printed board. This figure shows the front side and the back side of the PCB.

is designed to supply 30 W to a 35 V dc output from a 120 V_{rms} AC 60 Hz input. We utilize the control strategy described and demonstrated in simulation in Section II. The system comprises a line-frequency bridge rectifier and a small filter choke; a stack of two capacitors; a pair of regulating resonant-transition inverted buck converters; and an unregulated SC power-combining converter having two inputs and an output supplying the system output.

As shown in section II, the proposed architecture can buffer the ac energy with C_1 = 1μF C_2 = 50 μF at 30 W power level. In selecting practical capacitors, it must be recognized that the capacitance of high-k ceramic capacitors degrades with bias voltage. Consequently, we used 1 μF, 100 V X7R capacitance for C_1 and a (norminal) 225 μF, 100 V X7S ceramic capacitance for C_2 in this prototype.

Table 1 shows the component selection of the inverted resonant-transition buck converters used in the prototype. With these values the regulating converters operate in the range of 5–10 MHz under soft-switching conditions over their input voltage and power range. The SC circuit is designed with 20 μF, 100 V X7R energy transfer capacitors and GaN switches as presented in Table I, and operates at a fixed switching frequency of 30 kHz.

As illustrated in section II, the proposed ac-dc architecture dynamically buffers twice-line-frequency energy and draws a pre-defined ac current with high power factor by modulating two regulating converters over the line cycle. We used a microcontroller to control the average current of each regu-
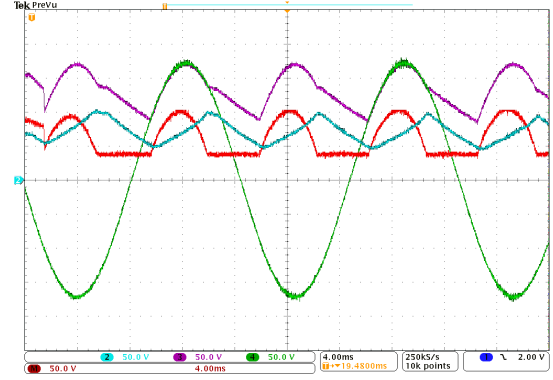

Fig. 13. The implemented converter is connected to 120 V_{rms} ac line voltage with at 35 V output at 30 W power. The ac line voltage is realized with a Agilent 6812B ac power supply., and the figure shows the measured voltage waveform across the ac line cycle (x: 4 ms/div). Ch2 (blue, y: 50 V/div) is the voltage across the capacitor C_2, ch3 (purple, y: 50 V/div) is the total stack capacitor voltage after the full-bridge, ch4 (green, y: 50 V/div) is the 120 V_{rms} ac line voltage, and ch M (red, y: 50 V/div) shows the voltage across the capacitor C_1. The capacitors C_1 and C_2 satisfy periodic-steady-state operation over the line cycle, and dynamically buffer twice-line-frequency energy.

lating converter and synchronize operation over the line cycle (Atmel, ATtiny 1634); Fig. 11 describes the control scheme. The microcontroller detects the zero-voltage crossing of the ac line voltage and resets the time state. The microcontroller monitors the capacitor stack voltage (the input voltage of each regulating converter) and sends updated pre-defined switch-turn-on duration information to each regulating converter every $\sim$80 μs. In addition, the microcontroller generates the 30 kHz 50 % duty ratio switching signal (with dead time) for the SC circuit.

C. Experimental Results

The prototype converter is designed to support up to 30 W output at 35 V from 120 V_{ac}. The prototype circuit of Fig. 10 was implemented on a 1.9 in x 1.4 in printed board as shown in Fig. 12.

Fig. 13 shows measured voltage waveforms of the converter at startup and during operation over the ac line cycle, when powered from a Agilent 6812B ac power supply. Ch 2 (blue) is the voltage across the capacitor C_2, and ch M (red) shows the voltage across the capacitor C_1. As can be seen, the capacitor C_2 fluctuates about 50 V over the line cycle in this prototype converter as it buffers the line-frequency energy.

Fig. 14 shows the measured input ac voltage and current. The prototype converter showed 93.3% efficiency with 0.89 power factor for a 35 V dc 30 W load.

The volume of the prototype converter is measured, and the "box power density" was calculated to 25 W/in^3. It is notable that this is much higher than the $\sim$5 W/in^3 found for typical commercial LED drivers at this power rating, even though we didn't optimize component layout for box-volume power density. The displacement volume was 0.23 in^3 yielding a "displacement power density" of 130 W/in^3; this illustrates the high power density achieved, and that layout can readily provide a greatly improved "box power density".
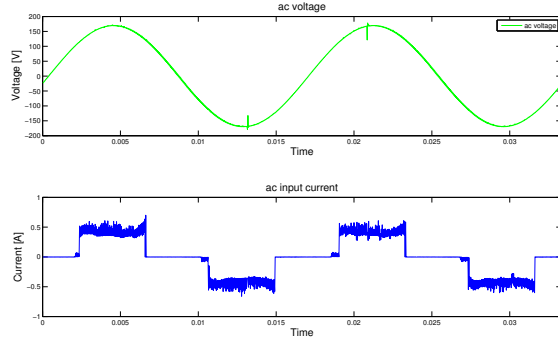
Fig. 14. The input ac current of the prototype converter was measured and plotted along with the input ac line voltage. The prototype converter showed 93.3% efficiency with 0.89 power factor at 35 V, 30 W load.
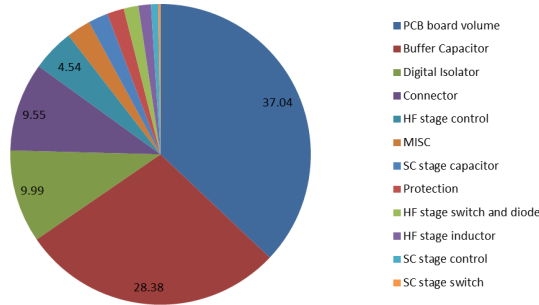

Fig. 15. The volume portion of each component was analyzed. The largest volume contributions of the prototype converter come from the PCB and energy buffer capacitors.

The volume portion of each component part is calculated and plotted as shown in Fig. 15. As can be seen in Figs. 12 and 15, there is substantial opportunity to reduce the size by integrating the control circuitry with an IC, using a high energy density electrolytic capacitor as C_2 (at the expense of converter lifetime), and designing with a thinner PCB board.

IV. Conclusion

A new ac-dc architecture suitable for single-phase grid interface at high switching frequency (above 3 MHz) is introduced and experimentally demonstrated. This new grid interface architecture is specifically intended for high frequency operation to deal with the needs of high efficiency, high power density, and high power factor for ac-dc applications. The proposed stacked-combined architecture can significantly decrease the voltage stress of the active and passive devices, enabling high-frequency operation and small size. Moreover good power factor is achieved while dynamically buffering twice-line-frequency ac energy with relatively small capacitors. The prototype implementation, which is suitable for LED driver applications, achieves 93.3 % efficiency and 0.89 power factor while maintaining high frequency operation and small size (130 W/in^3 displacement power density). The proposed architecture can be designed with different regulating and combining converter topologies, and can likewise be applied to the requirements of a variety of applications and power levels.

References

[1] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *Power Electronics, IEEE Transactions on*, vol. 18, no. 3, pp. 749–755, 2003.

[2] B. Singh, B. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. Kothari, "A review of single-phase improved power quality ac-dc converters," *Industrial Electronics, IEEE Transactions on*, vol. 50, no. 5, pp. 962–981, 2003.

[3] L. Huber, L. Gang, and M. Jovanovic, "Design-oriented analysis and performance evaluation of buck pfc front end," *Power Electronics, IEEE Transactions on*, vol. 25, no. 1, pp. 85–94, 2010.

[4] X. Wu, J. Yang, J. Zhang, and M. Xu, "Design considerations of soft-switched buck pfc converter with constant on-time (cot) control," *Power Electronics, IEEE Transactions on*, vol. 26, no. 11, pp. 3144–3152, 2011.

[5] J. Lam and P. Jain, "A novel high-power-factor single-switch electronic ballast," *Industry Applications, IEEE Transactions on*, vol. 46, no. 6, pp. 2202–2211, 2010.

[6] M. Chen, K. Afridi, and D. Perreault, "Stacked switched capacitor energy buffer architecture," *Power Electronics, IEEE Transactions on*, vol. 28, no. 11, pp. 5183–5195, 2013.

[7] A. Kyritsis, N. Papanikolaou, and E. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected ac-pv modules," in *Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1–10.

[8] ——, "Enhanced current pulsation smoothing parallel active filter for single stage grid-connected ac-pv modules," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 1287–1292.

[9] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *Power Electronics, IEEE Transactions on*, vol. 21, no. 5, pp. 1264–1272, 2006.

[10] S. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, vol. 3, 2003, pp. 1183–1190 vol.3.

[11] P. Krein and R. Balog, "Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and led lighting applications based on minimum capacitance requirements and a ripple power port," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 620–625.

[12] B. Pierquet and D. Perreault, "A single-phase photovoltaic inverter topology with a series-connected energy buffer," *Power Electronics, IEEE Transactions on*, vol. 28, no. 10, pp. 4603–4611, 2013.

[13] M. Araghchini, J. Chen, V. Doan-Nguyen, D. Harburg, D. Jin, J. Kim, M. S. Kim, S. Lim, B. Lu, D. Piedra, J. Qiu, J. Ranson, M. Sun, X. Yu, H. Yun, M. Allen, J. del Alamo, G. DesGroseilliers, F. Herrault, J. Lang, C. Levey, C. Murray, D. Otten, T. Palacios, D. Perreault, and C. Sullivan, "A technology overview of the powerchip development program," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4182–4201, 2013.

[14] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture for an led driver circuit," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 854–861.

[15] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, Feb. 2009, pp. 1 –14.

[16] C. Tse, M. H. L. Chow, and M. Cheung, "A family of pfc voltage regulator configurations with reduced redundant power processing," *Power Electronics, IEEE Transactions on*, vol. 16, no. 6, pp. 794–802, 2001.

[17] V. Vorperian, "Quasi-square-wave converters: topologies and analysis," *Power Electronics, IEEE Transactions on*, vol. 3, no. 2, pp. 183 –191, Apr 1988.

[18] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841 –851, March 2008.

[19] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. PP, no. 99, pp. 1 –11, 2012.