2012 IEEE Energy Conversion Congress and Exposition, pp. 4584-4591, Sept. 2012.

Integrated Low-Voltage Converter Architecture with AC Power Delivery

Wei Li, Nathaniel Salazar, David J. Perreault

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASSACHUSETTS 02139
EMAIL: fsrick@mit.edu

***Abstract*—Future computation systems pose a major challenge in energy delivery that is difficult to meet with existing devices and design strategies. To reduce interconnect bottlenecks and enable more flexible computation and energy utilization, it is desired to deliver power across the interconnect to the chip at high voltage and low current with on- or over-die transformation to low voltage and high current, while providing localized voltage regulation in numerous zones. This paper presents an integrated converter architecture with ac voltage transformation to provide very-high-frequency, low-voltage integrated power delivery.**

I. INTRODUCTION

Integrated low-voltage power delivery is drawing increasing attention due to both the expending personal electronics market and the increasing performance demands of computer systems. For example, according to the International Technology Roadmap for Semiconductors (ITRS) 2011, the current drawn by high performance microprocessors will increase to over 200 A by 2020 (Fig. 1). Moreover, even today about 2/3 of the total pins in the package are used for power and grounds [1], and this requirement increases with higher current. Chip power has increased greatly, and is effectively at or near the air cooling limit of approximately 100 W/cm^2 [2]. The need to deliver increasing current and achieve higher performance (including communications on and off die) represents a major challenge in CMOS scaling and IC packaging.

In order to reduce the interconnect loss and ease the pin count challenge, it is desired to deliver power across the interconnect at high voltage and low current with on- or over-die transformation to low voltage and high current, while providing localized voltage regulation in numerous zones. In doing this, voltage conversion ratios from 4:1 to more than 12:1, power conversion densities from 1 W/mm^2 to above 10 W/mm^2, and efficiencies greater than 90% are desired for local on-die conversion depending on system type.

These needs have not been met by any proposed conversion systems to date [3]–[6]. Existing integrated converter approaches are only sufficiently power dense and efficient for small conversion ratios (e.g., 2:1). Meeting the necessary conversion, power density, and efficiency targets requires power converter switching frequencies at many tens of megahertz and above, based on energy storage density considerations. On-chip Si transistor designs are capable of either efficient high-frequency switching or high blocking voltage, but not both. New approaches to power conversion and delivery need to be developed to break this trade-off.

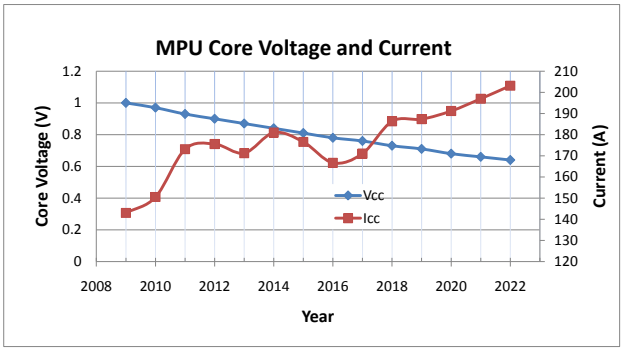


Fig. 1. Predicted microprocessor characteristics, drawn from the International Technology Roadmap for Semiconductors (ITRS) 2011.

Equally important are challenges associated with powering the myriad low-voltage electronic circuits in use today, including portable electronic devices, digital electronics, sensors and communication circuits among many items. These applications all require delivery of power at very low voltages (e.g., 0.5 - 3.3 V), often from much higher input voltages (e.g., $>$ 5 V). The size and cost of the power conversion electronics (dc-dc converters) for these applications are important, and limit overall system design. There is thus an evident need for advances in power conversion at low output voltages.

This paper presents a new power converter architecture utilizing ac power delivery to overcome the barriers described above. This power delivery architecture leverages high-voltage power devices (e.g., GaN-on-Si transistors) and low-voltage integrated Si CMOS transistors to provide power delivery solutions having greatly improved performance. Section II of the paper gives an overview of the ac power delivery architecture. Section III provides a detailed analysis of the system trade-offs and design considerations. Section IV presents the design and comparison of polyphase ac power delivery architectures, including the trade-off between converter efficiency and size. Experimental results from a prototype system are presented in section V, and section VI concludes the paper.

II. ARCHITECTURE

During the "War of Currents" era in the late 1880s, George Westinghouse and Thomas Edison became adversaries due to Edison's promotion of low-voltage direct current (dc) for the electric power distribution over alternating current (ac) supported by Westinghouse [7]. However, Edison's dc system suffered two major disadvantages: 1. The distribution range was limited and the cost penalty of the large required amount of conductor was high; 2. Higher distribution voltages could not easily be used with the dc system because there was no efficient, low-cost technology that would allow reduction of a high transmission voltage to a low utilization voltage. On the other hand, in the alternating current system, a transformer could be used to locally step down a high distribution voltage to low voltages for customer loads. With the ease of changing voltages using a transformer, a high-voltage, low-current ac system can greatly reduce the conduction loss and conductor cost in transmission, which is what led the ac power delivery to become the dominant electric-power transmission system.

Today, delivery of power to microprocessors represents a similar challenge. Delivery of power to the die at the final very low voltage requires a dominant portion of the chip pin count, that could be better employed for computation and communication. Moreover, the present system leads to challenges of voltage control (drop) and conductor loss both on die and in the interconnect to the die. The difficulties of making efficient high-conversion-ratio dc-dc converters on die provides a similar barrier to high-voltage distribution and local conversion as in the war of the currents, but on a different scale.

Fig. 2 shows the three major blocks of a dc-dc converter: inverter stage, transformation stage and rectification stage. A conventional buck converter has no transformation stage, so the inverting and rectifying devices each see both high current and high voltage, making this approach unattractive for high-conversion-ratio on-die dc-dc converters. Topologies with a transformation stage (e.g. coupled-inductor buck, flyback, etc.) can operate using only low-voltage rectifier devices. However, they require coupled magnetics (or transformers) which are not readily realized on die. Moreover, the inverter devices still must be both fast and high voltage, which are again unavailable in conventional processes. Magnetics based large-conversion-ratio dc-dc converters integrated on die in CMOS thus represent a major challenge. (Not considered here are switched-capacitor circuits [3], [4] and mixed capacitor-inductor circuits [8]–[10], which may represent a better opportunity, but have not yet fully proven themselves at high conversion ratio.)

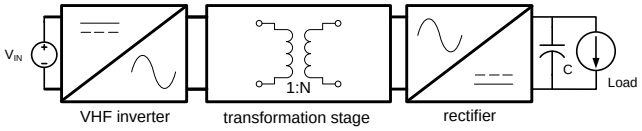
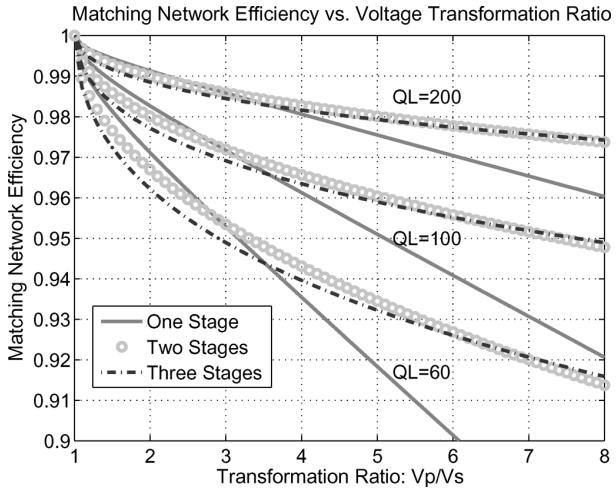


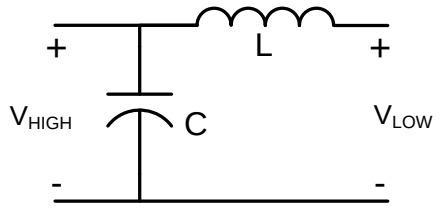
Fig. 2. General architecture of a dc-dc converter.

As in the war of the currents, another possibility is high-voltage ac distribution across the interconnect, with local (on-die) transformation and rectification. Indeed, a version of this general idea has been proposed previously [11], but without any enabling means of realizing the high-frequency on-die magnetic transformers that would be required. This limitation aside, ac distribution in this application has important merits: It allows high-voltage and low current distribution, allows the use of low-voltage CMOS rectifiers on die, and enables the inverter to be placed off die where size and loss are less important and where it can be effectively realized in a non-CMOS device process.

An alternative to magnetic transformers for providing voltage transformation is the use of matching networks or immittance conversion networks, which require only inductors and capacitors to realize. With the emergence of high-efficiency, high-power-density integrated inductors at very high frequencies (VHF), such as those developed in [12], an ac power delivery system starts to become practical. In [12], a Q of 66 at 100 MHz was reported, and inductors having Q of over 100 are under development; these quality factors are sufficient for constructing high-efficiency matching networks [13].



(a) Matching Network Efficiency Plot



(b) Sample Matching Network Schematic

Fig. 3. High efficiency matching network transformation stage [13].

A complete ac power delivery architecture (Fig. 4) is proposed here for a low-voltage integrated power delivery system. High-voltage discrete power devices (e.g., GaN-on-Si transistors) can be used for the VHF inverter stage off die, generating high-voltage, low-current power at VHF fre-

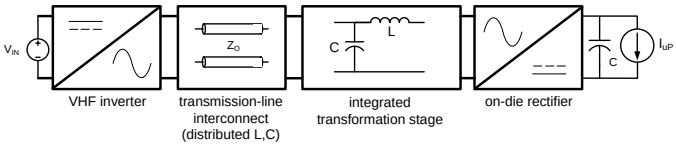


Fig. 4. Architecture of an ac power delivery system.

quencies (e.g. 50-100 MHz) which is delivered across the interconnect. Integrated passives form a matching network for the transformation stage, converting the VHF power to low voltage and high current. Integrated rectifiers using native low-voltage CMOS devices transform the waveforms back to dc, completing the power conversion system. To the authors' knowledge, no in-depth analysis of the proposed ac power delivery architecture has been published, nor has the feasibility of the approach been validated. Here we present an investigation of the achievable performance of such a system within currently available technology, along with a trade-off comparison among different implementation options. This paper also presents an experimental validation of the feasibility of VHF ac power delivery using a discrete component prototype system.

III. Analysis

Fig. 5 shows a setup for comparing loss among dc and ac delivery systems. Let both systems have the same output voltage V_o and same output power P. In order to compare the interconnect loss fairly, also let both systems have the same amount of area for interconnect conductor, with unit sheet resistance R. We first make a comparison without a transformation stage between the input and load. For the dc system, there are only two conductors for power delivery and (1) shows the current and power loss for the interconnect. For the ac system, consider use of a full bridge rectifier, with sinusoidal current in the interconnect. Equation (2) shows the amplitude of the ac current in the conductor and power loss in the interconnect. Without any transformation, single-phase ac power delivery has 23% more conduction loss than the dc power system. However, with a high-performance integrated ac transformation stage, interconnect loss will be reduced by the square of the voltage transformation ratio. Fig. 6 shows a simple schematic of a single phase ac power delivery system with full bridge rectifier. Full bridge rectification doubles the voltage swing at the rectifier input, reduces the current through the devices and increases the input impedance of the rectifier. This can give us more favourable passive values for the matching network in high output power applications. In addition, the voltage transformation ratio required for the matching network is reduced by a factor of 2 when overall conversion ratio is held constant, which will give better performance in the matching network.

$$I_{dc} = P/V_o; P_{Loss} = 2 \times I_{dc}^2 \times 2R = 4 \times P^2 \times R/V_o^2 \quad (1)$$

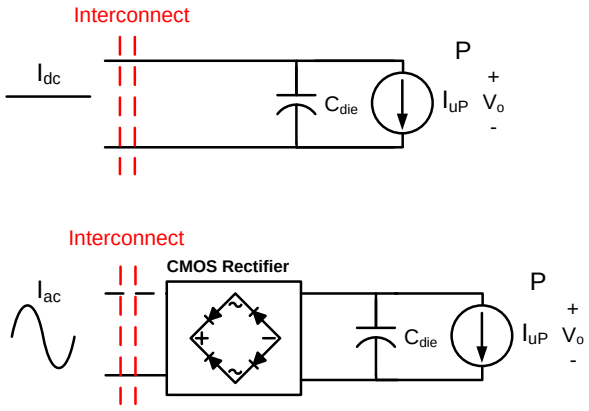


Fig. 5. System for comparison of ac and dc interconnect loss. It is assumed that each system has the same interconnect area, the same output voltage V_o and same output power P.

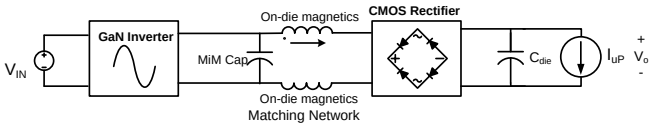


Fig. 6. Sample schematic of an ac power delivery system. Diodes are shown for illustration purposes only; a synchronous CMOS rectifier would be used for an integrated circuit implementation.

$$I_{ac} = \pi P/(2V_o); P_{Loss} = 2 \times \frac{1}{2} I_{ac}^2 \times 2R = \pi^2/2 \times P^2 \times R/V_o^2 \quad (2)$$

With a fixed voltage conversion ratio and given technologies for passive components, the output power level can be chosen to optimize the power density of the matching network. Fig. 7 shows an example of the area trade off in the matching network for an exemplary system having a 6:1 ac to dc voltage conversion ratio. In this example, a TSMC 1 nF/mm^2 MiM capacitor process (with 19 V blocking voltage) is used for calculation and thin-film v-groove magnetics (L=1.7 nH/mm, width=212 μm and Q of 66 @ 100MHz) [12] are used for matching network inductors. The ac input voltage of the matching network is 6 V from line to neutral (12 V_{pk} line-to-line voltage) and the dc output voltage of the rectifier is 1 V. The voltage transformation ratio of the matching network is thus (3π):1 and the full bridge rectifier provides a fundamental amplitude ac-to-dc conversion of ($2/\pi$):1. The plot shows that the inductor area dominates the total system area when the output power is less that 2 W. The optimal density is obtained at about 2.3 W when the areas of L and C are balanced. When the output power is larger than the optimal power, capacitor area becomes the major portion of the total system area. In addition, efficiency of the system degrades due to smaller Q in the larger capacitors as the output power increases. While the above work illustrates the promise of ac power delivery, this paper also explores methods to greatly improve achievable performance which includes the use polyphase power delivery

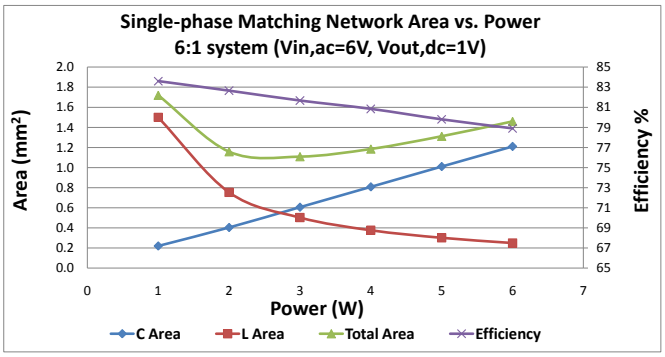


Fig. 7. This plot shows the area trade-off in the matching network for an exemplary ac power delivery system. With a given technology for passive components and voltage transformation ratio, the optimal power density of the matching network is output power dependent.

and voltage transformation.

IV. Polyphase System

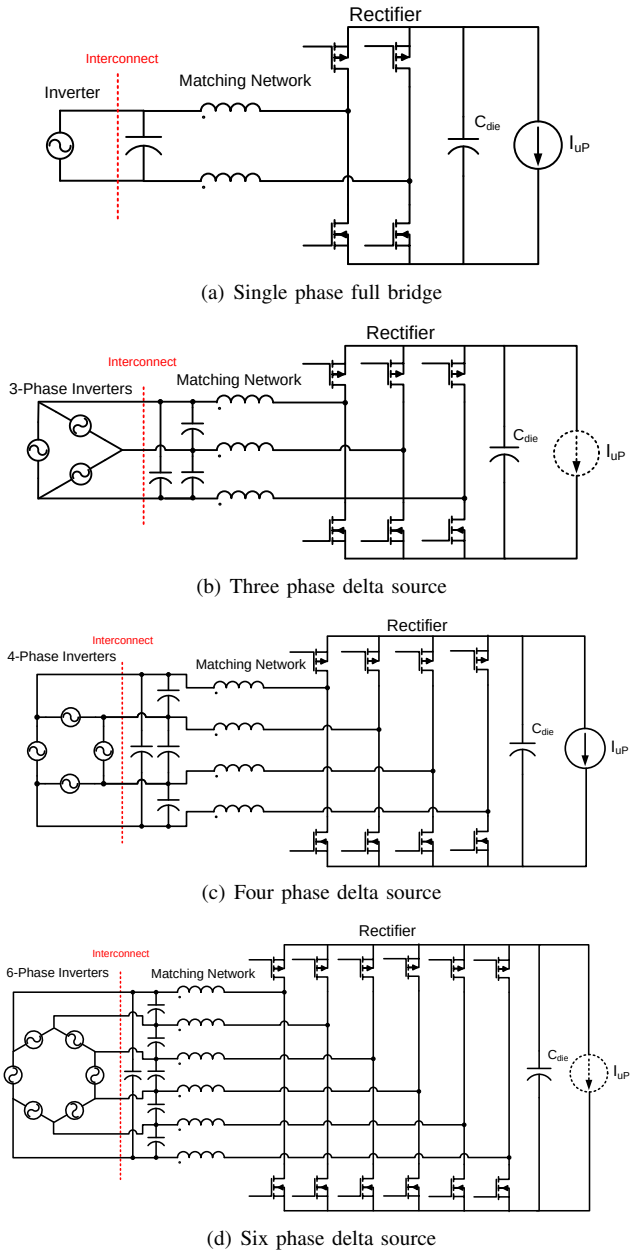
In conventional ac power distribution systems, polyphase power transmission is normally used to reduce conduction loss and harmonics in the ac system and the energy buffering/filtering requirements at the load. These advantages can also be leveraged in our integrated ac power delivery system. We also consider size and performance trade-offs for the polyphase systems. In this comparison, a 1 V output voltage is chosen. An operation frequency of 100 MHz and an output power of 2 watts is used to optimize the values of passive components for integration purposes. (This power level can represent that of a small zone in a microprocessor, or that of an entire low-power digital IC). Four different kinds of polyphase systems are used in this comparison: single-phase full bridge (two-phase 180^o system), 3-phase, 4-phase and 6-phase. The schematic of each system is shown in Fig. 8.

Matching networks are not traditionally employed in polyphase systems. However, we consider their designs here. For a polyphase "L-section" matching network, each phase branch has one series element and one shunt element. However, the shunt elements may be "delta" or "star" connected. Fig. 9 shows two configurations of a 3-phase matching network. For the matching network with star connected capacitors, the fundamental ac voltage at the "y" point is zero in balanced polyphase, but harmonics may exist. Depending on design choices and constraints, this center point can float or be connected to a fixed potential. So substrate-referenced capacitors can be used in the star system, but not the delta system. The values of the matching network elements with star-connected capacitors can be calculated from equations (3) and (4):

$$Q_T = \sqrt{(R_p/R_s - 1)} = \sqrt{(V_p^2/V_s^2 - 1)} \qquad (3)$$

$$L = Q_T \times R_s/(2\pi f); \quad C = Q_T/R_p/(2\pi f) \qquad (4)$$

The values of the matching network elements with delta



(a) Single phase full bridge

(b) Three phase delta source

(c) Four phase delta source

(d) Six phase delta source

Fig. 8. Polyphase power delivery systems.

connected capacitors can be calculated from equations (5) and (6):

$$Q_T = \sqrt{(R_p/R_s - 1)} = \sqrt{(V_p^2/V_s^2 - 1)} \qquad (5)$$

$$L = Q_T \times R_s/(2\pi f); \quad C = Q_T/R_p/[2sin(\frac{\pi}{m})]^2/(2\pi f) \qquad (6)$$

where m is the number of conductors (and half bridge rectifiers).

From equations (4) and (6), we can see that both star connection and delta connection require the same inductor value for a given voltage conversion ratio. However, the values

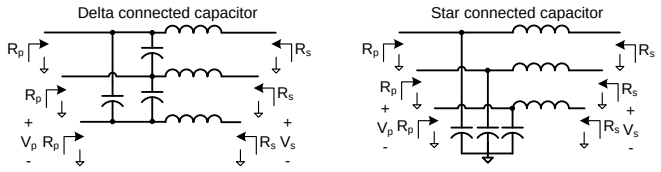


Fig. 9. This plot shows two configurations of a polyphase matching network connection. The left matching network is with delta-connected shunt elements (capacitors) and the right one is with star ("wye"/"y") connected shunt elements (capacitors).

TABLE I
CAPACITOR BREAKDOWN VOLTAGE REQUIREMENT FOR A POLYPHASE MATCHING NETWORK SYSTEM WITH 1V DC OUTPUT

Ratio	Phases	Line to line	Line to ground
2.5:1	Full Bridge	5	2.5
	3-phase	4.3	2.5
	4-phase	3.5	2.5
	6-phase	2.5	2.5
4:1	Full Bridge	8	4
	3-phase	6.9	4
	4-phase	5.7	4
	6-phase	4	4
6:1	Full Bridge	12	6
	3-phase	10.4	6
	4-phase	8.5	6
	6-phase	6	6

"line to ground" is the amplitude of the ac component of the line-to-ground voltage on each phase, "line to line" is the amplitude of the line-to-line voltage difference between adjacent phases, which is $2sin(\frac{\pi}{m})$ times the line-to-ground voltage.

of capacitors in the delta shunt matching network are a factor of $1/[2sin(\frac{\pi}{m})]^2$ times those appearing in the star-connected shunt network, so are smaller-valued for less than m=6 phases (or half bridge rectifiers) and have the same value for m=6. On the other hand, the capacitors in the delta network have voltage ratings that are $2sin(\frac{\pi}{m})$ times those in the star network, requiring higher blocking voltage for less than m=6 phases (The required shunt-element energy storage is identical for the two networks). Some example data is shown in Table I. The capacitor density usually decreases as the blocking voltage rating increases due to the thicker required insulation layer. Even though the delta-connected capacitor matching network requires smaller capacitance, the overall power density may not be higher due to the higher blocking voltage requirement. So the preferred polyphase matching network configuration depends on available capacitor characteristics.

In this polyphase system comparison, the total area for interconnect conductor is fixed for all systems, with unit sheet resistance R. According to equation (7), for the same power output and with ac sources connected off die, without considering any matching network voltage transformation, all polyphase systems have the same interconnect loss as long as they have the same line-to-neutral voltages. However, the capacitor blocking voltage will be different in different matching network configurations even with the same line-to-neutral voltages.

$$I_{ac} = \pi P/(mV_o)$$
$$P_{Loss} = m \times \frac{1}{2} I_{ac}^2 \times mR = \pi^2/2 \times P^2 \times R/V_o^2 \quad (7)$$

For integrated metal-insulator-metal (MiM) capacitors, SiO_2 is usually used for the dielectric, and the maximum blocking voltage depends on the thickness of the SiO_2. With a higher breakdown voltage rating, the required thickness (d) of the SiO_2 is larger since the maximum breakdown field of the SiO_2 is around 5.6MV/cm [14], and the capacitor density will be lower due to $C = \epsilon A/d$ (ϵ is the permittivity of the dielectric, A is the area of the capacitor and d is the insulation thickness). Moreover, the selection of the integrated capacitors is normally limited by the process. A typical TSMC MiM capacitor has a capacitance density of 1 nF/mm^2, and - based on density characteristics, and material parameters - has a capacitor breakdown rating estimated to be as high as 19 V. According to Table I above, for a 6:1 voltage conversion ratio in the matching network, the maximum blocking voltage required for the capacitor among all polyphase systems is 12 V, well below the estimated 19 V breakdown voltage rating in the TSMC 1 nF/mm^2 MiM capacitor. As a result, a matching network with delta-connected capacitors is used to optimize the power density in this typical case.

The total system area computed in our comparison includes the area of the matching network, rectifier and output decoupling capacitor. Inductor information is all based on Di's result in [12]. 1 nF/mm^2 MiM capacitors are assumed for the matching network capacitors. (Metal resistance of the MiM capacitor is estimated for the matching network performance calculation). A MOS capacitor is used for the output decoupling capacitor. Semiconductor size and performance are calculated based on an IBM 65nm process. Since the output power is the same, the total rectifier device area is the same for all systems. In addition, rectifier device losses are also the same, but output ripple and filtering requirements are different. While this results in reasonable design trade-offs, better performance could be achieved with more advanced technologies.

The comparison result in Fig. 10 shows that a 3-phase system has the best overall performance and density over different conversion ratios with the TSMC MiM capacitor technology. This topology appears best because it yields more favorable values of the passive components in the matching network and also minimizes the output capacitance due to the constant power delivery of the 3-phase system. The 3-phase matching network promises nearly 84% efficiency with a 6-to-1 conversion ratio and achieves close 1 W/mm^2 power density including the transformation and rectification stage and output decoupling capacitor. In addition, a 3-phase system cancels the third harmonic in the line-to-line voltages, which is better for the output filter design in the inverter. These results illustrate

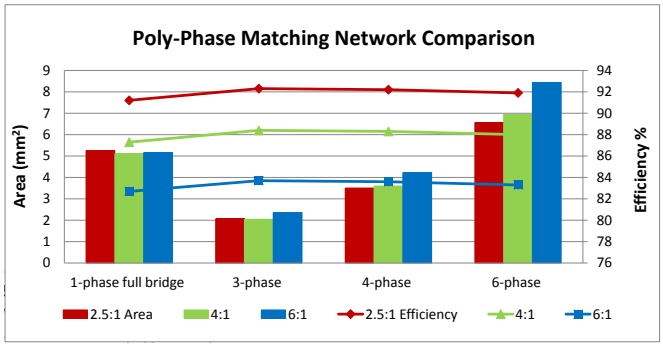


Fig. 10. Comparison of 2-W polyphase systems. The conversion ratio is the line-to-neutral voltage of the ac input to the dc output voltage. The efficiency shown is for the matching network only. The optimized rectifier performance based on IBM 65nm is about 94% in all cases. The rectifier area is about 0.1 mm^2, which is negligible compared to the rest of the system.

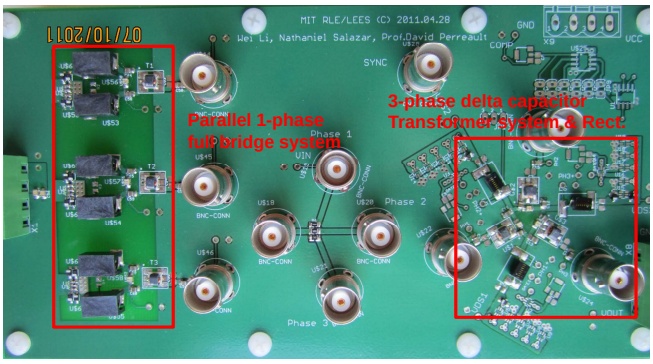


Fig. 11. Picture of the polyphase ac power delivery PCB prototype test board.

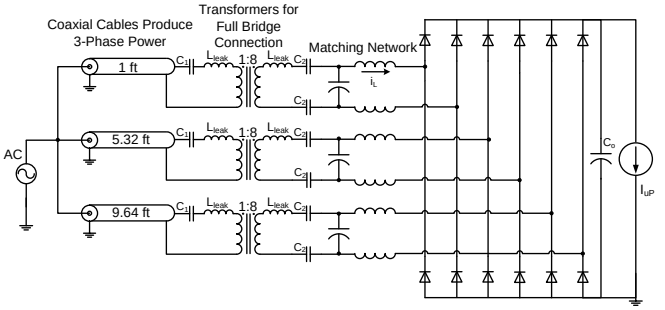


Fig. 12. Schematic of the prototype 3-phase system with separate single-phase matching networks and individual full bridge rectifiers. C_1 and C_2 are 680 pF and 68 pF respectively. They are used for transformer leakage inductance cancellation. 39 pF ATC capacitors and 135 nH Coilcraft Maxi Spring air core inductors were used to form the matching networks.

the tremendous potential of the proposed architecture.

V. Experimental Validation

In order to validate the feasibility of delivering polyphase ac power at VHF frequencies and rectifying it to provide a low-voltage dc output, a discrete experimental prototype was developed. It should be noted that proposed converter architecture is targeted for low-voltage integrated processes. The initial prototype introduced here is implemented with discrete components purely to validate the concept and provide insights for future designs based on integrated processes. It does not pursue the performance and power density expected in an integrated system. In addition, air core inductor and magnetic transformers are used instead of high-power-density integrated inductors (such as proposed in [12]) for this initial validation. The picture of the polyphase ac power delivery prototype board is shown in Fig. 11. For comparison purposes, two kinds of systems are implemented: a 3-phase system with separate single-phase matching networks and individual full bridge rectifiers, and a 3-phase system with Δ connected capacitor matching network and 3-phase bridge rectifier. For the initial testing, the ac power is supplied by a power amplifier instead of custom-built VHF inverters. 3-phase power is generated from this single-phase source by power-dividing this source equally into 3 coaxial cables, each different in length from an adjacent cable by a third of a wavelength; floating outputs are then generated with a set of RF transformers. 1:8 Coilcraft WBC8-1L RF transformers are used for power amplifier impedance matching and forming the 3-phase delta/full-bridge ac source. The system operates at 50 MHz with the input line-to-neutral ac voltage of 6 V and the DC output voltage of 2 V. Output power is about 0.5 W, which is limited by the discrete RF transformers. Infineon BAT60A diodes are used for the rectifiers, as CMOS rectifiers having appropriate characteristics were not available.

Fig.12 shows the schematic of 3-phase system with separate single-phase matching networks and individual full bridge rectifiers. 39 pF ATC capacitors and 135 nH Coilcraft Maxi Spring air core inductors were used to form each of the separate single-phase $3\pi/2$:1 matching networks. The rectifier provides a fundamental ac-to-dc conversion of $2/\pi$:1, and hence the overall voltage conversion ratio in the ac system is 3:1. Since this is a full bridge system, the line-to-line voltage is 12 V, which is twice the line-to-neutral voltage.

Fig. 13 shows the schematic of the 3-phase delta-source system. 68 pF ATC capacitors and 47 nH Coilcraft Midi Spring air core inductors were used to form the 3-phase delta connected capacitor matching network with a $3\pi/2$:1 voltage conversion ratio. Again the rectifier provides a fundamental ac-to-dc conversion of $2/\pi$:1. Thus the ac line-to-neutral to dc output voltage conversion ratio in the system is 3:1. Since the Δ to Y connection provides voltage conversion of $\sqrt{3}$:1, the line-to-line voltage in this system is $6\times\sqrt{3} \approx 10.4$ V.

The measured line-to-neutral voltages of the two systems are shown in Fig. 14. Both systems shows 3-phase 6 V line-to-neutral voltages and 2 V dc output voltage. In addition, Fig. 15 show the line-to-line voltages of both systems. The parallel single-phase system shows 12 V line-to-line input voltages, and the system with the 3-phase matching network having delta-connected capacitors shows around 10.5 V line-to-line ac voltages in the input. The full bridge rectifiers in the parallel single-phase system show the +/- V_o swing in the input of the rectifier, and the Y-connected 3-phase rectifiers in the 3-phase matching network system show only ground to V_o swing.

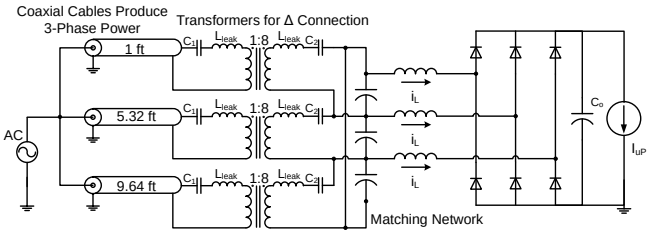


Fig. 13. Schematic of the prototype 3-phase delta-source ac power delivery system. C_1 and C_2 are 680 pF and 68 pF respectively. They are used for transformer leakage inductance cancellation. 68 pF ATC capacitors and 47 nH Coilcraft Midi Spring air core inductors were used to form the 3-phase delta-connected capacitor matching network.

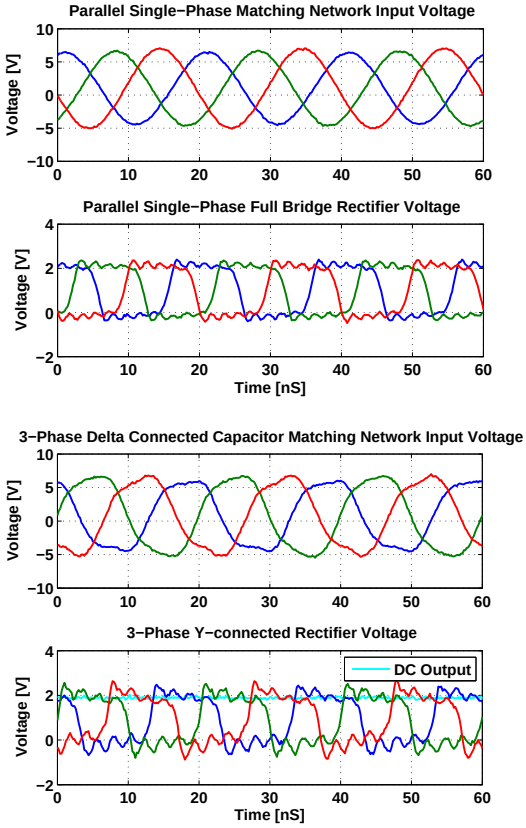


Fig. 14. Experimental results for the 3-phase 50 MHz power delivery systems. Both the system with parallel single-phase matching networks and the system with a 3-phase matching network having delta-connected capacitors shows 6 V line-to-neutral input ac voltages and 2 V dc output voltage.

The measured overall system efficiency is about 70% for the 3-phase system with separate single-phase matching networks and 65% for the 3-phase delta system, which matches the calculated performance. (Estimated transformer efficiency is 98%, matching network efficiency is 92% for the single phase and 91% for the delta network, and the rectifier efficiency is approximately 80% for the full bridge and 75% for the 3-phase bridge). The largest loss in the discrete prototype is due to the rectifier diode drops, which is not surprising given the low system output voltage. In the targeted applications, with fast low-voltage integrated CMOS technologies, synchronous rectification can provide much better performance for this converter architecture.

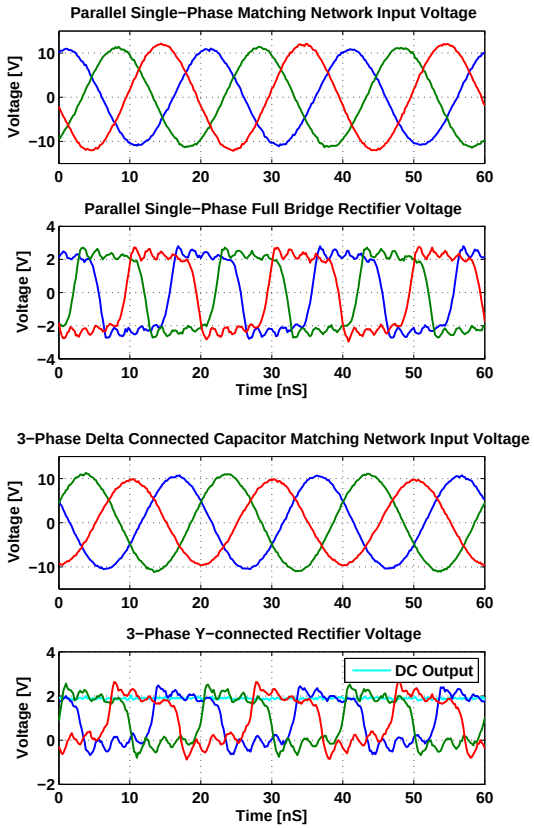


Fig. 15. Additional experimental results for the 3-phase 50 MHz power delivery systems. Top is the measured waveforms of the 3-phase system with separate single-phase matching networks and separate single-phase full bridge rectifiers. It has line-to-line ac voltages of 12 V. The next plot shows the +/- 2 V rectifier switching waveforms, with peak amplitude equal to the output voltage. The bottom plot of the half-bridge rectifier input waveforms is the result for the system with the 3-phase matching network with having delta-connected capacitors. It has a line-to-line voltage of 10.5 V and shows the rectifier inputs switching between 0 V and the output voltage.

VI. Conclusion

This paper presents an ac power delivery architecture for low-voltage electronics. This power delivery architecture leverages high-voltage power devices (which may be off die) and low-voltage integrated Si CMOS devices. It takes advantage of a transformation stage using integrated inductors to provide integrated power delivery. Analysis reveals that such a system is feasible, and that polyphase RF power delivery is advantageous. A discrete prototype operating at 50 MHz has been designed and built to demonstrate and verify the concept. With the ac power transformation stage and rectifier stage on die, this architecture promises to help reduce pin count and interconnect loss for microprocessors. It is also suitable for other portable electronics and applications where high power density is desired.

ACKNOWLEDGMENTS

The authors acknowledge the support of the Interconnect Focus Center, one of five research centers funded under the Focus Center Research Program, a DARPA and Semiconductor Research Corporation program.

REFERENCES

[1] "ITRS roadmap 2011," International Technology Roadmap for Semiconductors, 2011. [Online]. Available: http://www.itrs.net/Links/2011ITRS/Home2011.htm

[2] G. Shahidi, "Evolution of CMOS technology at 32 nm and beyond," in *IEEE Custom Integrated Circuits Conference, 2007. CICC '07.*, Sept. 2007, pp. 413 –416.

[3] H.-P. Le, M. Seeman, S. Sanders, V. Sathe, S. Naffziger, and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor dc-dc converter delivering 0.55W/mm2 at 81% efficiency," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010*, Feb. 2010, pp. 210 –211.

[4] H.-P. Le, S. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120 –2131, Sept. 2011.

[5] G. Schrom, P. Hazucha, F. Paillet, D. J. Rennie, S. T. Moon, D. S. Gardner, T. Kamik, P. Sun, T. T. Nguyen, M. J. Hill, K. Radhakrishnan, and T. Memioglu, "A 100MHz eight-phase buck converter delivering 12A in 25mm2 using air-core inductors," in *22nd IEEE Applied Power Electronics Conference, APEC 2007*, 25 2007-March 1 2007, pp. 727 –730.

[6] J. Sun, J.-Q. Lu, D. Giuliano, T. P. Chow, and R. J. Gutmann, "3D power delivery for microprocessors and high-performance asics," in *22nd IEEE Applied Power Electronics Conference, APEC 2007*, 25 2007-March 1 2007, pp. 127 –133.

[7] EdisonTechCenter, "AC power history," 2010. [Online]. Available: http://www.edisontechcenter.org/AC-PowerHistory.html

[8] R. Pilawa-Podgurski, D. Giuliano, and D. Perreault, "Merged two-stage power converterarchitecture with soft charging switched-capacitor energy transfer," in *IEEE Power Electronics Specialists Conference, 2008. PESC 2008.*, June 2008, pp. 4008 –4015.

[9] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1557 –1567, July 2012.

[10] B. Mahdavikhah, P. Jain, and A. Prodic, "Digitally controlled multi-phase buck-converter with merged capacitive attenuator," in *27th IEEE Applied Power Electronics Conference and Exposition (APEC), 2012*, Feb. 2012, pp. 1083 –1087.

[11] J. M. Cruz, R. J. Bosnyak, and S. Verma, "Powering ic chips using ac signals," U.S. Patent 6 597 593, Jul 22, 2003.

[12] D. Yao, C. Levey, and C. Sullivan, "Microfabricated v-groove power inductors using multilayer Co-Zr-O thin films for very-high-frequency dc-dc converters," in *IEEE Energy Conversion Congress and Exposition (ECCE), 2011*, Sept. 2011, pp. 1845 –1852.

[13] Y. Han and D. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1484 –1491, Sept. 2006.

[14] C. Sire, S. Blonkowski, M. J. Gordon, and T. Baron, "Statistics of electrical breakdown field in HfO2 and SiO2 films from millimeter to nanometer length scales," *Applied Physics Letters*, vol. 91, no. 24, pp. 242 905 –242 905–3, Dec 2007.