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Stacked Switched Capacitor Energy Buffer Architecture

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***Abstract*— Electrolytic capacitors are often used for energy buffering applications, including buffering between single-phase ac and dc. While these capacitors have high energy density compared to film and ceramic capacitors, their life is limited and their reliability is a major concern. This paper presents a stacked switched capacitor (SSC) energy buffer architecture and some of its topological embodiments which overcome this limitation while achieving comparable effective energy density without electrolytic capacitors. The architectural approach is introduced along with design and control techniques. A prototype SSC energy buffer using film capacitors, designed for a 320 V dc bus and able to support a 135 W load has been built and tested with a power factor correction circuit. It demonstrates the effectiveness of the approach.**

I. Introduction

Power conversion systems that interface between dc and single-phase ac need energy storage to provide buffering between the constant power desired for a dc source or load and the continuously-varying power desired for a single-phase ac system, as illustrated in Fig. 1. Applications for such buffering include power supplies, solar photovoltaic inverters, electric vehicle chargers and grid-connected light emitting diode (LED) drivers. Assuming unity power factor, the power from or to the single-phase ac system, $P_{ac}(t)$, varies sinusoidally at twice-line frequency (120 Hz in the US) between zero and twice its average value, $P_{\rm avg}$, with average ac system power equaling the dc system power, $P_{\rm dc}$:

$$P_{\rm ac}(t) = P_{\rm dc}(1 - \cos(2\omega_{\rm line}t)). \quad (1)$$

Here $\omega_{\rm line}$ is the line's angular frequency ($2\pi \times 60$ rad/s for the US). The difference in instantaneous power between source and load must be absorbed or delivered by the energy buffer:

$$P_{\rm b}(t) = P_{\rm dc} - P_{\rm ac}(t) = P_{\rm dc}\cos(2\omega_{\rm line}t). \quad (2)$$

The peak energy that needs to be buffered, $E_{\rm b}$, is the total energy delivered to (or extracted from) the buffer during a half-line cycle and given by:

$$E_{\rm b} = \frac{P_{\rm dc}}{\omega_{\rm line}}. \quad (3)$$

Since the peak buffered energy depends only on the dc system power and the line frequency, the volume of the energy buffer cannot be reduced simply by increasing the switching frequency of a power electronic converter interfacing the single-phase ac and dc systems.

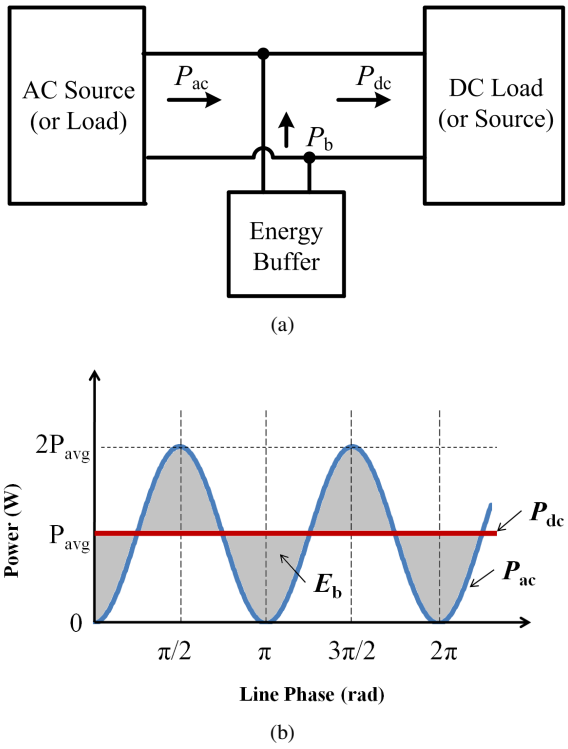


Fig. 1: Mismatch in instantaneous power between single-phase ac, $P_{\rm ac}$, and constant power dc, $P_{\rm dc}$, results in the need for an energy buffer, as shown in (a), to absorb and supply the energy, $E_{\rm b}$, indicated by the shaded area in (b).

Today, electrolytic capacitors are generally used to provide high-density energy storage for buffering. However, it is widely appreciated that despite providing the best available energy density, electrolytic capacitors represent a significant source of system lifetime and reliability problems. On the other hand, film capacitors have much higher reliability and lifetime, but considerably lower peak energy density. Hence, the development of energy buffering architectures that eliminate electrolytic capacitors while maintaining high energy storage density and high efficiency is important for future grid interface systems that have small size and high reliability.

While electrolytic capacitors provide much higher peak energy density than film capacitors (by an order of magnitude), electrolytic capacitors can only be operated over a narrow charge/discharge range (corresponding to a small voltage ripple) at 120 Hz for thermal and efficiency reasons. These considerations directly limit the energy buffering capability of electrolytic capacitors at 120 Hz. Thus, while peak energy densities of up to 0.8 $\mathrm{J/cm^3}$ can typically be achieved with commercially available electrolytic capacitors at the voltage and power levels we consider, the allowable energy swing at 120 Hz yields practical energy densities that are significantly lower [1]. Film capacitors typically have peak energy densities of only about 0.1 $\mathrm{J/cm^3}$. Therefore, if electrolytic capacitors are simply replaced by film capacitors (with similar voltage swing constraints), the passive volume would roughly increase by an order of magnitude, which is usually unacceptable. However, film capacitors have considerably lower series resistance compared to electrolytic capacitors which allows them to be efficiently charged and discharged over a much wider energy range. Using a large fraction of the capacitor's stored energy results in large voltage swings, which is also unacceptable in most applications. Therefore, if electrolytic capacitors are to be replaced by film capacitors while maintaining high energy density, this wide variation in capacitor voltage must somehow be curtailed.

This paper presents a new switched capacitor based energy buffer architecture that restricts the apparent voltage ripple while utilizing a large fraction of the energy in the capacitors, and successfully replaces electrolytic capacitors with film capacitors to achieve longer lifetimes while maintaining small volume. The remainder of this paper is organized as follows: Section II describes the past work on film-capacitor-based energy buffers and switched-capacitor-based energy storage architectures. Section III details the fundamental principles of the proposed stacked switched capacitor (SSC) energy buffer architecture. A specific topological implementation of this architecture and its extensions are described in section IV. This section also provides design guidelines for selecting an appropriate topology for a particular application. Section V describes the design and implementation of a prototype SSC energy buffer. The experimental results from this prototype are discussed and compared with simulation in section VI. Finally, section VII summarizes the conclusions of the paper and identifies directions for future work.

II. Past Work

In past efforts, bidirectional dc-dc converters have been employed to effectively utilize film capacitors while maintaining a desired narrow-range bus voltage [2], [3]. While this approach is flexible in terms of it use, it unfortunately leads to low buffering efficiency if high power density is to be maintained, due to losses in the dc-dc converter. Other systems have incorporated the required energy buffering as part of the operation of the grid interface power stage [4]–[7]. This can offset a portion of the buffering loss associated with introduction of a complete additional power conversion stage, but still introduces high-frequency loss and is quite restrictive in terms of operation and application.

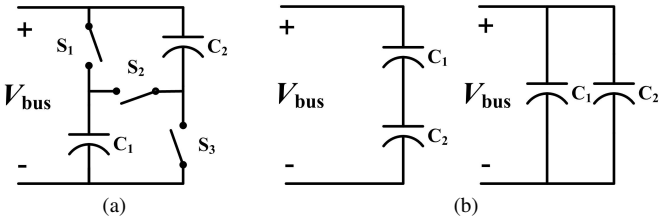


Fig. 2: (a) A simple parallel-series switched capacitor circuit, and (b) its two configurations under alternate switch states. This circuit can constrain bus voltage to within 33.3% of nominal value while providing energy buffering capability of 93.75% of total peak energy-storage capability of the capacitors.

An alternative approach relies on switched capacitor circuits. Switched capacitor circuits that reconfigure capacitors between parallel and series combinations have been used to improve the energy utilization of ultra-capacitors [8]–[10]. A simple version of this parallel-series switched capacitor circuit is shown in Fig. 2. While this circuit has a high energy buffering ratio[1] of 93.75%, it suffers from a large voltage ripple ratio[2] of 33.3%. More complex parallel-series switched capacitor circuits which achieve better voltage ripple ratio have also been developed [10]. However, they suffer from high circuit complexity when high energy utilization and small voltage ripple are required. For example, the circuit with the best performance in [10] (the 8-6-5-4-3 parallel-series switched capacitor circuit) has energy utilization of 92.09% and a voltage ripple ratio of 14.3%. However, it needs 41 switches and 120 capacitors. This makes it overly complicated for practical use.

III. Stacked Switched Capacitor (SSC) Energy Buffer Architecture

Figure 3 shows the general architecture of the proposed stacked switched capacitor (SSC) energy buffer. It is composed of two series connected blocks of switches and capacitors. The capacitors are of a type that can be efficiently charged and discharged over a wide voltage range (e.g., film capacitors). The switches enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer port (V_{bus}). The SSC energy buffer works on the principle that its individual buffer capacitors absorb and deliver energy without tightly constraining their individual terminal

[1] **Energy buffering ratio** (Γ_{b}) is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer, i.e., $\Gamma_{\mathrm{b}} = \frac{E_{\max} - E_{\min}}{E_{\mathrm{rated}}}$, where $E_{\max}$ and $E_{\min}$ are the maximum and minimum values of energy stored in the energy buffer during normal operation, and E_{rated} is the total energy capacity of the energy buffer.

[2] **Voltage ripple ratio** (R_v) is defined as the ratio of the peak voltage ripple amplitude to the nominal (or average) value of the voltage, i.e., $R_v = \frac{V_{\max} - V_{\min}}{2V_{\mathrm{nom}}}$, where $V_{\max}$, $V_{\min}$ and V_{nom} are the maximum, minimum and nominal values of the voltage, respectively [11].

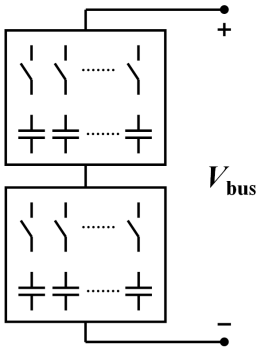


Fig. 3: General architecture of the stacked switched capacitor (SSC) energy buffer.

voltages, but maintain a narrow range voltage at the buffer port. The switching network is operated such that the voltage seen at the buffer port varies only over a small range as the capacitors charge and discharge over a wide range to buffer energy. This enables high effective energy density through maximum utilization of the capacitor energy storage capability.

Efficiency of the SSC energy buffer can be extremely high because the switching network need operate at only very low (line-scale) switching frequencies, and the system can take advantage of soft charging of the energy storage capacitors to reduce loss [12]. Moreover, the proposed buffer architecture exhibits losses that scale with the amount of energy that must be buffered, such that high efficiency can be achieved across the full operating range.

IV. SSC Energy Buffer Topologies

There are multiple embodiments of the proposed stacked switched capacitor (SSC) energy buffer [1]. In this paper we present one embodiment and its extensions.

A. 2-6 Bipolar SSC Energy Buffer

Figure 4 shows an example embodiment of the stacked switched capacitor energy buffer: the 2-6 bipolar SSC energy buffer. This topology has two backbone capacitors, C_{11} and C_{12}; six supporting capacitors, C_{21}, C_{22}, C_{23}, C_{24}, C_{25}, and C_{26}; and twelve switches, S_{11}, S_{12}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}, S_{h1}, S_{h2}, S_{h3}, and S_{h4}. This circuit can keep the bus voltage ripple within 10% of nominal value when designed and operated in the manner described below.

The eight capacitors are chosen to have identical capacitance, but different voltage ratings. The two backbone capacitors, C_{11} and C_{12}, have voltage rating of $1.6V_{\text{nom}}$, where V_{nom} is the nominal value of the bus voltage (V_{bus}). The voltage rating of the six supporting capacitors is as follows: $0.6V_{\text{nom}}$ for C_{21}, $0.5V_{\text{nom}}$ for C_{22}, $0.4V_{\text{nom}}$ for C_{23}, $0.3V_{\text{nom}}$ for C_{24}, $0.2V_{\text{nom}}$ for C_{25} and $0.1V_{\text{nom}}$ for C_{26}. A precharge circuit (not shown in Fig. 4, but discussed in section V-B) ensures that the following initial voltages are placed on the eight capacitors: $0.4V_{\text{nom}}$ on C_{11}, $0.4V_{\text{nom}}$ on C_{12}, $0.5V_{\text{nom}}$ on C_{21}, $0.4V_{\text{nom}}$ on C_{22}, $0.3V_{\text{nom}}$ on C_{23}, $0.2V_{\text{nom}}$ on C_{24}, $0.1V_{\text{nom}}$ on C_{25}, and 0V on C_{26}.

Figure 5 shows the switch states, the capacitor voltages and the resulting bus voltage for the 2-6 bipolar SSC energy buffer over a complete charge and discharge cycle. When the energy buffer starts charging up from its minimum state of charge, S_{h1}, S_{h4}, S_{21} and S_{11} are turned on with all the other switches turned off. In this state, C_{11} and C_{21} are connected in series and charged until the bus voltage rises from $0.9V_{\text{nom}}$ to $1.1V_{\text{nom}}$. At this instant the voltage of C_{21} (V_{21}) reaches $0.6V_{\text{nom}}$ and the voltage of C_{11} (V_{11}) reaches $0.5V_{\text{nom}}$. Then S_{21} is turned off and S_{22} is turned on; and the bus voltage drops back down to $0.9V_{\text{nom}}$. Then as the charging continues, the voltage of C_{22} rises to $0.5V_{\text{nom}}$ and the voltage of C_{11} reaches $0.6V_{\text{nom}}$ and the bus voltage again reaches $1.1V_{\text{nom}}$. Next S_{22} is turned off, S_{23} is turned on and C_{23} is charged. This process is repeated until C_{26} is charged. At this stage all the supporting capacitors are at their maximum voltage; the voltage of the backbone capacitors is: V_{nom} on C_{11} and $0.4V_{\text{nom}}$ on C_{12}; and the bus voltage is $1.1V_{\text{nom}}$. Next S_{h1} and S_{h4} are turned off, and S_{h3} and S_{h2} are turned on. This connects C_{26}, and the other supporting capacitors, in reverse orientation with C_{11} and the bus voltage again drops to $0.9V_{\text{nom}}$. Now C_{11} can continue to charge up through the now reverse-connected supporting capacitors through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through C_{26}, then through C_{25}, and so on until finally through C_{21}. At this stage C_{11} is fully charged to $1.6V_{\text{nom}}$ and charging of C_{12} must begin. For this the h-bridge switches are again toggled (i.e., S_{h3} and S_{h2} are turned off, and S_{h1} and S_{h4} are turned on), S_{11} is turned off and S_{12} is turned on. The charging process for C_{12} is identical to the charging process for C_{11}, as shown in Fig. 5. During the discharge period, the capacitors C_{11} and C_{12} are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period.

Throughout the charging and discharging period of this energy buffer, the bus voltage stays within the range $0.9V_{\text{nom}}$-$1.1V_{\text{nom}}$. Hence, the 2-6 bipolar SSC energy buffer operating in this manner has a bus voltage ripple ratio (R_v) of 10%. Furthermore, it has an energy buffering ratio (Γ_{b}) of 79.6%.

B. n-m Bipolar SSC Energy Buffer

The capacitors that buffer most of the energy in the circuit of Fig. 4 are the backbone capacitors C_{11} and C_{12}. Therefore, by adding additional backbone capacitors in parallel with C_{11} and C_{12} the energy buffer could potentially achieve better buffering performance. The number of supporting capacitors can also be changed. To evaluate the impact of the number of backbone and supporting capacitors on the performance of the energy buffer, the topology of Fig. 4 is extended by incorporating n backbone capacitors and m supporting capacitors, as shown in Fig. 6. The energy buffering ratio for this n-m bipolar SSC energy buffer (with n backbone capacitors of equal value C_1 and m supportive capacitors of equal value C_2) is given by:

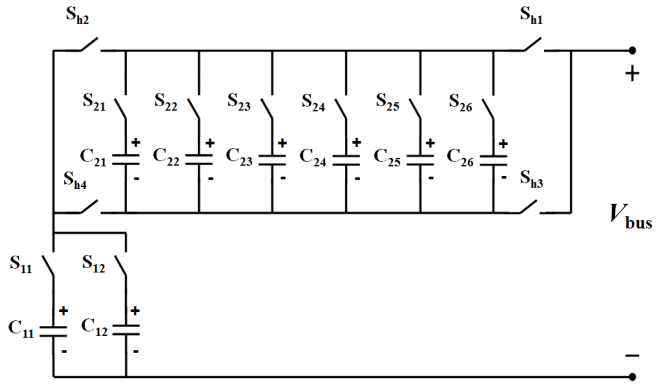


Fig. 4: An example embodiment of the SSC energy buffer architecture: the 2-6 bipolar SSC energy buffer. This circuit has two backbone capacitors C_{11} and C_{12} and six supporting capacitors C_{21} to C_{26} and twelve switches. Precharge and control circuits are not shown.

$$\Gamma_{\rm b} = \frac{nC_1(1+2mR_v\frac{C_2}{C_1+C_2})^2 - (1-2mR_v\frac{C_2}{C_1+C_2})^2}{nC_1(1+2mR_v\frac{C_2}{C_1+C_2})^2 + C_2(1+2^2+...+m^2)R_v^2}. \quad (4)$$

Figure 7 shows the variation in energy buffering ratio, $\Gamma_{\rm b}$, (with C_1 equal to C_2) as a function of the number of backbone capacitors n and the number of supporting capacitors m for three different values of voltage ripple ratio R_v. These plots indicate that there is an optimal number of supporting capacitors that should be used for a given number of backbone capacitors in order to maximize the energy buffering ratio. Note that this optimal number of supporting capacitors depends on the value of allowed voltage ripple ratio.

These plots can be used to select the optimal number of backbone and supporting capacitors to maximize the energy buffering ratio for a given bus voltage ripple ratio. If a larger voltage ripple ratio is allowed, a high energy buffering ratio can be achieved with fewer backbone and supporting capacitors. For a fixed number of backbone capacitors, a lower voltage ripple ratio requires a larger number of supporting capacitors if maximum energy buffering is to be achieved. However, increasing the number of supporting capacitors also increases the complexity of the circuit and the switching frequency of the switches associated with the supporting capacitors (S_{21}-S_{2m}).

For an R_v of 10% with 2 backbone capacitors, the optimal number of supporting capacitors is 6 (see Fig. 7(b)); hence our choice of the 2-6 bipolar SSC energy buffer discussed earlier to meet the 10% voltage ripple requirement. Note that for an R_v of 10%, with 8 backbone and 8 supporting capacitors, an energy buffering ratio of 91.6% can be achieved. Hence, the SSE energy buffer achieves performance similar to the 8-6-5-4-3 parallel-series switched capacitor circuit of [10] with only 16 capacitors and 20 switches instead of 120 capacitors and 41 switches.

V. Prototype Design

To validate the proposed concept we have designed and built a prototype of the 2-6 bipolar SSC energy buffer, similar to the one described in Section IV-A and shown in Fig. 4. The

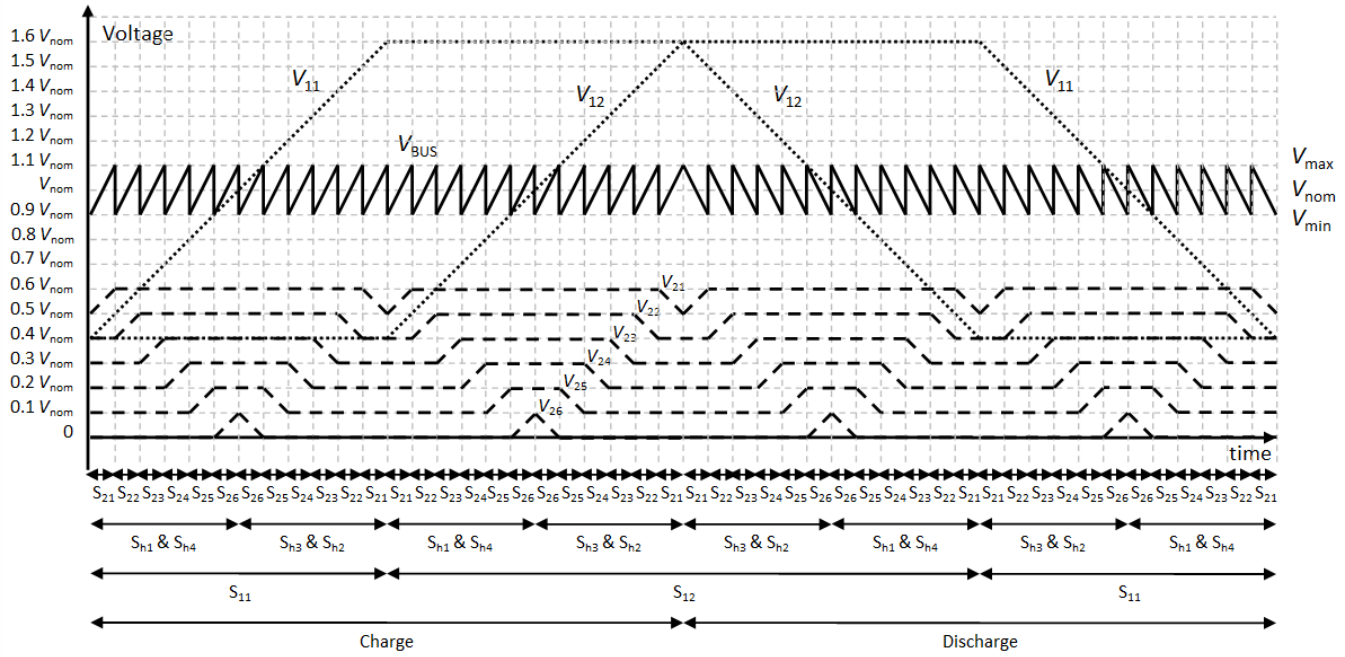


Fig. 5: Switch states, individual capacitor voltages, and resulting bus voltage over a charge and discharge cycle of the 2-6 bipolar SSC energy buffer of Fig. 4.

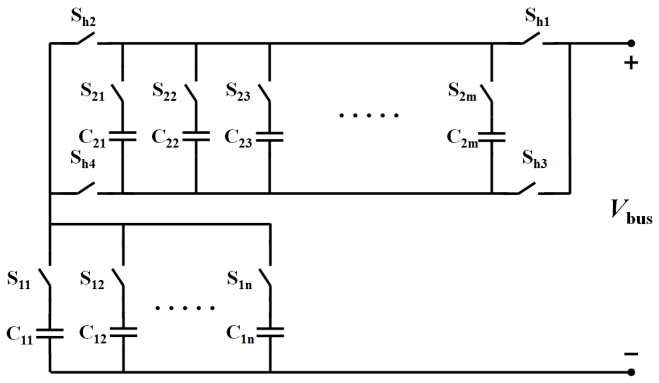


Fig. 6: The n-m bipolar SSC energy buffer. The circuit has n backbone capacitors, m supporting capacitors and (n+m+4) switches.

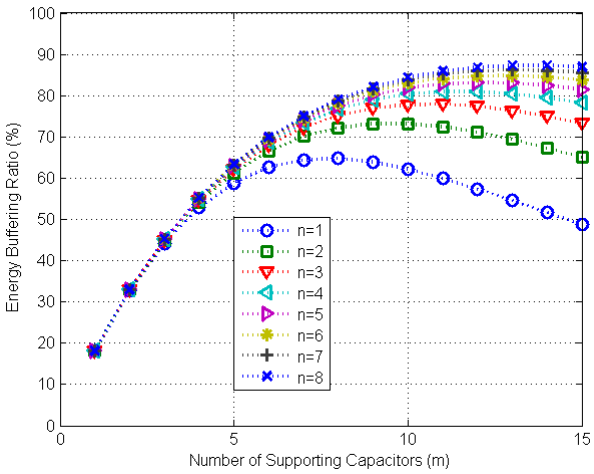
TABLE I: Design specifications for the 2-6 bipolar SSC energy buffer prototype.

Design Specification	Value
Maximum load power ($P_{\text{load(max)}}$)	135 W
Bus voltage (V_{bus})	320 V
Voltage ripple ratio (R_v)	10%

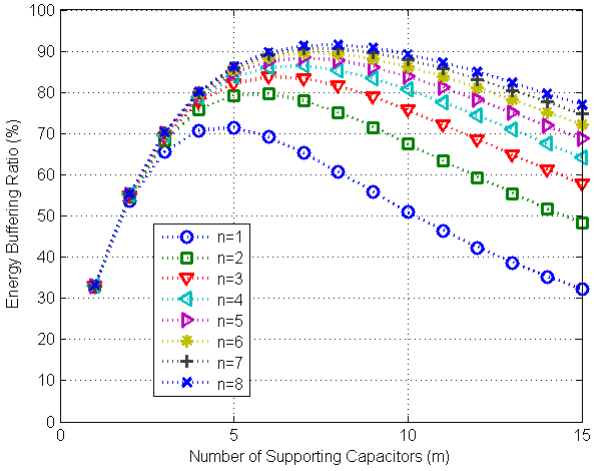
prototype is designed as the energy buffer for a power factor correction (PFC) front-end of a two-stage single-phase ac to dc power converter as shown in Fig. 8. The SSC energy buffer replaces the electrolytic capacitor normally connected at the output of the PFC. To simplify our implementation, a load resistor is used in place of the second-stage dc-dc converter. The SSC energy buffer is designed to meet a 10% bus voltage ripple ratio requirement on a 320 V dc bus with a maximum load of 135 W, as listed in Table I.

The PFC used for this prototype is a 400 W evaluation board from STMicroelectronics that uses their transition-mode PFC controller (L6562A). This controller operates the boost PFC at the boundary between continuous and discontinuous conduction mode by adjusting the switching frequency. The evaluation board has a 330 μF electrolytic capacitor at the output of the PFC, and according to the PFC datasheet can maintain a voltage ripple ratio of 2.5%, while supplying a 400 W load at a bus voltage of 400 V. We have experimentally verified that a 40 μF electrolytic capacitor is sufficient to support 135 W of output power with 10% voltage ripple ratio. The total volume of the 40 μF, 450 V electrolytic capacitor used for this verification is approximately 9 cm^3.

The energy buffer that replaces this electrolytic capacitor consists of three functional blocks: the energy buffer power circuit, the precharge circuit and the control unit, as shown in Fig. 8. In addition, the energy buffer needs to provide a feedback signal to the PFC for its proper operation. The design of each of these four elements is discussed below.



(a)



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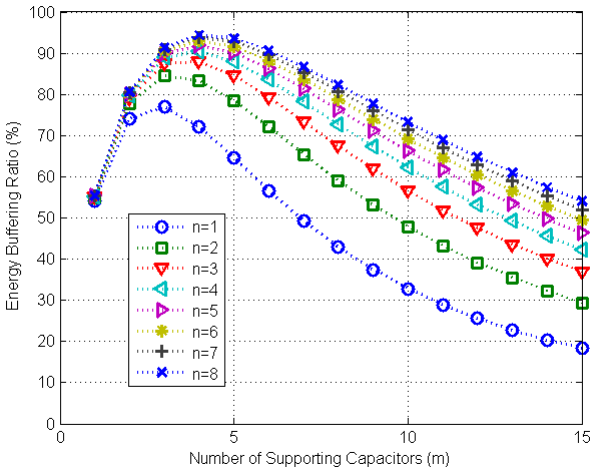

(c)

Fig. 7: Energy buffering ratio (Γ_{b}) as a function of the number of backbone capacitors n and number of supporting capacitors m for different values of voltage ripple ratio: (a) $R_v = 5\%$, (b) $R_v = 10\%$ and (c) $R_v = 20\%$.

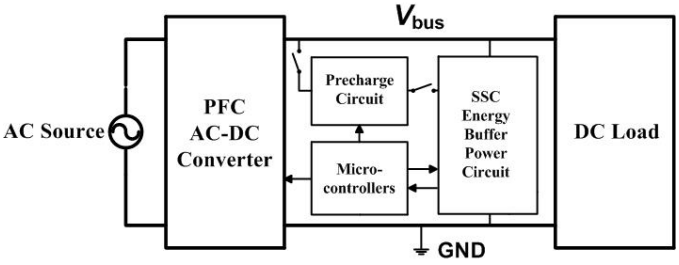

Fig. 8: Block diagram of the prototype setup consisting of a power factor correction (PFC) ac-dc converter, a dc load and the prototyped SSC energy buffer. The prototyped SSC energy buffer consists of: the SSC energy buffer power circuit, the precharge circuit, and the control unit.

A. Energy Buffer Power Circuit

As shown in Fig. 7(b), to achieve a voltage ripple ratio of 10% with a two-backbone-capacitor (n=2) bipolar SSC energy buffer, the optimal number of supporting capacitors is six, (i.e., m=6). Hence in the prototype, the electrolytic capacitor is replaced by a 2-6 bipolar SSC energy buffer. To meet the 10% voltage ripple requirement at the 320 V bus voltage and the 135 W output power level, the eight capacitors of the SSC energy buffer have to be 2.2 μF each. The required voltage rating of these film capacitors is different and ranges from 32 V to 512 V as discussed in section IV. However, for simplicity and to provide adequate safety margin, 700 V film capacitors are used as the two backbone capacitors and 250 V capacitors are used as the six supporting capacitors. All the switches are implemented using silicon power MOSFETs. Switches S_{11} S_{12}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25} and S_{26} are implemented with reverse voltage blocking capability.

B. Precharge Circuit

An important part of the SSC energy buffer is the precharge circuit. When the system starts, the precharge circuit draws power from the PFC to charge the individual capacitors of the energy buffer to the desired initial voltage levels. The precharge circuit designed here uses a linear regulator operated as a current source as shown in Fig. 9. The linear regulator used is Supertex's LR8 with a maximum output current of 20 mA. The linear regulator can be disconnected from the energy buffer power circuit by two isolating switches $S_{\rm p1}$ and $S_{\rm p2}$.

The precharge circuit is controlled by an ATMEL ATmega2560 microcontroller. The flow chart of the precharge control is shown in Fig. 10. A scaled down version of the voltage across each capacitor is compared with a specified reference provided by the microcontroller through a digital to analog converter (DAC). The results of the comparison are fed back to the microcontroller to trigger an interrupt.

During precharge, the microcontroller turns the switches on or off appropriately to connect the current source to the capacitor that needs to be charged. The states (on or off) of the switches for charging a particular capacitor during

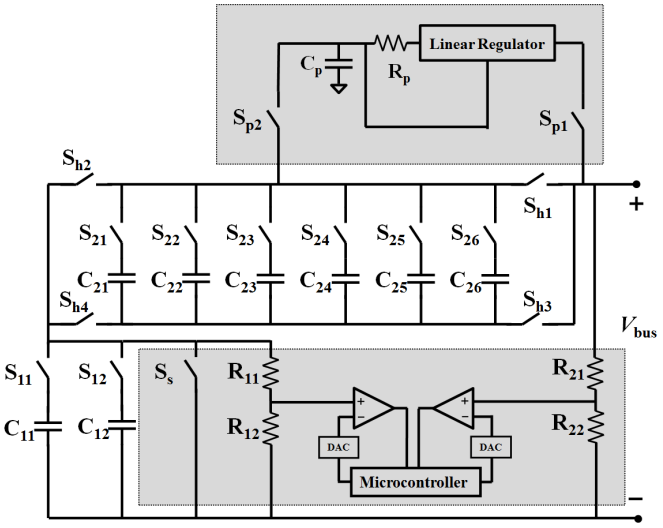

Fig. 9: Precharge circuit (shaded regions) for the 2-6 bipolar SSC energy buffer.

the precharge period are shown in Table II. First $S_{\rm p1}$, $S_{\rm p2}$, S_{21}, $S_{\rm h4}$ and $S_{\rm s}$ are turned on, and all the other switches are turned off to charge C_{21}. The microcontroller senses the voltage of C_{21} (through the voltage divider formed by R_{21} and R_{22}) and compares it with the specified precharge voltage ($0.5V_{\rm nom}$=160 V). Once the voltage of C_{21} reaches 160V, S_{21} is turned off and S_{22} is turned on to charge C_{22} to its specified precharge level. Similarly, C_{23}, C_{24}, C_{25} and C_{26} are charged one at a time to their designed initial level. Once C_{26} is charged, S_{26}, $S_{\rm h4}$ and $S_{\rm s}$ are turned off, and $S_{\rm h2}$ and S_{11} are turned on to charge C_{11}. Now the microcontroller senses the voltage of C_{11} (through the voltage divider formed by R_{11} and R_{12}) and compares it with the specified precharge voltage ($0.4V_{\rm nom}$=128 V). Once the voltage of C_{11} is larger than 128 V, S_{11} is turned off and S_{12} is turned on to charge C_{12}. Once all the capacitors are precharged, the precharge circuit is disconnected from the SSC energy buffer by switches $S_{\rm p1}$ and $S_{\rm p2}$, and the energy buffer enters normal operation.

C. Control

The normal operation of the energy buffer is also controlled by a state machine implemented in the ATMEL ATmega2560 microcontroller. The state machine controls the state (on or off) of the twelve switches in the SSC energy buffer power circuit. The state machine has a total of 24 states, with each state corresponding to a unique and valid combination of the states of the twelve switches, as shown in Table III.

The flow chart of the normal operation mode control logic of the energy buffer is shown in Fig. 10. In this flow chart, s denotes the current state of the state machine. The energy buffer starts normal operation in state 1 (i.e., s=1), which corresponds to minimum energy stored in the buffer, and starts to charge up. Once the bus voltage reaches the maximum allowed voltage, $1.1V_{\rm nom}$ (352 V), the $\widehat{\rm UP}$ interrupt is triggered and the

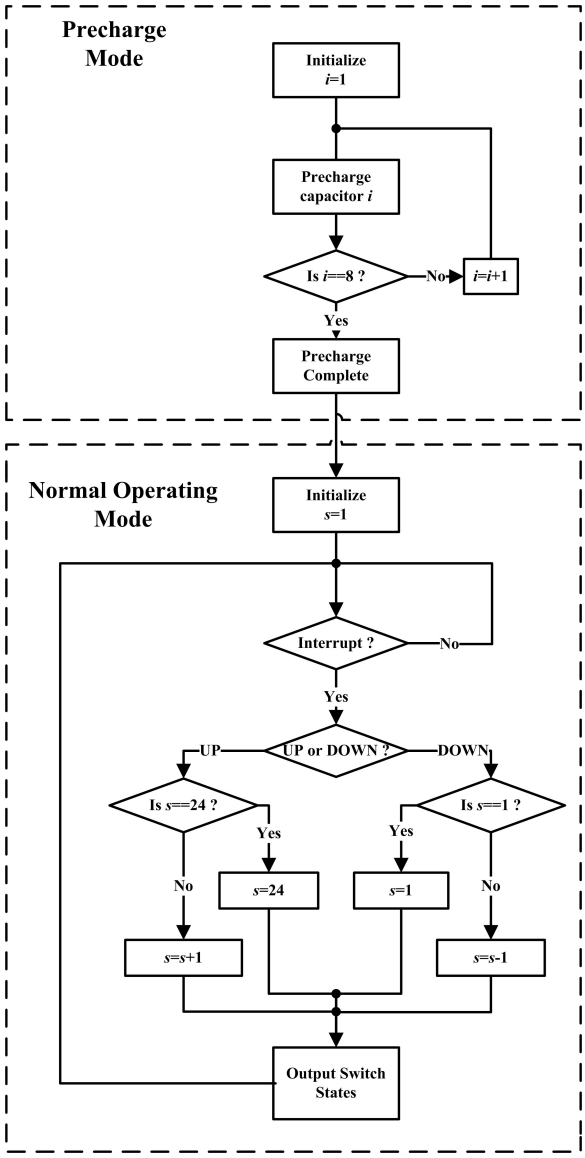

Fig. 10: Flow chart showing the control logic during precharge and normal operation of the 2-6 bipolar SSC energy buffer.

state is incremented by one (i.e., s=s+1). The microcontroller turns the appropriate power switches on or off to match the configuration for the new state. This drops the bus voltage back to $0.9V_{\rm nom}$ (288 V), and the charging of the energy buffer continues until it again reaches the upper voltage limit. This process is repeated as long as the energy buffer is being charged and it has not reached state 24. Once the energy buffer has reached state 24, the state machine stays in state 24 even if it receives additional $\widehat{\rm UP}$ interrupts. This helps protect the energy buffer to a certain extent in case load power exceeds its design specifications. During this overload condition the energy buffer looks like a 1.1 μF capacitor to the external system. The energy buffer will return to normal operation once the load power returns to the design range.

During discharge of the energy buffer, the $\widehat{\rm DOWN}$ interrupt is triggered when the bus voltage reaches the minimum allowed voltage, $0.9V_{\rm nom}$ (288 V). This decrements the state by one (i.e., s=s-1). The microcontroller turns the appropriate power switches on and off to match the configuration for the new state and the bus voltage increases to $1.1V_{\rm nom}$ (352 V). This process is repeated each time the bus voltage reaches the lower voltage limit until it has reached state 1. As in the case of charging, to protect the energy buffer, the state machine stays in state 1 even if it receives additional $\widehat{\rm DOWN}$ interrupts.

Hence during normal operation at maximum power, the state machine will iterate through states 1 through 24 in a sequential manner, first going from 1 to 24 as it charges, and then returning from 24 to 1 as it discharges, and this process is repeated as long as the energy buffer is in normal operation.

TABLE II: State of the switches during precharge of each of the eight capacitors of the 2-6 bipolar SSC energy buffer. Blank cell indicates the switch is off.

	$\mathbf{C_{11}}$	$\mathbf{C_{12}}$	$\mathbf{C_{21}}$	$\mathbf{C_{22}}$	$\mathbf{C_{23}}$	$\mathbf{C_{24}}$	$\mathbf{C_{25}}$	$\mathbf{C_{26}}$
$\mathbf{S_{11}}$	on							
$\mathbf{S_{12}}$		on						
$\mathbf{S_{21}}$			on					
$\mathbf{S_{22}}$				on				
$\mathbf{S_{23}}$					on			
$\mathbf{S_{24}}$						on		
$\mathbf{S_{25}}$							on	
$\mathbf{S_{26}}$								on
$\mathbf{S_{h1}}$								
$\mathbf{S_{h2}}$	on	on						
$\mathbf{S_{h3}}$								
$\mathbf{S_{h4}}$			on	on	on	on	on	on
$\mathbf{S_{p1}}$	on	on	on	on	on	on	on	on
$\mathbf{S_{p2}}$	on	on	on	on	on	on	on	on
$\mathbf{S_s}$			on	on	on	on	on	on

D. Artificial Voltage Feedback

In a conventional system with an energy buffering electrolytic capacitor at the output of the PFC, the PFC uses the bus voltage (i.e., the voltage across the buffering capacitor) to control its output current. The bus voltage is scaled down by a resistive divider and fed back to the PFC control chip. Since the bus voltage is a good measure of the energy stored in the capacitor, this feedback mechanism ensures that the average output power from the PFC matches the power drawn by the dc load and the system stays stable. However, when the electrolytic capacitor is replaced with the SSC energy buffer, the bus voltage is no longer a true representation of the energy stored in the energy buffer. Hence, an artificial signal must be generated (and fed back to the PFC control chip) that represents the energy stored in the energy buffer and mimics the bus voltage of the electrolytic capacitor. In our prototype this function is performed by a second ATMEL ATmega2560

TABLE III: States of the twelve switches in the 2-6 bipolar SSC energy buffer corresponding to each of the 24 states of the state machine. Blank cell indicates the switch is off.

States	S_{21}	S_{22}	S_{23}	S_{24}	S_{25}	S_{26}	S_{11}	S_{12}	S_{h1}	S_{h2}	S_{h3}	S_{h4}
1	on						on		on		on	
2		on					on		on		on	
3			on				on		on		on	
4				on			on		on		on	
5					on		on		on		on	
6						on	on		on		on	
7						on	on			on		on
8					on		on			on		on
9				on			on			on		on
10			on				on			on		on
11		on					on			on		on
12	on						on			on		on
13	on							on	on		on	
14		on						on	on		on	
15			on					on	on		on	
16				on				on	on		on	
17					on			on	on		on	
18						on		on	on		on	
19						on		on		on		on
20					on			on		on		on
21				on				on		on		on
22			on					on		on		on
23		on						on		on		on
24	on							on		on		on

microcontroller.

In the precharge mode, the SSC energy buffer behaves simply like two capacitors connected in series. Hence, during this period, the bus voltage reflects the energy stored inside the two capacitors and so the voltage that needs to be fed back is simply a scaled version of the bus voltage.

Once the energy buffer enters normal operating mode, its stored energy increases monotonically as it goes from state 1 to state 24 and then decreases monotonically as it returns to state 1. The energy that gets stored in the energy buffer as it goes from state 1 to state 24 is given by:

$$\Delta E(t) = \sum_{i=1}^{N} \frac{1}{2} C_i (V_i(t)^2 - V_{i0}^2), \tag{5}$$

where N is the total number of capacitors in the energy buffer (eight in the 2-6 bipolar SSC case), C_i is the capacitance of capacitor i, $V_i(t)$ is the voltage of capacitor i at time t, and V_{i0} is the initial voltage of capacitor i after it is precharged. In our prototype all eight capacitors have the same capacitance C_{b} (equal to 2.2 μF). The effective energy in the energy buffer as a function of time is given by[3]:

$$E_{\mathrm{b(eq)}}(t) = \frac{1}{2} C_{\mathrm{eq}} V_{\min}^2 + \Delta E(t), \tag{6}$$

where C_{eq} is an equivalent capacitance for this energy buffer valid while it is operating in normal operating mode, and is given by:

$$C_{\mathrm{eq}} = \frac{2 \int_{\mathrm{t_1}}^{\mathrm{t_2}} p(t)\, \mathrm{d}t}{V_{\mathrm{t_2}}^2 - V_{\mathrm{t_1}}^2}. \tag{7}$$

Here $p(t)$ is the power flowing into the energy buffer, and $V_{\mathrm{t_1}}$ and $V_{\mathrm{t_2}}$ are the voltages at beginning (time t_1) and the end (time t_2) of the charging period, respectively. For our prototype, C_{eq} is equal to 26.4 μF.

Hence, the voltage that needs to be fed back in normal operating mode is given by:

$$V_{\mathrm{fb}}(t) = \sqrt{\frac{C_{\mathrm{eq}} V_{\min}^2 + 2\Delta E(t)}{C_{\mathrm{eq}}}}. \tag{8}$$

[3]Note that $E_{\mathrm{b(eq)}}$ as given by Eq. 6 is not the actual energy in the energy buffer but rather the apparent energy.

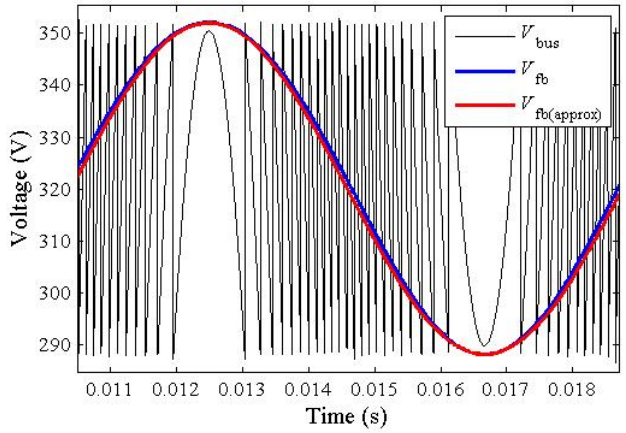

Fig. 11: Comparisons between the accurate ($V_{\rm fb}$) and approximate ($V_{\rm fb(approx)}$) artificial feedback voltages for a sinusoidal energy buffer terminal current.

This feedback signal reflects the apparent energy stored in the energy buffer.

While the expression given by Eq. 8 for the normal operating mode feedback signal can be implemented, it is simpler to implement an approximation to this expression which works just as well within the resolution of our 8-bit digital to analog converter (DAC). The approximate feedback signal is derived assuming that the feedback voltage signal is linear between two switching instances and the current flowing into or out of the energy buffer is constant (i.e., current has a square profile). This approximate feedback voltage is given by:

$$V_{\rm fb(approx)}(t) = V_{\rm min} + (V_{\rm max} - V_{\rm min})\frac{i}{24} + (V_{\rm bus}(t) - V_{\rm min})\frac{C_{\rm b}}{2C_{\rm eq}}. \quad (9)$$

Figure 11 shows that this approximate feedback signal matches the more accurate one quite well even when the terminal current of the energy buffer is sinusoidal. It has been experimentally demonstrated that the slower outer control loop of the PFC works well with this approximate feedback signal.

VI. Experimental Results

The prototype 2-6 bipolar SSC energy buffer has been successfully tested with the PFC and a load resistor up to power levels of 135 W. The measured waveforms from the energy buffer operated at 100 W are shown in Fig. 12. As the energy flows into and out of the energy buffer at 120 Hz, the backbone capacitors charge and discharge over a wide voltage range. However, this voltage variation is compensated for by the supporting capacitors and the bus voltage remains within the 300 V and 370 V range. Hence, it meets the voltage ripple ratio design requirement of 10%.

A PLECS[4] model for this energy buffer has also been built and simulated. In the simulation the terminal current of the energy buffer is assumed to be sinusoidal. Comparing Fig. 12 and Fig. 13, there is a reasonably close match between the experimental and simulated waveforms. The main difference is due to the fact that in the simulation the terminal current of the energy buffer is assumed to be perfectly sinusoidal, while in the case of the experimental setup that is not exactly the case. Figure 12(b) shows the state of the state machine. As can be seen, the state machine goes down to state 4 and up to state 24. The state machine does not go into states 1, 2 and 3 in its normal operating mode as the load power is not large enough to discharge it down to its minimum stored energy level. The circuit behaves as designed, and validates the concept of the stacked switched capacitor energy buffer.

[4]PLECS is a simulation tool for power electronic circuits.

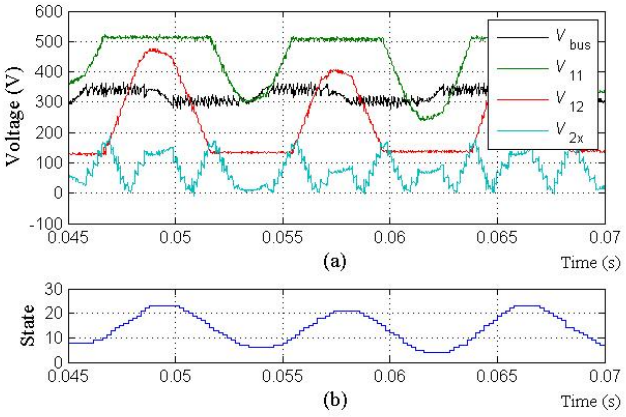

Fig. 12: Measured waveforms of (a) bus voltage ($V_{\rm bus}$), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine.

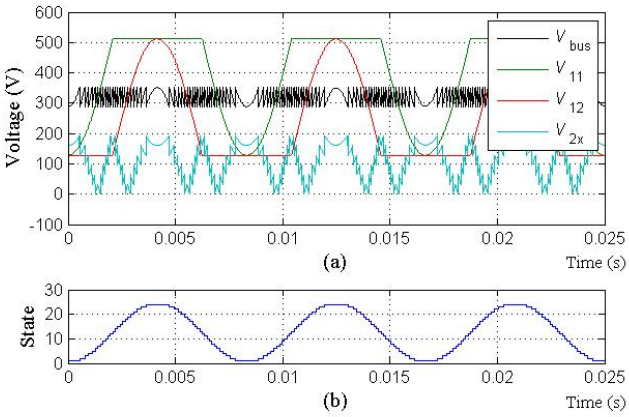

Fig. 13: Simulated waveforms of (a) bus voltage ($V_{\rm bus}$), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (V_{2x}), and (b) corresponding state (1-24) of the state machine.

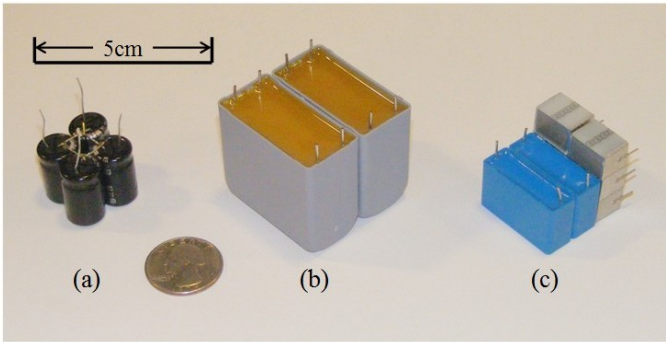

Fig. 14: Relative size of passive energy storage components in different energy buffer architectures: (a) electrolytic-capacitor-only (9 cm^3) (b) film-capacitor-only (65 cm^3) and (c) film-capacitor-based SSC (20 cm^3) energy buffer.

The round trip efficiency of the prototype 2-6 bipolar SSC energy buffer was measured for the 80 W to 123 W load power range. This efficiency stays above 94.4% throughout this power range. The peak measured efficiency is 95.5%. The measured efficiency does not include losses in the control and gate drive circuit as these parts were not designed for high efficiency. The control and gate drive losses can be minimized by appropriately designing these parts of the energy buffer.

The prototype energy buffer successfully replaces the function of the electrolytic capacitor at the output of the PFC. Its passive volume of 20 cm^3, which is much smaller than the 65 cm^3 needed for a film-capacitor-only solution, is only about twice the size of the 9 cm^3 electrolytic capacitor it replaces, as shown in Fig. 14. Hence, the SSC energy buffer achieves energy buffering density comparable to an electrolytic capacitor while providing much longer life.

VII. Conclusions and Future Work

This paper introduces a stacked switched capacitor (SSC) architecture for dc-link energy buffering applications, including buffering between single-phase ac and dc. This architecture utilizes the energy storage capability of capacitors more effectively than previous designs, while maintaining the bus voltage within a narrow range. This enables the energy buffer to achieve higher effective energy density and reduce the volume of the capacitors. A prototype 2-6 bipolar SSC energy buffer using film capacitors designed for a 320 V bus with 10% voltage ripple and able to support a 135 W load has been built and tested. It is shown that the SSC energy buffer can successfully replace limited-life electrolytic capacitors with much longer life film capacitors, while maintaining volume and efficiency at a comparable level.

As future work it would be valuable to evaluate the use of ceramic capacitors, in place of film capacitors, as the supporting capacitors in the SSC architecture. Also there are other implementations of the stacked switched capacitor energy buffer architecture. Some of these can also be explored in the future.

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References

[1] M. Chen, *Stacked Switched Capacitor Energy Buffer*, SM Thesis, Dept. of EECS, Massachusetts Institute of Technology, Cambridge, MA, Dec. 2011.

[2] A.C. Kyritsis, E.C. Tatakis, "A Novel Parallel Active Filter for Current Pulsation Smoothing on Single Stage Grid-Connected AC-PV Modules," *Proceedings of the 11th European Conference on Power Electronics and Applications (EPE)*, Aalborg, Denmark, Sep. 2007.

[3] A.C. Kyritsis, N.P. Papanikolaou, and E.C. Tatakis, "Enhanced Current Pulsation Smoothing Parallel Active Filter for Single Stage Grid Connected AC-PV Modules," *Proceedings of the International Power Electronics and Motion Control Conference (EPE-PEMC)*, pp. 1287-1292, Poznan, Poland, Sep. 2008.

[4] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-Type Single-Phase Utility-Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1264-1272, Sep. 2006.

[5] S.B. Kjaer and F. Blaabjerg, "Design Optimization of a Single-Phase Inverter for Photovoltaic Applications," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 1183-1190, Acapulco, Mexico, Jun. 2003.

[6] P.T. Krein and R.S. Balog, "Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port," *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 620-625, Washington, DC, Feb, 2009.

[7] B. J. Pierquet and D. J. Perreault, "Single-Phase Photovoltaic Inverter Topology with Series-Connected Power Buffer," *Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 2010.

[8] A. Rufer and P. Barrade, "A Supercapacitor-Based Energy Storage System for Elevators with Soft Commutated Interface," *IEEE Transactions on Industry Applications*, vol. 38, issue 5, pp. 1151-1159, Sept-Oct, 2002.

[9] S. Sugimoto, S. Ogawa, H. Katsukawa, H. Mizutani and M. Okamura, "A Study of Series-Parallel Changeover Circuit of a Capacitor Bank for an Energy Storage System Utilizing Electric Double-layer Capacitors," *Electrical Engineering in Japan*, vol. 145, pp. 33-42, 2003.

[10] X. Fang, N. Kutkut, J. Shen and I. Batarseh, "Ultracapacitor Shift Topologies with High Energy Utilization and Low Voltage Ripple," *International Telecommunications Energy Conference (INTELEC)*, Orlando, FL, June 2010.

[11] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*, pp. 126, Addison-Wesley, New York, 1991.

[12] R.C.N. Pilawa-Podgurski, D. Giuliano, and D.J. Perreault, "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 4008-4015, Rhodes, Greece, Jun. 2008.