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Enhanced Bipolar Stacked Switched Capacitor Energy Buffers

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***Abstract*—The Stacked Switched Capacitor (SSC) energy buffer is a recently proposed architecture for buffering energy between single-phase ac and dc. When used with film capacitors, it can increase the life of grid-interfaced power converters by eliminating limited-life electrolytic capacitors while maintaining comparable energy density. This paper introduces an enhanced version of the bipolar SSC energy buffer that achieves a higher effective energy density and round-trip efficiency, while maintaining the same bus voltage ripple ratio as the original design. Furthermore, the enhanced buffer uses fewer capacitors and switches than the original design. The enhancement in performance is achieved by modifying the control and switching patterns of the buffer switches. A prototype enhanced SSC energy buffer, designed for a 320 V bus and a 135 W load, has been built and tested. The design methodology and experimental results for the enhanced SSC energy buffer are presented and compared with the original design. The paper also presents a comparison of unipolar and bipolar SSC energy buffers. It is shown that while bipolar designs are superior in terms of effective energy density at low ripple ratios, unipolar designs can outperform bipolar designs at high ripple ratios.**

I. INTRODUCTION

Power conversion systems that interface between single-phase ac and dc at high power factor (such as power supplies, solar inverters, electric vehicle chargers and off-line LED drivers) need energy storage to provide buffering between the constant power desired by a dc source or load and the continuously-varying power desired for a single-phase ac system. The size of the energy buffer is proportional to the system average power and the line period, and cannot be reduced by simply increasing the switching frequency of the converter. While electrolytic capacitors are generally used to provide high-density energy storage for buffering, their temperature constraints, limited-life and reliability are a concern. Film capacitors have much longer life and higher reliability, but an order of magnitude lower peak energy density. Therefore, for long-life and compact grid-interface systems there is a strong interest in developing energy buffers based on film capacitors that provide effective energy density comparable to electrolytic capacitors.

Unlike electrolytic capacitors, film capacitors can be efficiently charged and discharged over a wide voltage range even at reasonably high frequencies. By using a larger fraction of the energy storage capability of a capacitor than is possible with electrolytic capacitors, film-capacitor-based energy buffers can be designed with effective energy densities comparable to electrolytics.

In the past, multiple approaches have been employed to effectively utilize film capacitors while maintaining a desired narrow-range bus voltage. These include approaches using bi-directional dc-dc converters [1,2], energy buffers incorporated into the operation of the power stage [3-6], and switched capacitor circuits that reconfigure capacitors between parallel and series combinations [7-9]. Approaches that rely on an extra bi-directional dc-dc converter as an interface between the main power converter and the energy buffer result in considerable additional losses when high power density is to be maintained. Incorporating the energy buffer into the operation of the main converter partially reduces these losses, but imposes constraints on the operation of the converter. Parallel-series reconfigurable switched capacitor circuits do not have these handicaps, but are complex as they need a very large number of switches and capacitors in order to maintain a narrow-range bus voltage while achieving high energy utilization. Recently, a new energy buffer architecture—the Stacked Switched Capacitor (SSC) energy buffer—has been proposed that partly overcomes the efficiency, flexibility and complexity-related shortcomings of the previous designs. This architecture, including both unipolar and bipolar variants [10,11], is useful in overcoming the lifetime and temperature limitations of electrolytic capacitors.

In this paper, we introduce an enhanced version of the bipolar SSC energy buffer that achieves improved performance in terms of effective energy density and round-trip efficiency using fewer capacitors and switches, while maintaining the same bus voltage ripple ratio. The remainder of this paper is organized as follows: Section II describes the operational principle of the SSC energy buffer. The

enhanced bipolar SSC energy buffer is described in section III. Section IV compares the performance of the enhanced bipolar design with other implementations of the SSC energy buffer, including unipolar designs. The design details of the enhanced bipolar SSC energy buffer tested in this paper are provided in section V. Section VI presents the experimental results for the enhanced design and compares them to those of the original bipolar SSC energy buffer. Finally, conclusions are presented in section VII.

II. SSC Energy Buffer: Operational Principle

The SSC energy buffer has two series-connected blocks, each comprising capacitors and switches. It works on the principle that while the voltages of individual capacitors and individual blocks can vary over a wide range, the voltage at the buffer port remains constrained to a desired narrow range by having the voltage variations of the two blocks compensate for each other.

There are many possible implementations of the SSC energy buffer architecture. One implementation known as the *n-m* bipolar SSC energy buffer is shown in Fig. 1(a) with *n* (the number of "backbone" capacitors in the lower block) and *m* (the number of "supporting" capacitors in the upper block) equal to 2 and 6, respectively [10]. In this design all the capacitors have equal capacitance, but different voltage ratings. Before the buffer starts normal operation, the capacitors are precharged to specified initial levels using a precharge circuit (not shown in Fig. 1(a)). During normal charge/discharge operation, the buffer operates as depicted by the switching patterns and associated voltage waveforms shown in Fig. 2(a). The buffer has 24 valid switch states and it traverses all 24 states when it is fully charged or fully discharged. In each state, one backbone capacitor and one supporting capacitor are connected in series across the buffer port, and charged (or discharged) by the twice-line-frequency current flowing through them and four series switches. The two backbone capacitors are charged (or discharged) sequentially; each requiring 12 states to fully charge (or discharge). During charging (or discharging) the bus voltage (v_{BUS}) is kept within its allowed range (±10% of nominal bus voltage, V_{NOM}, in this design) by changing the switch states and connecting a different supporting capacitor, with appropriate initial voltage, in series or anti-series with the backbone capacitor. Charging (and discharging) of each backbone capacitor can continue until all the supporting capacitors have been used. Since the switches in this architecture switch only at low multiples of the line frequency, the SSC energy buffer can be very efficient.

Important parameters of a switched capacitor energy buffer are the voltage ripple ratio and the energy buffering ratio. The voltage ripple ratio (R_v) is defined as the ratio of the peak voltage ripple amplitude to the nominal value of the voltage. For example, the bus voltage, v_{BUS}, of Fig. 2(a) which varies between $0.9V_{NOM}$ and $1.1V_{NOM}$ has a ripple ratio of 10%. The energy buffering ratio (Γ_b) is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer. Maximizing the energy buffering ratio for a given required voltage ripple ratio is desired as it ensures better usage of a given amount of capacitor energy capacity. The energy buffering ratio for an *n-m* bipolar SSC energy buffer is given by [10]:

$$\Gamma_b = \frac{n\left[(1+mR_v)^2-(1-mR_v)^2\right]}{n(1+mR_v)^2+(1+2^2+\ldots+m^2)R_v^2}. \quad (1)$$

The bipolar SSC energy buffer can be designed with any number of backbone and supporting capacitors. However, for a given voltage ripple ratio requirement and a given number of backbone capacitors there is an optimal number of supporting capacitors that yields the highest energy buffering ratio, and hence the highest effective energy density for the passive components. For example, for a 10% bus voltage ripple ratio requirement and with 2 backbone capacitors, the optimal design of a bipolar SSC energy buffer is one with 6 supporting capacitors (see Fig. 3).

III. Enhanced Bipolar SSC Energy Buffer

The *n-m* bipolar SSC energy buffer can also be controlled in a slightly different manner. Instead of charging and discharging the backbone capacitors only in series with the

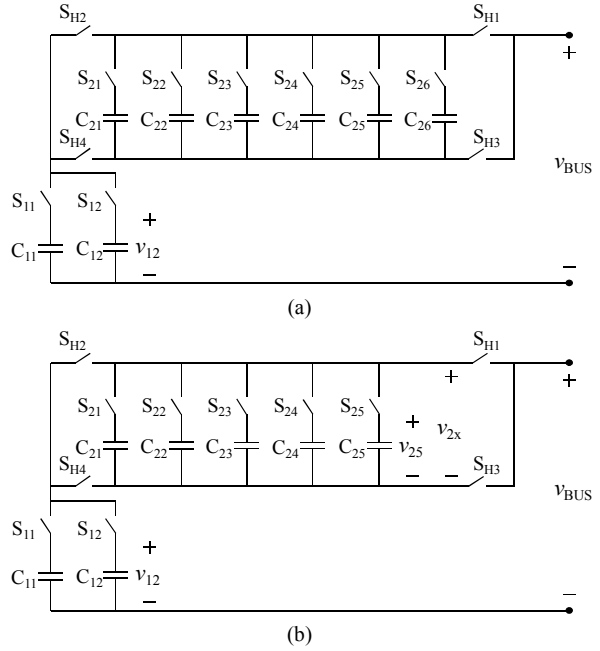

Figure 1. Original and enhanced bipolar SSC energy buffers with two backbone capacitors optimized for 10% bus voltage ripple ratio: (a) The original bipolar SSC energy buffer with two backbone and six supporting capacitors [10], and (b) the enhanced bipolar SSC energy buffer with two backbone and five supporting capacitors. The enhanced design requires fewer supporting capacitors and switches for a given performance level. Precharge and control circuits are not shown.

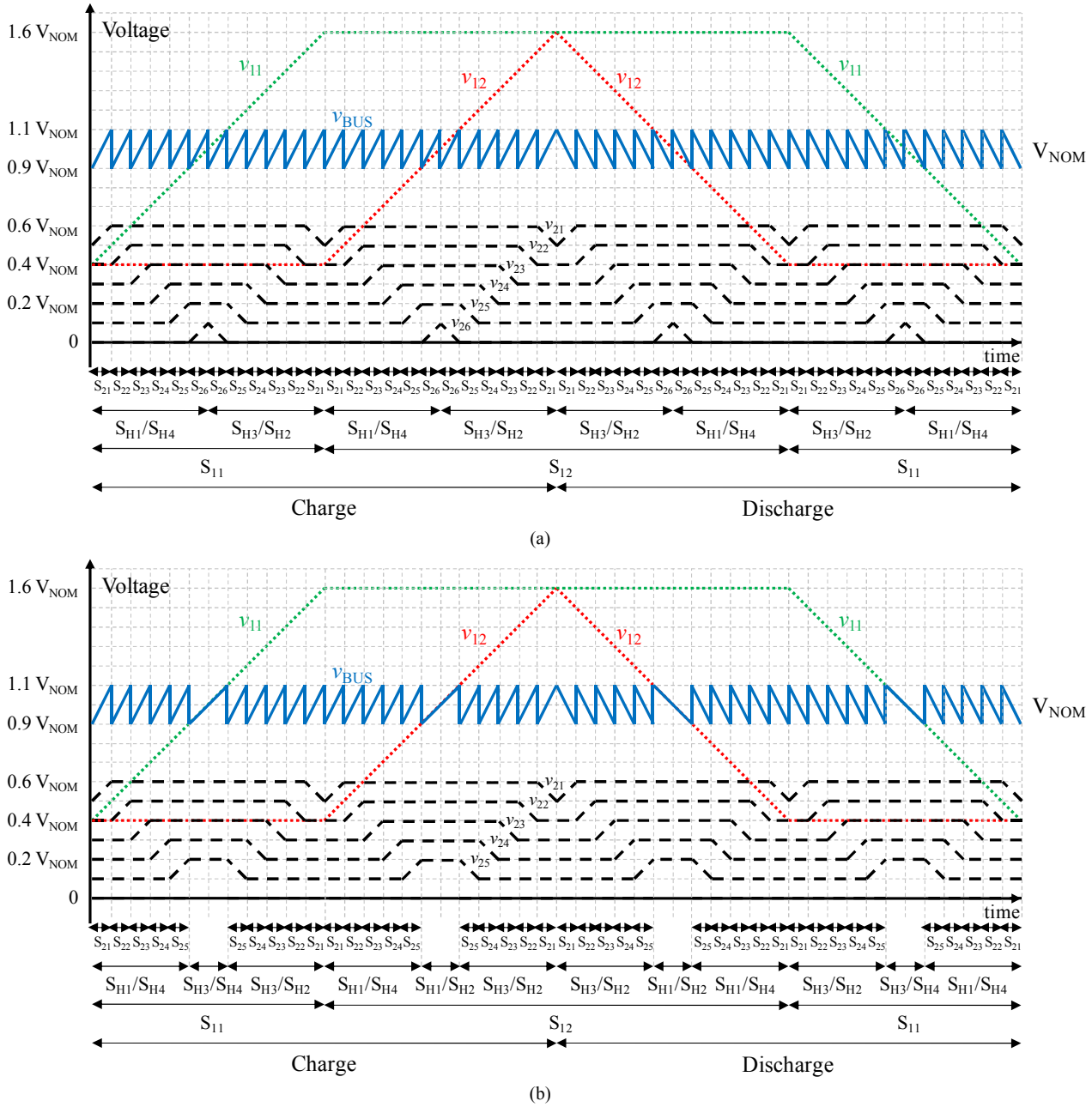

Figure 2. Switch states, individual capacitor voltages, and resulting bus voltage over a charge and discharge cycle of: (a) the original bipolar SSC energy buffer of Fig. 1(a), and (b) the enhanced bipolar SSC energy buffer of Fig. 1(b).

supporting capacitors, a state can be introduced by turning S_{H3} and S_{H4} (or S_{H1} and S_{H2}) on at the same time, during which the backbone capacitor is charged or discharged directly.

Consider the 2-5 enhanced bipolar SSC energy buffer shown in Fig. 1(b). Like the original 2-6 bipolar SSC energy buffer it is designed for a bus voltage ripple ratio of 10%. Its seven capacitors also have identical capacitance, but different voltage ratings. A precharge circuit (not shown in Fig. 1(b)) ensures that the following initial voltages are placed on the seven capacitors: $0.4V_{NOM}$ on C_{11}, $0.4V_{NOM}$ on C_{12}, $0.5V_{NOM}$ on C_{21}, $0.4V_{NOM}$ on C_{22}, $0.3V_{NOM}$ on C_{23}, $0.2V_{NOM}$ on C_{24}, and $0.1V_{NOM}$ on C_{25}.

When the energy buffer starts charging up from its minimum state of charge (as shown in Fig. 2(b)), S_{H1}, S_{H4}, S_{21} and S_{11} are turned on with all the other switches turned off. In this state, C_{11} and C_{21} are connected in series and charged until the bus voltage rises from $0.9V_{NOM}$ to $1.1V_{NOM}$. At this instant the voltage of C_{21} (v_{21}) reaches $0.6V_{NOM}$ and the voltage of C_{11} (v_{11}) reaches $0.5V_{NOM}$. Then S_{21} is turned

off and S_{22} is turned on; and the bus voltage drops back down to $0.9V_{NOM}$. Then, the voltage of C_{22} rises to $0.5V_{NOM}$ and the voltage of C_{11} reaches $0.6V_{NOM}$, and the bus voltage again reaches $1.1V_{NOM}$. Next S_{22} is turned off, S_{23} is turned on and C_{23} is charged. This process is repeated until C_{25} is charged. This charging pattern is identical to that of the original 2-6 bipolar SSC energy buffer, as can be seen by comparing Figs. 2(a) and 2(b). However, the next two states are different: instead of charging C_{11} in series with C_{26}, C_{11} is charged directly by turning off S_{H1} and turning on S_{H3}. This eliminates the need for capacitor C_{26} and switch S_{26} of the original design. This state is maintained until the voltage of C_{11} rises to $1.1V_{NOM}$. After this S_{H4} is turned off and S_{H2} and S_{25} are turned on. Now C_{11} can continue to charge up through the now reverse-connected supporting capacitors through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through C_{25}, then through C_{24}, and so on until finally through C_{21}.

At this stage C_{11} is fully charged to $1.6V_{NOM}$ and charging of C_{12} must begin. For this the H-bridge switches are again toggled (i.e., S_{H3} and S_{H2} are turned off, and S_{H1} and S_{H4} are turned on), S_{11} is turned off and S_{12} is turned on. The charging process for C_{12} is identical to the charging process for C_{11}. The switch states, the capacitor voltages and the resulting bus voltages over a complete charge and discharge cycle are shown in Fig. 2(b). During the discharge period, the capacitors C_{11} and C_{12} are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period.

Throughout the charging and discharging period of this energy buffer, the bus voltage stays within the $0.9V_{NOM}$-$1.1V_{NOM}$ range. Hence, the enhanced 2-5 bipolar SSC energy buffer operated in this manner also has a voltage ripple ratio of 10%. Furthermore, it has an energy buffering ratio of 79.73% which is higher than the energy buffering ratio (79.6%) of the original 2-6 bipolar SSC energy buffer. The original 2-6 bipolar SSC energy buffer has 8 capacitors and 12 switches, while the enhanced 2-5 bipolar SSC energy buffer has 7 capacitors and 11 switches. Hence, the enhanced version achieves the same bus voltage ripple ratio and a slightly better energy buffering ratio with fewer capacitors and switches.

The energy buffering ratio for an enhanced *n*-*m* bipolar SSC energy buffer (with all capacitors having identical capacitance) is given by:

$$\Gamma_b = \frac{n\left[(1+(m+1)R_v)^2-(1-(m+1)R_v)^2\right]}{n(1+(m+1)R_v)^2+(2^2+3^2+\ldots+(m+1)^2)R_v^2}. \qquad (2)$$

This expression is plotted as a function of the number of supporting capacitors (m) for different number of backbone capacitors (n) with 10% voltage ripple ratio in Fig. 3. Figure 3 also plots (as dashed lines) the energy buffering ratio of the original bipolar SSC energy buffer (as given by Eq. (1)). As can be seen from Fig. 3, the enhanced design achieves a slightly higher maximum energy buffering ratio than the original design. Furthermore, it achieves this higher maximum with fewer supporting capacitors than the original design for all values of n.

IV. Comparison With Unipolar SSC Energy Buffers

SSC energy buffers can also be designed without the four bridge switches (S_{H1}, S_{H2}, S_{H3} and S_{H4}), as shown in Fig. 4; such designs are referred to as unipolar designs. Figure 4(a)

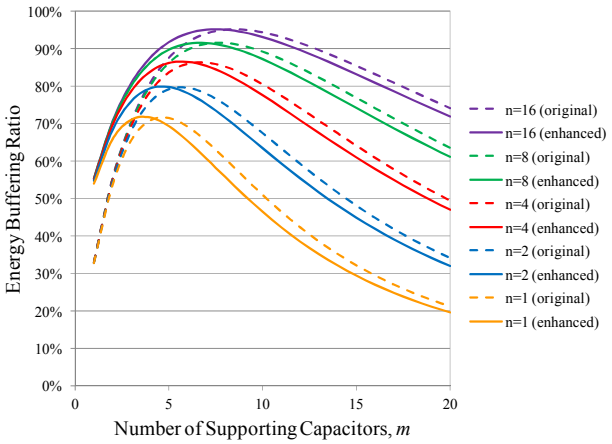

Figure 3. Comparison of energy buffering ratio of the enhanced and the original version of the *n*-*m* bipolar SSE energy buffer with 10% voltage ripple ratio.

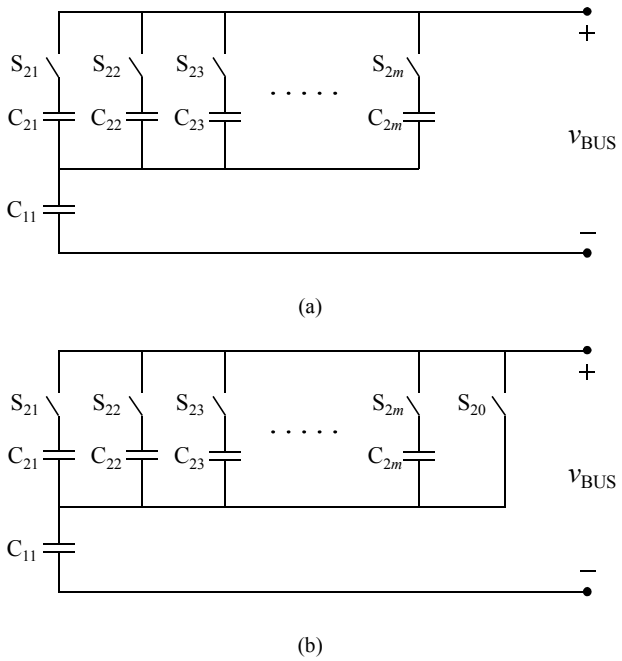

Figure 4. Unipolar SSC energy buffers: (a) 1-*m* unipolar SSC energy buffer and (b) enhanced 1-*m* unipolar SSC energy buffer.

shows the basic 1-*m* unipolar design (with 1 backbone and *m* supporting capacitors), and Fig. 4(b) shows the enhanced 1-*m* unipolar design, which incorporates an additional switch S_{20}. The extra switch in the enhanced unipolar SSC energy buffer allows direct charging of the backbone capacitor, similar to the concept employed in the enhanced bipolar design.

The unipolar SSC energy buffers are attractive as they have fewer switches than bipolar designs, and charging and discharging of the capacitors takes place through one series switch instead of four or three as is the case in the bipolar designs. Hence, unipolar designs can be less expensive and potentially more efficient. However, the unipolar SSC energy buffers can only have one backbone capacitor, as there is no way to discharge the supporting capacitors during a charge cycle and reuse them to support the bus voltage during the charging of any additional backbone capacitors. The energy buffering ratio of the 1-*m* unipolar design is given by:

$$\Gamma_b = 1 - \frac{(1+2^2+3^2+\ldots+(m-1)^2)R_v^2+(1-mR_v)^2}{(1+2^2+\ldots+m^2)R_v^2+1}, \quad (3)$$

while the energy buffering ratio of the enhanced 1-*m* unipolar design is given by:

$$\Gamma_b = 1 - \frac{(1+2^2+3^2+\ldots+m^2)R_v^2+(1-(m+1)R_v)^2}{(2^2+3^2+\ldots+(m+1)^2)R_v^2+(1+R_v)^2}. \quad (4)$$

As in the bipolar SSC energy buffer, there is an optimal number of supporting capacitors *m* that maximizes the energy buffering ratio of the unipolar designs and this optimal number depends on the desired bus voltage ripple ratio, R_v. For a given ripple ratio (up to over 50%), the enhanced unipolar SSC energy buffer that uses an optimal number of supporting capacitors (i.e., the optimal 1-*m* enhanced unipolar SSC energy buffer) achieves a higher energy buffering ratio than the optimal 1-*m* unipolar design, as can be seen from Fig. 5.

Figure 5 also compares the energy buffering ratio of the optimally designed unipolar SSC energy buffers with optimally designed 1-*m* and 2-*m* bipolar and enhanced bipolar SSC energy buffers for ripple ratios ranging from 1% to 50%. The energy buffering ratio of a single capacitor, given by:

$$\Gamma_b = 1 - \frac{(1-R_v)^2}{(1+R_v)^2}, \quad (5)$$

is also plotted for reference. Note that while the energy buffering ratio of a single capacitor is very low for small ripple ratios, it reaches 100% at a ripple ratio of 100%.

It is interesting to note that while the energy buffering ratio of the bipolar designs is considerably higher than that of the unipolar designs at low ripple ratios, this does not hold

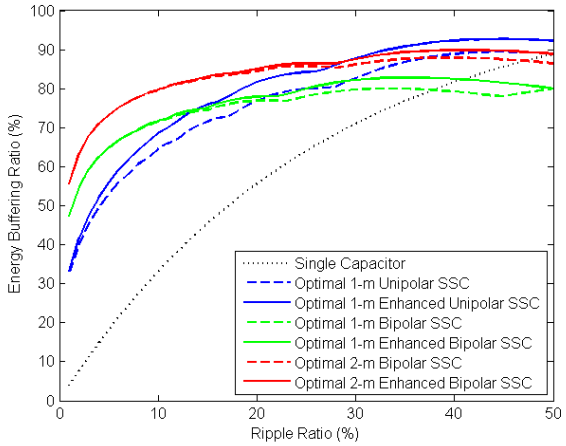

Figure 5. Energy buffering ratio as a function of ripple ratio for various energy buffering architectures. Each point of the plot represents the performance of a design with the optimal number of supporting capacitors for that ripple ratio.

true across the entire ripple ratio range. The optimal enhanced unipolar design has higher energy buffering ratio (and hence higher effective energy density) than the optimal 1-*m* enhanced bipolar SSC energy buffer (i.e., one with 1 backbone capacitor) when the required bus voltage ripple ratio exceeds 14%; and it is even better than the optimal 2-*m* enhanced bipolar design when the required ripple ratio exceeds 29%.

The reason for this is that as the ripple ratio increases the energy storage capability of the supporting capacitors becomes a larger fraction of the total energy storage capability (i.e., rated energy) of the entire energy buffer. However, unlike in the unipolar designs, the supporting capacitors in the bipolar designs do not contribute towards the energy buffering capability of the energy buffer, as their voltage has to return to its original value at the end of each charge (or discharge) cycle.

It is also interesting to note that at ripple ratios exceeding 55%, the single capacitor provides the highest energy buffering ratio of all the architectures considered above.

V. Prototype Design

A prototype 2-5 enhanced bipolar SSC energy buffer (Fig. 1(b)) has been built with exactly the same components as the original 2-6 bipolar SSC energy buffer presented in [10] and shown in Fig. 1(a). The only difference being that the enhanced design does not have the capacitor C_{26} and the switch S_{26}, and uses a modified control algorithm that produces the switching pattern shown in Fig. 2(b), implemented using a state machine with 22 states instead of the original 24. Both energy buffers are designed to provide 120-Hz buffering at the output of a power factor correction (PFC) circuit and maintain a 10% voltage ripple ratio on a 320 V bus with a maximum load of 135 W.

As in the original 2-6 SSC energy buffer, the capacitors are precharged using a linear regulator (Supertex LR8) operated as a current source. The precharge circuit also has two switches that disconnect it from the main power stage once precharge is complete. The SSC energy buffer is controlled using two microcontrollers (both ATMEL ATmega2560). One microcontroller controls the switches in the main power stage and the precharge circuit, while the other provides a feedback signal that mimics the bus voltage the PFC would have seen had there been a single energy buffering capacitor at its output. This ensures that the average output power of the PFC matches the power drawn by the dc load and the system stays stable. Details of the precharge and the control circuit are given in [10].

Also as in the original design, all the switches in the main power stage are implemented using power MOSFETs: S_{11} and S_{12} are implemented with reverse voltage blocking capability using two anti-series-connected 800 V power MOSFETs (STP12NK80Z). A single STP12NK80Z is used to implement each of the H-bridge switches, and S_{21}, S_{22}, S_{23}, S_{24} and S_{25} are implemented using two anti-series-connected 400 V power MOSFETs (STP12NK40Z).

The maximum energy that can be buffered by an *n-m* enhanced bipolar SSC energy buffer with all capacitors having equal capacitance *C* is given by:

$$\mathrm{E}_{b(max)} = \frac{1}{2} C \beta_b \mathrm{V}_{\mathrm{NOM}}^2 , \qquad (6)$$

where $\beta_b = n[(1+(m+1)R_v)^2 - (1-(m+1)R_v)^2]$. Hence, the necessary capacitance value for all the capacitors in the energy buffer can be determined from:

$$C = \frac{2\,P_{dc(max)}}{\omega_{\mathrm{line}} \beta_b \mathrm{V}_{\mathrm{NOM}}^2} , \qquad (7)$$

where $P_{dc(max)}$ is the maximum dc power of the system, and ω_{line} is the ac line's angular frequency (377 rad/sec in the US). For a 2-5 enhanced SSC energy buffer, with maximum load power of 135 W and a nominal bus voltage of 320 V, the necessary value of capacitance is 1.5 µF. To allow some headroom, 2.2 µF film capacitors, identical to the ones in the original design [10], are used. The backbone capacitors charge up to 512V; however, to provide adequate safety margin the selected backbone capacitors have a voltage rating of 700 V. The peak voltage on the supporting capacitors ranges from 64 V to 192 V, but identical 250 V capacitors are used for simplicity.

VI. Experimental Results

The prototype 2-5 enhanced bipolar SSC energy buffer has been tested with a power factor correction (PFC) circuit powering a resistive load. The SSC energy buffer replaces the electrolytic capacitor normally connected at the output of the PFC, as shown in Fig. 6. The SSC energy buffer is designed to meet a 10% bus voltage ripple ratio requirement on a 320 V dc bus with a maximum load of 135 W.

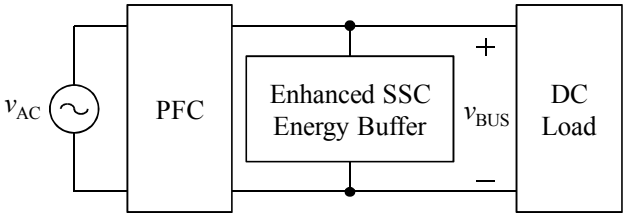

Figure 6. Configuration of the experimental system.

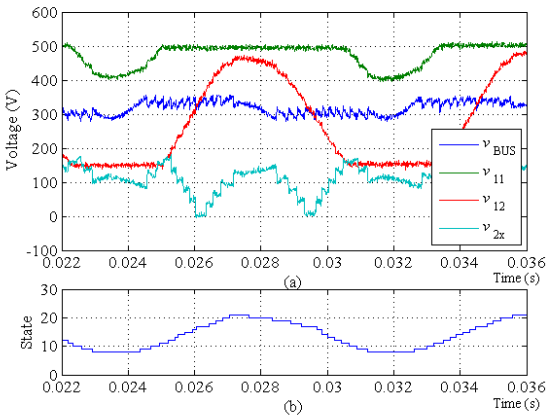

Figure 7. Measured waveforms for the 2-5 enhanced bipolar SSC energy buffer during normal operation: (a) bus voltage (v_{BUS}), backbone capacitor voltages (v_{11} and v_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (v_{2x}), and (b) corresponding state (1-22) of the state machine.

The measured waveforms from the 2-5 enhanced bipolar SSC energy buffer supporting a 100 W load are shown in Fig. 7. Clearly, the enhanced SSC energy buffer maintains the bus voltage within the ±10% specified range. Figure 8 shows the measured waveforms for this energy buffer during startup. The SSC energy buffer starts normal operation at t = 0.026 s. It takes 2 cycles for the bus voltage (v_{BUS}) to settle down within its designed ripple range, and also for the states of the state-machine to achieve periodic steady-state. Figure 9 shows the measured waveforms of the 2-5 enhanced SSC energy buffer during a load transient. The load steps from 50 W to 100 W at t = 0.052 s. The state machine traverses through higher and lower states within the first cycle and the system settles down to a new equilibrium in two cycles.

The round-trip efficiency of the 2-5 enhanced bipolar SSC energy buffer was measured across a wide load range (25 W – 130 W) and this data is plotted in Fig. 10. Figure 10 also plots the measured round-trip efficiency of the original 2-6 bipolar SSC energy buffer. For both energy buffers the measured efficiency does not include the power consumption of the control circuit and the gate drive, as these are the same in both designs and not optimized for high efficiency. As can be seen, the enhanced version has

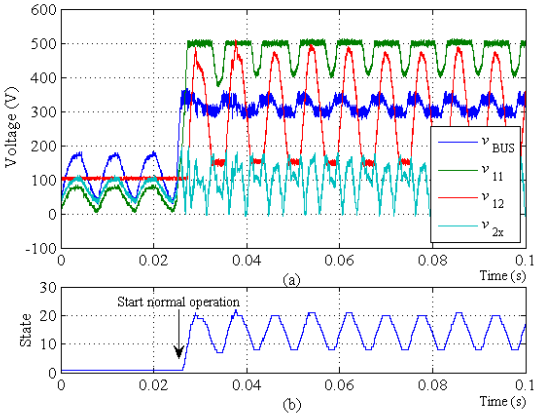

Figure 8. Measured waveforms for the 2-5 enhanced bipolar SSC energy buffer during startup: (a) bus voltage (v_{BUS}), backbone capacitor voltages (v_{11} and v_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (v_{2x}), and (b) corresponding state (1-22) of the state machine.

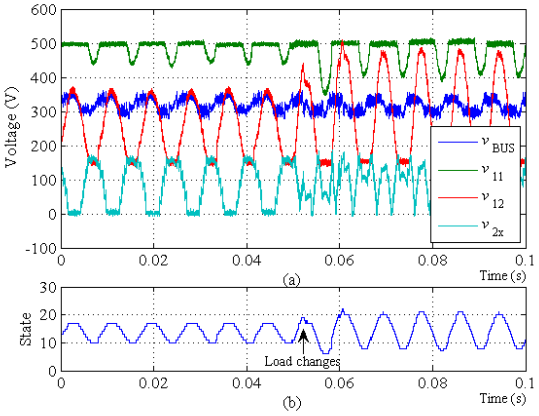

Figure 9. Measured waveforms for the 2-5 enhanced bipolar SSC energy buffer during a load transient: (a) bus voltage (v_{BUS}), backbone capacitor voltages (v_{11} and v_{12}) and voltage across the supporting capacitor that is charging or discharging at the time (v_{2x}), and (b) corresponding state (1-22) of the state machine.

roughly 1% higher round-trip efficiency. This represents a 20-25% reduction in loss as compared to the original design. The improvement in efficiency is primarily due to the fact that in the enhanced bipolar SSC energy buffer the capacitors charge and discharge for part of the cycle through 3 series switches instead of 4.

VII. Conclusions

This paper introduces an enhanced version of the bipolar SSC energy buffer which modifies the control and switching pattern of the buffer switches to yield improved performance. Performance comparisons are also made among the original and the enhanced bipolar SSC energy buffers and their unipolar counterparts.

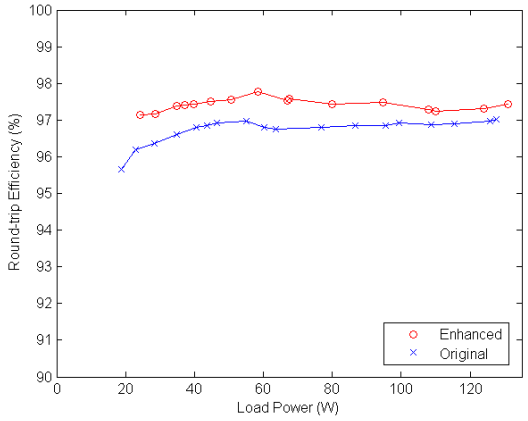

Figure 10. Comparison of round-trip efficiency of enhanced and original bipolar SSC energy buffer.

A prototype enhanced 2-5 bipolar SSC energy buffer, designed to maintain a 10% voltage ripple ratio on a 320 V dc bus and able to support a 135 W load, has been built and tested. The operational principle, design methodology and experimental results for the enhanced bipolar SSC energy buffer are presented and compared with the original design. It is shown that the enhanced SSC energy buffer achieves a higher effective energy density and round-trip efficiency, while maintaining the same bus voltage ripple ratio. Furthermore, the enhanced design uses fewer capacitors and switches than the original buffer.

The performance of the original and the enhanced bipolar SSC energy buffers is also compared with that of the unipolar SSC buffers. It is shown that while at low ripple ratios bipolar SSC energy buffers are superior to unipolar designs in terms of effective energy density, unipolar designs are superior to bipolar ones at large ripple ratios. Furthermore, unipolar designs use fewer switches and are therefore attractive in this regime.

References

[1] A.C. Kyritsis, N.P. Papanikolaou and E.C. Tatakis, "A Novel Parallel Active Filter for Current Pulsation Smoothing on Single Stage Grid-Connected AC-PV Modules," *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Aalborg, Denmark, September 2007.

[2] A.C. Kyritsis, N.P. Papanikolaou and E.C. Tatakis, "Enhanced Current Pulsation Smoothing Parallel Active Filter for Single Stage Grid Connected AC-PV Modules," *Proceedings of the International Power Electronics and Motion Control Conference (EPE-PEMC)*, pp. 1287-1292, Poznan, Poland, September 2008.

[3] T. Shimizu, K. Wada and N. Nakamura, "Flyback-Type Single-Phase Utility-Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1264-1272, September 2006.

[4] S.B. Kjaer and F. Blaabjerg, "Design Optimization of a Single-Phase Inverter for Photovoltaic Applications," *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, pp. 1183-1190, Acapulco, Mexico, June 2003.

[5] P.T. Krein and R.S. Balog, “Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port,” *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 620-625, Washington, DC, February 2009.

[6] B.J. Pierquet and D.J. Perreault, “Single-Phase Photovoltaic Inverter Topology with Series-Connected Power Buffer,” *Procedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2811-2818, Atlanta, GA, September 2010.

[7] A. Rufer and P. Barrade, “A Supercapacitor-Based Energy Storage System for Elevators with Soft Commutated Interface,” *IEEE Transactions on Industry Applications*, vol. 38, issue 5, pp. 1151-1159, September-October 2002.

[8] S. Sugimoto, S. Ogawa, H. Katsukawa, H. Mizutani and M. Okamura, “A Study of Series-Parallel Changeover Circuit of a Capacitor Bank for an Energy Storage System Utilizing Electric Double-layer Capacitors,” *Electrical Engineering in Japan*, vol. 145, issue 3, pp. 33-42, November 2003.

[9] X. Fang, N. Kutkut, J. Shen and I. Batarseh, “Ultracapacitor Shift Topologies with High Energy Utilization and Low Voltage Ripple,” *Proceedings of the International Telecommunications Energy Conference (INTELEC)*, Orlando, FL, June 2010.

[10] M. Chen, K.K. Afridi and D.J. Perreault, "Stacked Switched Capacitor Energy Buffer Architecture," *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 1404-1413, Orlando, FL, February 2012.

[11] A.H. Chang, J.J. Cooley and S.B. Leeb, "A Systems Approach to Photovoltaic Energy Extraction," *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 59-70, Orlando, FL, February 2012.